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# Electric-field-induced Shift in the Threshold Voltage in $LaAlO_3/SrTiO_3$ Heterostructures

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**The two-dimensional electron gas (2DEG) at the interface between insulating $LaAlO_3$ and $SrTiO_3$ is intriguing both as a fundamental science topic and for possible applications in electronics or sensors. For example, because the electrical conductance of the 2DEG at the $LaAlO_3/SrTiO_3$ interface can be tuned by applying an electric field, new electronic devices utilizing the 2DEG at the $LaAlO_3/SrTiO_3$ interface could be possible. For the implementation of field-effect devices utilizing the 2DEG, determining the on/off switching voltage for the devices and ensuring their stability are essential. However, the factors influencing the threshold voltage have not been extensively investigated. Here, we report the voltage-induced shift of the threshold voltage of $Pt/LaAlO_3/SrTiO_3$ heterostructures. A large negative voltage induces an irreversible positive shift in the threshold voltage. In fact, after the application of such a large negative voltage, the original threshold voltage cannot be recovered even by application of a large positive electric field. This irreversibility is attributed to the generation of deep traps near the $LaAlO_3/SrTiO_3$ interface under the negative voltage. This finding could contribute to the implementation of nanoelectronic devices using the 2DEG at the $LaAlO_3/SrTiO_3$ interface.**

Since the discovery of the two-dimensional electron gas (2DEG) at the interface between two band insulating oxides, $SrTiO_3$ (STO) and $LaAlO_3$ (LAO)[1,2], considerable efforts have been dedicated to the development of novel electronic devices utilizing this 2DEG[3–7]. For the implementation of such electronic devices, it is imperative to effectively control the physical properties of the 2DEG, such as its electric conductivity. Because of the finite carrier density of the 2DEG, carriers can easily be depleted at the interface so that a very high on/off ratio of the conductivity can be effectively achieved.

Although several external stimuli for controlling the electrical conductivity of the 2DEG have been proposed[8–19], an electric field is the most favorable stimulus from the perspective of device applications. Various field-effect devices for tuning of the electrical conductivity of the 2DEG have been studied[19–25]. Thiel et al. reported the modulation of the 2DEG at the LAO/STO interface by a gate voltage[19]. Since the field-effect devices in that study used 1 mm-thick STO substrates as the gate dielectric, a very large back-gate voltage (>70 V) was required for switching. The potential of oxide 2DEGs for nanoelectronics has also been examined by conductive atomic force microscopy, which showed that field-effect transistors even with characteristic lateral dimensions as small as 2 nm exhibited tunable conductance[20–23]. In those studies, a few volts was found to be enough to switch the devices because of the very thin LAO (<5 unit cells) used as the gate dielectric. Förg et al. also reported the fabrication of top-gate-structured field-effect transistors utilizing LAO/STO interfaces. These devices were switched with gate voltages below 1 V.[25]

The previous studies on devices utilizing 2DEG at the oxide interfaces have mostly been limited to realizing tunability of the 2DEG conductance. However, the implementation of nanoelectronics utilizing oxide 2DEGs requires more detailed studies on the device properties. In particular, the threshold voltage ($V_{th}$) for switching the field-effect devices on and off is one of the critical factors determining the transport properties of the devices. A large $V_{th}$ is not efficient in terms of power consumption. In addition, good stability of the $V_{th}$ of the devices should be obtained for highly reliable devices.

The $V_{th}$ of a metal-oxide-semiconductor (MOS) capacitor is generally dependent both on the work function difference between electrode and semiconductor and on charged defects in the dielectric or at the interfaces[26]. In

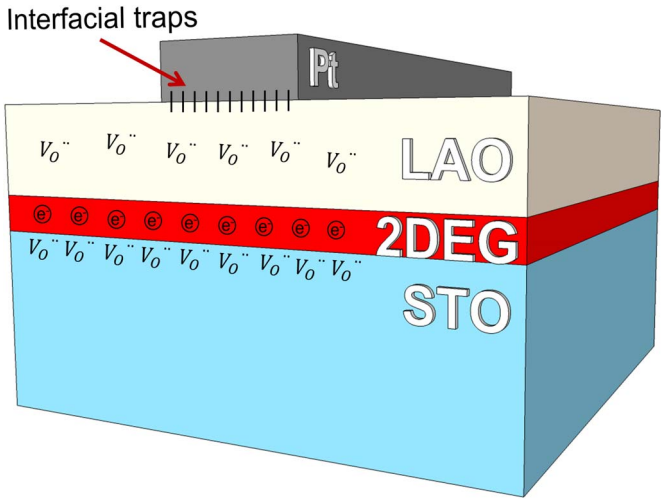


**Figure 1 | Schematic illustration of several kinds of defects in the Pt/LAO/STO heterostructure.**

LAO/STO heterostructures, several kinds of defects could exist in the heterostructures, as shown in Fig. 1: metal-induced gap states at the Pt/LAO interface, oxygen vacancies in the LAO layer, and oxygen vacancies in the STO near the interface. For a very thin LAO layer (usually <10 unit cells), a large electric field could generate traps in the LAO layer, as well. Therefore, the $V_{th}$ of LAO/STO devices will be determined by these defects in the LAO/STO heterostructure as well as by the work function difference between the top electrode and 2DEG.

Here, we report the voltage-induced $V_{th}$ shift of LAO/STO devices. We attribute the observed $V_{th}$ shift to the change in the defect density in the LAO layer. The $V_{th}$ shift after application of a negative voltage was not reversible by subsequent application of a positive voltage. This voltage direction dependency results from the nonequivalent electric field applied to the LAO layer. We fabricated capacitor devices consisting of Pt/LAO/STO heterostructures and measured the current – voltage (I–V) and capacitance – voltage (C–V) curves to analyze the electrical properties.

## Results and Discussion

The capacitor device for the electrical analysis is shown in Fig. 2 (a). Pt top electrodes were formed on the top of the LAO surface, and an Al wire was wedge-bonded to the LAO surface to make an ohmic contact to the 2DEG at the LAO/STO interface. A DC bias was applied to the top Pt electrode, and a lead wire was grounded. The resistance equivalent circuit for these devices can be simply assumed to be the series circuit in Fig. 2 (b). The total resistance of the devices can be expressed by the following equation:

$$R_{total} = R_{LAO} + R_{2DEG} + R_{2DEG}' \quad (1)$$

where $R_{total}$, $R_{LAO}$, $R_{2DEG}$, and $R_{2DEG}'$ are the resistances of the device, LAO layer, 2DEG layer beneath the Pt top electrode, and 2DEG layer in the periphery of the capacitor, which connects $R_{2DEG}$ with the Al wire. $R_{LAO}$ and $R_{2DEG}$ vary with the applied bias, while $R_{2DEG}'$ is not influenced by the applied bias. The resistance of the Pt top electrode and the Al wire is neglected because it is much smaller than those of LAO and 2DEG layers.

We first examined the I–V curves of the 4 nm-thick LAO/STO device in a positive bias region. It should be noted that electron carriers in the region corresponding to $R_{2DEG}$ are accumulated under the positive bias[27]. Under the positive bias, $R_{2DEG}$ can be ignored because the length of the resistor with $R_{2DEG}$ is much shorter than that (a few mm) with $R_{2DEG}'$, so $R_{total}$ is simply regarded as $R_{LAO}$ + $R_{2DEG}'$ under the positive bias. Figure 2 (c) shows I–V curves of the devices in the positive bias region. The current level is below 0.2 mA in the whole voltage range. If the LAO layer suffers breakdown, the

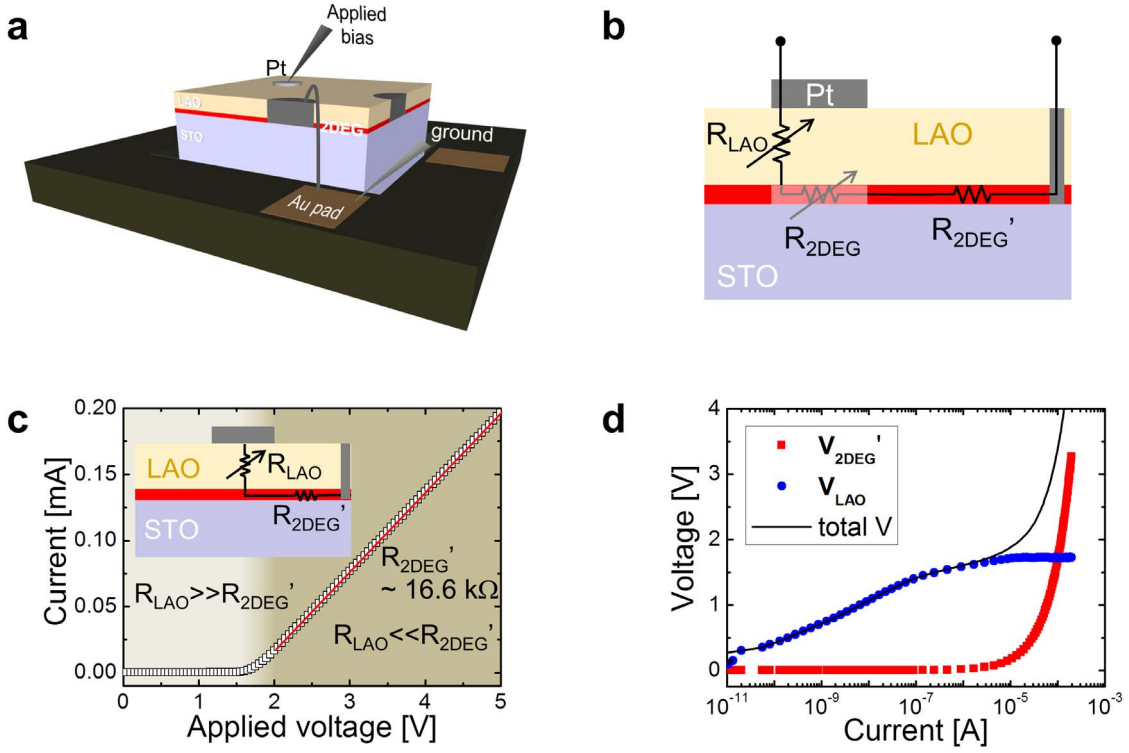


**Figure 2 |** (a) Schematic diagram of the Pt/LAO/STO capacitor devices. (b) A resistance equivalent circuit for the Pt/LAO/STO capacitor devices. (c) I–V curve of the device in a positive voltage region. The resistance of the device is considered to be the sum of the resistance of LAO layer and that of the 2DEG in the periphery of the capacitor. (d) Variation in the voltages applied to the LAO layer and the 2DEG in the vicinity of the capacitor.

current level should approach a high value (~0.1 A). This means that the LAO layer is not destroyed even under a high applied voltage. The current level in the positive bias region linearly increased with the applied voltage above approximately 1.7 V. Considering the Schottky contact between 2DEG and LAO, the linearity of the I–V curve is unexpected. Indeed, the linearity means that $R_{total}$ above approximately 1.7 V is determined by $R_{2DEG}'$. It should be noted that $R_{2DEG}'$ does not vary with the applied bias, whereas $R_{LAO}$ exponentially decreases with increasing applied bias. $R_{2DEG}'$ becomes much higher than $R_{LAO}$ in the high voltage region. In that high voltage region, the $R_{total}$ of the device is determined by $R_{2DEG}'$. Therefore, the value (~16.6 kΩ) of $R_{2DEG}'$ can be calculated from the inverse slope of the linear fit (Fig. 2 (c)), because $R_{2DEG}'$ is constant irrespective of the applied bias. In this capacitor device, it is possible that $R_{2DEG}'$ is smaller than $R_{LAO}$ despite the insulating property of LAO because the length of the resistor corresponding to $R_{2DEG}'$ is quite long (a few mm).

Based on the series connection of $R_{LAO}$ and $R_{2DEG}'$, the voltage applied to each resistance can be extracted as

$$V_{2DEG}' = R_{2DEG}'(16.6\ k\Omega) \times I_{total} \quad (2)$$

$$V_{LAO} = V_{total} - R_{2DEG}'(16.6\ k\Omega) \times I_{total} \quad (3)$$

The voltages applied to $R_{LAO}$ and $R_{2DEG}'$ are shown in Fig. 2 (d). Up to ~1.7 V, the total voltage is mostly applied to the LAO layer, and the voltage applied to the 2DEG is negligible because of the much higher resistance of the LAO. As the currents increase, on the other hand, the voltage applied to the LAO is saturated at ~1.7 V, and the voltage applied to the 2DEG abruptly increases. This means that the electric field applied to the LAO is saturated above a certain applied voltage even though the applied voltage increases greatly in the positive bias region. This is why the thin LAO film does not undergo electrical breakdown even under a high applied voltage.

I–V curves in a negative bias region show interesting behavior (Fig. 3 (a)). The current level increases with the applied voltage up to approximately −4.3 V and then suddenly decreases. The hump in the I–V curve indicates an abrupt increase in the resistance of the device below that voltage. The following I–V curve is quite different from the second I–V curve: no hump is observed, and the current level is much lower. The change in the resistance indicates that the application of negative voltages induces an irreversible change in the device. The subsequent I–V curve in a positive bias region (4th I–V curve), in contrast to the subsequent (3rd) I–V curve in a negative bias region, shows no difference from the initial (1st) I–V curve in the same bias region. To examine the origin of the irreversible change in the negative bias region, I–V sweeps were attempted in a different sweep order. Fig. 3 (b) shows the I–V curves of 5 nm-thick LAO/STO device. The 3rd I–V curve in the positive bias region is almost identical to the initial (1st) I–V curve in the same bias region, as is the case in Fig 3 (a). Despite the prior application of positive bias, interestingly, the current level in the 4th I–V sweep in the negative bias region does not return to the value in the 2nd I–V sweep and is much lower than that in the 2nd I–V sweep. To further investigate the irreversibility of the resistance change, I–V measurements were repeated alternately in the positive and negative bias regions. The inset in Fig. 3 (a) shows the I–V curves in the negative bias region. Despite the application of the positive bias, the current level was not recovered, but rather slightly decreased during the repeated measurements. This means that the resistance change induced by application of the negative bias is irreversible even under the application of a positive bias. The observed resistance change is different from the bipolar resistive switching in Pt/LAO/STO heterostructures reported by Wu et al.[28] In that report, the resistance state changed from low resistance state to high resistance state when a positive bias was applied. In addition, the I–V curve of the pristine sample in our study is almost identical to the subsequent I–V curve in Fig. 3 (c). This indicates that electrical forming, which is necessary for the resistive switching in transition metal oxides, does not occur in this study. We also compared I–V loops of the LAO/STO device in the voltage range of −8 ~ 8 V (V:

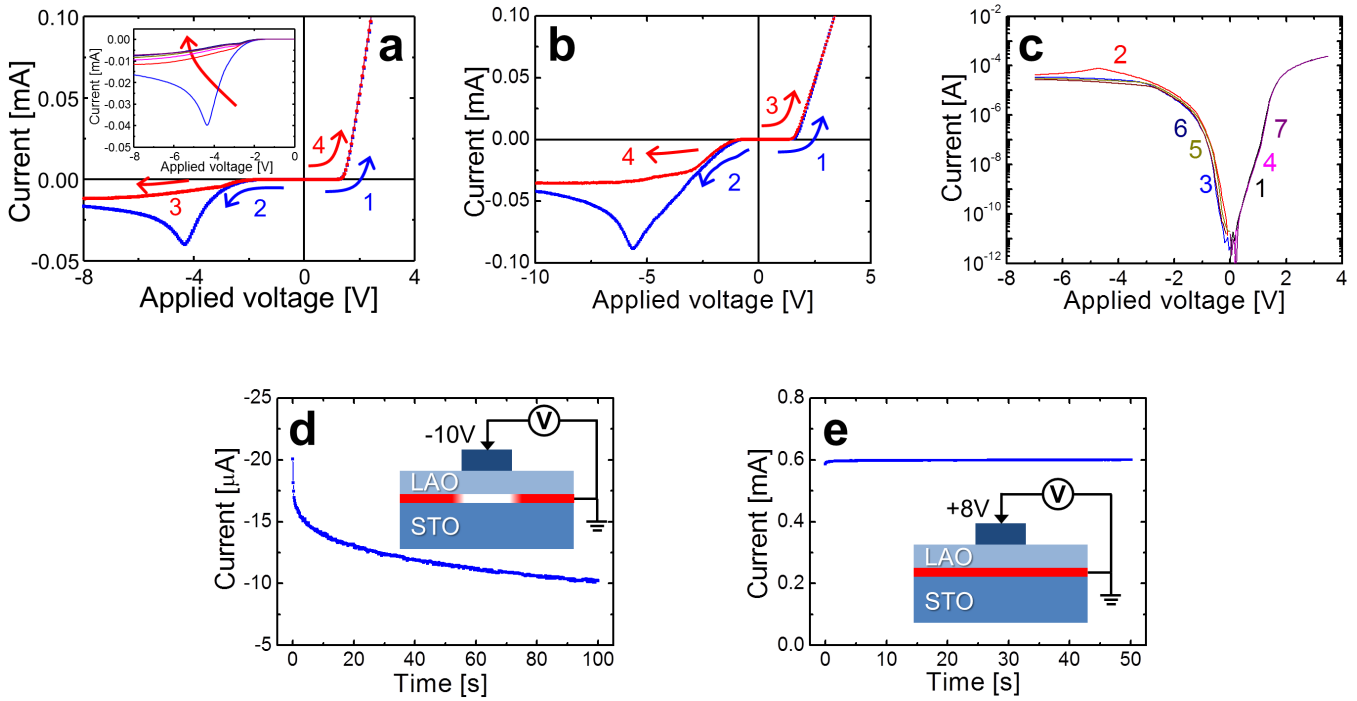


**Figure 3** | (a) I–V curves of the 4 nm-thick LAO/STO device in an applied voltage range of −8 to + 4 V. (b) I–V curves of the 5 nm-thick LAO/STO device in an applied voltage range of −10 to + 5 V. (c) I–V curves (log scale) of the 4 nm-thick LAO/STO device. (d) I–t curve of the device under a constant voltage of −10 V. (e) I–t curve of the device under a constant voltage of + 8 V.

0 V → 8 V → 0 V → −8 V → 0 V) with the I–V loops measured in the only negative voltage region (V: 0 V → −8 V → 0 V). (Fig. S1) Both measurements show quite similar I–V curves in the negative region. Therefore, the observed resistance change in our study is not related to common resistive switching behaviors.

The hump in I–V curve in the negative bias region in Fig. 3 (a) and (b) is attributed to two major factors: the depletion of the 2DEG and the positive shift in $V_{th}$ under a high negative bias. The finite carrier density and n-type nature of the 2DEG yield a C–V curve like that of a p-channel MOS capacitor[27]. Below $V_{th}$, the depletion of the 2DEG beneath the Pt top electrode leads to the abrupt increase in the device resistance ($R_{2DEG}$). If the depletion of the 2DEG below $V_{th}$ is the only reason for the hump in the I–V curve, the following (3rd) I–V curve in the same negative bias region should be identical in Fig. 3 (a). However, an irreversible resistance change in the negative bias region is still found. The $V_{th}$ shift due to the application of a negative bias seems to be the critical factor inducing the change in the I–V curve. The $V_{th}$ shift of the LAO/STO devices is discussed below in the context of the C–V measurements.

To further elucidate the irreversible negative-bias-induced resistance change of the LAO/STO devices, current-time (I–t) measurements were performed at a constant voltage. Figure 3 (d) and (e) show the I–t curves under the application of constant voltages of −10 and 8 V to the top electrode, respectively. The current level gradually decreased under the application of a constant voltage of −10 V, whereas under a constant voltage of 8 V the current level was almost constant irrespective of time. The large time constant of the exponential decay in the I–t curve in Fig. 3 (d) indicates the presence of deep trap levels due to the negative voltage or ionic movements induced by a highly negative electric field. These defects may be related to the negative-bias-induced irreversible resistance change.

Considering the very thin film thickness (~4 nm) of LAO, the applied electric field appears to be too high for the dielectric characteristics to be sustained. However, dielectric breakdown did not occur, and it is obvious that the LAO/STO devices were stable after the measurements. This stability is attributed to the decrease in the effective electric field. Under the application of a highly negative bias, the 2DEG beneath the Pt top electrode is fully depleted so that the effective electric field applied to the LAO layer is largely alleviated. Although the 2DEG accumulates beneath the top electrode under a positive bias, the non-negligible resistance of the 2DEG in the periphery induces a voltage drop as well. It should again be noted that the voltage applied to the LAO layer approached a certain low value (~1.7 V) as the applied voltage increased (Fig. 2 (d)).

We also performed a C–V analysis of the 4 nm-thick LAO/STO devices. The left panel in Fig. 4 (a) shows the measurement sequence used for the experiment. For the comparison of the voltage stress effects, we measured C–V curves three times before voltage stress and after the applications of −10 V for 100 s and 8 V for 50 s in sequence. All the C–V curves are characteristic of a p-channel MOS capacitor, as previously reported[27]. The capacitance values under accumulation of the 2DEG are approximately 0.7 nF, which is slightly lower than the actual capacitance (1.1 nF). This is because the C–V measurements were performed at a higher frequency of 100 kHz. Although the high-frequency measurement slightly underestimates the capacitance value, the measurement at 100 kHz is quite favorable for the determination of $V_{th}$.[27]

The C–V curve of the pristine LAO/STO capacitor before the voltage stress shows a highly negative $V_{th}$. The capacitance value abruptly decreased below approximately −4.5 V, which is consistent with the transition voltage in Fig. 3 (a). After a negative voltage stress of −10 V for 100 s, however, the C–V curve was greatly shifted to a positive bias ($\Delta V \sim 2.7$ V). The capacitance value approached zero below approximately −2 V, suggesting that the resistance of the capacitor was abruptly increased by the depletion of the 2DEG below that voltage. Therefore, the decrease in the current below −2 V after a negative voltage sweep in Fig. 3 (a) is ascribed to the positive shift in $V_{th}$. While the negative voltage stress shifted the C–V curve positively, the following positive voltage stress could not recover the C–V curve to the initial position. This is consistent with the irreversibility of the negative bias-induced change in the I–V curve in Fig. 3 (a). The C–V curve was slightly shifted toward a positive bias after the positive voltage stress, possibly because of the negative bias applied during the C–V measurement in the voltage range of −3.5 to 0 V. To verify this speculation, the change in the capacitance of the LAO/STO device under a mildly negative voltage was examined. Figure 4 (b) shows the variation in the capacitance as a function of time under a constant voltage of −2 V, which is near $V_{th}$. The capacitance still clearly decreased with the time even under this mild voltage. This indicates that $V_{th}$ is slightly shifted in a positive direction even under a constant voltage of −2 V (inset of Fig. 4 (b)), which supports the conclusion that the application of a negative bias during the C–V measurement causes the slight positive shift in $V_{th}$ in Fig. 4 (a).

Interestingly, hysteresis with a memory window of ~0.35 V was also observed after constant voltage stress at either a positive or negative voltage. As shown in Fig. 4 (c), the C–V curves show counterclockwise hysteresis irrespective of the sweep direction. LAO is hardly expected to exhibit hysteresis, since it is not ferroelectric. Bark et al. recently reported an electrically induced reversible polarization change in LAO/STO heterostructures[29]. They claimed that electric-field-induced redistribution of oxygen vacancies throughout the LAO layer led to the switchable hysteretic response[29]. Therefore, the hysteresis in the C–V curves in Fig. 4 (a) may be attributed to oxygen vacancy redistribution under the electric stimulus.

There are several kinds of defects in the Pt/LAO/STO heterostructures, as indicated in Fig. 1. The $V_{th}$ of the Pt/LAO/STO devices could be determined by both the defects in the structures and the work function difference between Pt and 2DEG. If the response of those defects to a highly negative voltage changes the effective work function difference or generates fixed charges, the $V_{th}$ of the LAO/STO device would shift after the application of a negative voltage stress.

The effective work function difference between the Pt top electrode and the 2DEG at the LAO/STO interface can be determined by various factors, as well as the work functions themselves of each material. The high density of interface states at a metal/semiconductor interface is known to pin the Fermi level at the energy level of the gap states regardless of the work function of the metal[30]. If the application of a highly negative voltage to the LAO/STO devices generates many interface states at the Pt/LAO interface, the $V_{th}$ can be shifted. Shifts in $V_{th}$ due to Fermi level pinning also accompany changes in the Schottky barrier height, resulting in variation of the leakage current. To determine whether Fermi level pinning causes the observed $V_{th}$ shift, we replaced 2DEG with a metallic (La,Sr)$MnO_3$ layer as a bottom electrode to fabricate Pt/LAO/(La,Sr)$MnO_3$/STO capacitors and examined the effect of a negative voltage sweep on the I–V curves (Fig. S2). If the Fermi level pinning leads to the positive shift in $V_{th}$ in Fig. 4 (b), the leakage current of the Pt/LAO/(La,Sr)$MnO_3$ capacitor should decrease after a negative voltage sweep. However, the first and second voltage sweeps in the negative voltage range show almost identical I–V curves, in contrast to those in Fig. 3 (a). This means that after the application of a negative voltage, the generation of interface states at the Pt/LAO interface is negligible, which supports the conclusion that variation in the Schottky barrier height at the Pt/LAO interface is not the reason for the $V_{th}$ shift.

Electric-field-induced ion accumulation could affect $V_{th}$, as well. In particular, it is known that there are many oxygen vacancies in the STO region near the LAO/STO interface[31–35]. The movement of charged oxygen vacancies under an applied electric field could change $V_{th}$. The accumulation of oxygen vacancies at the interface under a negative electric field should be easily relaxed in the absence of the electric field. However, the positive shift in $V_{th}$ under negative

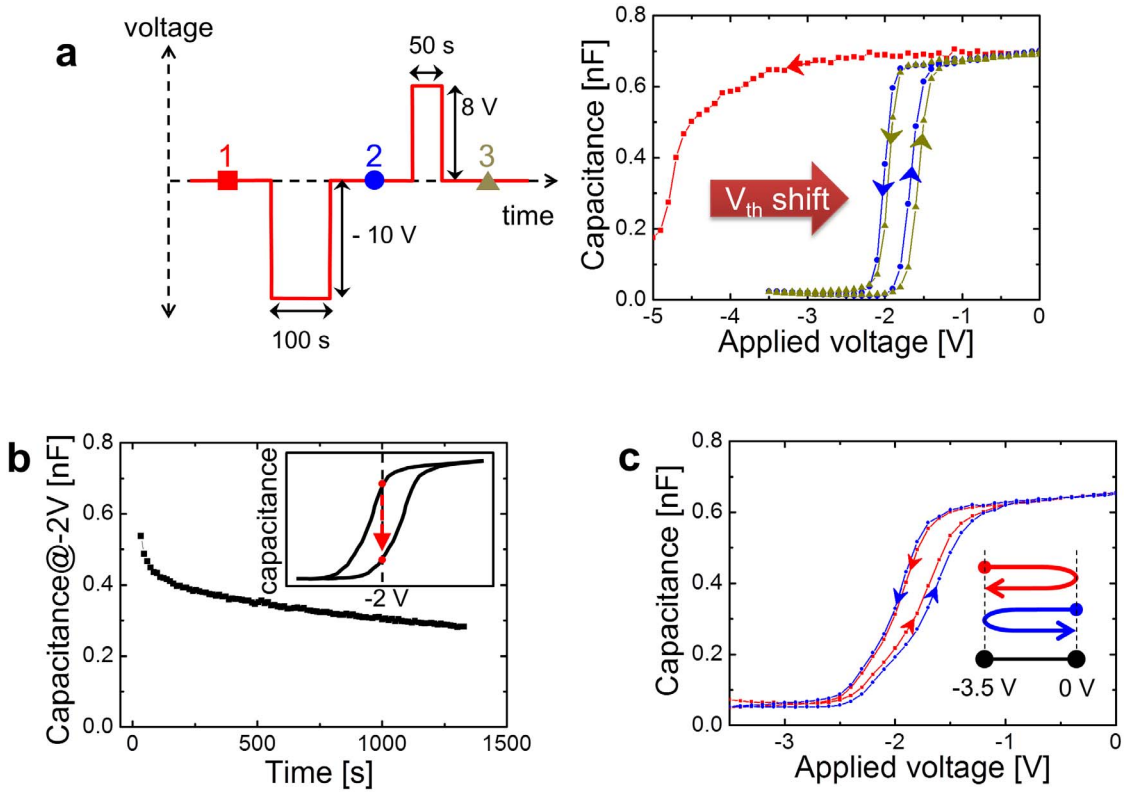


**Figure 4 | Capacitance – voltage analysis of Pt/4 nm-thick LAO/STO structure.** (a) Left: the measurement sequence for examination of voltage stress effects. Right: C–V curves before and after voltage stresses of −10 V for 100 s and 8 V for 50 s in sequence. (b) C–t curve of the device under a constant voltage of −2 V, which is near the threshold voltage. The inset indicates a scheme of both C–V curves before and after the voltage stress. (c) C–V curves of the device for different sweep directions.

voltage was not relaxed even 17 hours later (Fig. S3), supporting the conclusion that the contribution of the oxygen vacancy accumulation under the electric field to $V_{th}$ shift is negligible.

Therefore, it is likely that the $V_{th}$ shift of the LAO/STO devices is caused not by the change in the effective work function but by the variation in the fixed charge density in the LAO layer after the application of a negative voltage. A positive shift in the $V_{th}$ of a MOS capacitor indicates an effective increase in the negative fixed charge density near the oxide/semiconductor interface. It would seem that the application of a negative voltage to the top electrode of the LAO/STO capacitor generates negative fixed charges or eliminates pre-existing positive fixed charges in the LAO layer. Yu and Zunger recently reported that point defects such as $Sr_{La}$ or $Ti_{Al}$ can be formed at the LAO/STO interface and the point defects generate deep level traps in the band gap[36]. These charged point defects near the interface could be the origin of the fixed charges. As mentioned previously, the effective electrical field applied to the LAO layer under a positive voltage is limited. Thus, the fact that the shift in $V_{th}$ cannot be reversed by the application of a positive voltage is attributed to the insufficient positive electric field.

Further information on the irreversible negative-voltage-induced $V_{th}$ shift was obtained by studying the change in the 2DEG conductance before and after the application of a negative electric field. Figure 5 (a) shows the scheme of the four-point measurement pattern for a 2DEG channel with dimensions of 50 μm × 70 μm. A Pt top electrode with a diameter of 50 μm was lithographically patterned on the 2DEG channel. The detailed fabrication procedure was reported elsewhere[18]. The electrical conductance of the 2DEG channel was measured using a four-probe method before and after application of a constant voltage of −10 V for 80 s. The I-top gate voltage ($V_G$) curves of the LAO/STO device were examined before and after a constant voltage of −10 V was applied to the top gate electrode, as shown in Fig. 5 (b). The pristine LAO/STO cell shows a current hump at a voltage of ~ −4.7 V, whereas after the voltage stress the current hump disappeared and the current level of the LAO/STO cell was suppressed. These results are consistent with the I–V curves in Fig. 3 (a).

Figure 5 (c) shows the variation in the electric conductance ratio ($G_{Vstress}/G_{pristine}$) of the LAO/STO device in a wide temperature range from 30 to 300 K. The conductance ratio is around 0.9 in the whole temperature range despite the absence of a gate voltage. This indicates that the electric conductance of the 2DEG channel after the negative voltage stress is lower than that of the pristine cell at the same gate voltage. Considering the negligible temperature dependence of the conductance ratio, the conductance difference is attributed to the variation in the carrier density rather than the change in the carrier mobility. In a MOS transistor, the electronic carrier density is proportional to the difference between the gate voltage and $V_{th}$. The positive shift of the C–V curve in Fig. 4 (b) indicates that the effective electric field is significantly reduced after the application of a negative voltage stress. The decrease in the effective electric field induced by the positive shift in $V_{th}$ led to the decrease in the electric conductance in Fig. 5 (c).

## Conclusions

In summary, we investigated the voltage-induced changes in the electrical properties of LAO/STO devices. A largely negative voltage was found to induce an irreversible shift in $V_{th}$ in the positive direction. In fact, this $V_{th}$ shift could not be reversed by the application of a large positive voltage because of the insufficient positive electric field due to the large resistance of 2DEG in the periphery of the cell. For MOS devices, a low operating voltage is essential for low power consumption, and $V_{th}$ is a critical factor determining the operating voltage. In addition, a stable $V_{th}$ is necessary for high reliability of the

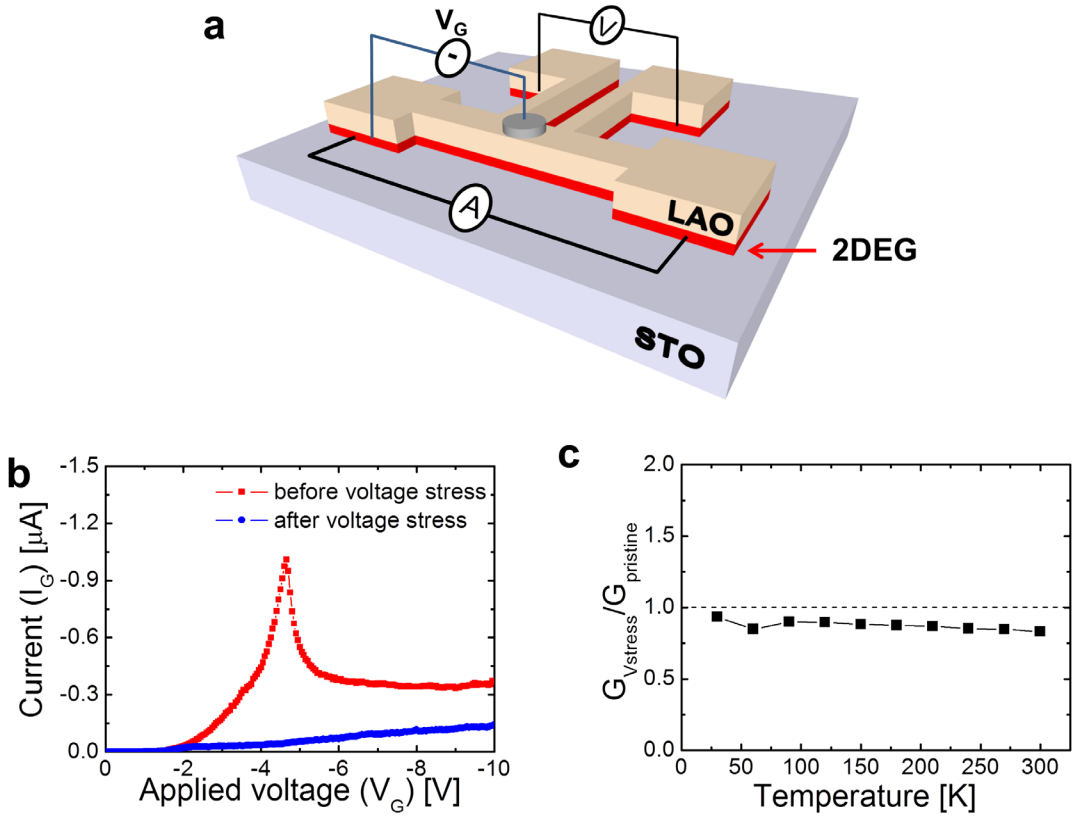


**Figure 5** | (a) Scheme of the four-point measurement of the 2DEG conductance. (b) I–V curves of the LAO/STO device before and after application of a constant voltage of −10 V. (c) Variation in the electric conductance ratio ((conductance of the 2DEG after the application of a constant gate voltage of −10 V)/(conductance of the 2DEG of a pristine structure)) of the LAO/STO device measured in a wide temperature range from 30 to 300 K.

devices. We believe that these results will contribute to an understanding of the physics of the LAO/STO devices and, furthermore, the realization of electronic devices utilizing oxide 2DEGs.

## Methods

$LaAlO_3$ films were epitaxially grown on a $TiO_2$-terminated (001) $SrTiO_3$ single crystal by pulsed laser deposition (PLD) using a KrF excimer laser ($\lambda$ = 248 nm). A laser beam was focused on a single-crystal $LaAlO_3$ target with a fluence of 1.5 J/cm$^2$ at a repetition rate of 2 Hz. The $LaAlO_3$ films were grown at a temperature of 700°C under an oxygen partial pressure of 1 mTorr. Pt top electrodes were deposited by DC sputtering at room temperature and were photolithographically patterned using a lift-off process.

The I–V measurements were performed using a Keithley 236 Source-Measure unit at room temperature. Four-point measurements were using a Keithley 6221 combined with Keithley 2182A in a wide temperature range from 30 to 300 K. The C–V characteristics of the devices were examined by a Solartron SI 1260 impedance analyzer at 100 kHz.


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## Author contributions

S.K.K. designed this work. S.K.K., H.L., D.S.J. and B.K. performed electrical measurements and analyzed the data. S.I.K. carried out the film growth. S.K.K., J.S.K. and S.H.B. arranged and supervised all experiments. All authors discussed the results and manuscript.

## Additional information

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