

Research Article

Design of LDMOS Device Modeling Method Based on Neural Network

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The rapid development of power semiconductor devices is helping to realize a low-carbon society and provide a better life for everyone. Power semiconductors not only are used in many large-scale industrial control fields such as power transmission and control in power grids, rail transit traction systems, and defense weapons and equipment, but also play a vital role in daily equipment such as home appliances, medical electronics, and electronic communications; all devices such as power steering in cars, battery chargers, cell phones, and microwave ovens utilize power electronics. This research mainly focuses on the high-voltage LDMOS device model and its implementation. Based on the in-depth study of the structure and physical mechanism of high-voltage LDMOS devices, with the help of BSIM4 core model, which is now very mature and widely used in industry, the drift region of high-voltage LDMOS is mainly modeled, and the drift region of LDMOS is modeled as a variable resistance controlled by voltage. Finally, Verilog-A language and neural network method are used to establish a compact model of LDMOS. The improved model is applied to LDMOS and can better fit the output characteristics with self-heating effect.

1. Introduction

The 21st century is an era of rapid development of science and technology, especially the rapid progress of electronic information technology, which benefits from the progress of the semiconductor industry and the development of the chip industry. In recent years, the development of our country's integrated circuit industry has a wide variety of integrated circuits and is used in automotive electronics, home appliances, mobile phones, computers, and wearable electronic devices. As the feature size of integrated circuits shrinks, the current state-of-the-art fabrication process has entered the 7 nm era. According to the scaling theory, the operating voltage of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices also decreases as the feature size of the device decreases. The operating voltage has dropped below 1 V, but high-voltage devices in power management, display drive, digital media, and mixed digital chips are still necessary [1–5], among which LDMOS (Laterally Diffused

MOSFET) device is a high-voltage device used in integrated circuits, and its performance and stability have been widely concerned as its important parameter indicators. At present, many foreign chip manufacturers have set up special departments to extract model parameters. Foreign research on model parameter extraction is relatively early, and the overall semiconductor technology level is relatively high, so the model parameter extraction technology is relatively advanced. In China, the development of model parameter extraction is slow and backward, which has a certain relationship with the overall backwardness of domestic semiconductor technology. In addition, the domestic semiconductor industry does not pay attention to the extraction of model parameters, and there is a relative shortage of talents in this area. Therefore, it is very important to increase the investment in model parameter extraction to improve the overall level of the semiconductor industry. In this study, on the basis of analyzing the characteristics of high-voltage LDMOS, the drift region is modeled, and some

special effect models are established at the same time. And the built LDMOS model is implemented by Verilog-A language, and the model parameter extraction and simulation curve fitting are completed. [1–9].

2. Related Work

Semiconductor device model is an abstraction that ignores the internal structure of semiconductor devices and directly reflects the output and transfer characteristics of devices. There are many kinds of semiconductor device models, which can be divided into DC, transient, and AC models according to different signal types. DC model is a static model, AC model is a small signal model, and transient model is a large signal dynamic model. According to the requirements of computational efficiency, device models can be divided into analytical model, look-up table model, and empirical model. SPICE model is one of the semiconductor device models. Its biggest feature is that it can be directly used in circuit simulator. In short, spice model is composed of a set of formulas and a set of parameters. Formulas are used to describe the characteristics of semiconductor devices. Parameters are the coefficients in these formulas. The establishment process of these formulas is called “modeling,” which is generally completed by universities or scientific research institutes. The process of extracting model parameters is called “model extraction,” which is usually completed by chip manufacturers, because different processes have corresponding model parameters. Generally speaking, model formulas have been integrated into circuit simulators, such as spice model BSIM4 of MOSFET 3. Therefore, the chip manufacturer only needs to hand over the extracted model parameters to the circuit designer, and the circuit designer can get the spice model of the corresponding process. Spectre is a completely customized integrated circuit simulation tool launched by cadence. It is mainly used for simulation of analog and digital analog hybrid integrated circuits. It is mainly used for UNIX workstations. It solves some numerical problems of spice, is suitable for RF circuit simulation, and supports all Berkeley MOS models. As mentioned above, there are several spice simulators, which must be used together with spice model for circuit simulation. These two together constitute the spice program. Spice simulator is spice’s math engine tool. It consists of some basic subroutines for mathematical analysis. One of the typical subroutines is to solve a matrix composed of n linear equations. When combined with Newton Raphson iteration, they can also solve the nonlinear equations of static node voltage and branch current of a given circuit. Another basic subroutine is to solve differential equations, which usually requires time as a variable for transient analysis. In these transient analyses, both voltage and current are functions of time. The second part of the spice program is the device model. There are many semiconductor devices in a circuit, such as diodes, bipolar transistors, capacitors, and MOS; these devices correspond to the device model [10–14]. In this study, the structure and

physical characteristics of LDMOS devices are analyzed. On the basis of physical derivation, an approximate method is used to establish a semiempirical compact model.

3. Related Theoretical Methods

3.1. The Basic Principle of WGAN. The original GAN is accompanied by problems such as gradient disappearance and model collapse. When dealing with some problems in specific fields, if it is not optimized, it will not get the desired results. In recent years, GAN has developed rapidly. Various optimization models of GAN have appeared one after another, and there are more and more derivative networks based on GAN. These problems have been solved after the emergence of WGAN. The original GAN used the KL divergence and the JS divergence to measure the distribution of two probabilities, but using such a measure presents a problem if the generated data and the real data are far apart and they do not overlap or overlap. When it can be ignored, the value of JS is constant, which means that the gradient is zero, the gradient disappears, and the training cannot proceed. Therefore, WGAN uses the Wasserstein distance to measure the distribution of two probabilities, and the expression of the Wasserstein distance is as follows [15, 16]:

$$W(P_{\text{data}}, P_g) = \inf_{a \in \prod (P_{\text{data}}, P_g)} E_{(x,y) \sim a} [\|x - y\|]. \quad (1)$$

P_{data} represents the real data, P_g represents the generated data, $\prod (P_{\text{data}}, P_g)$ represents the set of joint probability distributions of the real data and the generated data, and the marginal probability distributions of the joint probability distribution are P_{data} and P_g . (x, y) is any one sampled from the set of joint probability distributions; it represents how much weight from the P_g distribution to the P_{data} distribution is transported from x to y , so the Wasserstein distance is actually a function of calculating the optimal transport cost. The advantage of Wasserstein distance and JS distance is that even if the two distributions do not overlap or overlap very little, they can still distinguish the distance between the two distributions and keep the gradient updated continuously. Whereas the JS divergence is constant in this case, the gradient will vanish, the model will crash, and the KL divergence may be meaningless. The emergence of Wasserstein distance solves the problem of gradient disappearance and model collapse during original GAN training. It mainly uses the Lipschitz function to limit the range of gradients and avoid extreme conditions of gradients, thereby ensuring smooth training of GANs. To express the capabilities of the Lipschitz function, convert the Wasserstein distance to the formula:

The definition of the Lipschitz limit is also very simple; that is, for a continuous function, there is a K greater than or equal to zero, so that the maximum value of the absolute value of the derivative of a certain interval in the definition domain is less than or equal to K , then K can be called the Lipschitz constant, and the continuous function is called the Lipschitz constant. A function is a function with a

K-Lipschitz condition, and the expression for the K-Lipschitz condition is as follows:

$$|f(x_1) - f(x_2)| \leq K|x_1 - x_2|. \quad (2)$$

At this time, the loss function of WGAN can be expressed as

$$V(G, D) = \min_G \max_{D \in K\text{-Lip}} \{E_{x \sim P_{\text{data}}} [D(x)] - E_{x \sim P_G} [D(x)]\}. \quad (3)$$

There are some requirements for the discriminator; it must be a smooth function, as long as the value of K in the discriminator is not positive infinity, because it will only increase the gradient by K times and will not change the direction of the gradient. For the processing of gradients, a simple processing method can be adopted to limit the weight parameters of the neural network in the discriminator to a certain range $[-c, c]$; that is to say, when the parameters are updated, for the parameters less than $-c$, the weight is set to $-c$, and the weight greater than c is set to c , so the gradient will not exceed a certain range, which just satisfies the Lipschitz condition. In actual experiments, the weight parameters are updated first, and then the weights are clipped back to this range. The training process of WGAN is as follows:

First initialize a discriminator parameter w and generator parameter, initialize a clipping constant c , and optimize D first in each round of iterative training:

- (1) Sampling a batch of data $1/2 (x^1, x^2, \dots, x^m)$ from the real dataset.
- (2) Sample a batch of random noise $1/2 (Z^1, Z^2, \dots, Z^3)$ from the prior random distribution.

WGAN has also made some changes in network design from the original GAN:

- ① Do not take the logarithm of the loss in the generator and discriminator.
- ② Each time the parameters of the discriminator are updated, their absolute values are truncated to a fixed range.
- ③ The last layer of the discriminator removes the sigmoid function.
- ④ Do not use momentum-based optimization algorithm (momentum Adam); use RMSprop (root mean square prop) or SGD (stochastic gradient descent).

3.2. Structure and Process Method of LDMOS

3.2.1. Structure and Process of LDMOS. This study takes the NLDMOS of the CSMC 0.18 μm 25 V BCD process platform as an example to illustrate the structure and process flow of the LDMOS. Figure 1 shows a cross-sectional view of the LDMOS structure. This is an LDMOS with a bilateral structure. Two identical LDMOS devices are connected in parallel, which can improve the current capability of the LDMOS without changing other characteristics of the device. The main difference between a basic LDMOS device and ordinary MOS in structure is as follows: first, LDMOS is

an asymmetric structure. In order to improve the withstand voltage, a relatively long and low doping concentration will be formed on the side of the device near the drain. The drift region can effectively reduce the parasitic capacitance between the source and drain and weaken the short channel effect of LDMOS; secondly, the channel of LDMOS is formed by the lateral double diffusion process, that is, the P-type and the diffusion of N-type impurities, so the channel region is nonuniformly doped, and the formation of the channel is not determined by the gate length. The double diffusion process can precisely control the length of the channel and make the channel length very short. Compared with ordinary MOS, the current capability, transconductance, maximum operating frequency, and speed are greatly improved. Finally, the polysilicon gate of LDMOS not only covers the gate oxide above the channel region, but also covers the gate oxide and field oxide above the drift region. Because the thickness of the field oxide is much larger than that of the gate oxide, the polysilicon is removed from the gate. There is a slope from the top of the oxygen to the top of the field oxygen. In fact, the effective gate length is shorter than the physical length of the gate. [17–19].

For the specific LDMOS of 0.18 μm 25 V BCD process, its structural levels mainly include P-type substrate (Psub), N-type buried layer (BN), deep P-well (DP), deep N-well (DN), high-voltage P-well (PX), high-voltage N-well (NX), P-sinker (PK), P-shift (PM), N-shift (NM), N-offset (NG), N+ Source/Drain (N^+), P^+ body contact area, surface field oxide layer, polysilicon gate (Gate), source and drain metal electrodes, P substrate electrodes, etc.

As shown in Figure 2, first generate 1000 Å TEOS, and then perform ZO lithography to form part of the stripe pattern. The ZO cycle process is only done in the dicing lane area, and there is no ZO pattern in the device area. This process is beneficial to the alignment of the next BN, DN, DP, and PM layers.

Then there are N buried layer and P buried layer process, as shown in Figure 3. First perform BN implantation and push well to form an N-type buried layer. This process has a good isolation effect and can also effectively prevent the upper and lower punch-through breakdown of PLDMOS in the same BCD process. The trap is then pushed in nitrogen, followed by a field oxygen of 3000 Å to eliminate defects. Next is the fabrication of the P buried layer (BP). Figure 3 and the following schematic diagrams omit the BP structure. The formation of BP structure can effectively improve the punch-through breakdown between BNs.

Next is the epitaxy process, forming a P-type epitaxy layer with a thickness of 4.7 μm , as shown in Figure 4.

There are various isolation technologies in the BCD process. Here, a Deep N-well (DN) and a Deep P-well (DP) are formed successively to form a PN junction with isolation. The DN and DP used to make LDMOS devices are also here, formed simultaneously in one step, as shown in Figure 5.

In order to improve the characteristics of the LDMOS drift region, it is necessary to process the drift region and perform P-shift (PM) and N-shift (NM) implantation in the drift regions of PLDMOS and NLDMOS, respectively, as shown in Figure 6.

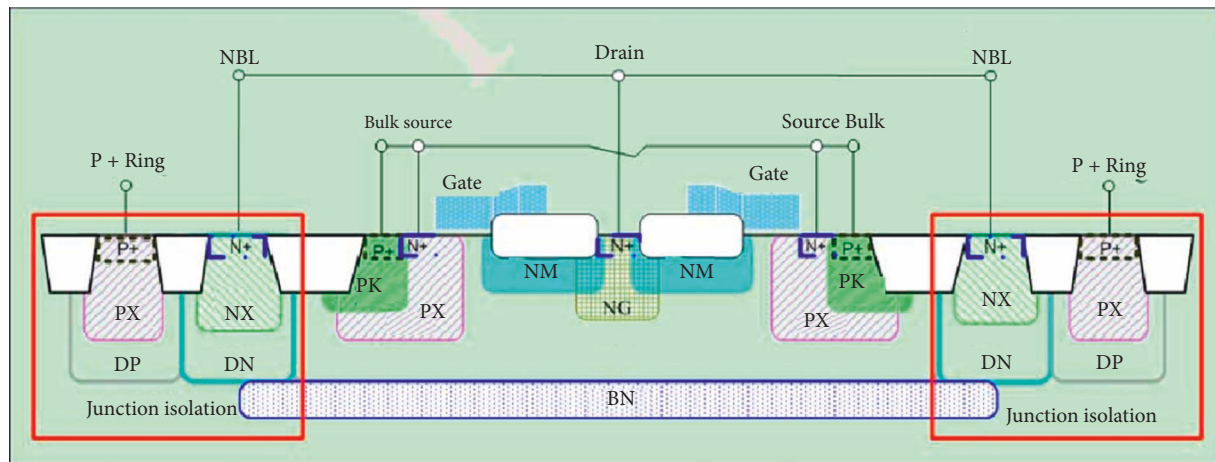


FIGURE 1: 25 V NLD MOS structure cross-sectional view.



FIGURE 2: ZO loop process.

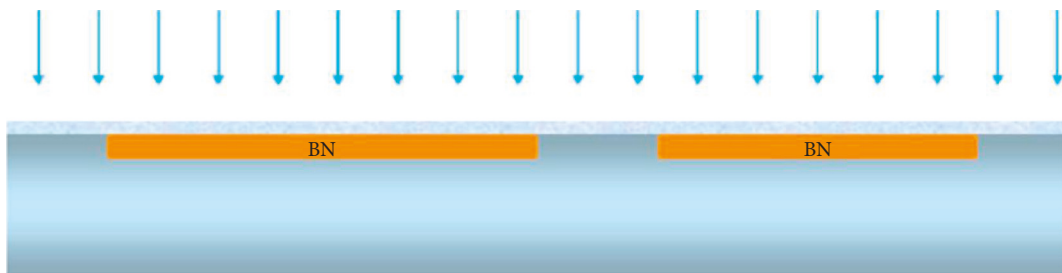


FIGURE 3: BN and BP process.

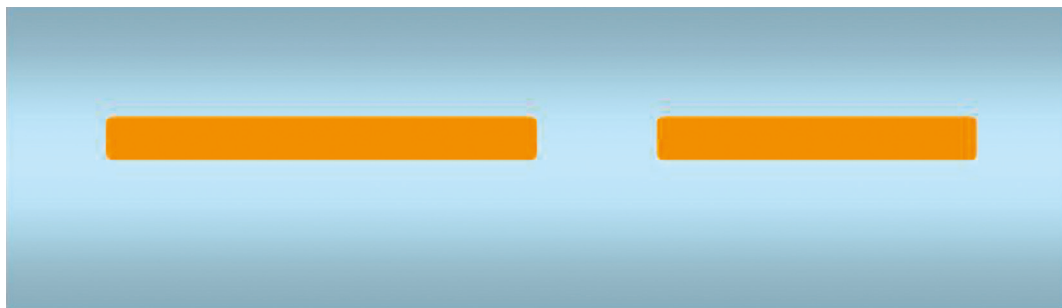


FIGURE 4: EPI loop process.

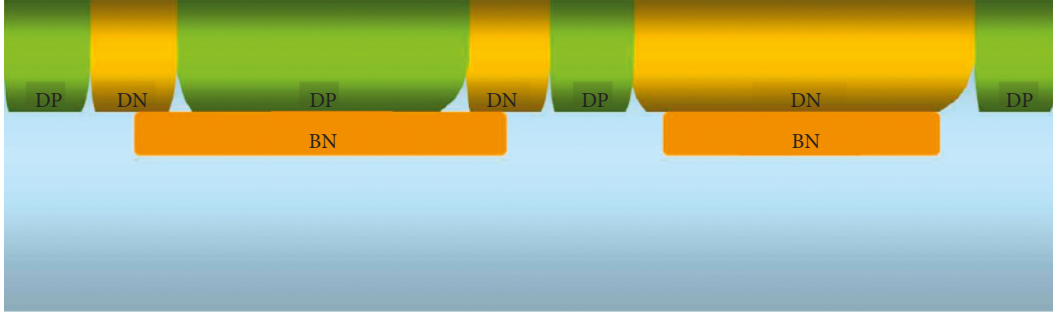


FIGURE 5: DN and DP loop process.

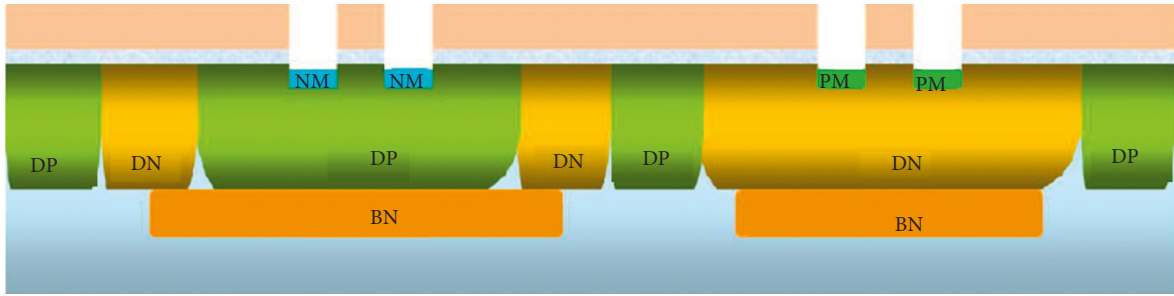


FIGURE 6: PM and NM loop process.

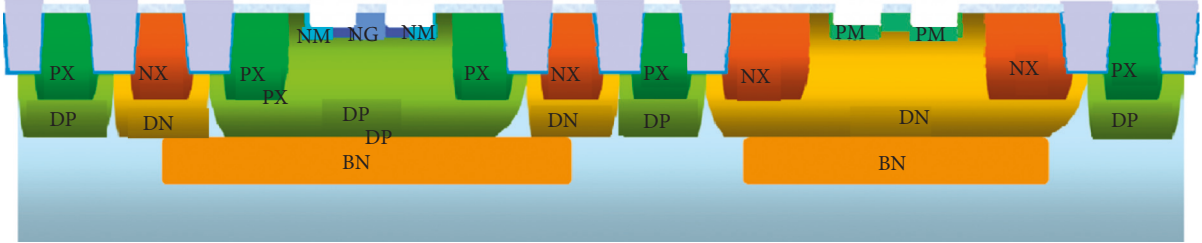


FIGURE 7: 5 V N/P-well.

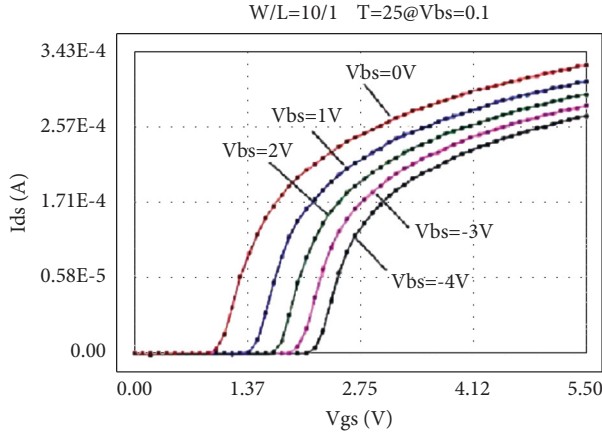
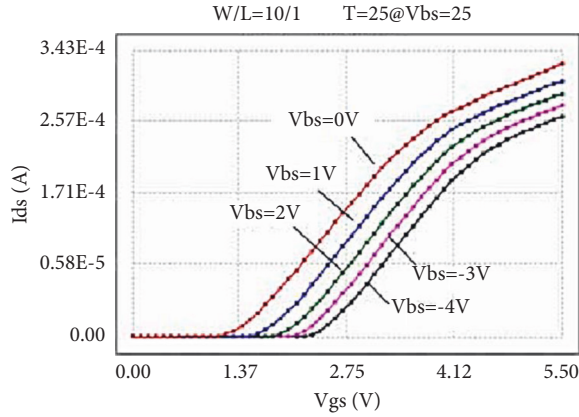
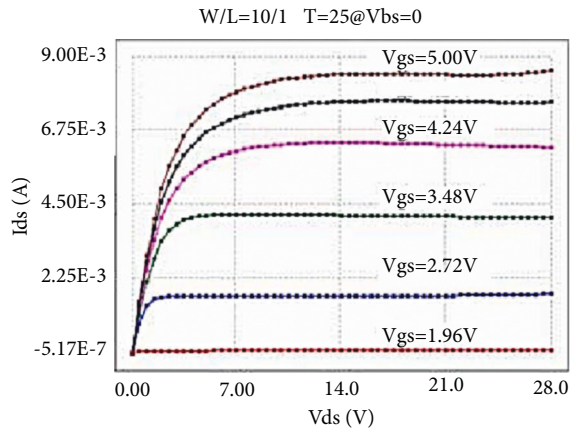
In the process of making high-voltage LDMOS, a 5 V N/P-well process is sometimes inserted, as shown in Figure 7. This process sequentially performs high-voltage N-well lithography, high-voltage N-well implantation, high-voltage P-well lithography, and high-voltage P-well implantation. This process can be used to adjust the threshold voltage V_t of high-voltage LDMOS.

3.2.2. Special Effects of LDMOS Devices. LDMOS is a MOS device with a special structure. When applied to low voltage, it has the characteristics of general MOS devices. For example, when $V_{ds} = 0.1$ V, the subthreshold region characteristics and transfer characteristics of LDMOS are similar to those of ordinary MOS. However, LDMOS devices are usually designed for high-voltage applications, which determines their device characteristics that are different from ordinary MOS devices. Due to the application of high voltage, the high electric field inside the LDMOS device makes it exhibit some special effects, such as quasi-saturation effect, self-heating effect, and impact ionization effect.

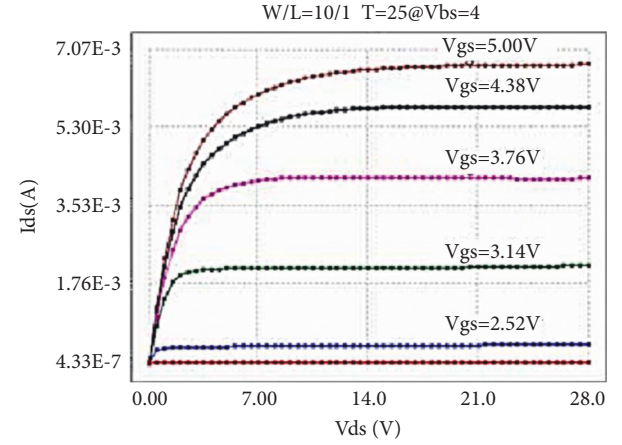
In fact, some of these special effects also appear in low-voltage MOSFETs, such as self-heating effects and impact ionization, because the electric field strength in low-voltage MOSFETs can become quite large as the channel length decreases [20–22].

4. LDMOS Modeling

4.1. General Drift Region Modeling. This research mainly studies the drift region modeling of LDMOS based on the BSIM4 model, taking a 0.18 μm 25 V BCD process platform as an example. The LDMOS drift region is equivalent to a voltage-controlled resistor controlled by gate voltage and drain voltage. Using a voltage-controlled resistor to model the LDMOS drift region, the model is relatively simple, which can not only ensure high accuracy, but also make the calculation converge quickly; by considering the depletion of the N-well in the LDMOS drift region, the JFET effect is formed, and a JFET is used, with device and a drift region resistor to model the drift region. An equivalent circuit is used to model the LDMOS drift region.

FIGURE 8: Transfer characteristic at $V_{ds} = 0.1$ V.FIGURE 9: Transfer characteristic at $V_{ds} = 25$ V.FIGURE 10: Output characteristics at $V_{bs} = 0$ V.

The LDMOS is tested for electrical characteristics, mainly to test the transfer characteristics and output characteristics. The test conditions are as follows: when the drain voltage V_{ds} is 0.1 V and 25 V, respectively, the gate voltage V_{gs} step size is 0.1 V, and the maximum voltage is 5.5 V for transfer characteristics; when the substrate bias V_{bs}

FIGURE 11: Output characteristics at $V_{bs} = -4$ V.

is 0 V and -4 V, respectively, there are output characteristics with a drain voltage step size of 0.5 V and a maximum voltage of 28 V at V. The test results are as follows: the threshold voltage V_t is 0.95 V, and the operating voltage ion is 8.46 mA. The curves obtained from the test are as follows: the transfer characteristic curve at $V_{ds} = 0.1$ V as shown in Figure 8, the transfer characteristic curve at $V_{ds} = 25$ V as shown in Figure 9, and the transfer characteristic curve at $V_{bs} = 0$ V as shown in Figure 10. The output characteristic curve and the output characteristic curve when $V_{bs} = -4$ V are shown in Figure 11.

When the external bias is small, the resistance of the channel region accounts for the main part, and the resistance of the drift region is less affected by the external bias, which can be regarded as a constant resistance. When the device is applied to a high-voltage bias, the current channel of the drift region becomes narrow, and the resistance increases rapidly, which is much larger than the resistance of the channel region. At this time, most of the voltage drop falls on the drift region. It can be seen that, in the whole working area, the voltage at the node Di in Figure 12 is always kept at a low value, and the internal MOS with Di as the intrinsic drain is little affected by the external high-voltage bias. Therefore, the method of subregional modeling can be used to separate the channel region and the drift region and establish the equivalent circuit diagram as shown in Figure 12. The channel region model still uses the original BSIM4 model, only the drift region needs to be modeled, and the two together constitute the LDMOS model.

4.2. Modeling of Special Effects. Due to the special structure and application in high-voltage applications, high-voltage LDMOS devices exhibit some special effects different from ordinary MOSFET devices, such as quasi-saturation effect and self-heating effect. In order to accurately describe the electrical characteristics of LDMOS, it is necessary to establish appropriate models for these special effects.

4.2.1. Quasi-Saturation Effect Model. LDMOS devices usually operate at high voltages, and the quasi-saturation effect is one of its common special effects. As shown in

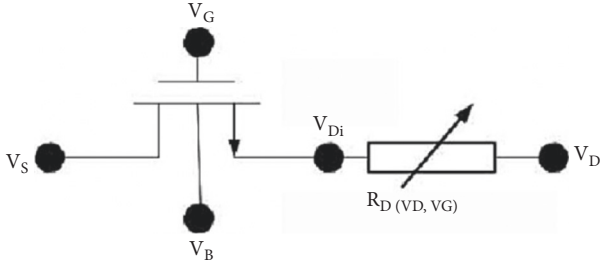


FIGURE 12: LDMOS equivalent circuit diagram.

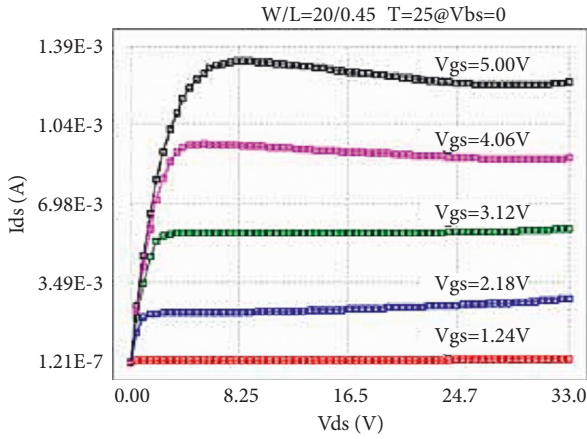


FIGURE 13: 30 V LDMOS output characteristics.

Figure 13, when the gate voltage is relatively large, if the drain voltage is relatively small, the LDMOS device is in the linear region, and the drain current increases linearly with the drain voltage; and when the drain voltage is very large, the drain current basically does not change with the drain voltage; that is, it enters the saturation region. Between the linear region and the saturation region, there is a transition region, and the drain current increases slowly with the drain voltage, which is the quasi-saturation region. This is due to the fact that the intrinsic MOS is not yet saturated, and the drift region carriers are the first to reach velocity saturation. In the quasi-saturation region, the intrinsic MOS is in the linear region and the drift region reaches speed saturation. The increase of the gate voltage V_{gs} will not significantly increase the drain current. At this time, the influence of the gate bias on the drain current is relatively small. Therefore, a voltage-controlled resistor controlled by the gate and drain voltages can be used to model the quasi-saturation effect.

4.2.2. Self-Heating Effect Model. Self-heating effect refers to the effect that the temperature of the device itself increases due to the heat generated by the power loss when the LDMOS device operates at high voltage and high current. Self-heating effects generally appear in devices operating at high power, and the increase in device temperature will affect its electrical properties, such as threshold voltage, mobility, and velocity saturation effects. Self-heating effect is

a relatively common physical phenomenon in LDMOS devices. As shown in Figure 13, it is the output characteristic curve of a 30 V LDMOS. Five different gate voltages were tested, the offset was 0, and the maximum drain voltage V_{ds} was measured to be 1.1 times its operating voltage. It can be seen from the figure that when the gate voltage is small or medium, there is no obvious difference from the output characteristics of ordinary MOS. However, when V_{gs} is greater than 4 V, in the saturation region, with the increase of V_{ds} , the drain current gradually decreases, and an obvious self-heating effect appears. Therefore, it is necessary to consider establishing the self-heating effect model of LDMOS.

5. Implementation of LDMOS Model Based on WGAN

The LDMOS model established in this study is relatively independent of its intrinsic MOS part and drift region part, and the Verilog-A language model of BSIM4 has been developed. Therefore, some changes can be made on the basis of the BSIM4 model to complete the modeling of LDMOS.

5.1. Drift Zone Model. Since the LDMOS channel region and the drift region are modeled separately, the drift region model has little effect on the channel region model. In order to make the model more extensible, a resistor can be added between the internal node (Si) and the external node (S) of the source. It is very helpful for the realization of the model. In addition, there is a resistor controlled by the gate voltage between the internal and external nodes of the source and drain terminals in BSIM4, which has little effect on the resistance of the drift region and can correct the model and retain it. Based on this, the Verilog-A model of BSIM4 is modified as follows: Define the input parameters. Define the model parameters that need to be tuned, such as

- (i) parameter real rcdw0 = 0;
- (ii) parameter real rcsw0 = 0;
- (iii) parameter real crd = 0;
- (iv) parameter real crs = 0;

5.1.1. Define Variables

- (i) Real rd, rs.
- (ii) Real BSIM4rcdw0, BSIM4rcsw0, BSIM4crd, BSIM4crs.

5.1.2. Establish the Drift Region Resistance Model: Taking the Drain Side as an Example, the Source Side Is Similar

- (i) $rd_tfac = 1 + BSIM4tcrd1 * delTemp + BSIM4tcrd2 * delTemp * delTemp;$
 $T0 = pow((BSIM4crd + BSIM4wcrd/w) * V(d, di), BSIM4eta);$
- (ii) $T1 = BSIM4prwbd * V(s, b);$

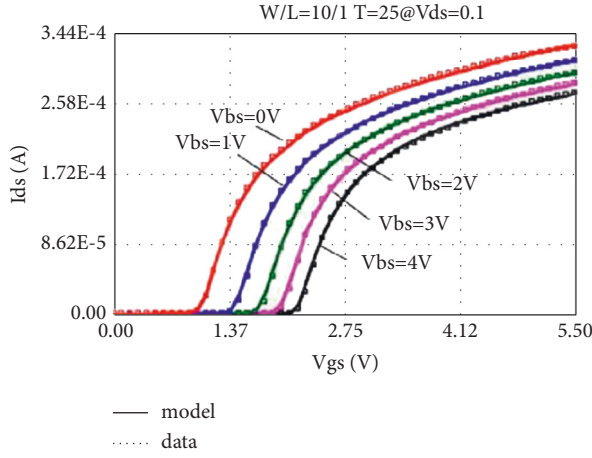


FIGURE 14: Transfer characteristics of BSIM4 model fitting ($V_{ds}=0.1$ V).

$$(iii) \quad T2 = 1/(1 + BSIM4prwgd * abs(V(g, s))); \quad T3 = pow(w_{eff} * 1E6, BSIM4wrdr); \quad rd = BSIM4rcdw0 * (T0 * (T1 + T2) + 1)/T3 * rd_{tfac}; \quad Rd = Rd + rd.$$

5.1.3. Branch Current Contribution. The effect of drift region resistance on drain current is achieved by the following expression: $I_{ddi} = V(d, di) * (BSIM4drainConductance / (1 + Rd * BSIM4drainConductance))$; $I(d, di) <+ I_{ddi}$; so far, the more important and difficult part of the LDMOS model, the drift region model, has been modified. Next, the model parameter extraction software MBP can be used to extract parameters from the built VA model. Whether the device model is accurate or not not only depends on whether the model itself is accurate enough, but also is closely related to the extraction of model parameters. In fact, if the device model is very accurate, but the extracted model parameters are not accurate enough; the simulation results often have large errors with the measured data. It can be seen that accurate model parameter extraction is very important for the device model.

Through the above method, the transfer characteristic curves of $V_{ds}=0.1$ V at normal temperature adjusted by the original BSIM4 model and the new LDMOS model are shown in Figure 14 and Figure 15, respectively.

By comparing the simulation results of the transfer characteristics of the two models after adjustment, it can be found that, at a lower drain voltage bias, both the BSIM4 model and the LDMOS model can achieve better results.

5.2. Self-Heating Effect Model. Self-heating effect is a special effect of high-voltage devices, which makes the saturation region of the output characteristic curve of LDMOS devices working in high-voltage state not straight, but slightly downward; that is, a negative resistance phenomenon occurs. Here, a 30 V NLD MOS is used as an example to illustrate the realization of the self-heating effect model. The curve fitting of the BSIM4 model without considering the self-heating effect is shown in Figure 16. Compared with the measured data (dotted line), the model curve (solid line) has

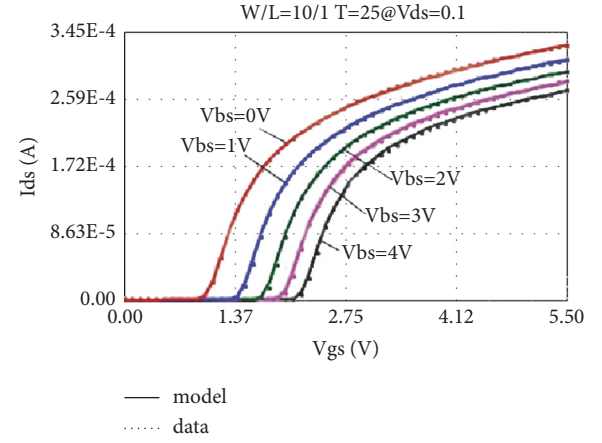


FIGURE 15: Transfer characteristics fitted by the LDMOS model ($V_{ds}=0.1$ V).

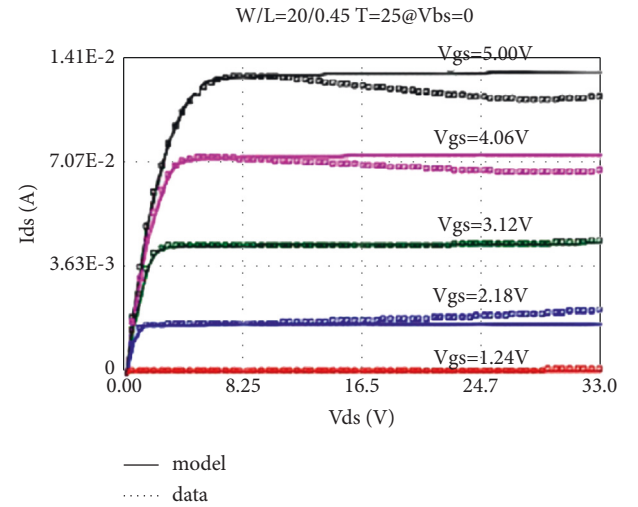


FIGURE 16: Output characteristics without considering self-heating effect ($V_{bs}=0$ V).

a relatively large deviation, and the trend of output current decline cannot be fitted.

The self-heating effect is achieved by contributing the self-heating effect to the drain current in the form of a drain current drop. The specific implementation method is as follows.

5.2.1. Definition of Parameters and Variables

- (i) Parameter real Kth = 'NOT_GIVEN'; parameter real Rth0 = 'NOT_GIVEN'.
- (ii) Parameter real Rti = 'NOT_GIVEN'.
- (iii) Real BSIM4Kth, BSIM4Rth0, BSIM4Rti, vdese.
- (iv) Integer BSIM4KthGiven, BSIM4Rth0Given.

5.2.2. Assign Values to Intermediate Variables

- (i) $BSIM4Kth = Kth$.
- (ii) $BSIM4Rth0 = Rth0$.

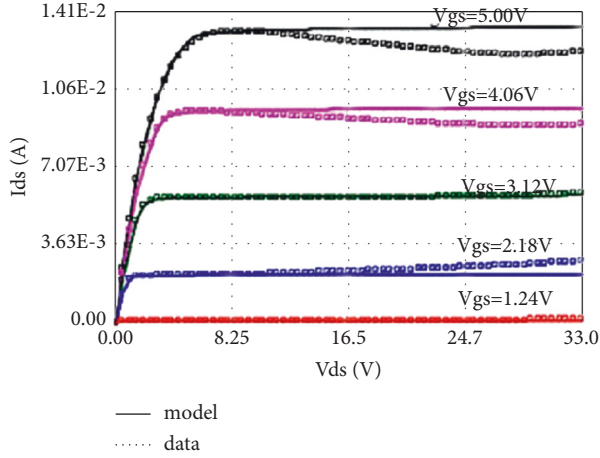


FIGURE 17: Output characteristics considering self-heating effect ($V_{bs} = 0$ V).

(iii) $BSIM4Rti = Rti$.

5.2.3. If the Parameter Is Not Initialized, It Needs to Be Given a Default Value

(i) $BSIM4KthG \text{ iven} = (BSIM4Kth == 'NOT_GIVEN') ? 0 : 1$.

(ii) $BSIM4Rth0Given = (BSIM4Rth0 == 'NOT_GIVEN') ? 0 : 1$.

(iii) $BSIM4RtiG \text{ iven} = (BSIM4Rti == 'NOT_GIVEN') ? 0 : 1$.

(iv) If ($!BSIM4KthGiven$).

(v) $BSIM4Kth = 1$.

(vi) If ($!BSIM4Rth0Given$) $BSIM4Rth0 = 1$.

(vi) If ($!BSIM4RtiGiven$) $BSIM4Rti = 1$.

5.2.2. Establish a Self-Heating Effect Model

(i) $v_{dese} = \text{abs}(V(s, si)) + \text{abs}(V(di, si)) + \text{abs}(V(d, di))$;

(ii) $T0 = BSIM4Rti * c_{drain} * T_{nom}$; $T1 = T0 * v_{dese}$;
 $T2 = T_{nom} + T1 * BSIM4Kth$;

(iii) $T3 = BSIM4Rth0 - BSIM4Kth * T_{nom}$; $c_{drain} = 2 * T0 / (T2 + \sqrt{T2 * T2 + 4 * T1 * T3})$.

So far, the LDMOS self-heating effect model has been established. The self-heating effect model has few parameters, only three parameters Kth , Rti , and $Rth0$. The extraction of the parameters of the self-heating effect model is also very simple. First, fit the output characteristic curve without considering the self-heating effect and then adjust the three parameters of Kth , Rti , and $Rth0$ to make the output characteristic curve slope downward. Of course, this process may also need to be repeated several times. The adjusted output characteristic curve with self-heating effect is shown in Figure 17. By comparing with Figure 16, it can be found that the self-heating effect part of the model has been significantly improved.

6. Conclusion

LDMOS is an important high-voltage device in BCD process. It has been widely used because of its high-voltage resistance and strong driving ability. Therefore, it is particularly important to establish an accurate LDMOS model. Based on the LDMOS physical model established by theoretical analysis, this research rewrites the Verilog-A language model code and related neural network of BSIM4 to realize the LDMOS model. The first is to implement the drift region model. After defining the parameters and variables, a voltage-controlled resistor controlled by the gate voltage and the drain voltage is added to the original drain resistor, and the temperature effect is considered and optimized. The model fits well the output characteristic curve of a 25 V LDMOS at room temperature and the characteristic curves at different temperatures. For the self-heating effect, the thermal resistance and heat-capacitance network model is simplified, and only the influence of thermal resistance on the channel current is considered. The improved model is applied to a 30 V LDMOS, and the output with self-heating effect is well fitted. Although this paper implements the Verilog-A language modeling of LDMOS in general, there are still some deficiencies. Because the original BSIM4 model is used in the dynamic characteristic model, the gate drain capacitance without considering the drift zone capacitance is not accurate enough.

Data Availability

The dataset can be accessed upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

- [1] R. Raich, H. Qian, and G. T. Zhou, "Orthogonal polynomials for power amplifier modeling and predistorter design," *IEEE Transactions on Vehicular Technology*, vol. 53, no. 5, pp. 1468–1479, 2004.
- [2] D. Wang, M. Aziz, and F. M. Ghannouchi, "Augmented real-valued time-delay neural network for compensation of distortions and impairments in wt," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 30, no. 1, pp. 242–254, 2019.
- [3] B. J. Baliga, "Power integrated circuits-A brief overview," *IEEE Transactions on Electron Devices*, vol. 33, no. 12, pp. 1936–1939, 1986.
- [4] V. Ningaraju, H. C. Lin, P. Chen, and K. LunLin, "Design and optimization of 30V fully isolated nLDMOS with low specific on-resistance for HVIC applications - ScienceDirect[J]," *Solid State Electronics Letters*, vol. 1, no. 2, pp. 119–130, 2019.
- [5] W. Chen, B. Zhang, and Z. Li, "Novel SJ-LDMOS with Partial N-Buried Layer for SPIC Applications[C]," in *Proceedings of the 2006 8th International Conference on Solid-State and Integrated Circuit Technology*, vol. 3, Shanghai, China, October 2006.

- [6] O. Z. Alngar, W. S. E. Deeb, E. Sayed, and M. E. Rabaie, "On-line predistortion algorithm for nonlinear power amplifiers with memory effects based on real-valued time-delay neural network[C]," in *Proceedings of the 35th National Radio Science Conference (NRSC)*, pp. 338–344, IEEE, Cairo, Egypt, March 2018.
- [7] M. R. Šikonja, "Data generators for learning systems based on RBF networks[J]," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 27, no. 5, pp. 926–938, 2016.
- [8] D. Phartiyal and M. Rawat, "LSTM-deep neural networks based predistortion linearizer for high power amplifiers[C]," in *Proceedings of the 2019 National Conference on Communications (NCC)*, pp. 1–5, IEEE, Bangalore, India, February 2019.
- [9] W. Chen, B. Zhang, Z. Li, and Z. Liu, "A novel high voltage LDMOS for HVIC with the multiple step shaped equipotential rings," *Solid-State Electronics*, vol. 51, no. 3, pp. 394–397, 2007.
- [10] Y. Choi, C. Jeon, and M. Kim, "Design and process considerations for 1200V HVIC technology[C]," in *Proceedings of the IEEE International Symposium on Power Semiconductor Devices and Ics*, pp. 311–314, Barcelona, Spain, June 2009.
- [11] S. Hardikar, M. De Souza, Y. Z. Xu, T. J. Pease, and E. M. S. Narayanan, "A novel double RESURF LDMOS for HVIC's," *Microelectronics Journal*, vol. 35, no. 3, pp. 305–310, 2004.
- [12] T. Okawa, H. Eguchi, M. Taki, and K. Hammada, "2000 V SOI LDMOS with New Drift Structure for HVICs[C]," in *Proceedings of the International Symposium on Power Semiconductor Devices & Ics*, pp. 435–438, Prague, Czech, July 2016.
- [13] G. Charitat, M. A. Bouanane, and P. Rossel, "A self-isolated and efficient power device for HVIC's: RESURF LDMOS with SIPOS layers," *Microelectronic Engineering*, vol. 19, no. 1-4, pp. 149–152, 1992.
- [14] M. Yamaji, K. Abe, and A. Jonishi, "New level-shift LDMOS structure for a 600 V-hvic on thick SOI[J]," *Journal of Energy and Power Engineering*, vol. 6, no. 9, pp. 1515–1520, 2012.
- [15] B. Yi and X. Chen, "300 V ultra low specific on-resistance high-side p-LDMOS with auto-biased n-LDMOS for SPIC [J]," *IEEE Transactions on Power Electronics*, vol. 24, no. 10, p. 1, 2016.
- [16] B. Yi, J. Cheng, and X. B. Chen, "A high-voltage "Quasi-p-LDMOS" using electrons as carriers in drift region applied for SPIC," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3363–3374, 2018.
- [17] M. Yoshino, K. Shimizu, and T. Terashima, "A New 1200V HVIC with a Novel High Voltage Pch-MOS[C]," in *Proceedings of the 2010 22nd International Symposium on Power Semiconductor Devices & IC's*, pp. 93–96, IEEE, Hiroshima, Japan, June 2010.
- [18] T. Y. Huang, C. H. Huang, and C. F. Huang, "A novel 80V HS-DMOS with gradual-RESURF profile to reduce Ron_sp for high-side operation[C]," in *Proceedings of the 2017 29th International Symposium on Power Semiconductor Devices & Ics*, vol. 55, no. 5, pp. 1137–1142, Royton Sapporo, May.2017.
- [19] S. Liu, W. Sun, W. Wan, W. Su, S. Wang, and S. Ma, "Anomalous hot-carrier-induced linear drain current degradation of LDMOS under pulse gate stress with different amplitudes," *IEEE Electron Device Letters*, vol. 34, no. 6, pp. 786–788, 2013.
- [20] H. Fujii, T. Mori, and T. Ipposhi, "A recessed gate LDMOSFET for alleviating HCI effects[C]," in *Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices & Ics*, pp. 167–170, Prague, Czech, July 2016.
- [21] W. Sun, C. Zhang, S. Liu, and L. Shi, "Hot-carrier-induced on-resistance degradation of n-type lateral DMOS transistor with shallow trench isolation for high-side application[J]," *IEEE Transactions on Device & Materials Reliability*, vol. 15, no. 3, pp. 458–460, 2015.
- [22] S. Liu, W. Sun, C. Zhang, and X. Ren, "OFF-state inrush-current-induced electrical parameter degradations for high-voltage lateral DMOS transistors," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3767–3773, 2015.