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# Chemical Vapor-Deposited Graphene on Ultraflat Copper Foils for van der Waals Hetero-Assembly

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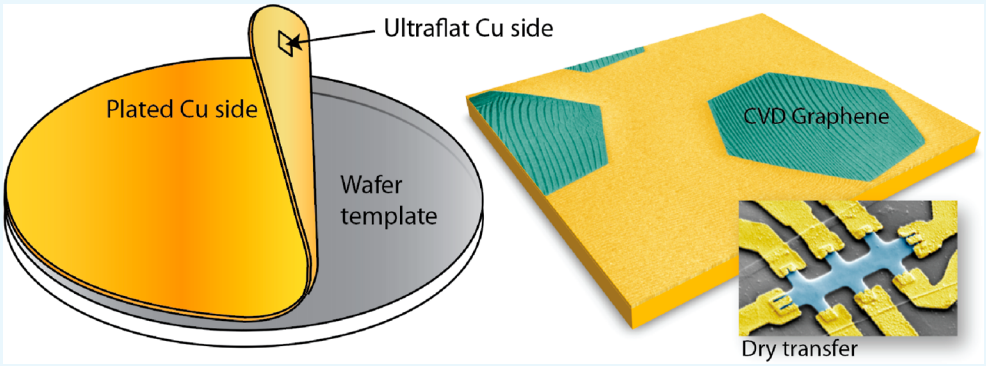


**ABSTRACT:** The purity and morphology of the copper surface is important for the synthesis of high-quality, large-grained graphene by chemical vapor deposition. We find that atomically smooth copper foils—fabricated by physical vapor deposition and subsequent electroplating of copper on silicon wafer templates—exhibit strongly reduced surface roughness after the annealing of the copper catalyst, and correspondingly lower nucleation and defect density of the graphene film, when compared to commercial cold-rolled copper foils. The "ultrafoils"—ultraflat foils—facilitate easier dry pickup and encapsulation of graphene by hexagonal boron nitride, which we believe is due to the lower roughness of the catalyst surface promoting a conformal interface and subsequent stronger van der Waals adhesion between graphene and hexagonal boron nitride.

## INTRODUCTION

Reliable fabrication of high-quality graphene is of utmost importance for its commercial use in electronics, photonics, sensors, and other application areas. The most widespread, scalable, and efficient method for single-layer graphene production is chemical vapor deposition (CVD) on copper (Cu) foils.[1] Commercially available cold-rolled copper foils tend to be rough on the microscale and may be surface-contaminated.[2] This can make the density of nucleation sites and the overall quality of graphene difficult to control, even for copper foils of nominally high purity,[3] which may contain other contaminants. The effect of surface impurities on nucleation density and CVD growth quality, as well as the methodologies to prevent or remove detrimental contamination-related effects, has been discussed extensively in the literature.[4−10]

In order to grow high-quality CVD graphene, copper pretreatments such as surface chemical etching or electropolishing[11] are combined with extended annealing in a reducing atmosphere to increase the catalyst grain size and reduce the graphene nucleation density. Growth recipes also have to be tuned specifically to suppress nucleation on such substrates.[12,13] Several studies[13,14] have shown how catalyst templating—the deposition of catalyst on an atomically flat surface such as a silicon wafer—can reduce the smoothness and increase the purity of the catalyst film. Yu et al.[13] showed improved graphene grain size and superior electrical properties over graphene from commercial copper foils, as measured in devices equipped with a liquid top-gate. This elegant approach combined the deposition of a thin (50 nm) layer of Cu onto a sapphire wafer, followed by electroplating of up to 25 $\mu$m copper. Mechanically peeling the copper layer off the substrate produces a bottom copper surface that inherits the smoothness and monocrystalline 111 orientation of the sapphire template, leading to an epitaxial growth of monocrystalline graphene.

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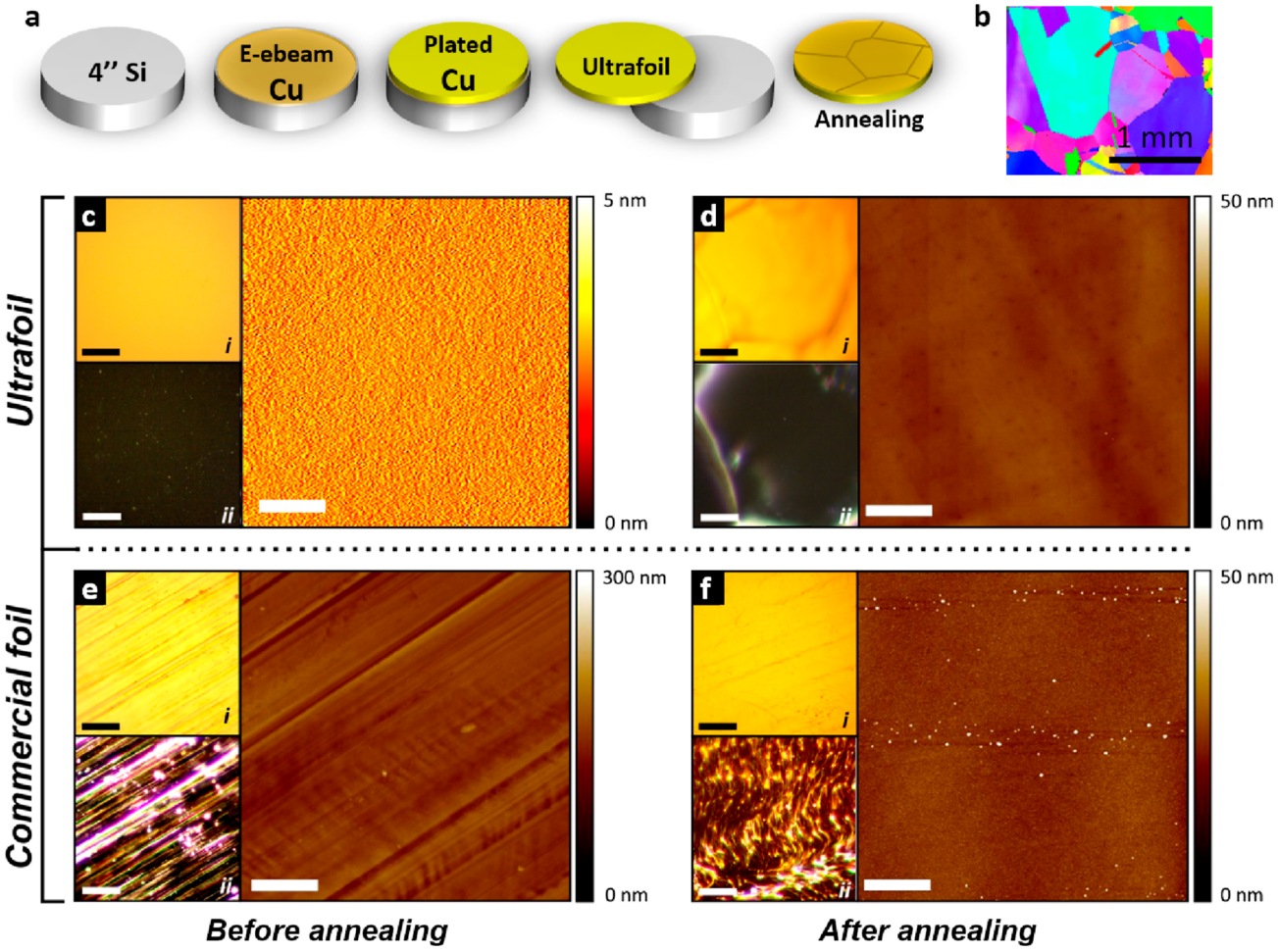


**Figure 1.** (a) Illustration of the ultrafoil fabrication process steps: e-beam evaporation, electroplating, delamination, and finally annealing of copper. (b) EBSD image of the ultrafoil sample after annealing. The full image is shown in Figure S1. (c,d) Ultrafoil substrates before and after annealing. The panel indicators (i), (ii), and (iii) show optical bright-field, dark-field (DF), and AFM images of the representative areas of each sample. (e,f) Commercial foils before and after annealing. The scale bars are 5 $\mu$m.

The method has been taken up and developed further by a number of studies,[15−25] most of which, however, involve the authors on the two original articles.[13,14] Considering the simplicity and attractive features of the "peel-off" or template method, the adoption by the research field is relatively low. We believe that deterministic growth is necessary for the maturation of high-level scalable applications, and deterministic growth substrates (crystallinity, purity, and morphology) could be key elements in achieving the ultimate consistency and quality needed for demanding future applications.

Here, we examine the peeling-off approach using standard silicon (Si) wafers as a template, colloquially terming the foils herein produced as "ultrafoils". We show ultralow postannealing surface roughness of the copper ultrafoils and find that nucleation density, catalyst grain size, graphene grain size, and defect density are consistently superior compared to graphene from commercial copper foils despite using identical growth conditions. We also show that the dry pickup technique demonstrated with CVD graphene[26] is not only possible but also far easier with ultrafoil-derived graphene as compared to commercial foils.

## MATERIALS AND METHODS

**Foil Preparation.** The steps in the fabrication process are illustrated in Figure 1a. The ultrafoil substrates were fabricated using a combination of a 1.5 $\mu$m thick high-purity (99.999%) copper film evaporated on a pristine 4″ Si wafer using an Alcatel electron beam (e-beam) evaporation deposition system.

**Electroplating.** This step was followed by a 10 $\mu$m thick low-stress copper film deposited by electroplating. The electrolyte consisted of very pure diluted sulfuric acid, copper sulfate, and a small amount of sodium chloride.[27] The deposition was performed in a 25 L tank at room temperature and with air agitation. To ensure low internal stress and relatively small crystal size of the deposited copper, pulse reversal plating was applied with alternating periods of 500 ms with copper dissolution (following the scheme called 4T2).[20] During the electroplating step, the sealing of the edges of the first copper layer is crucial to prevent the delamination of the e-beam-deposited initial copper layer and the Si wafer. The bilayer copper film is easily peeled off with a pair of tweezers after a rinse in water and drying with nitrogen. As a reference, Alpha Aesar 25 $\mu$m (99.8%) uncoated copper foil was used.

**Synthesis.** Graphene was grown by low-pressure CVD (5 mbar) in an Aixtron Black Magic cold wall CVD system. After



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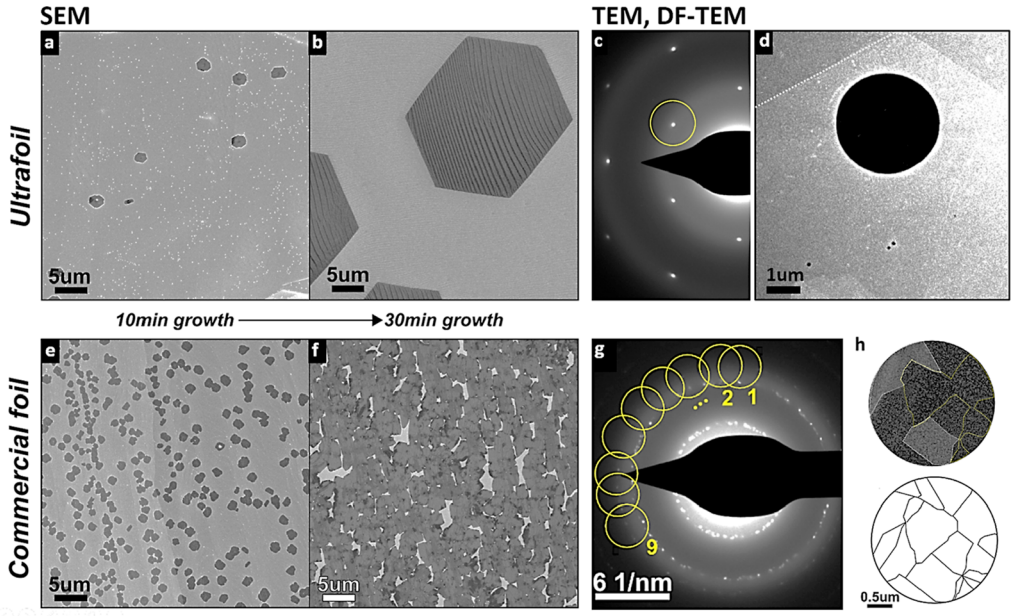


**Figure 2.** (a,b) SEM micrographs of the ultrafoil surface after 10 and 30 min graphene growth. (c) SAED diffraction spots show that the graphene flakes are single crystals. (d) Graphene flake covering a window in a TEM chip. (e,f) Commercial copper after 10 and 30 min graphene growth. (g) SAED image of a commercial foil with each ring, 1−9, being centered on selected diffraction spots, and (h) is the reconstructed grain structure based on nine such DF images.

15 min of annealing of the copper substrate in hydrogen (1000 sccm)/argon (700 sccm) at 1040 °C, growth was initiated by adding 1 sccm methane flow and maintained for various durations. The sample is then cooled under Ar flow by turning off the heaters. Detachment of graphene from the copper films was done by first letting copper oxidize in air, which took typically 1 day for commercial foils compared to 30 days for ultrafoils.

**Transmission Electron Microscopy.** Graphene grown on ultrafoils was transferred onto Quantifoil holey carbon grids by following the method described in ref 28. TEM was carried out in a FEI Tecnai T20 G2 system operated at 200 kV with a Gatan US1000 CCD camera. In DF transmission electron microscopy (DF-TEM), an objective aperture placed in the back focal plane is used to select certain reflections of the crystalline sample. By tilting the electron beam, reflections with different reciprocal lattice vectors are centered within the objective aperture. These diffracted beams contribute to the DF image, and crystalline areas that cause these beams appear bright in the DF image. The procedure is described in ref 29. A Thermo Fisher DXR Raman microscope equipped with a 532 nm laser source is used to acquire Raman spectra from the two graphene samples transferred to the $SiO_2$/Si substrate (900 points per sample; step size, 1 $\mu$m).

**Electron Backscatter Diffraction.** Electron backscatter diffraction (EBSD) images were acquired using a FEI Nova 600 NanoSEM system with a Bruker EBSD detector. Data were collected with a 10 $\mu$m step size. During EBSD collection, the probe current was 3.9 nA, the accelerating voltage was 15 kV, and the angle of incidence was 70°. Scanning electron microscopy (SEM) images were recorded in a Zeiss Supra 40VP instrument operated in in-lens detection mode at 5 keV. Atomic force microscopy (AFM) images were recorded in a Bruker Dimension Icon-PT instrument.

## RESULTS

As well documented in the literature, the catalyst grain size distribution is important for consistent, high-quality growth, with larger grains promoting epitaxial growth and reducing defect rates.[30,31] After annealing, EBSD revealed that the ultrafoil substrates display copper grain sizes in the 0.1−2 mm size range (Figure 1b). Figure 1c,d shows the copper foil before and after annealing. The optical microscope images in both normal (i) and DF (ii) modes are featureless, while AFM images show roughly 0.8 nm rms roughness before annealing. After annealing, the ultrafoil maintains a smooth surface (Figure 1d) with an rms of ∼1.2 nm and clearly visible metal grain boundaries in optical microscopy [see (i) and (ii)]. The commercial foils exhibited an rms roughness of ∼96 nm before growth, which decreased to ∼68 nm after growth, with clear signs of step-bunching[32] [see Figure 1f, panel (ii)] and particle precipitation seen as point-like protrusions in the AFM image.

Figure 2 shows two stages of graphene partial growth (10 and 30 min) on an ultrafoil (Figure 2a,b) and a commercial foil (Figure 2e,f) under identical growth conditions. Lower nucleation density on the ultrafoil leads to well-separated hexagonal graphene flakes even for relatively long growth times of up to 30 min and enables monocrystalline graphene regions 2 orders of magnitude larger than that on commercial foils before the graphene domains coalesce (see Figure 2a,e).

The graphene grain size distribution was investigated by TEM and selective area electron diffraction (SAED) analyses.[29] Graphene grown on ultrafoils and transferred to Quantifoil amorphous carbon support films exhibited diffraction patterns such as that shown in Figure 2c, showing the investigated area to be single crystals. Figure S2 shows that this is the case across the hexagonal domain and that the edges are zigzag-oriented. In contrast, the polycrystalline structure of graphene grown on commercial foils is apparent from the diffraction pattern shown in Figure 2g, with several monocrystalline graphene diffraction patterns rotated and


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superimposed. Following the procedure in ref 29, the individual grains within the freestanding graphene area are reconstructed from several SAED images (see Figure 2h). The defect density of the grown graphene films on the two different substrates was investigated by Raman spectroscopy across 30 × 30 $\mu$m areas (see Figure S3). Statistics of 900 spectra for each type of substrate shows a vanishing D-peak with the average Raman peak intensity ratio $I(D)/I(G)$ = 0.064, while the corresponding value for the commercial foil was $I(D)/I/(G)$ = 0.38.

To encapsulate the graphene films in hexagonal boron nitride (hBN), we follow the procedure described in ref 33 (see Figure 3a–f). First, 20–50 nm thick hBN flakes are

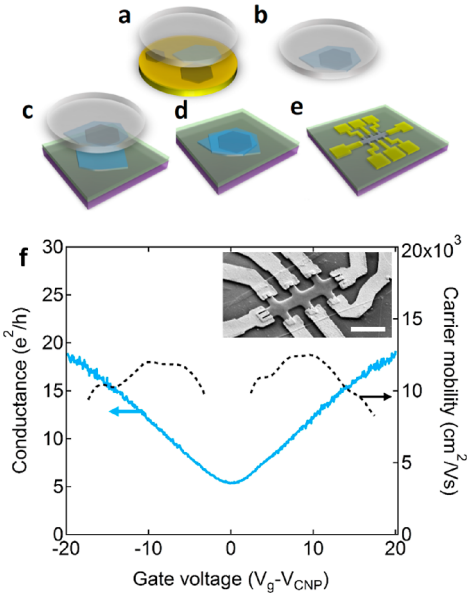


**Figure 3.** (a,f) Schematic of the device fabrication procedure, where (a) hBN crystal is dropped down on a hexagonal graphene domain using a PDMS/PPC stack. (b) Removal of copper was done by dry pickup from copper or alternatively by etching of copper in $FeCl_3$. (c) hBN–graphene stack is then deposited on a second hBN layer to complete the encapsulation (e). (f) Hall bar is defined by RIE etching and contacted by Cr/Au. The inset shows a SEM micrograph of a device fabricated by dry pickup. The scale bar is 2 $\mu$m. (h) Sheet conductance (green curve) and carrier mobility (dashed curve) versus gate voltage.

mechanically exfoliated on oxidized Si surfaces,[34,35] which are subsequently picked up with PDMS/PPC films, following the procedure in ref 36. With this procedure, we fabricated five devices from ultrafoil-grown graphene. In comparison, we were not able to fully pick up the graphene flakes grown on commercial copper foils; these crystals were either partly transferred or not at all (not shown). In both cases, the copper foils were oxidized before attempting the pickup. It should be stressed that different preparation techniques could lead to a higher success rate also for graphene grown on commercial foils, as previously demonstrated here by Banszerus et al.[26]

After pickup, hBN/graphene is then released onto another hBN flake, cleaved onto $SiO_2$, to fully encapsulate graphene without contact with water, solvents, or polymers.[37,38] After defining the device region by lithography and plasma etching, graphene is contacted with Cr/Pd/Au via the resulting exposed 1D edge.[38] Figure 3f shows the conductance versus gate voltage for such a device, where a voltage corresponding to a background doping of 2.6 × $10^{12}$ $cm^{-2}$ has been subtracted. The field effect mobility $\mu = C^{-1}(dG/dV_g)(L/W)$ for the device is around 12,000 $cm^2/V$ s for both electrons and holes. $C$ is the capacitance per area, while $W$ and $L$ are the device width and voltage probe distance, respectively.

## DISCUSSION

The production of copper foils through a combined physical vapor deposition and electrodeposition process, and using silicon as a template, enables the fabrication of copper catalyst layers with a very low surface roughness after annealing, even when compared to previous work.[13,14] The presence of particles and contaminants in commercial foils can have a serious impact on the graphene growth dynamics,[3,39] as impurity particles generally increase the catalytic reactivity of the copper surface, increasing the number of nucleation points during growth.

While a room-temperature carrier mobility of around $10^4$ $cm^2/V$ s for hBN-encapsulated devices cannot be considered exceptionally high, we note that dry pickup from of graphene flakes from the nanometer-smooth catalyst surface is not only possible but also significantly easier than that with a commercial foil, which suggests that the surface morphology of copper plays an important role in nondestructive transfer. We speculate that this could be due to the conformal contact with hBN, facilitated by the nanometer-smooth copper surface. The dimensions of the catalyst layer possible with this technique are limited only by the size of the templating wafer used.

One striking characteristic of the ultrafoil films is the absence of visible features outside the flakes, while inside the flakes, the step-bunches are nearly periodically spaced. We see this as an indicative of a very uniform interface compared to what is achieved by common surface treatments including electropolishing surfaces. An elegant *in situ* SEM study by Wang et al.[40] shows the evolution of surface transformations below CVD-grown graphene, leading to pronounced step-bunching appearing under the flakes during the cooling process. The step-bunching in our flakes is, however, far more uniform in appearance, which we attribute to the flatness and absence of features on our catalytic surfaces.

The process of oxidizing copper is a prerequisite for dry pickup, and one drawback of the ultrafoil is the longer oxidation time. Ambient air surface oxidation of the copper foil underneath the graphene progresses via a defined set of stages: (1) intercalation of water between graphene and copper, (2) oxidation of the copper surface to form $Cu_2O$, and (3) passivation of the copper surface against further oxidation by the $Cu_2O$ passivating layer. In this case, the oxide thickness and roughness do not progress further with ambient oxidation after the formation of this passivating oxide layer. Therefore, while ultrafoils require a longer time to fully oxidize [owing to a slower step (1)], any modifications to the resulting surface roughness are equally represented in both foils—given the self-passivating nature and thickness of the oxide−−and thus can be considered as accounted for (see ref 41). Also, Zhang et al. found that the surface roughness did not increase during oxidation under the CVD graphene film from 10 to 60 min.[42]

An intriguing aspect of the "peeling off" process is that the combination of the electroplating/PVD processes allows a wide variety of metals to be turned into pure, high-quality, atomically smooth foils, which facilitates the growth of graphene and other 2D materials with much reduced intrinsic


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nucleation density. Furthermore, flat and defect-free foils appear to facilitate the otherwise challenging dry pickup of graphene crystals from copper foils.[26] This is not at all obvious: the adhesion of graphene to copper foils is a complicated issue, depending on the catalyst crystal orientation, grain size, and oxidation of copper below graphene;[43] however, we find the ultrafoil approach a highly promising route to reduce the number of free parameters in the complex process of dry lamination and thereby an important step toward deterministic, large-scale van der Waals heterostructures.

Future work should benchmark the ultrafoils against a broader range of catalyst foils, such as other metals and alloys, as well as other deposition methods and surface treatments[44] such as chemical etching, physical polishing,[45] electropolishing,[11,46−48] annealing,[30] and resolidification.[49] It would also be interesting to compare our high-end e-beam evaporation/electroplated copper foils with commercial electroplated foils to see if the latter, cheaper solution could generate high-quality growth results as well, despite the template having a rougher substrate. We also note that the commercial and electroplated foils compared in this work were of different thicknesses (25 and 10 $\mu$m, respectively). While we find it unlikely that the thickness difference could account for the striking difference in the results for commercial and templated foils, a study of the thickness dependence on the performance of ultrafoils would nevertheless be relevant to carry out.

## ■ ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.2c01946.

EBSD image of ultrafoil graphene, showing the color codes corresponding to the copper crystal orientations [001], [101], and [111] after growth; histogram of copper crystal domain sizes showing a large number of domains in the 200 $\mu$m range and a few domains up to millimeter size; partial growth of two graphene flakes grown together, the step-bunching clearly visible under the graphene flakes; graphene flakes across a grain boundary with a secondary layer growth; DF-TEM images of polycrystalline graphene grown on commercial foil and suspended over a 2 $\mu$m aperture in an amorphous carbon support selected-area diffraction pattern; positions of the objective aperture; selected area aperture chosen to cover the entire suspended graphene region; map of grain boundaries; DF TEM image of monocrystalline graphene grown from an ultrafoil suspended over a 2 $\mu$m aperture in an amorphous carbon support;; montage of DF TEM images of large areas of graphene grown on an ultrafoil; Raman spectra recorded in 30 × 30 $\mu$m area, showing the $I(2D)/I(G)$ peak intensity ratio, the $I(D)/I(G)$ peak intensity ratio, and the full width at half-maximum of the 2D peak, for both ultrafoil and commercial foil (PDF)

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### Author Contributions

F.P. conceived the experiment and carried out the synthesis and characterization and wrote the first draft of the manuscript. L.G., B.S.J., N.P., and J.M.C. fabricated the electrical devices and performed the electrical measurements. P.R.W. and A.S. assisted in interpreting the results. J.K. carried out the TEM work. P.T.T. carried out the electroplating process. R.M. assisted in the preparation of ultrafoils. A.A., P.B., J.H., T.J.B., and P.B. supervised the technical aspects of the project. F.P., A.S., and P.B. wrote the manuscript. All authors contributed to editing the manuscript.

### Notes

The authors declare no competing financial interest.

Data Availability: The data that support the plots within this paper and other findings in this study are available from the corresponding author upon reasonable request.

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