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All-2D ReS_2 transistors with split gates for logic circuitry

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Two-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs) and black phosphorus, are the most promising channel materials for future electronics because of their unique electrical properties. Even though a number of 2D-materials-based logic devices have been demonstrated to date, most of them are a combination of more than two unit devices. If logic devices can be realized in a single channel, it would be advantageous for higher integration and functionality. In this study we report high-performance van der Waals heterostructure (vdW) ReS_2 transistors with graphene electrodes on atomically flat hBN, and demonstrate a NAND gate comprising a single ReS_2 transistor with split gates. Highly sensitive electrostatic doping of ReS_2 enables fabrication of gate-tunable NAND logic gates, which cannot be achieved in bulk semiconductor materials because of the absence of gate tunability. The vdW heterostructure NAND gate comprising a single transistor paves a novel way to realize "all-2D" circuitry for flexible and transparent electronic applications.

Ultrathin two-dimensional (2D) semiconducting materials are useful for a number of electronic applications because of their unique properties originating from their atomically thin nature[1–5]. Among them, transition metal dichalcogenides (TMDs) have been actively studied as channel materials because of absence of short-channel effect[6,7]. It has been anticipated that a scale-down limit can be overcome by 2D semiconductors for higher integration of electronic devices. In this regard, "all-2D" devices comprising only 2D materials, *i.e.*, van der Waals heterostructure (vdW) devices, have been demonstrated[8–11]. As emerging 2D materials, rhenium-based TMDs, such as ReS_2 or $ReSe_2$, have exhibited promising properties. Typically, few-layer TMDs outperform monolayer in terms of carrier mobility, while the band structure of TMDs transforms from direct to indirect band structure as the thickness changes from monolayer to few-layers, which limits their use for optoelectronic applications[12]. However, ReS_2 and $ReSe_2$ exhibit direct band structure at all thickness because of the distorted 1 T' structure and weak interlayer coupling[13]. Despite the unique properties of ReS_2 and $ReSe_2$, there have been only limited studies on them, which reported preliminary results of transistors and photodetectors based on ReS_2 and $ReSe_2$ with conventional device geometry[14–19].

To improve the device performance of 2D semiconductors, contact resistance and carrier scattering should be reduced. Significant contact resistance between deposited metal and 2D semiconducting channels severely deteriorates device performance due to the Fermi level pinning at the interface[20], which makes it difficult to utilize the 2D semiconductors for practical applications required by the industry. In addition, because the band gap of TMDs increases with decreasing thickness, the Schottky barrier height for monolayer TMDs is significantly higher than that for few-layer TMDs, leading to a lower field-effect mobility[21,22]. The use of graphene electrodes has been considered as a solution because of the de-pinning of the graphene Fermi level and absence of chemical bonds at a stacked heterointerface of 2D layers[23]. In addition, it has been shown that hexagonal boron nitride (hBN), used as an ultraflat dielectric, suppresses charged impurity scattering, resulting in enhanced carrier mobility of hBN-encapsulated 2D materials[9,11,24].

A number of logic devices based on 2D materials have been demonstrated by combinations of two different 2D transistors: n-type and p-type[5,25–28]. Even though the NMOS inverters using ReS_2 have been demonstrated[19,27], all of the logic devices reported so far are made of double devices (two connected devices). Therefore, for higher

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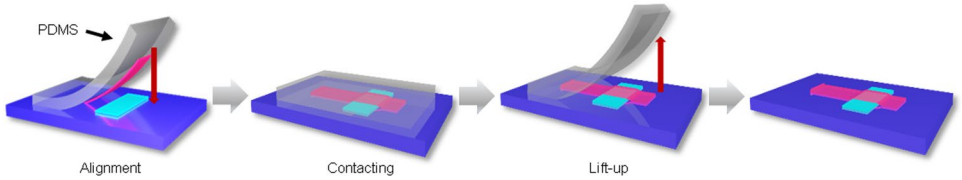

Figure 1. PDMS stacking process for fabrication of vdW heterostructure. The flake exfoliated directly on PDMS is aligned with a target flake on the SiO_2 substrate. The PDMS stamp is smoothly lowered for conformal contact onto the bottom target flake on the substrate. The lift-up process follows after five minutes.

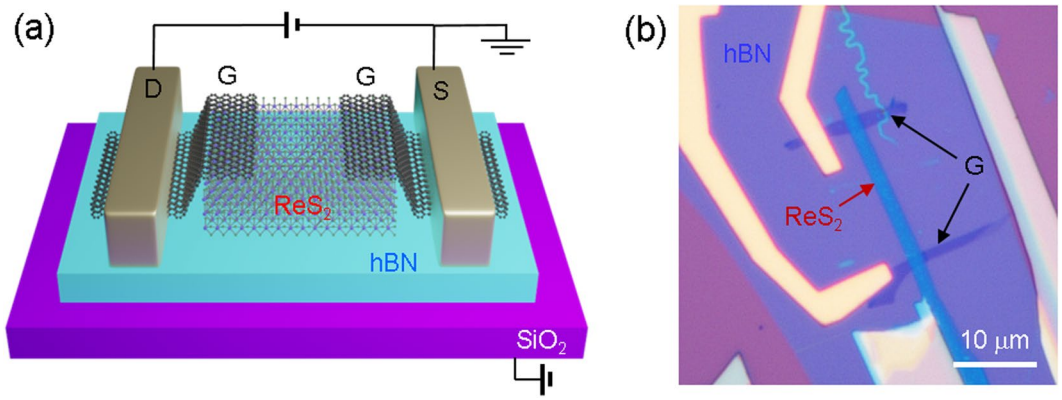

Figure 2. ReS_2 FET with graphene contacts and hBN dielectric. (**a**) Schematic of ReS_2 FET fabricated by stacking process. (**b**) Optical microscope image of fabricated tri-layer ReS_2 FET. Because of anisotropic transport of ReS_2, the elongated ReS_2, which is longer along the *a*-axis, is selected as a channel.

integration and functionality, a novel device geometry is required for logic devices. Because atomically thin 2D materials are highly sensitive to electric fields with no screening effect, it is possible to locally tune the densities and types of carriers, leading to electrically controlled p-n junction devices comprising graphene or WSe_2[29–33]. Therefore, by locally tuning the Fermi level of a 2D channel, a multi-functional logic device can be realized in one 2D channel.

Here we report a NAND gate based on a single ReS_2 channel with a graphene split gate. We first demonstrate ReS_2 field-effect transistors (FETs) on an hBN substrate with graphene electrodes. The field-effect mobility (μ_{FE}) of an n-type ReS_2 FET is 35 $cm^2/V{\cdot}s$ and the on/off ratio is as high as 10^6 at room temperature. When the graphene split gate is used to locally modulate the channel, two regions, separately tuned by the split gates, act as independent transistors, which can be used as a gate-tunable NAND logic gate.

Results

For "all-2D" devices, a vdW heterostructure of ReS_2, graphene, and hBN was fabricated by stacking the exfoliated nanosheets, as shown in Fig. 1. The 2D nanosheets were exfoliated directly onto a polydimethylsiloxane (PDMS) stamp and transferred onto another flake on the SiO_2 substrate[22]. The ReS_2 channel was placed on the hBN to reduce scattering from charged impurities of the substrate and interfacial impurities. As ReS_2 has a smaller effective mass along the a-axis, it has anisotropy in conductance, leading to higher carrier mobility along the a-axis[27]. Therefore, the ReS_2 flake, which has an elongated shape along the a-axis, was chosen as a channel. Graphene was used as an electrode to lower the Schottky barrier. Two pieces of graphene were placed on the ends of the ReS_2 channel to form source and drain electrodes. After stacking, e-beam lithography and metal deposition (1 nm Cr/50 nm Au) were used to define the metal electrodes. Figure 2(a,b) show the schematic and optical microscopic (OM) images of the fabricated device.

The electrical performance of the tri-layer ReS_2 FET on the hBN substrate with graphene electrodes is shown in Fig. 3. The few-layer graphene (>10 L) and thick hBN of 6.4 nm were used in the device. The output curves ($I_{DS} - V_{DS}$) at different back gate voltages (V_{BG}) clearly exhibit a gate-dependent linearity, as shown in Fig. 3(a). The linear output curves at small gate voltages indicate that the ReS_2-graphene interface forms Ohmic contact even at low carrier concentrations. As shown in the transfer curves ($I_{DS} - V_{BG}$) in Fig. 3(b), ReS_2 exhibits n-type transport as typically observed in MoS_2 or WS_2[34]. Because of the low contact resistance and reduced carrier scattering in the vdW heterostructure device, higher mobility ($\mu_{FE} = 35\ cm^2/V{\cdot}s$) and a high on-off ratio (~10^6) were extracted, compared with the same ReS_2 FET with metal electrodes on a SiO_2/Si substrate (Fig. S1). It should be noted that the field-effect mobility of a vdW heterostructure device of ReS_2 is significantly greater than previously reported values (<10 $cm^2/V{\cdot}s$) of ReS_2 devices with metal or graphene electrodes and SiO_2 dielectric[14–19]. We also fabricated $ReSe_2$ devices using the same procedure and device structure. As $ReSe_2$ exhibits a smaller mobility of 6.6 $cm^2/V{\cdot}s$ than ReS_2, ReS_2 was used for the logic device. (Fig. S2)

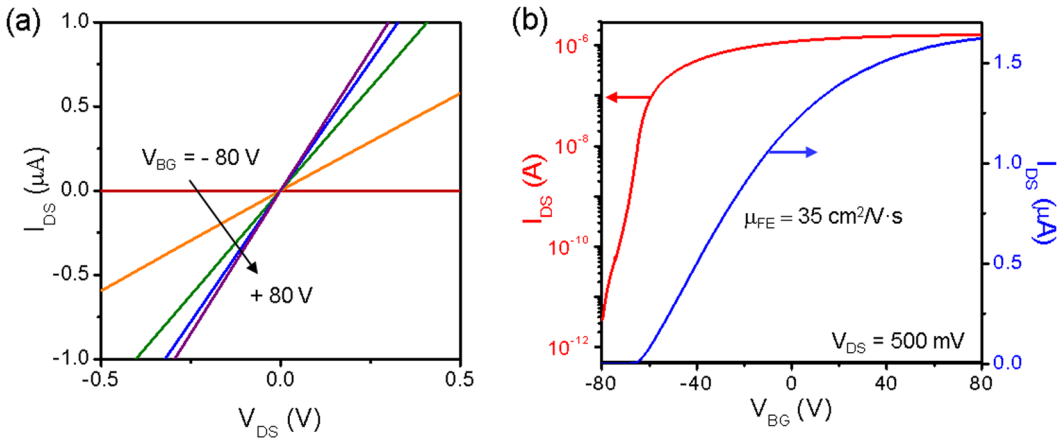

Figure 3. Electrical characteristics of tri-layer ReS_2 FET. (**a**) Output curves ($I_{DS} - V_{DS}$) of device. Linearity of output curves at all gate voltages indicates that graphene-ReS_2 junction is Ohmic contact. (**b**) Transfer curves ($I_{DS} - V_{BG}$) plotted in semi-log scale (red) and linear scale (blue). The ReS_2 FET exhibits high field effect mobility of 35 cm^2/V·s and on-off ratio of 10^6.

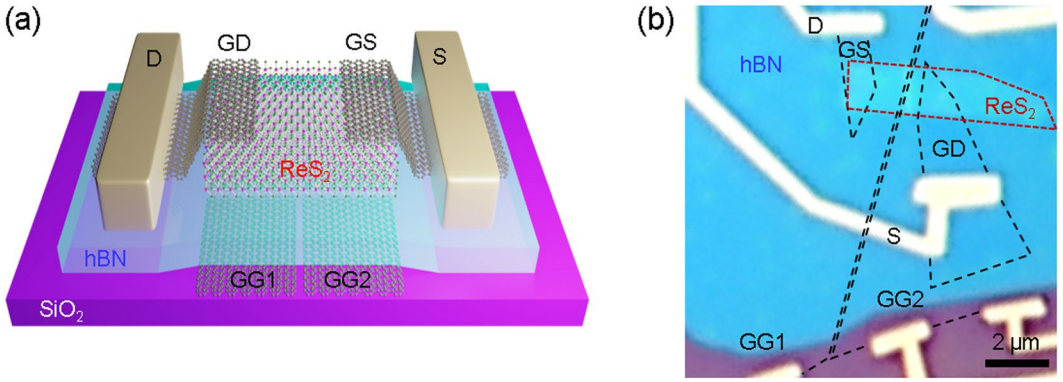

Figure 4. Tri-layer ReS_2 FET with graphene split gates. (**a**) Schematic of device. GD, GS, GG1, and GG2 indicate graphene drain, graphene source, graphene gates 1 and 2, respectively. (**b**) Optical microscope image of fabricated device.

We modified the previous device structure to demonstrate the logic devices comprising a single 2D channel. To locally tune the ReS_2 channel, graphene was inserted between the bottom hBN and SiO_2 and patterned into split gates separated by a nanogap, as shown in Fig. 4(a). (See Fig. S3 for detail of the fabrication.) After exfoliation of the graphene on the SiO_2 substrate, e-beam lithography is performed to define a nanogap on the graphene, followed by reactive-ion etching (RIE) etching for cutting. The patterned graphene split gates are annealed at 350 °C for 4 hrs in forming gas (5% H_2 in Ar) to remove residue. After cleaning, other 2D flakes of hBN dielectric, ReS_2 channel, and graphene electrodes were sequentially transferred by the PDMS stamping technique as described in Fig. 1. After stacking, e-beam lithography and metal deposition were conducted to form metal contacts to the source, drain, and gate graphene electrodes. The OM image in Fig. 4(b) shows the fabricated tri-layer ReS_2 device with graphene split gates.

When different voltages are applied separately to the two graphene split gates (V_{GG1} and V_{GG2}), the corresponding band alignments are shown in Fig. 5(a). When both gate voltages of V_{GG1} and V_{GG2} are higher than the threshold voltage (V_{th}), the whole channel region is conductive and the Schottky barrier is lowered because of the simultaneous up-shift of the graphene Fermi level, which results in n-type conductance of the device. When the V_{GG1} is higher than the threshold voltage and V_{GG2} is smaller, carrier transport through the ReS_2 channel is blocked because of the depletion of the negatively gated ReS_2 region, while the Schottky barrier is still small, resulting in carrier injection of the positively gated channel (middle of Fig. 5(a)). When both gate voltages are within the off-state, carrier transport is impossible due to depletion of the channel and higher contact barrier, resulting in a significantly low off-current level. Figure 5(b) shows the transfer curves ($I_{DS} - V_{GG1}$) of the ReS_2 device with graphene split gates when V_{GG1} is varying while V_{GG2} is fixed. The transfer curves are plotted on a semi-log scale in Fig. 5(c). In the device, hBN was used as an ultrathin and ultraflat dielectric in the device geometry, which is appropriate for "all-2D" devices. A small operating voltage ($V_{BG} < 3$ V) and low subthreshold swing (SS) of <300 mV/dec were obtained, which were an order of magnitude smaller in the ReS_2 device on the

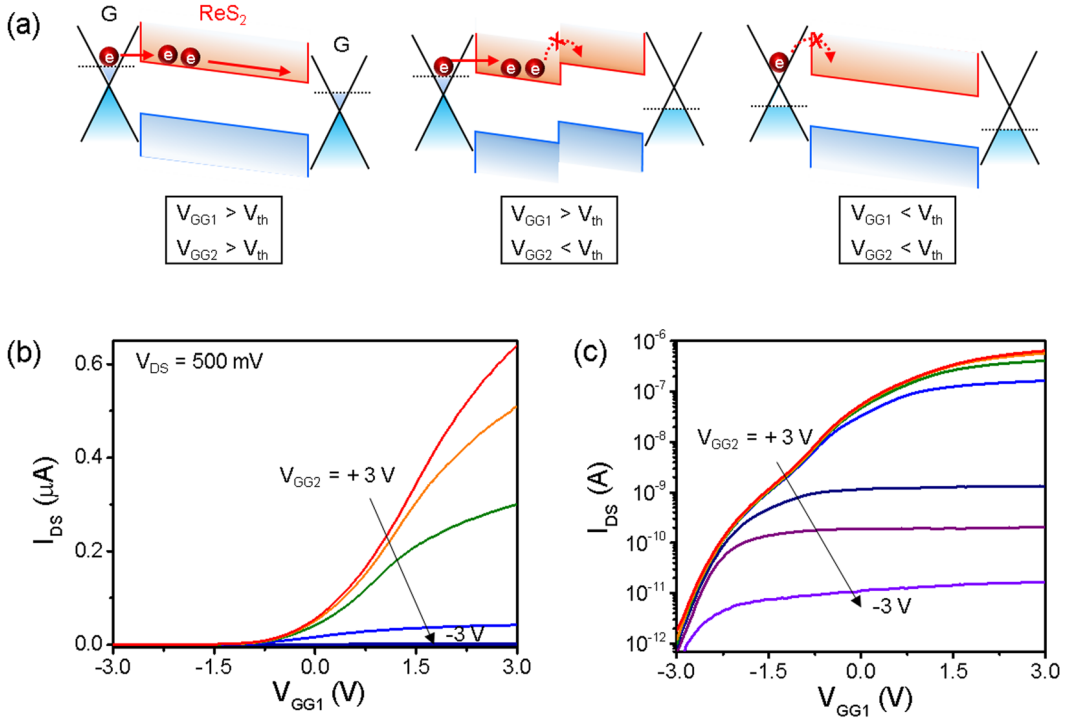

Figure 5. Band diagram and electrical modulation characteristics of the device. (**a**) Band alignment under various combinations of different gate voltages by split gates. When both gates are on (V_{GG1} and $V_{GG1} > V_{th}$), charge carriers transport through ReS_2 channel (left). If one of split gates is off ($V_{GG1} > V_{th}$ and $V_{GG1} < V_{th}$), half of channel is depleted and charge carriers do not transport (middle). When both gates are off (V_{GG1} and $V_{GG1} < V_{th}$), charge carriers cannot be injected from graphene and transport through channel (right). (**b**,**c**) Transfer curves ($I_{DS} - V_{GG1}$) of the ReS_2 FET at varying V_{GG2} and fixed V_{GG1} in linear scale (**b**) and semi-log scale (**c**).

300 nm-thick SiO_2 substrate which is calculated from the device described in Figs 2, 3. In the on-state ($V_{GG1} > -1.5$ V), conductance of the whole channel increases with increasing V_{GG1}. However, in the off-state ($V_{GG1} < -1.5$ V), the off-current remains at a low level of 10^{-12} A at different V_{GG1} because the region where V_{GG1} is applied is completely off. Therefore, the on-current can be strongly modulated by V_{GG1} and V_{GG2}. The on-off ratio modulation ranges from 10^2 to 10^6, which is beneficial for multifunctional applications (more clearly observed in the semi-log scale plot of Fig. 5(c)). Regardless of a gap (~200 nm), it is validated that the device operates reliably without significant deterioration of the performance, which have been also verified in previous reports[29,32].

The logic device characteristics of the ReS_2 device with graphene split gates was measured, as shown in Fig. 6. As can be seen in the circuit diagram of Fig. 6(a), two graphene split gates are used as input signal gates. An external load of 100 MΩ, the middle off and on resistances value of the device, was used. Input terminals 1 (in1) and 2 (in2) were set as the GG1 and GG2, respectively. Because of high modulation ability, one half of the channel (controlled by one of split gates) operates as an independent inverter. The voltage transfer curves (VTCs) of Fig. 6(a) show the inverter characteristics. When V_{in1} varies with a fixed V_{in2}, it can be clearly seen that the output signals are inverted, indicating that only half of the channel plays a role as an inverter. However, when the current is totally blocked by depletion of the half of the channel modulated by V_{in2}, there is no inversion of the output signal. This means that the output signals can be effectively controlled by two input signals from the graphene split gates. The calculated gain values of the ReS_2 inverter, defined as dV_{out}/dV_{in}, are shown in Fig. 6(b). Even though the gain value is relatively lower than those of previously reported 2D-materials-based inverters comprising two n-type and p-type transistors (similar to complementary metal oxide semiconductor (CMOS)), it is comparable to the gain values of unipolar-type inverters[5,27,35,36]. In addition, the supply voltage (V_{DD}) used in this study is 1 V and the dielectric constant ($\varepsilon_r = 3$–4) of hBN is relatively small compared to previous studies[37,38]. Therefore, the gain can be further enhanced by increasing V_{DD} as shown in the inset in Fig. 6(c). In this study, V_{DD} was set as 1 V because the VTC exhibits a mirror reflection and a gain larger than 1 (unity gain), as shown in Fig. 6(c), compared to lower or higher V_{DD}.

To utilize ReS_2 devices as NAND logic devices, output voltages were measured under different combinations of input states, as shown in Fig. 6(d). Because the output voltage is linked to the V_{DD}, a logic state of 1 can be realized when either V_{in1} or V_{in2} is −3 V (defined as an input logic state of 0). For V_{out} of state 0, positive input voltage of 3 V was applied to both graphene split gates of GG1 and GG2. If a gate voltage smaller than −1.5 V is applied to one of the two gates, the whole device is non-conducting. Therefore, ReS_2 devices with graphene split gates can be used as a NAND gate, one of the universal logic gates. It should be noted that a NAND gate was fabricated on a single 2D channel material, which is distinct from other reports using two transistors regardless of the carrier

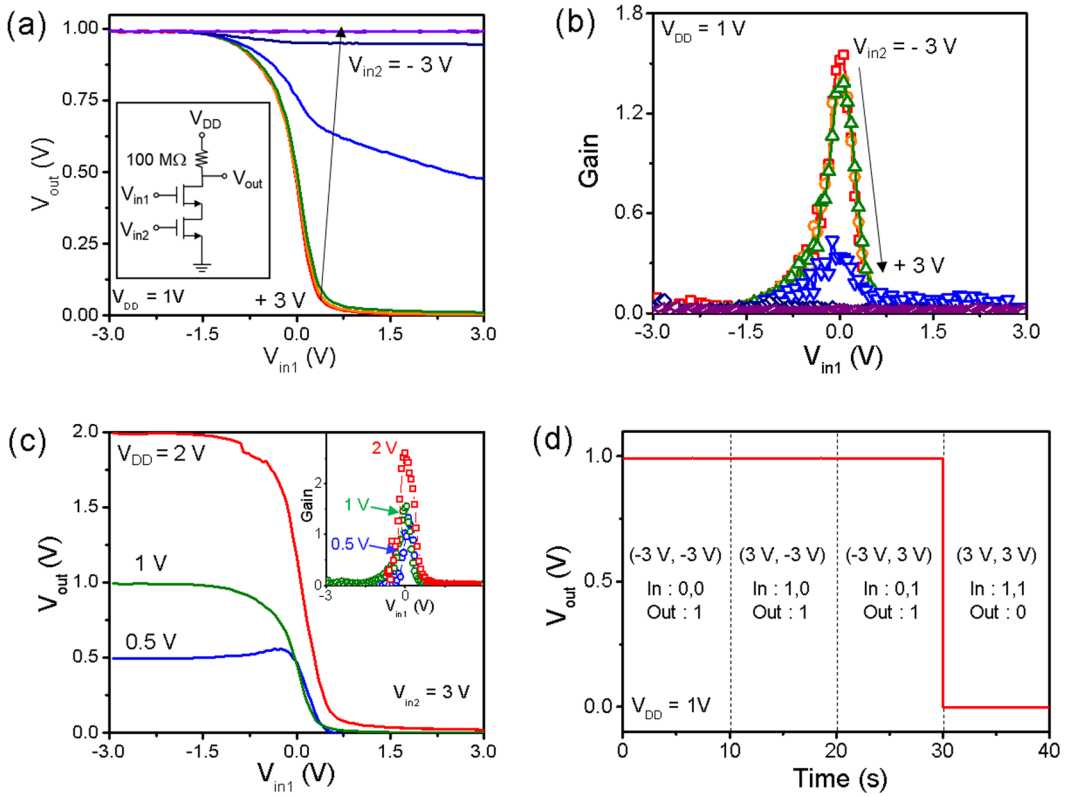

Figure 6. Logic device characteristics of ReS_2 FET with graphene split gates. (**a**) Voltage transfer curves (VTCs) of GG1 region ($V_{out} - V_{in1}$) at $V_{DD} = 1$ and varying V_{in2}. Inset shows circuit diagram of logic device. External load is 100 MΩ. At $V_{in2} > 1$ V, VTC exhibits mirror symmetry. (**b**) Gain extracted by VTC as function of V_{in2}. Maximum gain is 1.6 at $V_{in2} = -3$ V. (**c**) VTC at varying V_{DD} and fixed V_{in2} of 3 V. The inset shows gain extracted from VTC. (**d**) Time domain plot of output voltage for NAND logic gates.

type. Output voltages measured at different combinations of the two input signals are shown in Fig. 6(d). This indicates that a single channel ReS_2 device with graphene split gates operates well as a NAND gate. Unlike bulk materials, gate tunability of 2D semiconducting materials enables independent control of the separated channel regions by split gates. Therefore, NAND logic device can be fabricated within single 2D channel, which is clearly different from conventional logic gates that require more than two separate transistors.

Discussion

In conclusion, we fabricated high performance ReS_2 transistors by using graphene and hBN as electrode and dielectric, respectively. The high field effect mobility of 35 $cm^2/V{\cdot}s$ and high on-off ratio of 10^6 were obtained by suppression of Fermi level pinning at the graphene-ReS_2 junction and reduction of charged impurity scattering. For the "all-2D" integration, we also fabricated ReS_2 devices with graphene split gates for logic devices. The graphene split gates and bottom hBN enables us to locally and effectively modulate channel regions. By independently changing gate voltages from the two split gates, the device conductance can be controlled with a higher degree of freedom: the whole device is turned off by applying a negative voltage to only one gate, while a positive gate voltage is applied to both split gates to turn-on the device. By utilizing local tunability of the channel by split gates, it was shown that the ReS_2 device with graphene split gates can be used as an efficient NAND gate, which is one of the most essential elements in integrated circuits. The vdW heterostructure NAND gate comprising a single transistor fabricated in this work provides a further step toward realization of "all-2D" circuitry for flexible and transparent electronic applications.

Methods

Device fabrication. PDMS transfer First, the PDMS base (Sylgard 184) was cured with 10 wt% of curing agent at 120 °C for 2 h. We then mechanically exfoliated hBN, which is the bottom of the heterostructure on SiO_2/Si chips, and exfoliated other 2D materials, such as graphene and ReS_2, separately onto each cured PDMS flake on glass slides. After careful alignment with a micromanipulator in the transfer stage, the PDMS with 2D materials were attached and detached, as carefully and slowly as possible, at room temperature.

E-beam lithography. To pattern metal electrodes on the as-stacked heterostructure or gap on the graphene for the split gate, we performed e-beam lithography with a Raith Pioneer 2 nanolithography system.

Metal deposition. We deposited metal electrodes (Cr 1 nm/Au 50 nm or Cr 1 nm/ Pd 20 nm/Au 30 nm) with an e-beam evaporator (Korea Vacuum Tech.) in a high vacuum, of approximately 10^{-8} Torr, to create the interconnection to the pads for the electrical measurement from the graphene electrodes, where 1 nm of Cr is an adhesive layer. For the lift-off process, the samples were soaked in acetone overnight.

Reactive ion etching. We etched the developed region after the e-beam lithography using O_2 RIE (Femto Science) for only 5 s to prevent etching of e-beam resist. (100 kHz, 100 W in 10^{-2} Torr of O_2) We then put the samples in acetone to remove the e-beam resist.

Electrical characterization. All electrical measurements were carried out by semiconductor parameter analyzers at room temperature under ambient condition. (Keithely 4200, Keithely for FET characterization in Figs 3, 5; and HP 4155 C, Agilent Technologies for logic device measurement in Fig. 6)

Data Availability

The authors declare that all data supporting the findings of this study are available within the paper and its supplementary information files.

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Author Contributions

J.Kwon and G.-H.L. conceived and designed the study. J.Kwon fabricated samples and carried out all related experiments under the guidance of G.-H.L. and with the help of the other authors. Y.S. assisted in the preparation of heterostructure samples. H.K. carried out the logic device measurement under the guidance of S.I., J.Y.L. performed electrical measurements under the guidance of C.-H.L., H.P. assisted electrical measurements under the guidance of J.Kim, K.W. and T.T. prepared high quality hBN crystals. All authors contributed to the discussion of this work. J.Kwon and G.-H.L. wrote the manuscript.

Additional Information

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