APPLIED SCIENCES AND ENGINEERING

Superconducting disordered neural networks for neuromorphic processing with fluxons

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In superconductors, magnetic fields are quantized into discrete fluxons (flux quanta Φ_0), made of microscopic circulating supercurrents. We introduce a multiterminal synapse network comprising a disordered array of superconducting loops with Josephson junctions. The loops can trap fluxons defining memory, while the junctions allow their movement between loops. Dynamics of fluxons through such a disordered system through a complex reconfigurable energy landscape represents brain-like spiking information flow. In this work, we experimentally demonstrate a three-loop network using $YBa_2Cu_3O_{7-\delta}$-based superconducting loops and Josephson junctions, which exhibit stable memory configurations of trapped flux in loops that determine the rate of flow of fluxons through synaptic connections. The memory states are, in turn, affected by the applied input signals but can also be externally configured electrically through control current/feedback terminals. These results establish a previously unexplored, biologically similar architectural approach to neuromorphic computing that is scalable while dissipating energy of atto Joules/spike.

INTRODUCTION

Realizing a physical system that can mimic information processing in biological brains [known as a neuromorphic computer (1)] is a primary objective of next-generation artificial intelligence systems and motivation for this work. There is still lack of full understanding of how memory and computation occurs in brains that lead to higher-level properties such as cognition. Behavior of individual network elements, however, such as neurons, synapses, etc. are sufficiently well understood (2–5) and implemented in different hardware systems (6–12). In neurons, packets of information flow in the form of action potentials as the accumulated signals (charge) from various other neurons surpass their the thresholds. This flow between neurons is regulated by the synapses in between them. By varying their connection strengths or weights, memory storage can be represented and can either be potentiated or be depressed in response to the information flow (13). This potential energy profile inspires the exploration of materials and devices that exhibit tunable electrical conductance behavior for use as synapses in neuromorphic computing (14–17).

At the network level, neuromorphic computation has been broadly understood as an emergent phenomenon arising from the collective behavior of these network elements through nonlinear interactions, similar to other complex systems (18–20). In case of convolutional neural networks, processing is understood and practically implemented in the form of clustering and classification of digital information through a learning process, as the system converges to an energy minimum over a complex energy landscape (21–23). Physical implementation of analog information processing in neural networks is similarly explored in systems that exhibit complex energy landscape with nonlinear spatial and temporal dynamics between network elements. Examples of such systems that result in emergent phenomena include disordered systems such as spin glasses (24, 25),

coupled oscillator networks (26–28), and also experimentally explored in nanowire networks (29, 30).

Complex systems with induced disorder in the network topology are also widely noted to be efficient for information processing (31) and often observed in biological brain networks (32). We have therefore proposed a spiking recurrent neural network architecture based on a disordered array of superconducting loops, where disorder is introduced in the form of circuit topology between network connections (i.e., synaptic network between neurons) (33, 34).

Fluxon generation and propagation through Josephson junctions (35), observed as spiking voltages, are well understood, and superconducting loop–based circuits encompassing individual fluxons are subsequently developed for use in rapid single-flux quantum digital circuits for energy-efficient and high-speed digital computing (35–40). Collection of a large number of this quantized flux can similarly be stored in superconducting loops in the form of circulating supercurrents with Josephson junctions, interrupting that loop acting as gateways for their entrance or exit (36, 41). These spiking signals can therefore represent both spatial and temporal information similar to that of biological brains. Therefore, a multiterminal network of disordered loops with junctions such as that shown in Fig. 1A can replicate the individual synaptic connections of a recurrent neural network such as that shown in Fig. 1B, where complex nonlinear interactions between the incoming and the stored fluxons result in variation of the average flow of spiking signals between any pair of input-output terminals, as shown in Fig. 1C. The rate of flow of fluxons between any two terminals, defined quantitatively and demonstrated experimentally in Results and discussion, may be characterized as synaptic weight between them.

Specifically, the incoming flux at I_1 say enters in the form of current pulses that propagate through the network in different time-dependent paths to different output terminals such as O_1. When some of these currents surpass the superconducting critical current of a junction in its path, I_c, fluxons enter the corresponding loop and are stored in the form of circulating current (i.e., memory) around that loop. These processes are schematically shown in a network of 10 loops with four input and four output terminals (I_n and O_n) in Fig. 1A. The flow of flux can also be separately controlled using the current

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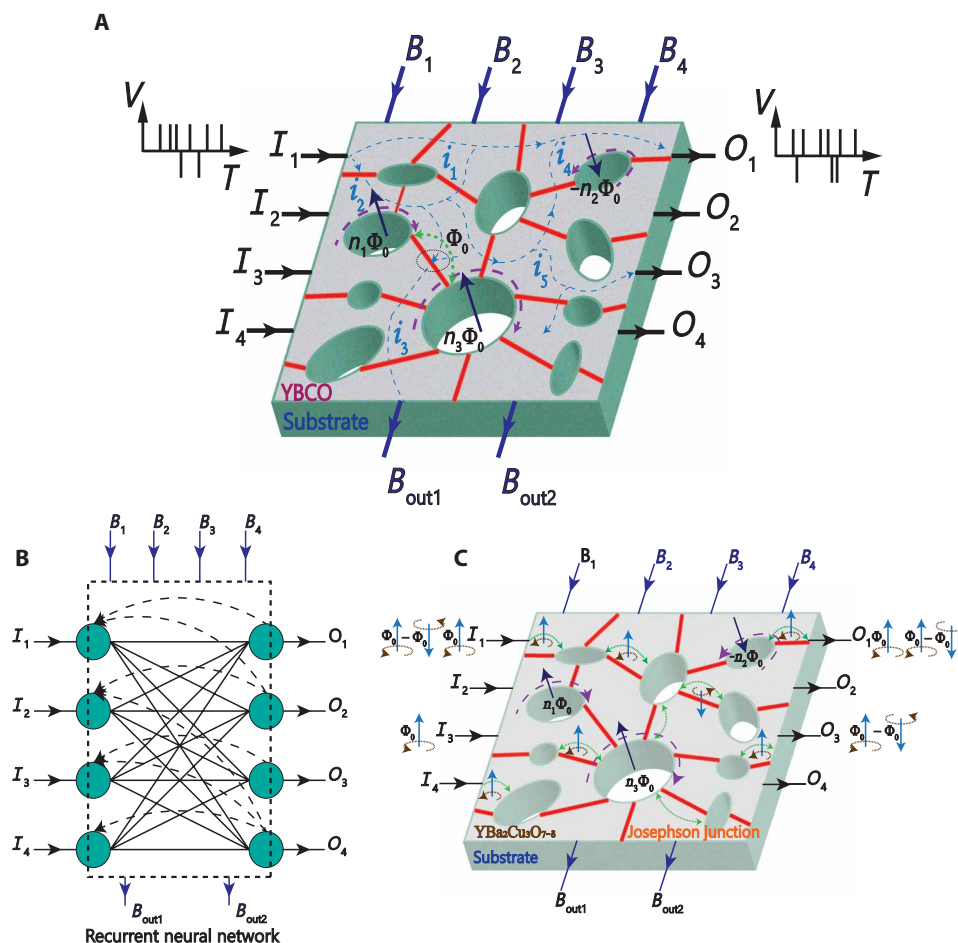
Fig. 1. Schematic of four by four superconducting disordered loop neural networks with helium ion beam-defined Josephson junctions. (**A**) Synapse network with four input, four output, and four control current/feedback channels to represent all the individual synaptic connections of the recurrent neural network shown in (B). The network comprises 10 superconducting loops connected through various Josephson junctions of different sizes. Incoming and outgoing spike trains are schematically represented for terminals I_1 and O_1. The input spike trains from all the terminals are converted into current pulses that take various time-dependent paths through Josephson junctions shown as i_1, i_2, etc. Some current pulses switch Josephson junctions above their critical currents and are stored as circulating currents in adjacent loops (i.e., flux perpendicular to the plane), representing the memory state of the synapse. The switching event and the generation/transfer of flux quanta are schematically shown using the dotted circle, and the flux stored in various loops is represented as $n_1\Phi_0$, $n_2\Phi_0$, etc. (**B**) Schematic of an equivalent recurrent neural network with four input (labeled I_1, I_2, I_3, and I_4), four output channels (labeled O_1, O_2, O_3, and O_4), and four external control current/feedback channels for external memory configuration. (**C**) Flux quanta propagation through the synapse network shown in (A). Flux can get trapped in loops and can propagate along different paths through the junctions to various output terminals. Variations in memory states result in differences in populations of flux quanta at each of the outputs.

terminals (B_n), which can also be a function of outgoing signals through a feedback loop (from perhaps O_n) as discussed in (*33*).

Here, we present an experimental manifestation of such a collective synapse network composed of a network of interconnected YBa$_2$Cu$_3$O$_{7-\delta}$ (YBCO) superconducting loops and Josephson junctions, where disorder is introduced into the network architecture in the form of geometry and physical properties of loops and Josephson junctions (i.e., the loop inductances and junction critical currents). The YBCO-based experimental three-loop network with one-input (I_1), one-output (O_1), and one-feedback (B_1) terminal is shown in Fig. 2. These networks can be combined with compatible elements such as superconducting spiking neurons (*10*, *11*, *33*, *34*) etc., to form fully connected recurrent neural networks that can be configured to perform both supervised and unsupervised learning.

Each superconducting loop of Fig. 1A can accommodate one or several fluxons up to $n_i\Phi_0$ (where Φ_0 is the flux quantum) in the

form of circulating supercurrents, in contrast with single-flux quantum–based circuits (*36*). Here, the maximum number of flux quanta n_i in loop i is determined by its inductance; numerically, it is given by $n_i = \frac{L_i I_c}{\Phi_0}$, where L_i is the inductance of the superconducting path around loop i and I_c is the critical current of the smallest Josephson junction in that loop. Therefore, the total number of distinct static memory configurations available for an array with number of loops equal to i is given by $(2n_1 + 1) \cdot (2n_2 + 1) \cdots (2n_i + 1)$, accounting for states with no current, clockwise- or anticlockwise-circulating currents in the loops. This number grows exponentially as the number of loops increase. The memory states can be characterized as metastable states of circulating currents corresponding to local energy minima for flux propagation through the network. Because of the presence of nonuniform loop inductances and junction critical currents, each of the pathways for the flow of flux between any two terminals is subjected to a distinct energy landscape that is dependent
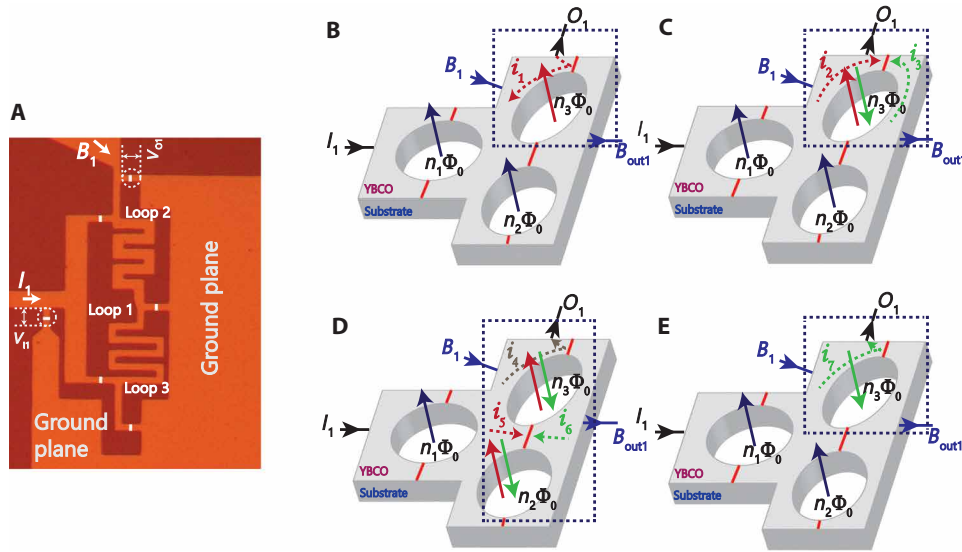
Fig. 2. Experimental three-loop one by one superconducting disordered neural network. (**A**) Optical microscope image of a YBCO-based three-loop network with focused helium ion Josephson junctions used in the experiment to study the synaptic properties between one input-output terminal pair shown as I_1 and O_1. A control current parameter with current flowing between B_1 and the ground can be used to change the memory configurations. Experiments involve excitation of the device with currents I_1 and B_1. The input and the control current are also varied in time relative to each other. (**B**) Schematic of a three-loop network showing currents and flux configurations in memory state S_1. Outgoing flux corresponds to anticlockwise-circulating currents in loop 2. (**C**) Three-loop network schematic showing memory state S_2 with an outgoing flow rate of zero. Currents and flux configuration correspond to the superconducting state of junction at O_1, with the current difference $i_2 − i_3$ below its critical current. (**D**) Three-loop network schematic showing memory state S_4 with increased outgoing flux flow. One of the junctions in loop 3 is in the superconducting state (i.e., $i_5 − i_6$ below its critical current), resulting in additional current diverted to the output. (**E**) Three-loop network schematic showing memory state S_5 with outgoing flux corresponding to clockwise-circulating current in loop 2.

on the memory state, as well as the input conditions, similar to the models described in (*18, 21, 24*). As the flux gets trapped and is propagating between loops, the memory state and its corresponding energy configuration define the propagation probability of an input fluxon (and, therefore, the corresponding fluxon flow rate) through any of the available paths (allowing measurement of the memory state and its time evolution) as shown schematically in Fig. 1C. Specifically, the potential energy stored in a loop k due to the flux storage and current paths through it can be calculated following (*42, 43*), as shown in Eq. 1 below. Similarly, the energy landscape of any of the current paths from an input node (I_1) to an output node (O_4) can be calculated as a function of junction and inductance parameters along the pathway using Eq. 1

$$
U_k = -\sum_{m=1}^{M} \frac{I_{C_m}\Phi_0}{2\pi}\cos(\phi_m + \alpha_m) + \\
\sum_{n=1}^{N} \frac{(\Phi_0 \cdot (\phi_m + \beta_n + 2\pi n_i))^2}{4\pi L_n}
\tag{1}
$$

Here, the loop k is assumed to contain M different Josephson junctions with critical currents I_{Cm} and N different inductances, representing the N branches of the loop between the junctions. Φ_0 is the magnetic flux quantum of value $2.06783383 \times 10^{-15}$ weber. Following the Josephson equations for overdamped junctions (*44–46*), ϕ_m is the phase difference across junction m and is dependent on the current through it, while α_m is due to the flux in the inductively coupled adjacent loop branch. n_i is the number of flux quanta stored in the loop i, and β_n is a function of the control or input currents. Therefore, the potential energy of the loop depends on the flux stored along with the input and control currents. In a dynamic system with

continuous spiking excitation at the inputs, the incoming flux encounters multiple paths to all the output terminals, with different time-dependent energy landscapes resulting in a different rate of flow of flux for each path corresponding to the memory/flux configurations. The different paths represent synaptic weights. While it is considerably complex to experimentally determine the energy distribution in each of these paths as a function of time, the effect of different energy landscapes on fluxon flow rates can be experimentally measured as shown as in the following section. These flux outputs can be connected to superconducting leaky integrate-and-fire neurons (*33*) and feedback loops, where the flow rate of flux above a frequency threshold is translated into the amplitude and frequency of spiking action potentials.

RESULTS AND DISCUSSION

A simplified network of three disordered loops with a total of five dissimilar Josephson junctions shown in Fig. 2A was designed to experimentally realize the synaptic properties discussed in the previous section. The network is fabricated using high-temperature superconductor YBCO with Josephson junction barriers defined using focused helium ion beam direct writing (*47*). Loop 1 is inductively coupled to loops 2 and 3, which are connected to each other through a Josephson junction. An additional junction shunted to ground is connected to loop 1 at its input terminal. The input current applied predominantly passes through this junction, generating a spiking input to the three loops equivalent to the average rate of incoming flux quanta $\frac{V_\Pi}{\Phi_0}$ proportional to current I_1 (*48*). A control current signal B_1, which can also be programmed to represent a feedback signal (*33*), is applied to loop 3 near the output junction

across which the average frequency of outgoing flux quanta $\frac{V_{O1}}{\Phi_0}$ is measured, such that feedback current can induce back-propagating flux. The three-loop design encompasses at least one instance of all possible flux-current interactions occurring in a larger nonuniform network. Therefore, it can also be considered as a subset of a larger network where the applied currents I_1 and B_1 correspond to some instances of flux and continuous current entering from neighboring loops. I_1 and B_1 in Fig. 2 were systematically varied to drive the network into different stable memory states and, therefore, to map the memory state space represented by the the resulting input and output voltages V_{I1} and V_{O1}, equivalent to their respective incoming and outgoing frequencies of fluxons into the network. Each of the loops was designed to accommodate a total circulating current equivalent to a few tens of flux quanta before the critical currents are reached, and the flux quanta begin to exit the loops through the junctions, thus allowing a large number of distinct memory configurations. Nonuniformity was built into the network in the form of dissimilarities in loop geometries (i.e., inductances) and junction critical currents. The network corresponding to results in Figs. 3 to 6 and figs. S3 to S6 is operated at 28 K. However, another three-loop network designed with different junction critical currents but similar loop inductances and operated at 4.2 K produced qualitatively similar results with similarly evolving memory states (see fig. S1), indicating that the accuracy of the design parameters and the measurement temperature (below its superconducting critical temperature) are not crucial to achieve a particular operation of the neural network. Furthermore, this implies that our approach is robust to effects of disorder from uncontrollable fabrication processes and material variations.

The flux flow rate through the network between any pair of input-output terminals in the network is defined as change in the average number of fluxons, leaving the network through the output V_{O1} with respect to change in the average number of fluxons entering the network at the input terminal V_{I1}. Therefore, in the three-loop network, the flow rate of fluxons between the input and output terminals, equivalent to its synaptic weight, is given by $\frac{dV_{O1}}{dV_{I1}}$.

Static operation

Initially, current I_1 is sinusoidally varied between −1 and 1 mA, while the current B_1 is fixed. The measurement is repeated for different values of B_1 ranging from 0 to 90 μA. The applied currents are substantially larger than the critical currents of the junctions or the circulating currents corresponding to different memory states. This is, by design, such that the flux propagation through the
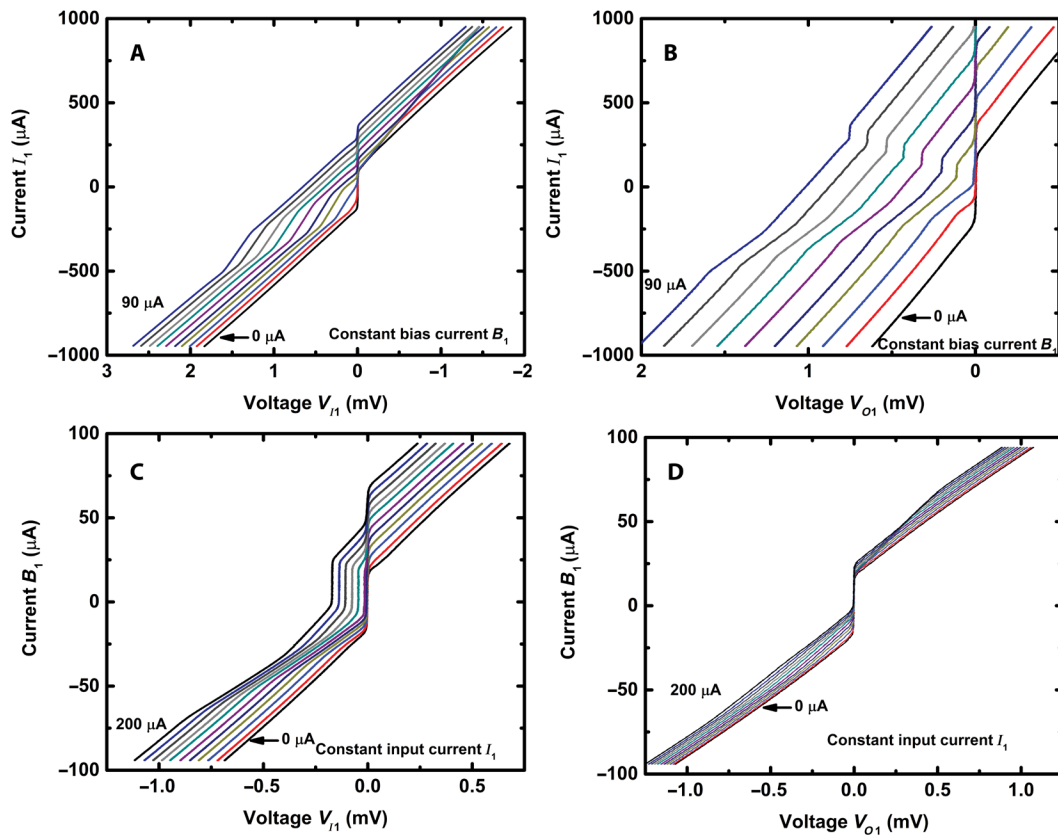

Fig. 3. Electrical characteristicsstatic operation. Current-voltage characteristics of the three-loop network shown in Fig. 2 corresponding to the experimental results of static operation. (**A**) Current at input I_1 continuously varied between −1 and 1 mA is plotted against the measured input voltage V_{I1}, while a constant control current is applied at B_1. Ten different measurements corresponding to currents at B_1 with values from 0 to 90 μA with an increment of 10 μA are plotted. (**B**) Current at input I_1 continuously varied between −1 and 1 mA is plotted against the measured output voltage V_{O1} at different constant control currents B_1 ranging from 0 to 90 μA with an increment of 10 μA. (**C**) Current at B_1 continuously varied between −90 and 90 μA is plotted against the measured input voltage V_{I1} while a constant input current is applied at I_1 (constant values ranging between 0 and 200 μA with an increment of 20 μA). (**D**) Current at B_1 continuously varied between −90 and 90 μA is plotted against the measured input voltage V_{O1} while a constant input current is applied at I_1 (constant values ranging between 0 and 200 μA with an increment of 20 μA).
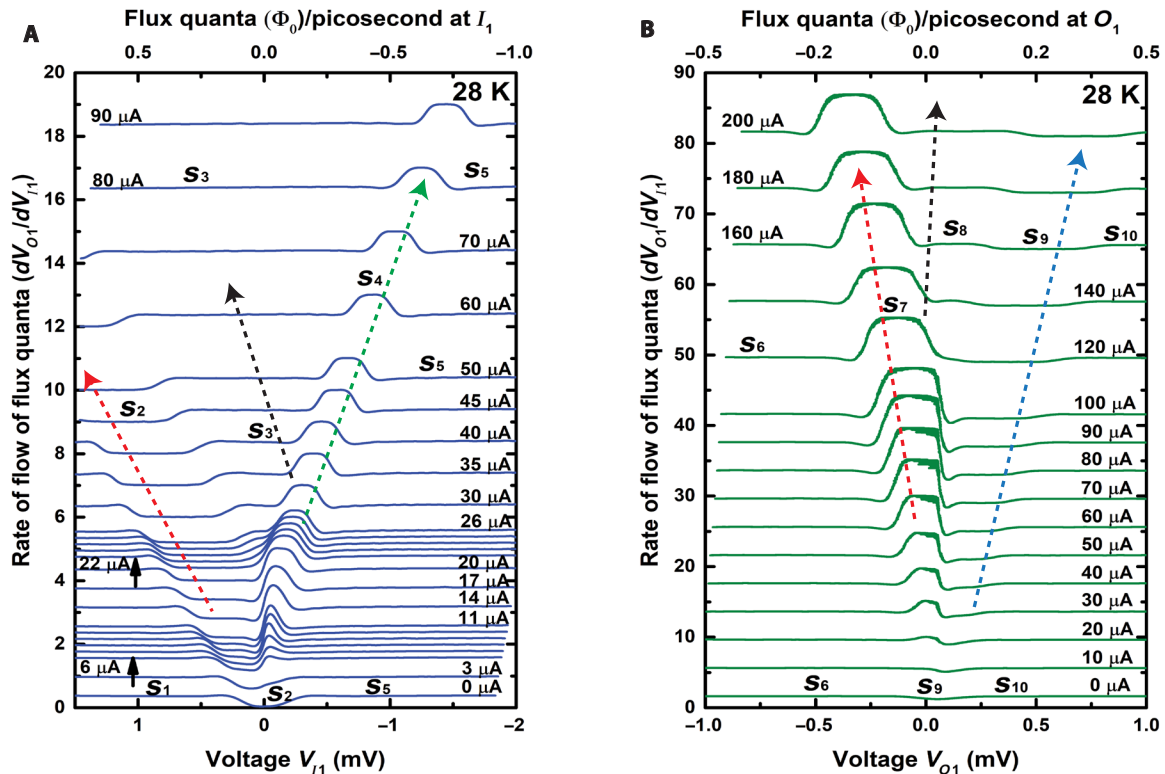
Fig. 4. Evolution of memory states observed as different rates of flow of flux. Experimental observation of stable memory states in superconducting synapse networks in the form of rate of flow of flux between input-output terminals defined in a state space of voltages (or frequencies of spiking signals into the network) and control currents. (**A**) Rate of flow of flux quanta $\left(\frac{dV_{O1}}{dV_{I1}}\right)$ through the three-loop disordered array synapse network (Fig. 2A) measured at 28 K while varying the input voltage V_{I1} (or corresponding current I_1) at different constant current biases B_1. The curves are offset in the y axis, with an offset value proportional to control current B_1 (i.e., an offset of 0.2 per 1 μA of B_1). Stable memory states are observed as constant rates of flow of flux labeled from S_1 to S_5. Three stable memory states exist at B_1 of 0 μA, with two new states emerging as B_1 are increased. (**B**) Rate of flow of flux quanta $\left(\frac{dV_{O1}}{dV_{I1}}\right)$ through the three-loop synapse network (Fig. 2A) measured while continuously varying the input voltage V_{O1} (or corresponding current B_1) at different constant current inputs I_1. Three different stable memory states are revealed initially, with two additional emergent states as I_1 is increased. The curves are offset in the y axis, with an offset value proportional to control current B_1 (i.e., an offset 1 per 2 μA of I_1). The voltages at which these states occur, and the width of the states can be configured using I_1.

network occurs at very high frequencies (up to terahertz), and the resulting memory states are stable and considerably distinct in their respective energy landscapes. Only such memory states are observed as causing substantial differences in rates of flux flow, and the patterns in these emergent memory states are clearly seen, as input conditions are varied. However, at much lower currents, the differences in flow rates between each different memory state may be observed in the output spiking signals. We note that the frequencies of sinusoidal current inputs are in the range of a few hertz to 1 kHz. This is five orders of magnitude slower than the corresponding spiking frequencies and, therefore, allows enough time for the system to relax to a local energy minimum (representing the memory state), behaving as a quasi-static system on the time scale of applied currents. The input current–input voltage characteristics of the three-loop network are shown in Fig. 3A, and the input current–output voltage characteristics are shown in Fig. 3B. The rates of flux flow, i.e., $\frac{dV_{O1}}{dV_{I1}}$, obtained from our measurements are plotted against the input voltage V_{I1} for different constant control currents B_1 in Fig. 4A. The corresponding voltages V_{O1} against V_{I1} representing the rate of incoming and outgoing fluxons to the network from which the flux flow rates (Fig. 4A) are obtained, for some of the constant currents at B_1 are shown in fig. S3C.

Our results show that multiple stable memory states exist (different values of $\frac{dV_{O1}}{dV_{I1}}$), labeled as S_1, S_2, ... S_6 in Fig. 4A, during which the rate of flow of fluxons between the input-output terminals remains constant. The average fluxon flow rates through the network are different for different input voltage ranges, as shown in Fig. 4, and are also observed as linear current-voltage regions in Fig. 3 (A and B). The changes in the slope of these linear regions correspond to the transitions in memory states, indicating that the total current through different paths changes with memory (flux) configurations. Alternatively, this can be described as a different rate of flow of flux through each of the paths for different memory states. These results also show different mechanisms for switching between memory states as described schematically in Fig. 2 (B to E). For example, a superconducting to voltage state transition occurs at zero voltage in the plots shown in Fig. 3 (A to D). These transitions correspond to different current configurations (i.e., at I_1 and B_1) at which the current through junctions at V_{I1} or V_{O1} abruptly surpasses their respective critical currents. However, these abrupt transitions also occur at finite voltages as observed in Fig. 3 (B and C), indicating that one of the other junctions in the network transitioned between superconducting and voltage states. These transitions correspond to differences between memory states described as S_1, S_2, and S_5 in Fig. 2 (B to E). The transitions
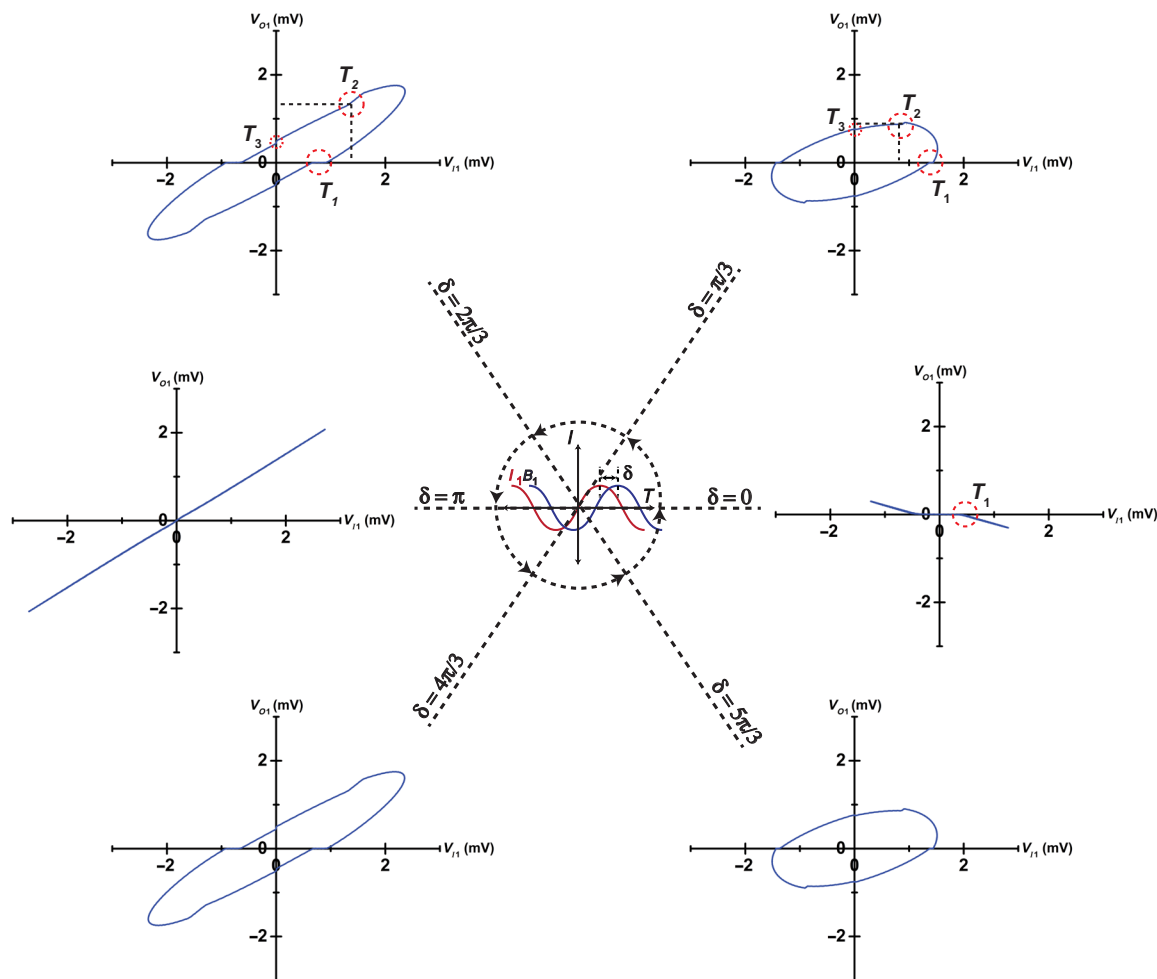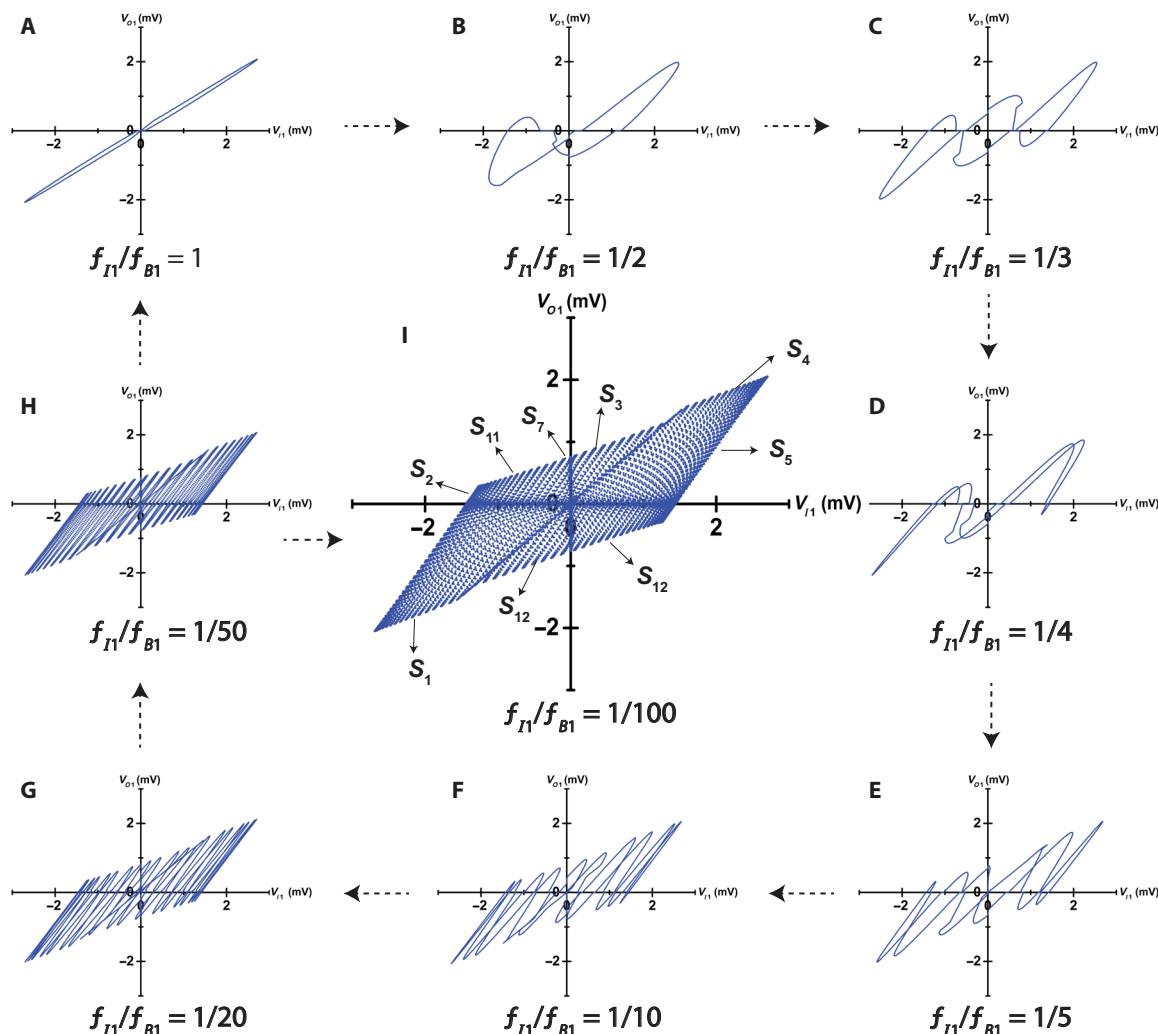
Fig. 5. Dynamic transitions between memory states dependent on relative phase difference of input signals. Dynamic memory states and the corresponding state transitions experimentally observed in the state space of V_{I1} and V_{O1} as the phase difference δ is varied from 0 to 2π between sinusoidal current inputs I_1 and B_1, both 1 Hz of frequency and 1 mA and 100 μA of amplitudes, respectively. The movement of states and the state transitions around the space as δ is varied are labeled T_1, T_2, and T_3.

can also occur over a range of voltages (for example, between −2 and 0 mV for currents between −500 and 0 μA in Fig. 3A), where the changes in current paths from one configuration to the other is gradual, therefore acting as another stable memory state shown as S_4 in Fig. 4.

These stable states correspond to sets of trapped flux configurations during which the changes in current through the junction at O_1 is negligible. This is because the applied currents at I_1 and B_1 are considerably larger than the circulating currents due to flux in loops. However, differences in the flow rates are significant between different stable states. Distinctions in flow rates between each fluxon configuration (memory state) are expected to be observed when the currents through any of the paths are of magnitude similar to the critical currents of junctions in that path. When B_1 is 0 μA, three different memory states, labeled S_1, S_2, and S_5, are observed, with transitions occurring at −0.2 and 0.2 mV. When V_{I1} is between −0.2 and 0.2 mV, $\frac{dV_{O1}}{dV_{I1}}$ is 0, and the output junction is in superconducting state corresponding to zero output flow rate in Fig. 4A. Input voltage V_{I1} versus voltage V_{O1} (Fig. 4A) and input current I_1 versus voltage V_{O1} Fig. 3B also show that the junction is in the zero voltage state in S_2. At more than 0.2 mV and less than −0.2 mV, the V_{O1} varies linearly with V_{I1} to yield respective constant average fluxon flow rates.

Increasing B_1 (Fig. 4A) results in new memory states gradually emerging from within the existing states. Two such instances are observed with state S_4 emerging between B_1 of 6 and 11 μA (schematically shown in Fig. 2D) and with state S_3 emerging between 22 and 26 μA. The number of observable memory states in the form of distinct flow rates increase from 3 at B_1 of 0 μA to 5 at B_1 of 30 μA. These different states correspond to one of the junctions switching between the superconducting and voltage states either abruptly (i.e., at fixed values of I_1 or B_1) or gradually over a range of values of I_1 due to continuous transfer of flux quanta between loops. For example, a memory state S_4 with a larger fluxon flow rate fully emerges at B_1 of 26 μA between V_{I1} of 0 and 0.4 mV. These distinct states are a result of one of the junctions in loop 2 transitioning from the superconducting to voltage state, resulting in a considerable increase in current through the output junction in that state as shown in Fig. 2D. The control current B_1 can also be used as a controllable parameter to change the input frequency (i.e., $\frac{V_{I1}}{\Phi_0}$) and the bandwidth over which different memory states are observed, shown in Fig. 4A. When B_1 is increased, the memory states corresponding to a flow rate of 0 gradually shift away from V_{I1} of 0 mV to negative voltages until they are out of the measurement scale above B_1 of 70 μA. The voltage range

Fig. 6. Electrical scan of state space of operation of the three-loop one by one superconducting neural network. Dynamic memory states and the corresponding state transitions experimentally observed in the state space of V_{I1} and V_{O1}, as the frequency of sinusoidal control current B_1 is varied from 1 to 100 Hz with the input current at 1 Hz. The amplitudes of I_1 and B_1 are 1 mA and 100 μA, respectively. (**A**) $\frac{f_{I1}}{f_{B1}} = 1$. (**B**) $\frac{f_{I1}}{f_{B1}} = 1/2$. (**C**) $\frac{f_{I1}}{f_{B1}} = 1/3$. (**D**) $\frac{f_{I1}}{f_{B1}} = 1/4$. (**E**) $\frac{f_{I1}}{f_{B1}} = 1/5$. (**F**) $\frac{f_{I1}}{f_{B1}} = 1/10$. (**G**) $\frac{f_{I1}}{f_{B1}} = 1/20$. (**H**) $\frac{f_{I1}}{f_{B1}} = 1/50$. (**I**) $\frac{f_{I1}}{f_{B1}} = 1/100$. Different memory states, labeled from S_1 to S_{13}, and transitions between them can be observed that overlap with the states observed in Fig. 4 (A and B).

(bandwidth) of the memory state increased from 0.4 mV (193 GHz) at B_1 of 0 μA to 0.8 mV (387 GHz) at B_1 of 26 μA and remains constant at larger currents. Similar patterns are observed in all the other memory states, where the bandwidth and voltage ranges for the memory states and their emergence can be continuously tuned.

An inverted test is conducted to induce back-propagating flux (49) (i.e., from output O_1 to input I_1) by continuously varying the control current B_1 between −100 and 100 μA at different lower constant input currents I_1. The resulting flux flow rates are plotted against the output voltage V_{O1} for I_1 between 0 and 200 μA in Fig. 4D. A completely different set of memory states labeled from S_6 to S_{10} are observed, characterized by different flow rates, voltage ranges, and bandwidths. These are observed as linear current-voltage regions across input and output junctions in Fig. 3 (C and D). Patterns similar to that of Fig. 4A can be observed, with three distinct states at I_1 of 0 μA evolving in to five states at I_1 of 160 μA and larger. However, the corresponding rates of flow of flux are substantially larger than "1," indicating that fluxon flow rate is in the opposite direction (from output O_1 to input I_1).

Dynamic operation

The results in the previous section prove that stable memory/flux configurations exist in synapse networks that can be classified into different categories corresponding to their rates of flow of flux quanta between the input-output nodes in the state space defined by input voltage V_{I1} and output voltage V_{O1}. In addition, these categories can be continuously configured using the control currents. These results represent static operation where the network is subjected to constant frequency spiking input $I_1(B_1)$ and a constant control current $B_1(I_1)$ that holds the network in a stable memory state. A change in memory state corresponds to a significant change in the flux flow rate $\frac{dV_{O1}}{dV_{I1}}$ for the same input frequency $\frac{V_{I1}}{\Phi_0}$ as shown in Fig. 4. A leaky integrate-and-fire neuron such as that discussed in (33) can be configured to generate action potentials over a specific range of frequencies defined by $\pm f_T$, where f_T is the frequency threshold of the neuron, acting as a band-pass filter for spiking signals. Here, the negative frequency represents flux flow in the opposite direction. Therefore, the relative population densities of outgoing

flux quanta associated with each memory state defined in a configurable frequency window $\pm f_T$ can be measured.

However, during the neural network operation of the disordered array of superconducting loops, the input spike frequency dynamically changes with respect to the control current (i.e., both the signals are actively changing with respect to each other). While the spiking input signal maps the spatial and temporal information on to the memory state space, the feedback/control current signal reconfigures the memory state space according to the outgoing spike signals during the learning process. In this dynamic operation, the fluxon flow rate (equivalent to its synaptic weight) depends on the relative time difference Δt between the pre- and post-synaptic spiking analogous to that of spike timing–dependent plasticity. Experimentally, the dynamic behavior is experimentally observed in frequency state space (of input and output spiking signals) by dynamically varying both the currents I_1 and B_1 relative to each other. The memory states and their history can be mapped on to the state space of incoming and outgoing spike frequencies, and the effect of Δt on the flux flow rate can be observed by varying the phase δ and frequency f of one of these currents with respect to the other, where $\Delta t = \frac{\delta}{2\pi f}$. The memory states observed in Fig. 4 and the transitions between them are continuously configured between a wide range of voltages and across different bandwidths as the relative phase δ or frequency f of one current signal is varied with respect to the other. The results are shown in Figs. 5 and 6 as Lissajous curves in the spiking signal frequency state space defined by V_{I1} and V_{O1}, as the space is scanned by continuously varying the currents I_1 and O_1.

Initially, a sinusoidal signal of amplitude of 1 mA and frequency of 1 Hz is applied at I_1, and a similar signal of amplitude of 100 μA at the same frequency is applied at B_1, similar to the currents applied in static operation in Fig. 4. Figure 5 shows V_{O1} against V_{I1}, as the phase of B_1 is varied relative to I_1. Transitions between memory states are labeled in the figure as T_1, T_2, and T_3, with T_1 corresponding to transitions $S_1 - S_2 - S_3$, T_2 corresponding to transitions $S_3 - S_4 - S_5$, and T_3 corresponding to $S_3 - S_7 - S_{11}$. As phase difference δ is varied between 0 and 2π, state transitions move around the state space of V_{I1} and V_{O1}, as the span of frequency windows, i.e., the bandwidths across which the transitions are observed, changes in size. For example, T_1 is observed between V_{I1} of ± 0.5 mV at $\delta = 0$, but is moved to V_{I1} between 1.3 and 1.5 mV at $\delta = \pi/3$, and V_{I1} between 0.6 and 1 mV at $\delta = 2\pi/3$ as it completely disappears at $\delta = \pi$. Similar dynamics are observed for T_2 and T_3.

To further explore the memory states and their transitions in the space defined by V_{I1} and V_{O1}, frequency of one of the currents, i.e., B_1, is varied with respect to the other, i.e., I_1, and the results are shown in Fig. 6. By systematically increasing the frequency of one of the current signals with respect to another, the entire memory state space where the neural network can operate (for the given bandwidth) has been mapped. Here, a current amplitude of 1 mA and frequency of 1 Hz is applied at I_1, while a current amplitude of 100 μA is applied at B_1 with its frequency varying from 1 to 100 Hz. Different memory state classifications separated by their transitions evolve as the frequency ratio is increased. Each of these memory states corresponds to a different fluxon flow rate between I_1 and O_1 (Fig. 2). An almost continuous state space is divided into nine different categories that can be distinguished by various transitions caused by different junctions in the network switching into and out of the superconducting state. The state space is also scanned by varying the frequency of I_1 from 1 to 100 Hz with B_1 constant at

1 Hz to reveal the nine different memory states as shown in fig. S6. We note that the transitions are also labeled as memory states here as they present a region in the state space where they are stable.

During the neural network operation, the spiking signals and the currents are dynamically varying in response to the input information. As the corresponding transient current flows through different paths of the disordered network into multiple outputs as shown in Fig. 1, the information is classified or clustered into different categories that can be observed in the form of different populations of flux quanta across the stable memory states observed in the frequency state space of input and output spiking signals. Different neurons such as that discussed in (33) can be designed to access these flux quanta populations in specific frequency bands corresponding to either individual or multiple overlapped memory states. The neurons and synapse networks can be connected in the form of recurrent neural networks enabling hierarchical architecture similar to biological brains (33). This superconducting disordered loop array architecture–based network also provides a platform to explore rich spatial and temporal dynamics associated with analog neural networks.

In conclusion, we have experimentally studied a network of YBCO-based superconducting loops with Josephson junctions in the context of a dynamic memory/synapse network for use in neuromorphic computing. The role of disorder in neuromorphic network architectures can be understood through complex superconducting networks, which can also be expanded to other material systems such as that discussed in (34). However, superconducting networks correspond to superior operating speeds with maximum spike frequencies up to a few terahertz with an ultralow-energy dissipation in the order of $\approx 2 \times 10^{-18}$ J per spike, with power dissipation dependent on the operating frequencies. In addition, the proposed YBCO-based superconducting loops enable high scalability with loop widths as small as 10 nm (50), higher operation temperatures, and exponentially scaling memory capacity with a number of loops.

MATERIALS AND METHODS
Fabrication
The experimental three-loop disordered array, shown in Fig. 1, is fabricated from the high-temperature superconductor YBCO film. Josephson junction barriers are defined using a focused ion beam from a helium ion microscope. In this particular device, each loop is designed to have a large inductance to accommodate several flux quanta ranging between 20 and 60 Φ_0 per loop. The critical currents of different junctions are varied between 100 and 150 μA using the dose of the ion irradiation while fabricating the tunnel barrier with junction width kept constant.

Samples were fabricated from wafers of 35-nm-thick YBCO capped with 200 nm of gold deposited in situ for electrical contact. The YBCO layer was grown via thermal reactive coevaporation on a CeO_2 buffered sapphire substrate (51). These wafers were purchased from Ceraco GmbH. Samples were diced from this wafer into 5 mm by 5 mm squares.

A photolithography and ion milling process was used to define the bulk electrodes that would make up the loop array, ground plane, and terminals. Samples were spin-coated for 45 s at 5000 rpm with Fuji OCG 825 photoresist. A Microtech LaserWriter exposed the photoresist with a 405-nm GaN solid-state laser defining the layout pattern. The photoresist was developed with OCG 934 and mounted into a broad-beam argon ion mill. This ion milling

isolated the traces and loops of the layout design by milling away the material. A second lithographic step was performed to open apertures in the gold capping layer such that the helium ion irradiation could be incident directly on the YBCO layer. A 200 μm by 200 μm square region that contained all the locations for the Josephson junctions was exposed to Ki^+ etch to chemically remove the gold layer while maintaining the YBCO thin film. An optical image of the output of these fabrication steps is presented in Fig. 2A of the article.

The sample was then mounted in a Zeiss Orion NanoFab gas field ion source. The focused ion beam produced in the NanoFab can be focused to a beam spot size on the scale of 1 nm and controlled with subnanometer resolution. The beam parameters used in the fabrication of the Josephson junctions was a 0.5-pA helium ion beam accelerated at 32.5 kV. This beam was rastered in a line across the lithographically defined electrodes, introducing an average ion fluence of 4×10^{16} ions/nm to define the Josephson barriers. Ion fluence influences the nature of the barrier, practically effecting the critical current of the Josephson junctions. Actual ion fluence was varied up to 25% from the average, causing variations in the Josephson junction critical currents intentionally to introduce the disorder (i.e., nonuniformity) in the loop array. Locations of the Josephson junction–irradiated regions are indicated in Fig. 2A of the article.

Test setup

After fabrication, the sample was mounted on a J-Lead 44-pin chip carrier. Electrical contacts between the sample and the chip carrier were made via Al wire bonds. The chip carrier was then inserted into a socket at the tip of a cryogenic insert probe that was evacuated and back-filled with 500 mtorr of helium gas meant for temperature exchange. The insert was cooled inside a liquid helium storage dewar where the temperature may be controlled by adjusting the tip height in relation to the liquid helium surface. The temperature was held at 28 K temperature for all the experiment measurements reported, except for the results shown in fig. S1; the measurements of which were performed at 4.2 K.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at https://science.org/doi/10.1126/sciadv.abn4485

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