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All Solution-Processed Inorganic, Multilevel Memristors Utilizing Liquid Metals Electrodes Suitable for Analog Computing

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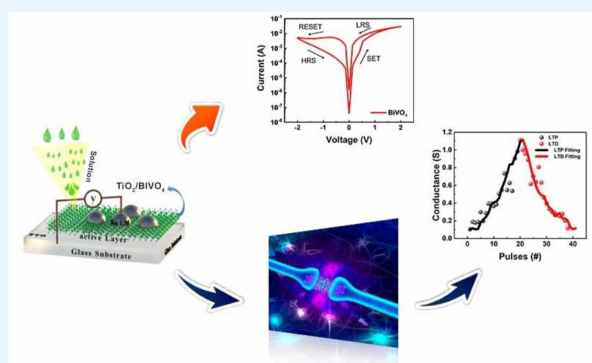
ABSTRACT: Herein, we report a solution-processable memristive device based on bismuth vanadate ($BiVO_4$) and titanium dioxide (TiO_2) with gallium-based eutectic gallium−indium (EGaIn) and gallium−indium-tin alloy (GaInSn) liquid metal as the top electrode. Scanning electron microscopy (SEM) shows the formation of a nonporous structure of $BiVO_4$ and TiO_2 for efficient resistive switching. Additionally, the gallium-based liquid metal (GLM)-contacted memristors exhibit stable memristor behavior over a wide temperature range from −10 to +90 °C. Gallium atoms in the liquid metal play an important role in the conductive filament formation as well as the device's operation stability as elucidated by *I*−*V* characteristics. The synaptic behavior of the GLM-memristors was characterized, with excellent long-term potentiation (LTP) and long-term depression (LTD) linearity. Using the performance of our device in a multilayer perceptron (MLP) network, a ~90% accuracy in the handwriting recognition of modified national institute of standards and technology database (MNIST) was achieved. Our findings pave a path for solution-processed/GLM-based memristors which can be used in neuromorphic applications on flexible substrates in a harsh environment.



1. INTRODUCTION

Interest in analog computing has been growing over the past few years to address the challenges of future computing. With the growing demand for data-driven applications such as the next-generation machine learning accelerators and Internet of Things, the traditional von-Neumann architecture with disjoint memory and processing units suffers from huge memory latency and limited data bandwidth. This is further intensified by the scaling limits of silicon transistors. In order to surpass these bottlenecks, analog computing, or in-memory computing, is a potential solution. The use of memristors, an emerging nonvolatile memory, exhibit characteristics that suit this purpose.[1−9] Memristors' simple device structure, high operating speed, low operating power, and ability to be tuned to various resistance states for multibit storage in a single device make them an active area of research over the past decade. Physical vapor deposition (PVD) and atomic layer deposition (ALD) techniques are two common approaches for memristor fabrication due to their potential for large-scale implementation in industry. However, the strict requirements on the processing temperature and materials choice restrict their use in beyond-silicon technology. On the other hand, solution-processing techniques appear to show greater promise in fabricating electronics in different forms such as those requiring a nonplanar substrate.[10−13] Moreover, solution-processing can be done at room temperature (suitable for flexible substrates) and can be large area deposited.[14,15] Recently, researchers have reported on solution-based inorganic semiconducting materials bismuth vanadate ($BiVO_4$) and titanium dioxide (TiO_2) for various applications such as energy production, energy storage, photocatalysis, and environmental remediation.[3,16] $BiVO_4$ and TiO_2 (having bandgaps of 2.4 and 3.2 eV, respectively) are chemically stable and nontoxic materials in the solid and aqueous states and have also been demonstrated to exhibit memristive behaviors.[17,18] The unique advantages of $BiVO_4$ and TiO_2 are summarized in Table 1.

These inorganic semiconducting materials naturally contain defects in the form of oxygen vacancies (V_o) for resistive switching. The optimization of defects density in such materials are poised to further reduce the switching voltage

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Table 1. Unique Advantages of TiO_2 and $BiVO_4$

Materials	Advantages	References
TiO_2	Nontoxicity, high refractive index, high photostability, high binding affinity, large covering power, low cost, mechanical, thermal, and chemical stability.	19, 20
$BiVO_4$	Resistant to photo corrosion, narrow bandgap, good chemical stability, low toxicity, low synthesis cost, and works under visible light.	21, 22

and power. However, the mechanisms and characteristics of these solution process fabricated materials are still not well understood.

Electrodes play an important role in a memristor's behavior, e.g., digital, or analog switching. Liquid metal (LM) alloys such as eutectic-gallium−indium (EGaIn) and gallium−indium−tin (GaInSn) alloy are interesting electrode materials to research due to their potential flexible and deformable properties as well as their low electrical resistivity; in addition, they are nontoxic in nature. They have already been reported in various applications such as flexible capacitors, inductors, resistors, actuators, power sources, thermal management, antennas, and bio applications.[23−33] Hence, GLMs find potential use in soft material liquid-like memristors such as electrolytes, gels, and ionic liquids and find similar behavior as compared to its conventional memristor counter-parts for use in biomimicking and neuromorphic applications apart from its pliability and substrate insensitivity.[34−38]

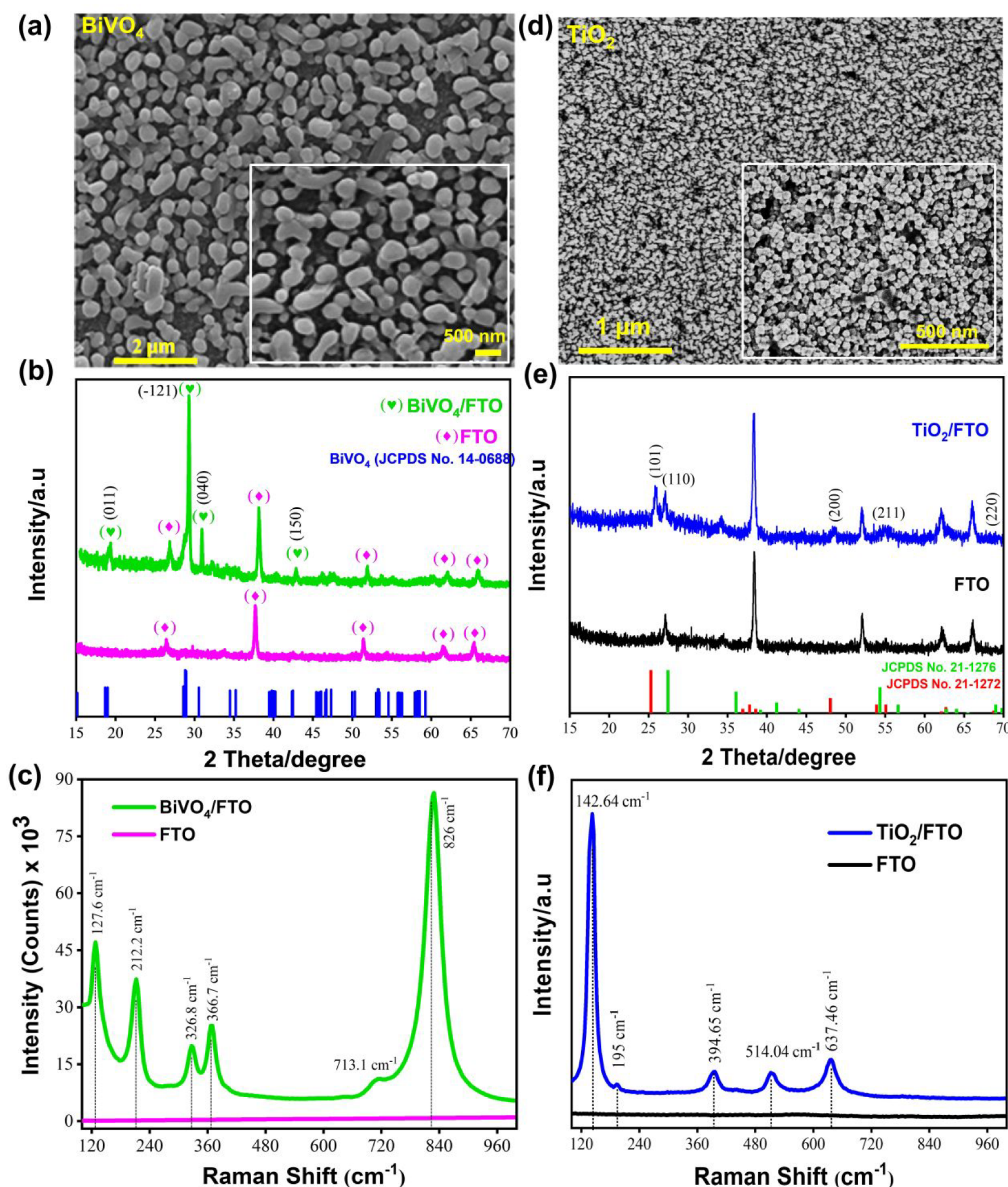

Figure 1. (a) SEM image of $BiVO_4$ on FTO substrate, (b) XRD of $BiVO_4$ film, (c) Raman spectrum of the naked FTO and $BiVO_4$ film, (d) SEM image of synthesized TiO_2, (e) XRD of TiO_2, and (f) Raman spectrum of FTO and TiO_2.

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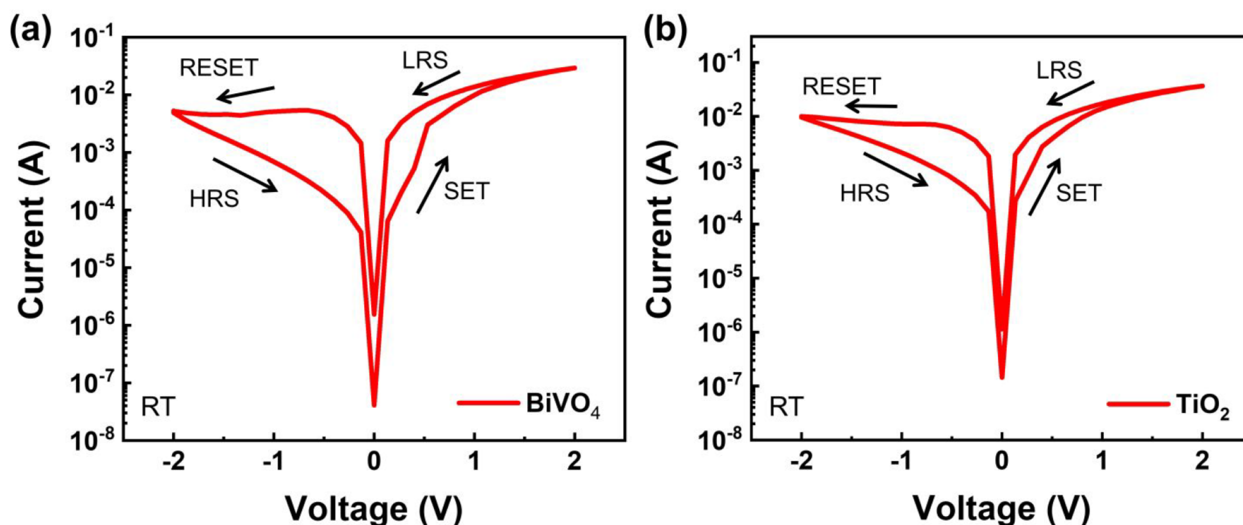

Figure 2. Electrical characterization of GLM-based inorganic prototype devices; arrows show the voltage directions; active layer thickness was about ∼100 nm. (a) EGaIn/$BiVO_4$/FTO device *I*−*V* characterization under 2 V. (b) *I*−*V* measurements of the EGaIn/TiO_2/FTO prototype structure under 2 V.

Our recent work based on EGaIn liquid metal (LM) based memristors demonstrated memory behavior independent of intermediate insulator material type. However, the effects of individual components of LM in the switching behavior were not studied, nor was the behavior at elevated temperature and synaptic behavior.[39] The study of such effects could possibly provide the key to realize the high performance of GLM memristor devices for use in a plethora of applications. Herein, we report on a solution-processed memristor based on inorganic materials—$BiVO_4$ and TiO_2—loaded with LMs (EGaIn and GaInSn 68.5% gallium, 21.5% indium, and 10% tin) with a droplet as the top electrode. Detailed characterizations of the $BiVO_4$ and TiO_2 materials were carried out using SEM, XRD, and RAMAN spectroscopy. The as-deposited materials show nonporous microstructure, good crystallinity, and organized arrangement of local microstructures, proving beneficial for resistive switching. The *I*−*V* switching curve measurements of the memristors exhibit stable performance over a wide range of temperatures from −10 to +90 °C, well suited for use in a harsh environment. Hence, our findings suggest that GLM-based memristor devices may be suitable for future memory device technology for use in a harsh environment.

2. RESULTS AND DISCUSSION

The morphology, crystal phase, and local structure of fabricated materials were studied by using scanning electron microscope (SEM), X-ray powder diffraction (XRD), and Raman spectroscopy. Figure 1(a) shows the nanoporous morphology of the $BiVO_4$ layer. The $BiVO_4$ particles have a diameter of ∼200 nm with pore sizes ranging from 20 to 100 nm. The purity and crystal phase of the $BiVO_4$ is shown in the XRD spectra in Figure 1(b). It is seen that the $BiVO_4$ layer exhibits a monoclinic scheelite structure according to the joint committee on powder diffraction standards (JCPDS) PDF No.14-0688. The distinctive peaks located at 18.98°, 28.82°, 30.54°, 42.33°, and 53.44° match well to the crystal planes (0 1 1), (−1 2 1), (0 4 0), (1 5 0), and (3 1 0). These distinctive peaks are clear indication of the good crystallinity of the coated $BiVO_4$ layer. Figure 1(c) shows the Raman spectrum of $BiVO_4$ over wavelengths of 100−1000 cm^{-1}. Distinctive Raman bands at 826 and 713.1 cm^{-1} are attributed to V−O symmetric and antisymmetric stretching modes (A_g), respectively.[40,41] The bands at 366.7 and 326.8 cm^{-1} are recognized as symmetric (B_g) and antisymmetric (A_g) V−O bending mode of the VO_4, while the bands at 212.2 and 127.6 cm^{-1} are ascribed to the rotational and translational modes of $BiVO_4$.

Figure 1(d) shows the nanoporous morphology of the TiO_2 layer under SEM with a diameter of ∼150 nm and pore sizes ranging from 21 to 90 nm. The XRD spectra of the TiO_2 layer show the tetragonal pattern of the anatase and rutile phases in accordance with JCPDS File Nos. 21-1272 and 21-1276 (Figure 1(e)). The observed TiO_2 peaks at 27.45° and 36.08° correspond well with the crystal plane (110) and (101) of the rutile phase, while the peaks at 25.28°, 48.04°, and 55.06° correspond to the crystalline planes (101), (200), and (211) of anatase, respectively. The diffraction peaks of FTO in fabricated samples present a thin thickness and high porosity. Figure 1(f) shows the Raman spectroscopy of the TiO_2 layer at 142.64 (E_g), 195 (E_g), 394.65 (B_{1g}), 514.04 (A_{1g}), and 637.46 cm^{-1} (E_g), which are assigned to the anatase phase of TiO_2, while a minor peak at 445 (E_g) corresponds to the rutile phase of TiO_2, in good agreement with XRD measurements in Figure 1(e). The cross-sectional image of a representative fabricated memristor is shown in Figure S1, where each layer is marked out. The plane view SEM image of the FTO substrate is shown in Figure S2, showing a smooth and uniform surface, consistent with that reported in the literature.[42] The tilted SEM view of the drop-casted sample is presented in Figure S3, showing a generally smooth surface for unintentional particles generated during sample preparation for characterization.

Figure 2 shows the semi logarithmic *I*−*V* plot of the EGaIn/$BiVO_4$/FTO (Figure 2(a)) and EGaIn/TiO_2/FTO memristors (Figure 2(b)), over an applied DC voltage ±2 V at room temperature. The freshly fabricated devices are initially at a high resistance state (HRS). As the voltage is swept from the positive to negative region as indicated by the arrows in Figure 2, clear transition of the devices' resistance state from high → low → high was observed. Both types of devices exhibit a bipolar switching behavior. Interestingly, all devices exhibit a

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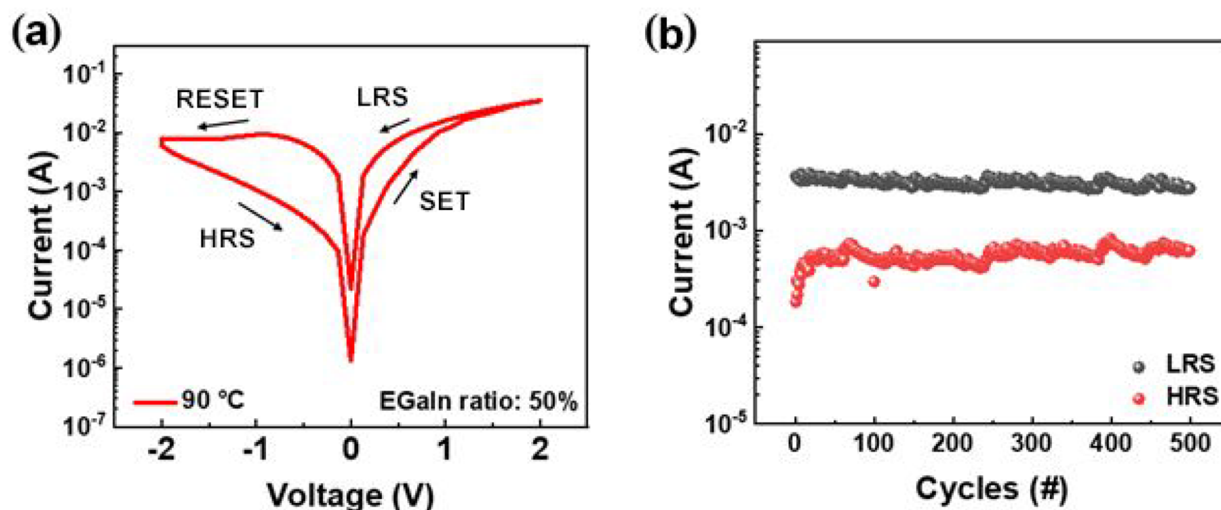

Figure 3. (a) Temperature-dependent electrical characterizations of EGaIn/$BiVO_4$/FTO prototype device structure at 90 °C under ±2 V with Ga (50%) and In (50%) ratio, respectively. (b) DC endurance characterization of device (a).

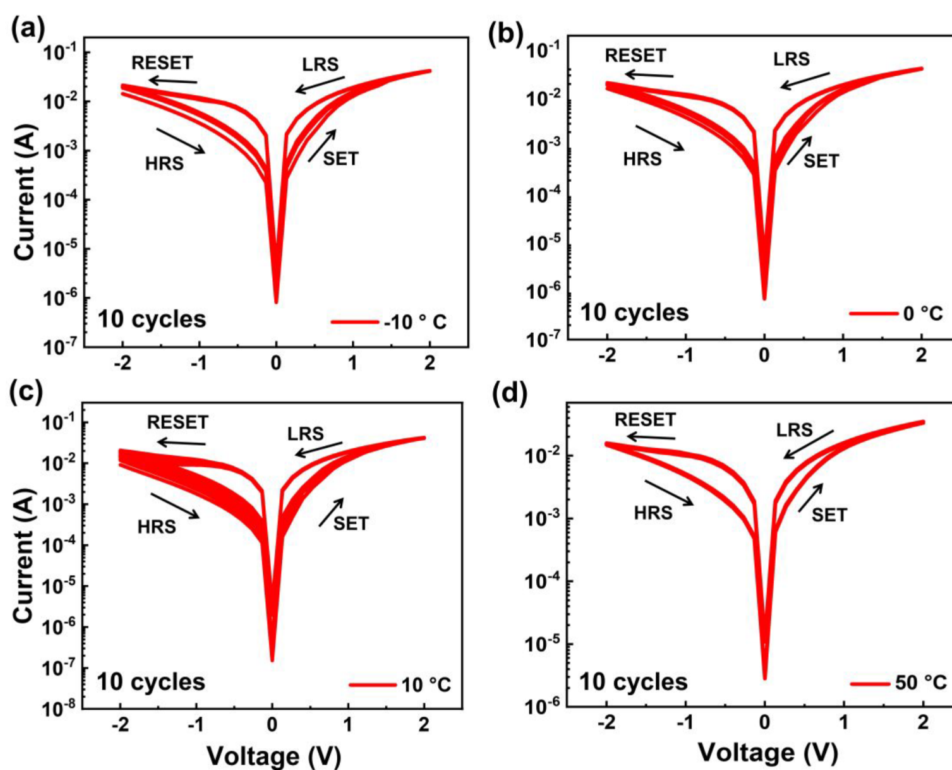

Figure 4. Temperature-dependent electrical characterizations. Gallium-based EGaIn liquid metal in a droplet shape was used as the top electrode with gallium (Ga: 75%), indium (In: 25%) ratio, respectively. The *I*−*V* characterizations are measured at (a) −10 °C, (b) 0 °C, (c) 10 °C, and (d) 50 °C under 2 V bias.

forming free behavior. This behavior is likely due to the nanoporous structure as evidenced by the SEM images in Figure 1(a),(d). The large particle surface area to volume ratio is advantageous in increasing the percolation path for ease of filament formation during resistive switching, thus leading to a forming free behavior. In addition, the $BiVO_4/TiO_2$ composite device also shows bipolar resistive memory (Figure S4 (a)) with repeatable behavior (Figure S4(b)). Observing similar behavior in both materials, we focused on the $BiVO_4$-based memristors in the subsequent discussion. Moreover, the $BiVO_4$ memristors' device to device variation of the set and rest states are shown in Figure S5.

Based on the previous findings on the filament formation mechanism, thickness-dependent EGaIn LM particles or ions/atoms are responsible for the conductive filaments, which may form and rupture by oxidation/reduction of the LM surface under the electrical bias.[43−47] In order to further understand the switching mechanism, i.e., the effects of individual components of gallium (Ga) and indium (In), the EGaIn with Ga (50%) and In (50%) in an EGaIn/$BiVO_4$/FTO device structure at an elevated temperature of 90 °C was studied.

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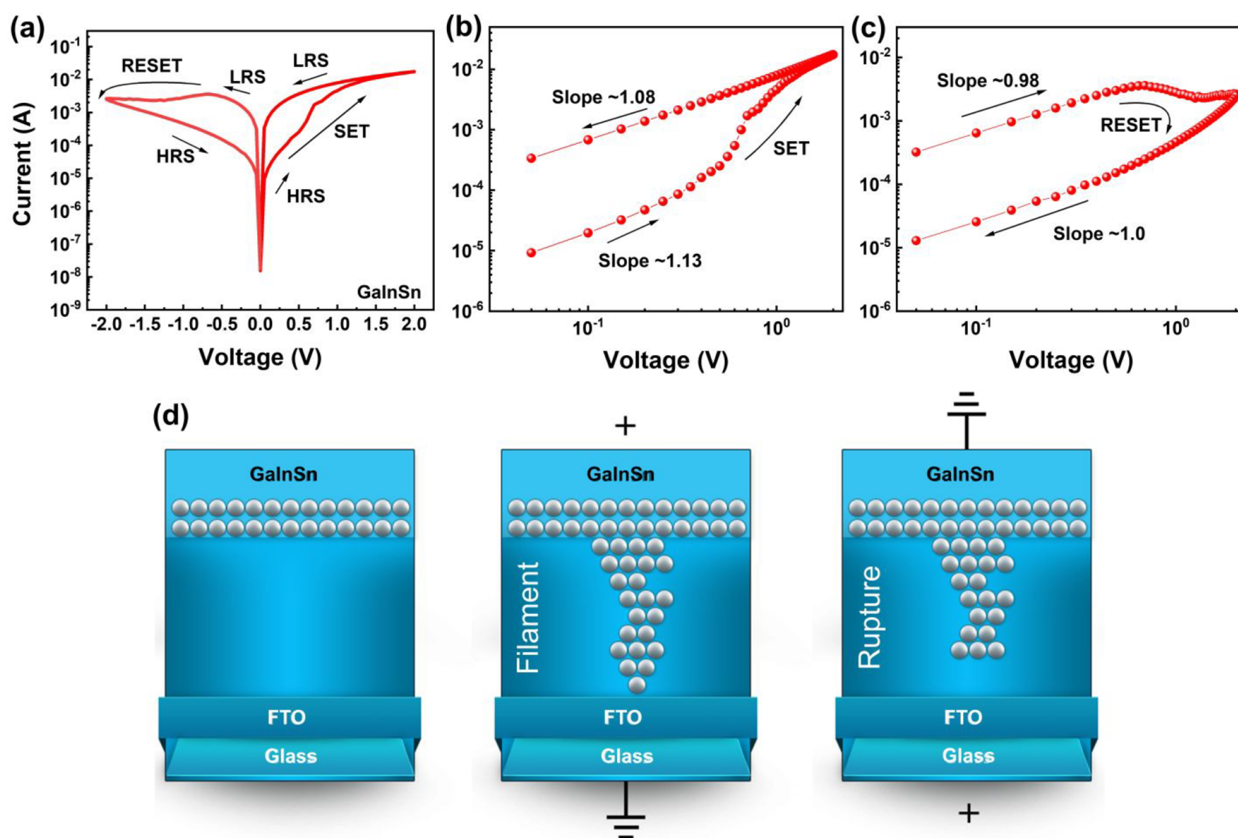

Figure 5. Electrical characterization and schematic illustration of the mechanism for GaInSn as the top electrode at ±2 V bias. All characterizations were done at room temperature. (a) Semilogarithmic *I*−*V* characterizations of GaInSn/$BiVO_4$/FTO show bipolar memristor properties. (b) Curve fitting in log−log scale under positive *I*−*V* bias. (c) Curve fitting in log−log scale under negative *I*−*V* bias. (d) Schematic illustration of device switching mechanism in the virgin state, filament formation state—under the positive bias application, and filament rupture state—under the negative bias application.

Figure 3(a) shows the *I*−*V* switching characteristics, indicating bipolar switching well within 2 V. Even at continuous voltage sweeps over 500 DC cycles, the device exhibits stable and few fluctuations of the HRS and LRS states with a read voltage (V_{read}) of 0.2 V (Figure 3(b)). A further retention characterization of the device at 90 °C shows that the LRS state is retained up to 1.5×10^4 s (Figure S6). The retainment of the bipolar resistive memory properties with a different Ga ratio suggests the role of indium in lowering the LM melting temperature, while the formation of a conductive filament for the resistive memory properties is dominated by Ga. The small variation of resistance changes as the number of switching cycles is increased demonstrates good reliability for use at elevated temperatures. Furthermore, it supports the interpretation of a common switching mechanism even when changing the ratio of Ga and In in the top electrode for the formation of a conductive filament during the set process.

In order to further understand the role of Ga and In in the resistive switching behavior, we further characterized an EGaIn/$BiVO_4$/FTO device with Ga (75%) and In (25%) ratios under various elevated temperatures (−10, 0, +10, and +50 °C) as shown in Figure 4(a−d). In addition, bipolar resistive memory properties are observed even up to 75 and 90 °C, as shown in Figure S7(a),(b) respectively. To further understand the role of GLMs in the device-switching behavior, a slope-fitting method was used to extract the nature of the metal-switching layer contact, where in both negative and positive operating regimes (Figure S8 and Figure S9, respectively) the fitted slope has a gradient ranging from 1 to 1.2 (ohmic contact). This behavior is independent of the device temperature, suggesting the stability of the conductive filament in this device structure. These findings suggest that further scaling of GLM-based memristor devices depends on the conductive filament size as well as the ease of formation and rupture of the conductive filament at each set and reset state, respectively.

Subsequently, we characterized a GaInSn (65.5%, In 21.5%, 10% Sn)/$BiVO_4$/FTO device structure with resistive switching behavior with the sequence shown on the arrow (Figure 5(a)). Similar to the EGaIn top electrode, stable bipolar resistive memory behavior was obtained, suggesting that Ga atoms are the main contributor to the filament formation/rupture during the set and reset operation. In addition, by changing the compliance current during the set process, the device is able to be set to different resistance levels, indicating that the size of the filament in this device can be modulated (Figure S10).

Figure 5(b),(c) shows the fitting curves of the GaInSn/$BiVO_4$/FTO device structure at the positive and negative operating regimes, respectively, at room temperature. In the HRS and LRS, a fitted slope of ∼1.13 and ∼1.08, respectively, are extracted, of which both indicate ohmic contact, further establishing the key role of Ga in the formation and rupture of the conductive filament during the set/reset process. Moreover, the ohmic slope calculations could indicate conductive filament as well as Schottky and space charge limited currents. However, the LM used and our measurements suggest the

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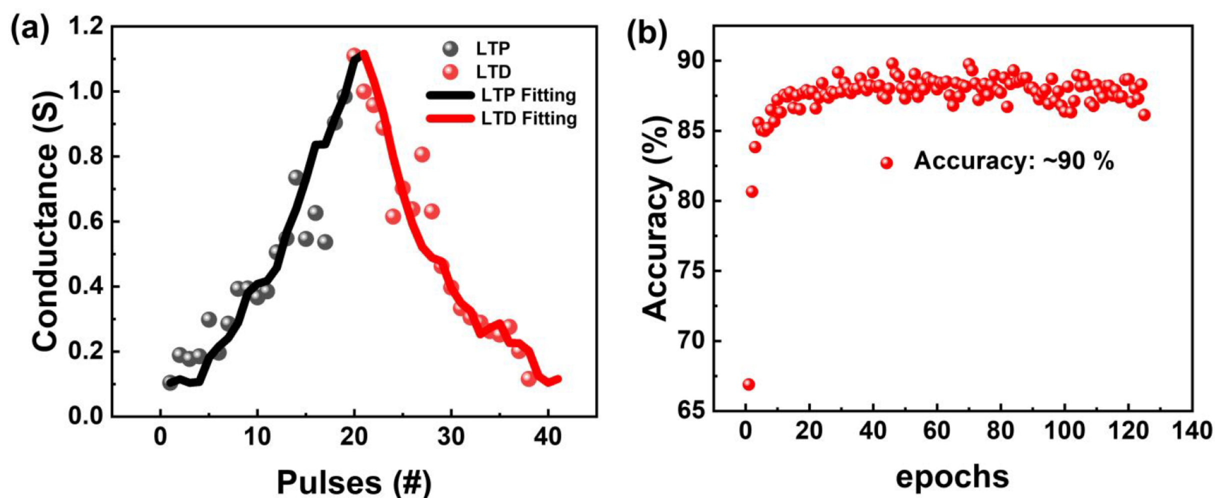

Figure 6. (a) Potentiation and depression characterizations with 20 positive and 20 negative pulses; black and red color correspond to LTP and LTD fitting, respectively. (b) Two-layer neural network-based simulation accuracy in determining handwritten patterns.

penetration of highly diffusive Ga atoms/particles/ions from the LM into the switching layer during the set and reset process. Hence, based on the above analysis of the different devices, we illustrated the switching mechanism of this class of device structure in Figure 5(d). Before the application of electrical voltage, the device is at a virgin state (Figure 5(d)), with no filament connected between the top and bottom electrodes. When the threshold voltage (resulting in set of devices) is applied, the device switches to the LRS state, where the GLMs quickly form conductive Ga filaments inside active layers, improving the ohmic contact nature further (fitted slope transiting from ~1.13 to ~1.08) as depicted in the filament formation stage in Figure 5(d). Under sufficient negative bias, the conductive Ga filament starts to rupture (fitted slope transiting from ~0.98 to ~1.05) as depicted in the filament rupture stage in Figure 5(d). Similar to the EGaIn top electrode, there is no observation of a forming process in the memristor device, attributed to the nanoporous structure and presence of an intrinsically large number of defects. Hence, it is clear that there is a common switching mechanism when GLMs top electrodes are used, regardless of the Ga concentration. It is worth pointing out that liquid metal is used for the fabrication of the top gate for memristor application of liquid. It is a relatively easy process, but the area or dimension quantification of this type of electrode is also challenging due to the liquid state of the metal, with the possibility of filling the porous structure in the switching layer.

In this section, we evaluate the potential of the device reported in this work in an example of supervised artificial neural network (ANN) for MNIST database handwriting recognition. The analog conductance modulation properties of the GaInSn/$BiVO_4$/FTO device exhibit good potentiation and depression properties as shown in Figure 6(a). A fitted nonlinearity factor of −2.92 and −1.75 for long-term potentiation (LTP) and long-term depression (LTD) (Figure S11 caption shows write voltage and pulse width values) were obtained as per eqs 1−3.[48] In the same plot, the fitted line using a variation value of 2% is plotted. The variation of 2% is fitted with respect to our experimental data as shown in Figure 6(a)

$$G_p = B(1 - e^{(-\frac{P}{A_p})}) + G_{min} \quad (1)$$

$$G_d = B(1 - e^{(\frac{P-P_{max}}{A_d})}) + G_{max} \quad (2)$$

$$B = \frac{(G_{max} - G_{min})}{(1 - e^{(-\frac{P_{max}}{A})})} \quad (3)$$

where G_{max} is the maximum conductance, G_{min} is the minimum conductance, and P_{max} is the maximum number of pulses required to switch the device between minimum and maximum conductance states. A_p and A_d correspond to the potentiation and depression linearity attributes, respectively. B represents the functions of A for fitting in the range of G_{max}, G_{min}, and P_{max} fitting. G_p and G_d represent the LTP and LTD conductance, respectively.

A two-layer multiplayer perceptron (MLP) neural network model with 400 input neurons, 100 hidden neurons, and 10 output neurons was utilized (Figure S11). The 400 input neurons correspond to a downscaled 20 × 20 MNIST data, and the 10 output neurons correspond to 10 classes of digits (0−9); more details are given in the Figure S11 caption. In the simulation training, the adaptive moment estimation (ADAM) optimization method was used while obtaining a simulated recognition training accuracy of ~90% as shown in Figure 6(b). It is worth pointing out that the simulated accuracy may be further improved by optimizing the weight tuning schemes by increasing the number of analog states as well as device structure engineering to achieve a higher nonlinearity factor. Nonetheless, the initial results of our solution-processed device provide a feasible path for use in ANN applications with further optimization.

3. CONCLUSION

In summary, we have investigated the performance of facile, room-temperature solution-processed memristors based on $BiVO_4$ and TiO_2 with GLMs as the top electrode. All of the fabricated devices showed stable memristor behavior up to an elevated temperature of 90 °C. The switching behavior was elucidated to be related to the Ga conductive filament formation and rupturing from the electrical characterizations of devices with both EGaIn and GaInSn top electrodes. Synaptic behavior manifesting in the form of LTP and LTD with good nonlinearity factor can be obtained by controlling

the size of the filament via current limitation of constant voltage pulses. An evaluation of our memristor performance using an MLP network for handwriting recognition of the MINIST database results in a learning accuracy of ~90% and can be further improved via device optimizations. Our findings show that our solution-processed GLMs-based memristor could pave a path for future electronics applications requiring nonplanar surfaces and harsh environments.

4. EXPERIMENTAL SECTION

4.1. Experimental Reagents. Bismuth nitrate pentahydrate (Bi $(NO_3)_3 \cdot 5H_2O$, ≥98.0%), and ammonia (NH_3, ≥99.0%) were bought from Aladdin Industrial Co., Ltd. (Shanghai, China). Ethylenediaminetetraacetic acid disodium salt ($C_{10}H_{14}N_2Na_2O_8.2H_2O$, ≥99.4%) and ethanol ($C_2H_5OH$, ≥99.4%) were purchased from Sinopharm Chemical Reagent Co., Ltd. Fluoride-tin oxide glass (FTO) with size 50 × 10 mm^2 and thickness 1 mm was obtained from Wuhan Jinge-Solar Energy Technology Co., Ltd. and Vanadium oxide (V_2O_5, ≥98.0%) was acquired from Alfa Aesar. GLMs (EGaIn and GaInSn) were obtained from Beijing Hualide Technology Co., Ltd. FTO impurities were removed through sonication by dipping in the acetone (C_3H_6O), ethanol (C_2H_5OH), and deionized (DI) water solution. All chemical reagents were of analytical grade and used without any further purification.

4.2. Device Fabrication Method. A drop coating method was used for the fabrication of $BiVO_4$, and TiO_2 films on a fluorine−tin-oxide (FTO) covered area 1.25 × 1 cm^2 substrate. Meanwhile, FTO acts as the bottom electrode for the memristor. The schematic presentation of the preparation method for $BiVO_4$ and TiO_2 is ashown in Figure S12(a),(b).

Electrical characterizations of our fabricated devices were carried out using a Keysight semiconductor device parameter analyzer (B1500A). GLMs such as EGaIn, (Ga [75%], In [25%]), (Ga [50%, In [50%]), and GaInSn (Ga 65.5%, In 21.5%, 10% Sn) acting as deformable top electrodes were used for all prototype memristor devices. We used a micropipette to deposit liquid metal droplets (volume of ~4 μL) with a diameter of less than 1 mm. In a crossbar structure integration for instance, the electrodes can be formed by utilizing approaches such as (1) printing[12,49] or (2) microfluidics channel,[50] similar to that used in reports of flexible electronics fabrication. A schematic of the fabricated device sample is illustrated in Figure S12(c). In our measurements, the FTO layer is grounded while electrical bias is applied to the contacted GLM droplet. All the electrical characterization measurements were carried out at room temperature and at elevated temperatures (−10, 0, +10, +50, +75, and +90 °C).

4.3. Synthesis and Preparation of the $BiVO_4$ Layer. $BiVO_4$ was prepared by using the drop-coating method according to the report of Bacha et al.[40,41] Briefly, 4 mmol of diethylenetriaminepentaacetic acid (DTPA) and 1.5 mL of NH_3 (13.0 mol L^{-1} in water) were mixed in hot DI water (40 mL) using a magnetic stirrer to create a uniform suspension. Thereafter, Bi $(NO_3)_3 \cdot 5H_2O$ (2 mmol) and V_2O_5 (0.97 mmol) were added to the above solution at a temperature of 70 °C and further stirred until the solution turned transparent. The elevated temperature promotes the reaction and dissolution rate. 15 μL of the prepared precursor solution was then drop-cast on conductive side of FTO. The coated substrate was then dried in the oven at 60 °C, followed by calcination at 500 °C for 3 h with a 2 °C min^{-1} ramping rate in a muffle furnace.

4.4. Synthesis and Preparation of the TiO_2 Layer. TiO_2 was synthesized by using a drop-coating method following the Nabi et al. report.[51] First, a commercial Degussa TiO_2 powder (P25) was ground in a mortar following the addition of DI water (7 mL) in a dropwise manner to get a uniform precursor solution. Thereafter, the precursor solution was sonicated for 60 min to create a uniform suspension of TiO_2. 15 μL of precursor solution was then dropped-cast on FTO, dried at 70 °C in an oven, followed by calcination of the TiO_2 layer at 500 °C for 3 h with a 2 °C min^{-1} ramping rate. The drop-casting method leads to the formation of nonuniform films which might result performance degradation of the memristor. Careful control in obtaining uniform film is essential to ensure consistent performance of the memristors to be implemented on a large scale.

4.5. Synthesized Material Characterization. The morphological characterization was analyzed by scanning electron microscopy (SEM) (Model No. HITACHI FE-SEM SU8230). The used electrode ($BiVO_4$ and TiO_2) crystal structures were studied by using X-ray diffraction (XRD) patterns with a Bruker instrument, and the Cu Kα value was from 15° to 70° (2° per min scanning speed). The structural information on the used materials ($BiVO_4$ and TiO_2) was acquired with a HORIBA RAMAN Xplore Plus spectrometer with laser (λ = 532 nm).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.2c03893.

(Figure S1) Cross-sectional SEM image of the EGaIn/$BiVO_4$/FTO structure. (Figure S2) SEM image of FTO substrate. (Figure S3) SEM view of the inorganic layer. (Figure S4) (a) EGaIn/$BiVO_4$/TiO_2/FTO heterostructure device electrical characterization under ±2 V; arrows show the voltage sweep directions; active layer thickness is about ~100 nm; (b) Multicycle (50 cycles) *I*−*V* for the device in (a). (Figure S5) Cumulative probability plot of the $BiVO_4$ memristor HRS/LRS resistance states extracted from nine different devices at room temperature. (Figure S6) Retention characterization of the EGaIn/$BiVO_4$/FTO device under 90 °C. Read voltage used is 0.2 V. (Figure S7) Temperature-dependent electrical characterizations, gallium-based EGaIn liquid metal in droplet shape was used as top electrode with gallium (Ga: 75%), and indium (In: 25%) ratio, respectively. The *I*−*V* characterizations at (a) 75 °C, (b) 90 °C under ±2 V bias are shown. (Figure S8) *I*−*V* curve slope vs temperature graph in logarithmic scale under positive bias. (Figure S9) *I*−*V* curve slope vs temperature graph in logarithmic scale under negative bias. (Figure S10) Multilevel resistance states at various compliance current (c.c) levels for the GaInSn/$BiVO_4$/FTO device under room temperature. (Figure S11) Schematic of two-layer multilayer perceptron (MLP) neural network for MINIST handwriting (0−9) recognition. (Figure S12) Illustration of the drop coating method for (a) $BiVO_4$, and (b) TiO_2 materials, and (c) schematic illustration of the GLMs prototype memristor devices (PDF)

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The authors declare no competing financial interest.

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