

State-of-the-Art β -Ga₂O₃ Field-Effect Transistors for Power Electronics

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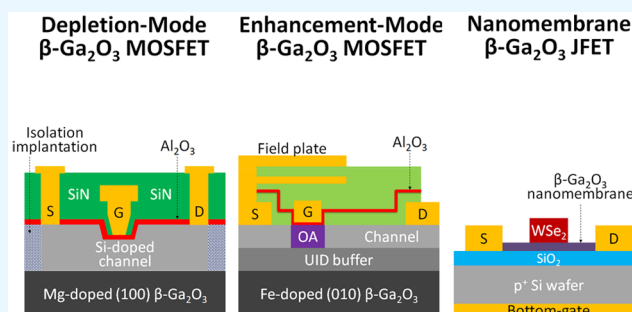
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ABSTRACT: Due to the emergence of electric vehicles, power electronics have become the new focal point of research. Compared to commercialized semiconductors, such as Si, GaN, and SiC, power devices based on β -Ga₂O₃ are capable of handling high voltages in smaller dimensions and with higher efficiencies, because of the ultrawide bandgap (4.9 eV) and large breakdown electric field (8 MV cm⁻¹). Furthermore, the β -Ga₂O₃ bulk crystals can be synthesized by the relatively low-cost melt growth methods, making the single-crystal substrates and epitaxial layers readily accessible for fabricating high-performance power devices. In this article, we first provide a comprehensive review on the material properties, crystal growth, and deposition methods of β -Ga₂O₃, and then focus on the state-of-the-art depletion mode, enhancement mode, and nanomembrane field-effect transistors (FETs) based on β -Ga₂O₃ for high-power switching and high-frequency amplification applications. In the meantime, device-level approaches to cope with the two main issues of β -Ga₂O₃, namely, the lack of p-type doping and the relatively low thermal conductivity, will be discussed and compared.



INTRODUCTION

Gallium oxide, as a type of semiconducting sesquioxide, has been known for decades.^{1–3} In recent years, owing to the tremendous progress in crystal growth and epitaxy techniques,^{4–8} gallium oxide, particularly β -Ga₂O₃, has attracted renewed attention as one of the fourth-generation ultra-wide-bandgap (UWBG) semiconductors, in addition to AlGaN, diamond, and cubic boron nitride.⁹ In comparison to the well-established SiC and GaN technologies, β -Ga₂O₃ with a larger energy bandgap (4.9 eV) exhibits higher breakdown electric field (8 MV cm⁻¹) and better Baliga's figure of merit (BFOM) (Table 1), suggesting much less power loss incurred in the power devices based on β -Ga₂O₃.^{10–14} The first single-crystal field-effect transistors (FETs) based on β -Ga₂O₃ homoepitaxial layers were demonstrated in 2012.¹⁵ Furthermore, since the β -Ga₂O₃ crystals can be synthesized by various melt growth methods at atmospheric pressure, such as the floating zone (FZ), Czochralski (CZ), and edge-defined film-fed growth (EFG) methods, the cost for producing large-area, uniform, single-crystal substrates can be greatly reduced.^{4–6} In contrast, the bulk crystals of SiC and GaN can only be manufactured by the less efficient vapor growth methods, such as the sublimation method for SiC crystals and the sodium flux and ammonothermal methods for GaN crystals.^{16–18} So far, β -Ga₂O₃ wafers with diameters up to 4 in. have already been

demonstrated or commercialized by companies, such as Tamura, Koha, and Novel Crystal Technology.⁶ Due to its UWBG nature, β -Ga₂O₃ has found various optoelectronic applications, including solar-blind deep ultraviolet (DUV) photodetectors and transparent conductive oxide (TCO) electrodes for the light emitting diodes (LEDs).^{19,20} Furthermore, the β -Ga₂O₃ nanowires and thin films with extraordinary chemical and thermal stabilities have been explored as highly sensitive gas sensors,²¹ and the amorphous and stoichiometric Ga₂O₃ thin films deposited on GaAs (001) substrates can potentially serve as the GaAs gate dielectrics.²²

As electric vehicles revolutionize the automotive market, power electronics, a vital component of electric powertrains alongside batteries and traction motors, have emerged as a new research focus. The power electronics in electric vehicles mainly include the AC-to-DC rectifiers for charging the batteries, the DC-to-DC converters between high- and low-voltage batteries, and most importantly, the DC-to-AC

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Table 1. Material Properties, BFOMs, JFOMs, and HCAFOMs of Different Semiconductors, Including Si, GaAs, 4H-SiC, GaN, β -Ga₂O₃, and Diamond^{10–14a}

Crystal Type	Crystal Structure	Energy Bandgap (eV)	Dielectric Constant (ϵ_r)	RT Electron Mobility (μ , cm ² V ⁻¹ s ⁻¹)	Breakdown Electric Field (E_{BR} , MV cm ⁻¹)	Electron Saturation Velocity (v_{sat} , $\times 10^7$ cm s ⁻¹)	Thermal Conductivity (W m ⁻¹ K ⁻¹)	BFOM ($\epsilon_r \mu E_{BR}^3$)	JFOM ($E_{BR}^2 v_{sat}$)	HCAFOM ($\epsilon_r \mu^{1/2} E_{BR}^2 v_{sat}$)
Si	Face-Centered Cubic	1.1	11.8	1400	0.3	1	150	1	1	1
GaAs	Zinc Blende	1.4	12.9	8000	0.4	1.2	55	15	2	5
4H-SiC	Cubic and Hexagonal	3.3	9.7	1000	2.5	2	270	340	17	48
GaN	Wurtzite	3.4	9.0	1200	3.3	2.5	210	870	28	85
β -Ga ₂ O ₃	Monoclinic	4.9	10	300 (estimated)	8	2	13 [100] 21 [010]	3444	53	279
Diamond	Face-Centered Cubic	5.5	5.5	2000	10	1	1000	24644	33	619

^aThe BFOM, JFOM, and HCAFOM of Si are normalized to 1.

inverters for powering the traction motors. Any performance enhancement in the power devices, particularly high-power inverters, can considerably extend the vehicle driving range with the same battery capacity. Nowadays, the vast majority of electronic systems are built upon Si, and thanks to the modern semiconductor manufacturing technologies, the performance of Si-based devices has improved dramatically over the past few decades. On the other hand, for the power electronics, it was demonstrated that with the same breakdown voltage and device structure, the on-resistance of power transistors is inversely proportional to the third power of the energy bandgap and inversely proportional to the charge carrier mobility.²³ In this regard, the UWBG of β -Ga₂O₃ (4.9 eV) clearly outperforms Si (1.1 eV) and other wide bandgap semiconductors, such as SiC (3.3 eV) and GaN (3.4 eV). Moreover, the high breakdown electric field of β -Ga₂O₃ (8 MV cm⁻¹) allows for much miniaturized device structures, resulting in significant reduction of parasitic capacitance and thus improvement in frequency response. This article aims to provide a comprehensive overview on the material properties, crystal growth and deposition methods of β -Ga₂O₃, and most importantly, the state-of-the-art depletion mode, enhancement mode, and nanomembrane FETs based on β -Ga₂O₃ for high-power switching and high-frequency amplification applications. In the meantime, device-level approaches to cope with the two main issues of β -Ga₂O₃, namely, the lack of p-type doping and the relatively low thermal conductivity compared to SiC and GaN, will be discussed and compared.

MATERIAL PROPERTIES OF GALLIUM OXIDE

As early as 1952, various polymorphs of Ga₂O₃ and phase equilibria of the Al₂O₃–Ga₂O₃–H₂O systems were determined.¹ The five polymorphs are α , β , γ , δ , and ϵ , where the α -phase is corundum, β -phase monoclinic, γ -phase defective spinel, ϵ -phase orthorhombic, and δ -phase most likely orthorhombic.^{1,2,24} In general, the theoretical formation energies of the five polymorphs follow the tendency of $\beta < \epsilon < \alpha < \delta < \gamma$.²⁵ As a result, the monoclinic β -Ga₂O₃ is the most stable structure, while the remaining polymorphs are metastable. Furthermore, due to its high melting point of ~ 1793 °C, β -Ga₂O₃ is the only polymorph whose bulk crystal can be grown by using the melt growth methods.²⁶ In comparison, the metastable ϵ -Ga₂O₃ and α -Ga₂O₃ can only withstand temperatures up to 870 and 600 °C, respectively. In

fact, all phases of Ga₂O₃ can transition to other phases by annealing and would eventually end up transforming to the most stable β -phase.¹ Therefore, until now the great majority of research on gallium oxide has been devoted to β -Ga₂O₃. On the other hand, the heteroepitaxy of α -Ga₂O₃ and ϵ -Ga₂O₃ on sapphire substrates has also attracted much attention, because compared to the monoclinic β -Ga₂O₃, the corundum α -Ga₂O₃ and the orthorhombic ϵ -Ga₂O₃ have a better symmetry match with the hexagonal *c*-plane sapphire substrates.^{27–30}

The β -Ga₂O₃ has a monoclinic crystal structure with the space group of *C2/m* and the lattice constants of $a = 12.2$ Å, $b = 3.0$ Å, $c = 5.8$ Å, and $\beta = 104^\circ$ (Figure 1).²⁴ The β -Ga₂O₃

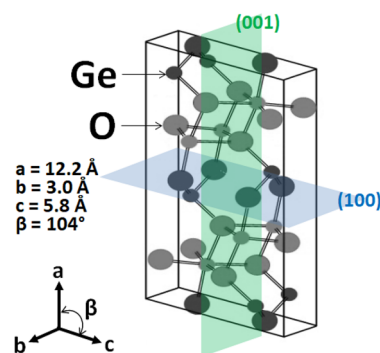


Figure 1. Crystal structure and lattice parameters of β -Ga₂O₃.²⁴

crystal is composed of sixfold coordinated Ga–O octahedra and fourfold coordinated Ga–O tetrahedra. The different arrangements of Ga and O atoms along different directions lead to anisotropic physical properties. For example, the thermal conductivity along the [010] direction is 21 W m⁻¹ K⁻¹, while it is 13 W m⁻¹ K⁻¹ along the [100] direction.^{31–33} The static dielectric constants of β -Ga₂O₃ perpendicular to the (100), (010), and (001) planes are also slightly different from each other.³⁴ The β -Ga₂O₃ crystal structure has two cleavage planes, namely, (100) and (001), and since the lattice parameter along the [100] direction is higher than the [010] and [001] directions, it is easy to exfoliate ultrathin films along the (100) plane direction.¹⁴ After washing with organic solvents and annealing in oxygen ambient, the typical β -Ga₂O₃ wafer surface should exhibit a regular step-and-terrace morphology.⁷ The terrace width is a function of the substrate disorientation; the smaller the miscut angle, the larger the

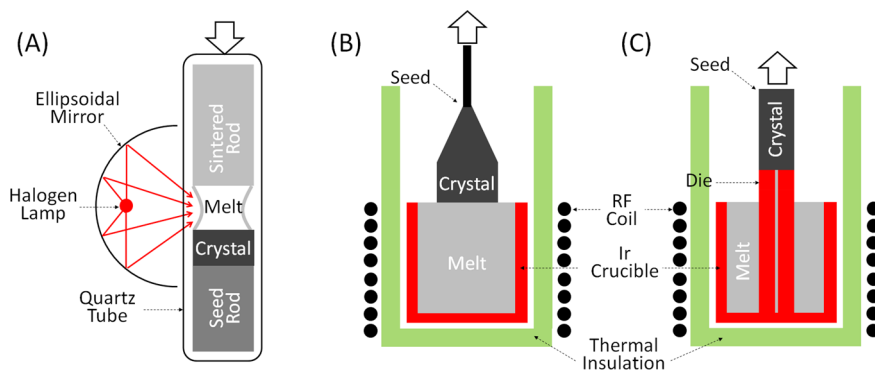


Figure 2. Schematic drawings of (A) the FZ method,⁵⁹ (B) the CZ method,⁶⁰ and (C) the EFG method,⁵⁷ respectively.

terrace width of the substrate. The typical atomic force microscopy (AFM) image reveals that the (100) plane of a β -Ga₂O₃ substrate with a miscut angle of $\sim 0.2^\circ$ has the terrace width of 70 to 100 nm.⁷ During homoepitaxy, the adhesion energy on the terraces of the (100) plane is weaker than at the steps and kinks, therefore promoting the step-flow growth.³⁵

The energy bandgap of pure β -Ga₂O₃ has been determined to be 4.7–4.9 eV.^{4,36} Therefore, β -Ga₂O₃ should be transparent from the UV to visible range, as evidenced by the crystal clear, 2-in.-diameter Ga₂O₃ wafer synthesized by the EFG method.^{37,38} The intrinsic electron mobility in the drift layers of β -Ga₂O₃ power devices is estimated to be 100–300 cm² V⁻¹ s⁻¹ for the electron density 10¹⁵–10¹⁶ cm⁻³.^{15,39} Based on the first-principle band structure calculation, the monoclinic β -Ga₂O₃ has an indirect bandgap of 4.84 eV and a direct bandgap of 4.88 eV, and a relatively light electron effective mass of $\sim 0.28m_0$, where m_0 is the free electron mass.⁴⁰ In contrast, the hole effective mass is very large, because the valence band is relatively flat in the momentum space.^{40,41} Therefore, the unintentionally doped (UID) β -Ga₂O₃ is typically n-type with the carrier concentrations in low 10¹⁷ cm⁻³. The n-type conductivity can be further enhanced by intentionally doping with the shallow dopants, such as Si, Ge, and Sn. On the contrary, Mg and Fe are often used as the compensating acceptors for obtaining semi-insulating β -Ga₂O₃. For evaluating different semiconductors for the power device application, in addition to the BFOM, which only accounts for the DC conduction loss, the Johnson figure of merit (JFOM, power-frequency product) and the Huang's chip area manufacturing figure of merit (HCAFOM, manufacturability and expense) are also commonly considered. Thanks to the high breakdown electric field (8 MV cm⁻¹), the JFOM and HCAFOM of β -Ga₂O₃ obviously stand out in comparison to Si, GaAs, SiC, and GaN (Table 1).

CRYSTAL GROWTH OF GALLIUM OXIDE

Being able to grow bulk single crystals by using the relatively low-cost melt growth methods is one significant advantage of β -Ga₂O₃. In 1964, the first melt-grown β -Ga₂O₃ crystals were obtained with the use of the Verneuil method.⁴² However, not so many relevant research activities had been reported in the following years until 1996, when the FZ method was used to grow β -Ga_{2-x}In_xO₃.⁴³ Later, β -Ga₂O₃ single-crystal boules with diameters up to 8 mm were successfully synthesized by the FZ method.^{44–48} The starting material of the FZ method is 5N-grade β -Ga₂O₃ powder, which is pressed into rods by a cold isostatic press process (50 to 300 MPa). Then, the rods are sintered at $\sim 1500^\circ\text{C}$ in air for 10 h. During the crystal growth,

the sintered rod is positioned on the upper shaft, slowly rotating in an opposite direction to a β -Ga₂O₃ seed crystal positioned on the lower shaft. Four high-power (1.5 kW) halogen lamps and the corresponding ellipsoidal mirrors are used as the heating system. The growth rate is 1 to 20 mm h⁻¹ under dry air or synthetic air (21 vol % O₂ + 79 vol % N₂) flow. The crystal growth process is illustrated in Figure 2A. The major concerns of the FZ method are the collapse of the liquid melt which is barely held by the surface tension and the crack formation in the grown crystal due to high thermal gradients.

The feasibility of using the CZ method with Ir crucibles for growing β -Ga₂O₃ single crystals was demonstrated in 2000,⁵ and major improvements have been made since 2010.^{49–55} The starting material, 5N-grade β -Ga₂O₃ powder, is first placed in the Ir crucible, which is heated by the surrounding radiofrequency (RF) inductor to form the β -Ga₂O₃ melt. A seed crystal is introduced into the melt and then slowly pulled up (1 to 2 mm h⁻¹) while rotating (5 to 10 rpm). The crystal growth process is illustrated in Figure 2B. The β -Ga₂O₃ cylindrical boules with diameters up to 50 mm can be obtained using this method.⁵³ The major concern of the CZ method is the decomposition of Ga₂O₃ into volatile species, such as Ga, GaO, and Ga₂O, in an oxygen-deficient atmosphere. On the contrary, the Ir crucible and other Ir parts are prone to oxidation in an oxygen-rich atmosphere. It was found that an appropriate growth atmosphere comprising CO₂, Ar, and O₂, along with overpressure, can effectively suppress the decomposition of Ga₂O₃ without harming the Ir crucible.⁴⁹ The influence of other parameters on the grown crystal quality, such as furnace design, crucible aspect ratio, crystal-to-crucible diameter ratio, heating and cooling rates, growth and rotation rates, seed preparation, and crystallization ratio, have also been investigated.⁵⁶

The EFG method, featuring high growth speed and precise control of crystal size and shape via the use of a die, has been applied to the growth of β -Ga₂O₃ since 2008.⁶ Similar to the FZ and CZ methods, the starting material of the EFG method is 5N-grade β -Ga₂O₃ powder, which is placed in an Ir crucible along with an Ir die in the middle. The heating of the crucible is carried out by using an RF induction coil. Once the melting point is reached, the β -Ga₂O₃ melt moves up through the slit of the Ir die by capillary force, and a β -Ga₂O₃ seed crystal is positioned in contact with the melt on top of the die to initiate the crystal growth process, as illustrated in Figure 2C.⁵⁷ The shape of the grown crystal is determined by the shape of the top surface of the die. The growth rate can reach 15 mm h⁻¹ under the growth atmosphere comprising 2 vol % O₂ + 98 vol

Table 2. Homoepitaxy of β -Ga₂O₃ Layers on (100) and (010) β -Ga₂O₃ Substrates, by Various Epitaxy Techniques, Including MOCVD, LPCVD, HVPE, and PA-MBE^a

Epitaxial Layers	Substrates	Conditions	Crystal Characteristics	ref
(A) β -Ga ₂ O ₃	(100) β -Ga ₂ O ₃	MOCVD: TMGa and O ₂ or H ₂ O; 750–850 °C; 5–100 mBar	Nanocrystals of Ga ₂ O ₃ were formed with O ₂ as oxidant, while smooth epitaxial layers of Ga ₂ O ₃ were formed with H ₂ O as oxidant.	7
(B) Sn-doped β -Ga ₂ O ₃	(100) β -Ga ₂ O ₃	MOCVD: TEGa, O ₂ , and TESn; 850 °C; 5 mBar	RMS surface roughness of \sim 0.6 nm was achieved. The maximum electron mobility of 41 cm ² V ⁻¹ s ⁻¹ was obtained with the carrier concentration equal to 1×10^{16} cm ⁻³ .	61
(C) β -Ga ₂ O ₃	(100) β -Ga ₂ O ₃	MOCVD: TEGa and O ₂ ; 850 °C; 5 mBar	The Ga ₂ O ₃ layer grown on a substrate with 0.1° miscut angle exhibited high twin lamella (stacking fault) density, while the layer grown with 6° miscut angle exhibited nearly zero twin lamella.	62
(D) Sn- and Si-doped β -Ga ₂ O ₃	Fe-doped (010) β -Ga ₂ O ₃	MOCVD: TEGa, O ₂ , TEOS, and TESn; 850 °C; 5 mBar	A RMS surface roughness about 0.6 nm was achieved. No dislocations or planar defects were observed. The maximum electron mobility of about 130 cm ² V ⁻¹ s ⁻¹ was obtained with the carrier concentration equal to 1×10^{17} cm ⁻³ regardless of the dopant type.	64
(E) β -Ga ₂ O ₃	(010) β -Ga ₂ O ₃	LPCVD: Ga pellets and O ₂ ; 780–950 °C	A maximum growth rate of 1.3 μ m h ⁻¹ was obtained at 850 °C, while a RMS surface roughness about 7 nm was obtained at 950 °C.	65
(F) β -Ga ₂ O ₃	Sn-doped (001) β -Ga ₂ O ₃	HVPE: GaCl and O ₂ ; 800–1050 °C; 0.5 mBar for GaCl and 2.5 mBar for O ₂	A growth rate approximately 5 μ m h ⁻¹ was obtained at 900 °C and above. The thick layers of β -Ga ₂ O ₃ grown at 1000 °C were smoother at the surface and had higher crystalline perfection than those grown at 800 °C.	66
(G) β -Ga ₂ O ₃	(100) β -Ga ₂ O ₃	PA-MBE: evaporated Ga and O ₂ plasma; 800 or 900 °C; Ga beam equivalent pressure (BEP) 1.1×10^{-7} or 2.4×10^{-7} Torr	Ga BEP = 1.5×10^{-7} mBar and 800 °C was the optimal growth condition. A RMS surface roughness of \sim 0.5 nm was achieved. The grown films were easily cleaved at the (100) and (001) planes. The easy cleavability of (100) planes facilitates the step-flow growth and terrace formation.	35
(H) β -Ga ₂ O ₃	(001) β -Ga ₂ O ₃	PA-MBE: evaporated Ga and O ₂ plasma; 700–800 °C; Ga beam equivalent pressure (BEP) 1.7×10^{-8} or 9.5×10^{-8} Torr	The growth rate increased with increasing Ga BEP, reaching a plateau of 56 nm h ⁻¹ , and then decreased at higher Ga BEP. The growth rate decreased with the substrate temperature increasing from 750 to 800 °C. The growth rate became negative (i.e., etching) when only Ga flux was supplied.	79

^aCharacteristics of the grown crystals are summarized. TMGa represents trimethylgallium, TEGa triethylgallium, TESn tetraethyltin, and TEOS tetraethylorthosilicate.

Table 3. Heteroepitaxy of β -Ga₂O₃, ϵ -Ga₂O₃, and α -Ga₂O₃ Layers on *c*-Plane and *a*-Plane GaN, *c*-Plane AlN/SiC Substrates, by Various Epitaxy Techniques, Including MOCVD, PA-MBE, HVPE, and Mist-CVD^a

Epitaxial Layers	Substrates	Conditions	Heteroepitaxy	Crystal Characteristics	ref
(A) β -Ga ₂ O ₃	<i>a</i> - and <i>c</i> -plane sapphire	MOCVD: TMGa and O ₂ ; 600–800 °C; 66 mBar	The Ga ₂ O ₃ films grown on <i>c</i> -plane sapphire substrates were (−201)-oriented, while the Ga ₂ O ₃ films grown on <i>a</i> -plane substrates were less oriented and contained α -phase. The film density (5.6 g cm ^{−3}) was lower than the theoretical value (6.4 g cm ^{−3}), indicating the presence of gallium or oxygen vacancies.		67
(B) Sn-doped β -Ga ₂ O ₃	<i>c</i> -plane sapphire	MOCVD: TMGa, H ₂ O and TESn, 775–850 °C; 5–50 mBar	The Ga ₂ O ₃ films grown on <i>c</i> -plane sapphire substrates were (−201)-oriented with the Sn-doping concentration 10 ¹⁷ –10 ¹⁹ cm ^{−3} . The growth condition 850 °C and 50 mBar led to better crystal quality than 800 °C and 5 mBar. Ga vacancy-related defects and carbon-related complexes act as acceptors.		68
(C) Si-doped β -Ga ₂ O ₃	<i>c</i> -plane sapphire	MOCVD: TMGa, H ₂ O and TEOS, 800 °C; 5 and 10 mBar	The Ga ₂ O ₃ films grown on <i>c</i> -plane sapphire substrates were (−201)-oriented. The Si-doping concentration in the range 10 ¹⁷ –10 ¹⁸ cm ^{−3} did not degrade the crystal quality.		8
(D) β -Ga ₂ O ₃	<i>c</i> -plane sapphire	MOCVD: TMGa and H ₂ O, 800 °C; 5–50 mBar	A 3-nm-thick layer of α -Ga ₂ O ₃ was observed at the interface between the β -Ga ₂ O ₃ layer and <i>c</i> -plane sapphire substrate. The β -Ga ₂ O ₃ layer was composed of rotational domains due to symmetry mismatch between the monoclinic β -Ga ₂ O ₃ and trigonal α -Ga ₂ O ₃ .		69
(E) ϵ -Ga ₂ O ₃	<i>c</i> -plane Sapphire	MOCVD: TMGa and H ₂ O; 550, 650, and 715 °C; 100 mBar	If the growth temperature was 550 °C, the deposited films were amorphous. If the growth temperature was increased to 715 °C, (−201)-oriented β -Ga ₂ O ₃ with poor crystalline quality was obtained. Only when the growth temperature was controlled at 650 °C was high quality ϵ -Ga ₂ O ₃ obtained.		72
(F) β -Ga ₂ O ₃ and ϵ -Ga ₂ O ₃	<i>c</i> -plane sapphire	MOCVD: TEGa and O ₂ ; 450–570 °C; 12.1 mBar	The Ga ₂ O ₃ films grown on the <i>c</i> -plane sapphire substrates were polycrystalline. If the growth temperature was above 535 °C, pure (−201)-oriented β -Ga ₂ O ₃ was obtained. If the growth temperature was 505 °C, a mixture of β -Ga ₂ O ₃ and ϵ -Ga ₂ O ₃ was obtained.		76
(G) β -Ga ₂ O ₃	6H-SiC	MOCVD: TEGa and O ₂ ; 500 °C; 35 mBar	The Ga ₂ O ₃ films grown on 6H-SiC substrates were ϵ -phase pure and in high crystal quality. If annealed at 850 °C, transition to (−201)-oriented β -Ga ₂ O ₃ started to occur. If annealed at 900 °C, all ϵ -Ga ₂ O ₃ was converted to β -Ga ₂ O ₃ .		77
(H) β -Ga ₂ O ₃	<i>c</i> -plane sapphire	PA-MBE: evaporated Ga and O ₂ plasma; 600–750 °C; Ga beam equivalent pressure (BEP) 5 × 10 ^{−9} to 2 × 10 ^{−7} Torr	The Ga ₂ O ₃ films grown on <i>c</i> -plane sapphire substrates were (−201)-oriented and β -phase pure. With the low Ga flux (high growth rate), three-dimensional columnar structures were obtained. With the high Ga flux (low growth rate), a typical terrace surface morphology was obtained.		78
(I) β -Ga ₂ O ₃	<i>a</i> - and <i>c</i> -plane sapphire	PA-MBE: evaporated Ga and O ₂ plasma; 600–800 °C; 5 × 10 ^{−4} Torr	The Ga ₂ O ₃ films grown on <i>c</i> -plane and <i>a</i> -plane substrates were both (−201)-oriented, with no α -phase diffraction peak observed. Six types of β -Ga ₂ O ₃ grains on the <i>c</i> -plane substrate, with the orientation rotated every 60° from the Al ₂ O ₃ [110] direction, were observed.		80
(J) ϵ -Ga ₂ O ₃	<i>c</i> -plane GaN; <i>c</i> -plane AlN/SiC	HVPE: Ga, HCl and O ₂ ; 550 °C; 2.5 mBar for HCl and 10 mBar for O ₂	A growth rate of approximately 20 μ m h ^{−1} was achieved for ϵ -Ga ₂ O ₃ on <i>c</i> -plane AlN/SiC substrates. The as-grown films on GaN and AlN/SiC substrates were (0001)-oriented ϵ -phase pure. The ϵ -Ga ₂ O ₃ film was thermally stable up to 700 °C and exhibited an optical bandgap equal to 4.9 eV.		29
(K) α -Ga ₂ O ₃	<i>c</i> -plane sapphire	Mist-CVD: Gallium acetylacetonate Ga(C ₂ H ₃ O ₂) ₃ in deionized water with slight addition of HCl; 470 °C	The as-grown α -Ga ₂ O ₃ was phase pure and remained so after annealing at 550 °C. However, if the annealing temperature increased to 600 °C, α - to β -phase transition started to occur. The α -phase completely disappeared at 700 °C.		82

^aCharacteristics of the grown crystals are summarized. TMGa represents trimethylgallium; TEGa, triethylgallium; TESn, tetraethyltin; and TEOS, tetraethylorthosilicate.

% N₂. Later, the pulling rate and die geometry of the EFG method were further optimized to improve the grown crystal quality and shape.⁵⁸ It is worth mentioning that for the FZ, CZ, and EFG methods discussed above, the doping of the β -Ga₂O₃ crystals is usually accomplished by mixing the dopants, such as SnO₂ and SiO₂, with the starting materials, β -Ga₂O₃ powder, before the crystal growth process.

DEPOSITION OF GALLIUM OXIDE

Homoepitaxy by MOCVD. Among various deposition methods, metal–organic chemical vapor deposition (MOCVD) has drawn much attention, because it is most suitable for large-scale production and has precise control of growth rate and doping. For the homoepitaxy of β -Ga₂O₃ by MOCVD, (100)- and (010)-oriented wafers are generally used. In 2014, Wagner et al. demonstrated homoepitaxy of β -Ga₂O₃ on a (100) substrate by using trimethylgallium (TMGa) as the gallium precursor and oxygen gas or water as the oxygen precursor (Table 2A).⁷ When using pure oxygen gas, the formation energy of oxygen vacancies is greatly increased, and the byproduct Ga₂(CO₃)₃ may act as deposition masks, resulting in Ga₂O₃ nanocrystals instead of coherent films. In contrast, when using water as the oxygen source, since the oxygen part is fully consumed by the reaction with gallium, the formation of carbonate-related byproducts is prevented and the remaining hydrogen part may form Ga–H passivation, which can reduce the surface state density and promote the layer-by-layer growth.⁷ In 2016, Baldini et al. demonstrated homoepitaxy of n-type β -Ga₂O₃ on a (100) substrate by using triethylgallium (TEGa), oxygen gas, and tetraethyltin (TESn) as the precursors (Table 2B).⁶¹ Despite the ultraflat surface with the root-mean-square (RMS) surface roughness of only \sim 0.6 nm, the transmission electron microscopy (TEM) analysis reveals stacking faults in the form of twin lamellae, which may act as the compensation and scattering centers of electrons, limiting the electron mobility.⁶¹ To resolve this issue, it was found that using substrates with relatively large miscut angles can effectively avoid the formation of twin lamellae (Table 2C).⁶² For example, the β -Ga₂O₃ layer homoepitaxially grown on a 0.1° miscut (100) substrate has an estimated twin lamella density as high as 1×10^{17} cm⁻³. In contrast, if the miscut angle is increased to 6°, β -Ga₂O₃ layers free of twin lamella can be achieved. Considering the relatively low diffusion coefficient of gallium at the gas–solid interface (7×10^{-9} cm² s⁻¹ at 850 °C), the substrate with a small miscut angle has larger terrace width and therefore a higher chance of forming two-dimensional islands which further lead to the stacking faults.⁶² For example, the 0.1° miscut (100) β -Ga₂O₃ substrate exhibits a wide terrace, and the as-grown epitaxial layer has elongated islands on the surface and contains a high density of twin lamellae. In contrast, the 4° miscut substrate yields a narrow terrace, few two-dimensional islands, and sporadic twin lamellae.⁶² Finally, quantitative calculations using Read's model of charged dislocations confirm the reduction of electron mobility caused by the twin lamellae.⁶³

In general, the β -Ga₂O₃ films grown on the (010) β -Ga₂O₃ substrates have higher crystalline perfection than on the (100) β -Ga₂O₃ substrates. Besides, the maximum electron mobility achieved by the (100) β -Ga₂O₃ films so far is only \sim 40 cm² V⁻¹ s⁻¹,⁶¹ while the electron mobility of the (010) β -Ga₂O₃ films grown by molecular-beam epitaxy (MBE) can be >100 cm² V⁻¹ s⁻¹.³⁹ Furthermore, the heat transfer along the [010] direction (21 W m⁻¹ K⁻¹) is more efficient than along the

[100] direction (13 W m⁻¹ K⁻¹),^{31,32} making the (010) β -Ga₂O₃ films more advantageous for the power device application due to the faster heat dissipation. Therefore, in this paragraph we focus on the homoepitaxial growth of β -Ga₂O₃ on the (010) substrates by MOCVD. In 2017, Baldini et al. demonstrated homoepitaxy of Si- and Sn-doped β -Ga₂O₃ on Fe-doped (010) substrates (Table 2D).⁶⁴ The as-grown layers are ultraflat with the RMS surface roughness only \sim 0.6 nm and are exempt of dislocations or planar defects. Furthermore, due to the very high crystalline perfection, there is no distinguishable interface between the epitaxial layer and the (010) substrate.⁶⁴ Compared to Sn, Si is the better dopant because it has higher doping efficiency and no memory effect. The maximum electron mobility equal to \sim 130 cm² V⁻¹ s⁻¹ can be achieved with the carrier concentration equal to 1×10^{17} cm⁻³ regardless of the dopant type.⁶⁴

Homoepitaxy by Other Techniques. In 2016, Rafique et al. demonstrated homoepitaxy of (010) β -Ga₂O₃ films by low pressure CVD (LPCVD) and investigated the influence of growth temperature on the crystal quality (Table 2E).⁶⁵ With sufficiently high growth temperatures, the deposited crystals achieve high crystalline perfection, i.e., undifferentiable interface between the epitaxial layer and substrate, and the surface morphology exhibits a terrace-like structure, which basically reproduces the substrate's terrace morphology.⁶⁵ The RMS surface roughness is \sim 40 nm with the growth temperature equal to 780 °C but only \sim 7 nm if the growth temperature increases to 950 °C.⁶⁵ In 2015, Murakami et al. demonstrated that thick layers of β -Ga₂O₃ can be homoepitaxially grown on (001)-oriented Sn-doped β -Ga₂O₃ substrates by halide vapor phase epitaxy (HVPE) with gaseous GaCl and O₂ as the precursors, and the influence of growth temperature on the crystal quality was investigated (Table 2F).⁶⁶ Compared to those grown at 800 °C, the β -Ga₂O₃ layers grown at 1000 °C are much smoother at the surface and have higher crystalline perfection, as revealed by the narrower X-ray rocking curves. In 2008, Oshima et al. demonstrated homoepitaxy of β -Ga₂O₃ layers on (100) β -Ga₂O₃ substrates by plasma-assisted MBE (PA-MBE) using evaporated Ga and O₂ plasma (Table 2G).³⁵ The deposited films and the substrate exhibit the same β -Ga₂O₃ (020) X-ray diffraction (XRD) peaks, and the film surface morphology features a duplicate of the substrate terrace with the RMS surface roughness only \sim 0.5 nm. The grown films can be easily cleaved at the (100) and (001) planes. The excellent cleavability of the (100) planes facilitates the step-flow growth and terrace formation.³⁵ In 2018, Oshima et al. studied how the Ga-flux and the substrate temperature affect the PA-MBE growth rate (Table 2H).⁷⁹ The growth rate of β -Ga₂O₃ increases with higher Ga-flux, reaching a plateau of 56 nm h⁻¹. Further increase of Ga-flux decreases the growth rate. The growth rate also declines with the substrate temperature elevating from 750 to 800 °C. Noticeably, the growth rate becomes negative, i.e., net etching, when only Ga-flux is supplied.⁷⁹

Heteroepitaxy by MOCVD. For the heteroepitaxy of β -Ga₂O₃ by MOCVD, *c*-plane sapphire substrates are most commonly used. The sapphire substrates are relatively cheap and able to provide electrical isolation for the power FETs. In 2016, Tadjer et al. compared the *a*-plane and *c*-plane sapphire substrates for the heteroepitaxy of β -Ga₂O₃ (Table 3A).⁶⁷ Based on the XRD analysis, the β -Ga₂O₃ layer grown on the *c*-plane substrate reveals clear β -phase diffraction peaks attributed to the (−201) plane, while the β -Ga₂O₃ layer

grown on the *a*-plane substrate exhibits an obvious α -phase diffraction peak along with some other β -phase diffraction peaks, suggesting a less crystalline and less oriented crystal structure.⁶⁷ Besides, the deposited film density (5.6 g cm^{-3}) is significantly lower than the theoretical value (6.4 g cm^{-3}), indicating the presence of gallium or oxygen vacancies.⁶⁷ Another study of heteroepitaxy of Sn-doped β -Ga₂O₃ on *c*-plane sapphire substrates also suggested that the grown films are clearly monoclinic and (-201)-oriented with the Sn doping concentration 10^{17} – 10^{19} cm^{-3} (Table 3B).⁶⁸ However, the Ga vacancy-related defects and the residual carbon complexes from the TMGa precursors may act as acceptors which compensate the Sn donors.⁶⁸ Similarly, the Si-doped β -Ga₂O₃ epitaxial layers on *c*-plane sapphire substrates were also (-201)-oriented, and no deterioration of crystal quality was observed in the doping range 10^{17} – 10^{18} cm^{-3} (Table 3C).⁸ However, when the Si doping concentration is up to $5 \times 10^{19} \text{ cm}^{-3}$, amorphization of the films occurs and only very low conductivity is obtained.⁸ On the other hand, different grains or domains have been observed in the heteroepitaxially grown β -Ga₂O₃. In 2015, Schewski et al. found a 3-ML-thick layer of crystalline α -Ga₂O₃ sandwiched between the β -Ga₂O₃ epitaxial layer and *c*-plane sapphire substrate (Table 3D).⁶⁹ Besides, the β -Ga₂O₃ layer on top of the α -Ga₂O₃ layer is composed of rotational domains, which can be attributed to the symmetry mismatch between the monoclinic β -Ga₂O₃ and trigonal α -Ga₂O₃.⁶⁹ Furthermore, despite the pure β -phase XRD pattern shown, the TEM investigation reveals that the β -Ga₂O₃ epitaxial layer actually contains in-plane grains rotated 120° to each other.⁶⁸ Moreover, the actual lattice constants *a* and *c* are estimated to be smaller and the lattice constant *b* and angle β are estimated to be larger, compared to the standard values of single-crystal β -Ga₂O₃.⁷⁰ In summary, while the (-201)-oriented β -Ga₂O₃ can indeed grow on the *c*-plane sapphire substrate epitaxially, the grown films can hardly be single-crystal due to the symmetry mismatch between the monoclinic β -Ga₂O₃ and hexagonal Al₂O₃.

Compared to the monoclinic β -Ga₂O₃, the crystallographic symmetry of orthorhombic ε -Ga₂O₃ is better matched to the sapphire substrates.⁷¹ Besides, the ε -Ga₂O₃ also possesses the wide bandgap nature of the β -Ga₂O₃ and can be grown in a relatively mild condition. In 2016, Boschi et al. found that the growth temperature plays a critical role in deciding the crystal form (Table 3E).⁷² For example, the films deposited at 550 °C are basically amorphous. If the growth temperature elevates to 715 °C, only weak and broad XRD peaks related to the (-201)-oriented β -Ga₂O₃ are observed, as the crystalline β -Ga₂O₃ are usually obtained at higher temperatures. However, when the growth temperature is controlled at 650 °C, intense and narrow XRD peaks corresponding to the ε -Ga₂O₃ are shown.⁷² Furthermore, although the SEM images showed hexagonal nucleation islands at the film surface and the large-area electron diffraction patterns suggested pseudo-hexagonal symmetry with the *P6₃mc* space group,⁷² the actual structure of ε -Ga₂O₃ is composed of ordered 120°-rotational twin domains, each of which has diameters of 5 to 10 nm and orthorhombic symmetry with the *Pna2₁* space group.⁷³ The high-resolution cross-section TEM image indicates that the ε -Ga₂O₃ film grown at 650 °C possesses a columnar structure and γ -Ga₂O₃ epitaxial islands are present at the interface between the ε -Ga₂O₃ film and *c*-plane sapphire substrate.⁷³ Based on the photon energy for the onset of photoconductivity and band-to-band absorption, the optical bandgap of the ε -Ga₂O₃ films is

between 4.6 and 4.7 eV, which is close to that of β -Ga₂O₃, and the cathodoluminescence spectroscopy indicates a group of deep donors located at $\sim 0.7 \text{ eV}$ below the conduction band and three defect states below the midgap.⁷⁴ Lastly, the thermal stability of the ε -Ga₂O₃ films grown on *c*-plane sapphire substrates was investigated via differential scanning calorimetry (DSC), TEM, and XRD (Table 3F).^{75,76} After heteroepitaxy at 650 °C, the film was placed inside a tubular furnace for the heat treatment. The film can withstand prolonged heat treatment up to 700 °C. However, if the annealing temperature is higher than 900 °C, a complete transition to the β -phase occurs.⁷⁵ Similar thermally induced transition was observed for the ε -Ga₂O₃ films grown on 6H-SiC substrates by MOCVD (Table 3G).⁷⁷ The as-grown films are ε -phase pure and in high crystal quality. However, the diffraction peaks corresponding to the (-201)-oriented β -Ga₂O₃ start to appear if the annealing temperature increases to 850 °C, and the ε -Ga₂O₃ is completely converted to β -Ga₂O₃ if annealed at 900 °C.⁷⁷

Heteroepitaxy by Other Techniques. In 2010, Tsai et al. demonstrate that by using PA-MBE, phase pure, (-201)-oriented β -Ga₂O₃ films were successfully deposited on *c*-plane sapphire substrates (Table 3H).⁷⁸ With the low gallium flux which leads to high growth rate, the as-grown film is composed of three-dimensional columnar structures. On the contrary, with the high gallium flux and thus low growth rate, a typical terrace surface morphology is obtained.⁷⁸ The decreasing growth rate with increasing gallium flux is likely due to the formation and desorption of gallium suboxides and was also observed in another PA-MBE work (Table 2H).⁷⁹ In 2012, Nakagomi et al. compared the (-201)-oriented β -Ga₂O₃ films heteroepitaxially grown on *c*-plane and *a*-plane sapphire substrates by PA-MBE (Table 3I).⁸⁰ Both types of the sapphire substrates can lead to strong (-201)-oriented β -Ga₂O₃ XRD patterns.⁸⁰ In contrast, the β -Ga₂O₃ film grown on the *a*-plane sapphire substrate by MOCVD includes certain α -Ga₂O₃.⁶⁷ Moreover, the β -Ga₂O₃ film on the *c*-plane sapphire substrate contains six types of grains, with the orientation rotated every 60° from the Al₂O₃ [110] direction.⁸⁰ Similar results have also been observed for other β -Ga₂O₃ films grown by MOCVD.^{68,69} In 2015, Oshima et al. demonstrated heteroepitaxy of ε -Ga₂O₃ and β -Ga₂O₃ on various substrates, including sapphire, GaN, and AlN/SiC, by using HVPE (Table 3J).^{29,81} Compared to MOCVD, the major advantage of HVPE is the relatively high growth rate (approximately $20 \mu\text{m h}^{-1}$ for ε -Ga₂O₃ grown on *c*-plane AlN/SiC substrates and $250 \mu\text{m h}^{-1}$ for β -Ga₂O₃ quasi-epitaxially grown on off-angled *c*-plane sapphire substrates), and the crystal qualities of the as-grown films are comparable to those grown by MOCVD.^{29,81} In 2013, Lee et al. demonstrated that mist-CVD can be a low-energy-consumption alternative to grow α -Ga₂O₃ films on *c*-plane sapphire substrates (Table 3K).^{27,82} Compared to the monoclinic β -Ga₂O₃, the corundum α -Ga₂O₃ is better matched to the hexagonal sapphire substrates, resulting in epitaxial layers with fewer defects. After growth at 470 °C with optimal flow rates, the α -Ga₂O₃ films were annealed at different temperatures step-by-step. The α -phase can be maintained for the annealing temperature up to 550 °C but gradually converted to β -phase if the annealing temperature higher than 600 °C.⁸²

■ DEPLETION-MODE β -GA₂O₃ FETS

Given the difficulty of p-type doping in β -Ga₂O₃, recent device performance milestones have been mainly achieved by the

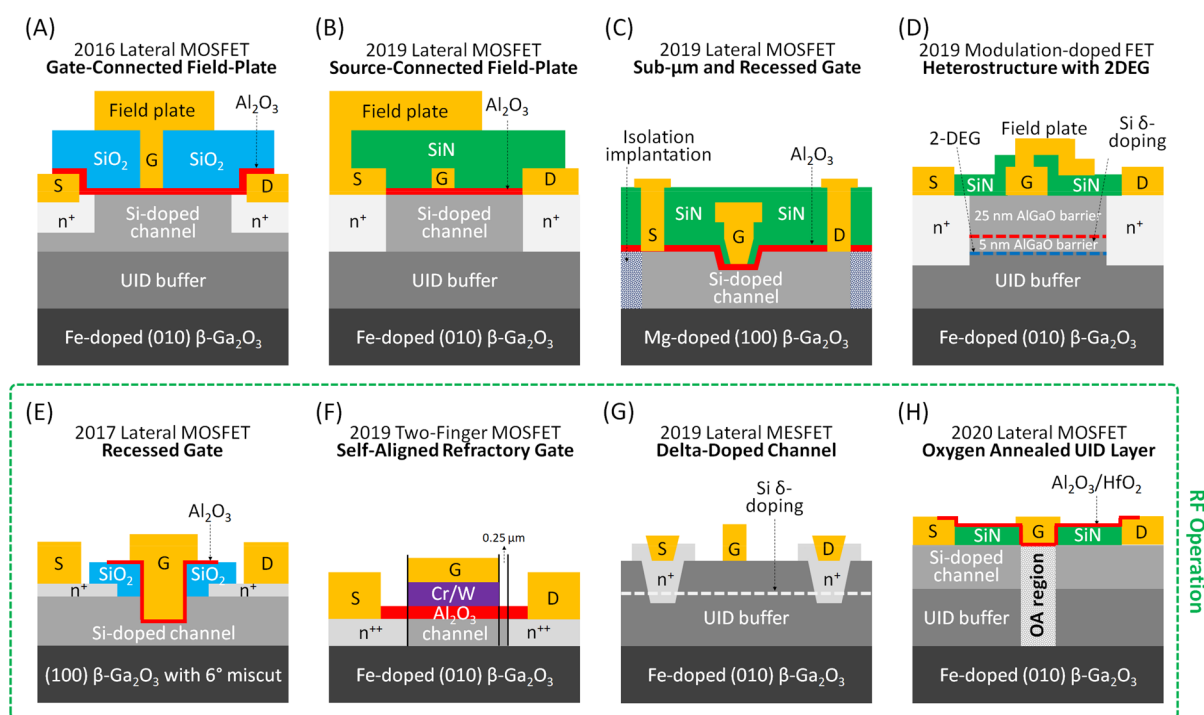


Figure 3. Cross-section illustrations of representative depletion-mode β -Ga₂O₃ FETs, including (A) MOSFET with a gate-connected field-plate,⁸⁴ (B) MOSFET with a source-connected field-plate,⁹² (C) MOSFET with a sub- μ m and recessed gate,⁹⁴ (D) heterostructure FET with 2DEG channel,⁹⁷ (E) MOSFET with a recessed gate for RF operation,¹⁰⁶ (F) two-finger MOSFET with a self-aligned refractory gate for RF operation,¹⁰⁷ (G) MESFET with a delta-doped channel for RF operation,¹⁰⁸ and (H) MOSFET with an oxygen annealed UID layer for RF operation.¹⁰⁹

depletion-mode FETs based on epitaxial layers grown on single-crystal β -Ga₂O₃ substrates. For the power switching application, the essential parameter for evaluating the device performance is the power figure of merit (PFOM) = $V_{br}^2/R_{on,sp}$, where V_{br} (V) is the three-terminal off-state breakdown voltage and $R_{on,sp}$ (m Ω cm²) is the on-resistance normalized by the device area. To exploit the full potential of β -Ga₂O₃ as predicted by the BFOM,⁸³ many device-level approaches have been developed to increase V_{br} while decreasing $R_{on,sp}$ as discussed below.

Gate-Connected Field-Plates. For metal-oxide-semiconductor FETs (MOSFETs), the gate-connected field-plate is a useful design to manage the electric field distribution between the gate and drain, so that the peak electric field in the channel region will not exceed the breakdown electric field of β -Ga₂O₃ (8 MV cm⁻¹). In 2016, Wong et al. demonstrated depletion-mode β -Ga₂O₃ MOSFETs with gate-connected field-plates for the first time (Figure 3A).⁸⁴ An area-selective Si-ion implantation technique was employed to fabricate the channel region and the source/drain (S/D) regions on an UID epitaxial layer grown on a Fe-doped (010) β -Ga₂O₃ substrate by ozone assisted (OA)-MBE. By using Silvaco two-dimensional device simulations, the most favorable field-plate geometry, which balances the peak electric fields among the drain, gate, and field-plate, can be obtained. The β -Ga₂O₃ MOSFET with the optimized field-plate design can achieve $V_{br} = 755$ V, $R_{on,sp} \sim 55$ m Ω cm², and PFOM ~ 10.4 MW cm⁻² (Table 4B).⁸⁴ In comparison, without the gate-connected field-plate, a similar depletion-mode β -Ga₂O₃ MOSFET can only achieve $V_{br} = 370$ V, $R_{on,sp} \sim 69$ m Ω cm², and PFOM ~ 2 MW cm⁻² (Table 4A).⁸⁵ Another major difference between the two devices is the incorporation of an UID layer below the channel region.⁸⁴ The highly resistive UID buffer layer can protect the channel

against charge compensation due to the outdiffusion of Fe deep acceptors from the Fe-doped (010) β -Ga₂O₃ substrate,⁸⁶ while providing effective device isolation without the need of mesa etching.⁸⁴

Ge-Doped Channels and Fluorinert Immersion. In 2017, Moser et al. demonstrated two-finger depletion-mode β -Ga₂O₃ MOSFETs with the channel regions doped with Ge (6.1×10^{17} cm⁻³) and mesa etching for device isolation.⁸⁷ Compared to other β -Ga₂O₃ MOSFETs having similar device structures but with the channel regions doped with Sn (1.7×10^{18} cm⁻³),⁸⁸ the two devices can achieve comparable PFOMs of ~ 11 MW cm⁻², but the device with Ge doping exhibits significantly higher channel electron mobility (111 cm² V⁻¹ s⁻¹) than the device with Sn doping (19.7 cm² V⁻¹ s⁻¹) (Table 4C and D), suggesting Ge might be a better dopant kind than the commonly used Si or Sn. In 2018, Zheng et al. demonstrated depletion-mode β -Ga₂O₃ MOSFETs with not only gate-connected field-plates but also Fluorinert FC-770 immersion.⁸⁹ It was reported that the breakdown through air, which has the dielectric strength of ~ 3 kV mm⁻¹, might be the major premature breakdown mechanism limiting the V_{br} within 300–400 V.^{90,91} Therefore, by replacing air with Fluorinert FC-770, which has the dielectric strength higher than 15 kV mm⁻¹, the V_{br} of the gate field-plated MOSFET can be significantly improved from 440 V in air to 1850 V in Fluorinert. However, due to the relatively long channel length (28 μ m), the $R_{on,sp}$ of the device is ~ 2000 m Ω cm², resulting in relatively low PFOM of ~ 1.7 MW cm⁻² (Table 4F).⁸⁹

Source-Connected Field-Plates. In 2019, Lv et al. demonstrated depletion-mode β -Ga₂O₃ MOSFETs with source-connected field-plates as an improvement to gate-connected field-plates (Figure 3B).⁹² The Si-doped channel layer and the UID buffer layer were homoepitaxially grown on

Table 4. Representative Depletion-Mode β -Ga₂O₃ FETs with Various Device Structures and Fabricated by Different Deposition Techniques^a

Depletion-Mode β -Ga ₂ O ₃ FETs										
Features	Substrates/Gates Dielectric	Epitaxial Layers	Donor Concentrations	V_{tr} (V)	$R_{on,sp}$ (m Ω cm ²)	$V_{br}/R_{on,sp}$ (MW cm ⁻²)	$I_{b,stat}$ (mA mm ⁻¹)	I_{on}/I_{off}	ref	
(A)	<ul style="list-style-type: none"> • Circular MOSFET • Annealed Ti/Au for ohmic contacts • Si implantation for S/D 	Fe-doped (010) β -Ga ₂ O ₃ / 20 nm Al ₂ O ₃	<ul style="list-style-type: none"> • MBE • 0.30 μm Sn-doped channel 	<ul style="list-style-type: none"> • Channel: Sn, 7×10^{17} cm⁻³ • S/D: Si, 5×10^{19} cm⁻³ 	370 ($V_{GS} = -20$ V)	~ 69 ($V_{GS} = 4$ V)	~ 2.0	39 ($V_{GS} = 4$ V)	$> 10^{10}$	2013 ⁸⁵
(B)	<ul style="list-style-type: none"> • Lateral MOSFET • Gatefield-plate • Si implantation for channel and S/D • UID layer for device isolation 	Fe-doped (010) β -Ga ₂ O ₃ / 20 nm Al ₂ O ₃	<ul style="list-style-type: none"> • OA-MBE • 0.30 μm Si-doped channel • 0.90 μm UID buffer layer 	<ul style="list-style-type: none"> • Channel: Si, 3×10^{17} cm⁻³ • S/D: Si, 5×10^{19} cm⁻³ 	755 ($V_{GS} = -55$ V)	~ 55 ($V_{GS} = 4$ V)	~ 10.4	78 ($V_{GS} = 4$ V)	$> 10^9$	2016 ⁸⁴
(C)	<ul style="list-style-type: none"> • Two-finger MOSFET • Channel $\mu_n = 19.7$ cm² V⁻¹ s⁻¹ (by Hall effect) • Mesa etching for device isolation 	Mg-doped (100) β -Ga ₂ O ₃ / 20 nm Al ₂ O ₃	<ul style="list-style-type: none"> • MOCVD • 0.20 μm Sn-doped channel 	<ul style="list-style-type: none"> • Channel: Sn, 1.7×10^{18} cm⁻³ 	230 (V_{GP}) ($V_{GS} = -30$ V)	4.9 ($V_{GS} = 0$ V)	11	~ 60 ($V_{GS} = 0$ V)	$\sim 10^7$	2016 ⁸⁸
(D)	<ul style="list-style-type: none"> • Two-finger MOSFET • Channel $\mu_n = 111$ cm² V⁻¹ s⁻¹ (by Hall effect) • Mesa etching for device isolation 	Fe-doped (010) β -Ga ₂ O ₃ / 20 nm Al ₂ O ₃	<ul style="list-style-type: none"> • MBE • 0.20 μm Ge-doped channel 	<ul style="list-style-type: none"> • Channel: Ge, 6.1×10^{17} cm⁻³ 	479 ($V_{GS} = -20$ V)	~ 20 ($V_{GS} = 0$ V)	~ 11.5	80 ($V_{GS} = 0$ V)	$> 10^8$	2017 ⁸⁷
(E)	<ul style="list-style-type: none"> • Lateral MOSFET • SOG doping for S/D • Specific contact resistance = 2.1×10^{-5} Ω cm⁻² • UID layer for device isolation 	Fe-doped (010) β -Ga ₂ O ₃ / 20 nm SiO ₂	<ul style="list-style-type: none"> • OA-MBE • 0.20 μm Sn-doped channel • 0.20 μm UID buffer layer 	<ul style="list-style-type: none"> • Channel: Sn, 1×10^{18} cm⁻³ • S/D: Sn, $> 10^{21}$ cm⁻³ by SOG 	382 ($V_{GS} = -25$ V)	~ 171 ($V_{GS} = 14$ V)	~ 0.9	35 ($V_{GS} = 14$ V)	$\sim 10^8$	2017 ¹⁰³
(F)	<ul style="list-style-type: none"> • Lateral MOSFET • Gate field-plate • SOG doping for S/D • Fluorinet Immersion • UID layer for device isolation 	Fe-doped (010) β -Ga ₂ O ₃ / 20 nm SiO ₂	<ul style="list-style-type: none"> • MBE • 0.20 μm Sn-doped channel • 0.20 μm UID buffer layer 	<ul style="list-style-type: none"> • Channel: Sn, 2×10^{17} cm⁻³ • S/D: Sn, $> 10^{21}$ cm⁻³ by SOG 	<ul style="list-style-type: none"> • 1850 in Fluorinet • 440 in air ($V_{GS} = -32$ V) 	~ 2000 in Fluorinet ($V_{GS} = 12$ V)	~ 1.7	1.5 ($V_{GS} = 12$ V)	$\sim 10^8$	2018 ⁸⁹
(G)	<ul style="list-style-type: none"> • Lateral MOSFET • Source field-plate • Si implantation for S/D • SiN_x internal passivation • Mesa etching for device isolation 	Fe-doped (010) β -Ga ₂ O ₃ / 25 nm Al ₂ O ₃	<ul style="list-style-type: none"> • MOCVD • 0.24 μm Si-doped channel • 0.40 μm UID buffer layer 	<ul style="list-style-type: none"> • Channel: Si, 8×10^{17} cm⁻³ • S/D: Si, $\sim 10^{20}$ cm⁻³ 	<ul style="list-style-type: none"> • 480 with $I_{SD} = 11$ μm • 680 with $I_{SD} = 18$ μm ($V_{GS} = -55$ V) 	<ul style="list-style-type: none"> • 4.58 with $I_{SD} = 11$ μm • 11.7 with $I_{SD} = 18$ μm ($V_{GS} = 5$ V) 	<ul style="list-style-type: none"> • 50.4 with $I_{SD} = 11$ μm • 39.5 with $I_{SD} = 18$ μm 	<ul style="list-style-type: none"> • 267 with $I_{SD} = 11$ μm • 222 with $I_{SD} = 18$ μm ($V_{GS} = 5$ V) 	$\sim 10^6$	2019 ⁹²
(H)	<ul style="list-style-type: none"> • Lateral MOSFET • Source field-plate 	Fe-doped (010) β -Ga ₂ O ₃ / 20 nm Al ₂ O ₃	<ul style="list-style-type: none"> • OA-MBE • 0.15 μm Si-doped channel 	<ul style="list-style-type: none"> • Channel: Sn, 1.5×10^{18} cm⁻³ 	2321 in Fluorinet ($V_{GS} = -10$ V)	959 ($V_{GS} = 1$ V)	5.6	~ 6.5 ($V_{GS} = 1$ V)	$\sim 10^7$	2019 ⁹³

Table 4. continued

Depletion-Mode β -Ga ₂ O ₃ FETs									
Features	Substrates/Gates Dielectric	Epitaxial Layers	Donor Concentrations	V_{br} (V)	$R_{on,sp}$ (m Ω cm ²)	$V_{br}^2/R_{on,sp}$ (MW cm ⁻²)	$I_{ds,sat}$ (mA mm ⁻¹)	I_{on}/I_{off}	ref
<ul style="list-style-type: none"> Thin and heavily doped channel Mesa etching for device isolation Lateral MOSFET 0.7-μm-long and recessed gate SiN_x internal passivation Multiple energy nitrogen implantation for device isolation 	Mg-doped (100) β -Ga ₂ O ₃ with 6° miscut/25 nm Al ₂ O ₃	<ul style="list-style-type: none"> MOCVD 0.20 μm Si-doped channel 	<ul style="list-style-type: none"> Channel: 2.3 \times 10¹⁷ cm⁻³ (charge carrier) 	1830 ($V_{GS} = -20$ V) ($L_{GD} = 10$ μ m)	21.6 ($V_{GS} = 10$ V) ($L_{GD} = 10$ μ m)	155	120 ($V_{GS} = 10$ V)	>10 ¹⁰	2019 ⁹⁴
<ul style="list-style-type: none"> Lateral MOSFET CF₄ plasma treatment for n-type doping β-Ga₂O₃ epitaxial layer on sapphire substrate 	c-plane Sapphire/40 nm Al ₂ O ₃	<ul style="list-style-type: none"> HVPE 0.15 μm Si-doped channel 	<ul style="list-style-type: none"> Channel: F, 2.3 \times 10¹⁸ cm⁻³ at 5–10 nm deep from the surface 	\sim 155 ($V_{GS} < -21$ V)	\sim 47k ($V_{GS} = -12$ V)	\sim 5 \times 10 ⁻⁴	\sim 1 \times 10 ⁻¹	\sim 10 ⁶	2021 ⁹⁹
<ul style="list-style-type: none"> Modulation-doped hetero-structured FET Gate field-plate 	Fe-doped (010) β -Ga ₂ O ₃ /Pt/Au Schottky gate contact	<ul style="list-style-type: none"> PA-MBE β-(Al_{0.22}Ga_{0.78})₂O₃ 5 nm spacer and 25 nm barrier 0.10 μm UID buffer layer 	<ul style="list-style-type: none"> Channel (2DEG): 1.85 \times 10¹² cm⁻² S/D: Si, \sim10²⁰ cm⁻³ 	1365 ($V_{GS} = -5$ V) ($L_{SD} = 16$ μ m)	120.1 ($V_{GS} = 0$ V) ($L_{GD} = 16$ μ m)	15.5	41 ($V_{GS} = 2$ V)	\sim 10 ⁷	2019 ⁹⁷
<ul style="list-style-type: none"> Patterned regrowth of n⁺ β-Ga₂O₃ for S/D SiN_x internal passivation Mesa etching for device isolation 									

^aFor each power device, the parameters for evaluating the power switching performance are summarized, including the three-terminal off-state breakdown voltage (V_{br}), on-resistance normalized by the device area ($R_{on,sp}$), power figure of merit (PFOM = $V_{br}^2/R_{on,sp}$), maximum saturation drain current ($I_{ds,sat}$) and I_{on}/I_{off} ratio.

a Fe-doped (010) β -Ga₂O₃ substrate by MOCVD, and then the S/D regions were formed by area-selective Si-ion implantation. The MOSFET with the optimized field-plate design and the channel length (L_{SD}) = 11 μ m can achieve V_{br} = 480 V, $R_{on,sp}$ = 4.58 m Ω cm², and PFOM = 50.4 MW cm⁻². When the L_{SD} was extended to 18 μ m, although the V_{br} could increase to 680 V, the $R_{on,sp}$ increased to 11.7 m Ω cm² accordingly, making the PFOM slightly decreased to 39.5 MW cm⁻² (Table 4G).⁹² In 2019, Mun et al. further improved the source-connected field-plate design by adopting a thin and heavily doped channel. Besides, the deposition conditions for the Al₂O₃ gate dielectric and SiO₂ internal passivation were optimized, leading to record high V_{br} .⁹³ The channel of the β -Ga₂O₃ MOSFET is composed a 150-nm-thick Si-doped (1.5×10^{18} cm⁻³) β -Ga₂O₃ epitaxial layer grown on a Fe-doped (010) β -Ga₂O₃ substrate by MBE. Since the channel doping concentration is high enough, there is no need for the area-selective Si-ion implantation at the S/D regions. Such a design has also been seen in other β -Ga₂O₃ MOSFETs.^{87,88} The MOSFET with the optimized field-plate design (L_{FP} = 3 μ m and L_{GD} = 25 μ m) can achieve V_{br} = 2321 V in Fluorinert, but relatively large $R_{on,sp}$ = 959 m Ω cm² and thus relatively low PFOM = 5.6 MW cm⁻² (Table 4H).⁹³

Recessed Gates and Heterostructure FETs. To further decrease $R_{on,sp}$ while maintaining high V_{br} , in 2019, Tetzner et al. demonstrated depletion-mode β -Ga₂O₃ MOSFETs featuring sub- μ m gate length and gate recess for low $R_{on,sp}$ and SiN_x internal passivation for high V_{br} (Figure 3C).⁹⁴ The channel region is composed of a 200-nm-thick Si-doped β -Ga₂O₃ layer homoepitaxially grown on an Mg-doped (100) β -Ga₂O₃ substrate with a 6° miscut toward the [001] direction. The miscut angle was for avoiding the formation of twin lamellae.⁶² The 100-nm-deep recessed gate was lithographically structured by using BCl₃ reactive ion etching (RIE), followed by atomic layer deposition (ALD) of 25-nm-thick Al₂O₃ gate dielectric. The device isolation was carried out by a multiple energy N-ion implantation. The β -Ga₂O₃ MOSFET with the L_{GD} = 10 μ m can achieve V_{br} = 1830 V, $R_{on,sp}$ = 21.6 m Ω cm², and record high PFOM = 155 MW cm⁻² (Table 4I).⁹⁴ Despite the high breakdown electric field of β -Ga₂O₃ (8 MV cm⁻¹) which enables high V_{br} , most β -Ga₂O₃ MOSFETs suffer from large $R_{on,sp}$, especially when the gate-drain distance needs to be long for reducing the peak electric field. Considering the relatively low intrinsic electron mobility of β -Ga₂O₃ (estimated 100–300 cm² V⁻¹ s⁻¹) compared to SiC and GaN (Table 1), the heterostructure FETs with two-dimensional electron gas (2DEG) channels can achieve high channel mobility due to the absence of impurity scattering.^{95,96} In 2019, Joishi et al. demonstrated β -(Al_{0.22}Ga_{0.78})₂O₃/Ga₂O₃ modulation-doped heterostructure FETs with gate-connected field-plates and SiN_x passivation layers (Figure 3D).⁹⁷ The device epitaxial layers comprise a 100 nm UID β -Ga₂O₃ buffer layer, a 5 nm β -(Al_{0.22}Ga_{0.78})₂O₃ spacer, a delta sheet of Si dopants, and a 25 nm β -(Al_{0.22}Ga_{0.78})₂O₃ barrier, all grown on a Fe-doped (010) β -Ga₂O₃ substrate by PA-MBE. The temperature dependent Hall measurements indicated that the charge density of the conducting channel, mainly composed of the 2DEG, is 3.4×10^{12} cm⁻² with the electron mobility equal to 101 cm² V⁻¹ s⁻¹, which is comparable to the electron mobility achieved by the Ge-doped β -Ga₂O₃ channels (111 cm² V⁻¹ s⁻¹).⁸⁷ It is worth mentioning that similar β -(Al_xGa_{1-x})₂O₃/ β -Ga₂O₃ modulation-doped heterostructure FETs with a delta sheet of Ge dopants has also been demonstrated.⁹⁸ The field-plate design

with SiN_x internal passivation is expected to yield higher V_{br} , because the SiN_x exhibits a (dielectric constant, ϵ_r) \times (dielectric strength, kV mm⁻¹) product of 75 MW cm⁻¹, which is higher than SiO₂ (39 MW cm⁻¹) and Al₂O₃ (69.4 MW cm⁻¹).^{99,100} The β -(Al_{0.22}Ga_{0.78})₂O₃/Ga₂O₃ modulation-doped heterostructure FET with the L_{GD} = 16 μ m can achieve V_{br} = 1365 V, $R_{on,sp}$ = 120.1 m Ω cm², and PFOM = 15.5 MW cm⁻² (Table 4K).⁹⁷

Ohmic Contact Formation. On the aspect of reducing $R_{on,sp}$, one primary task is to form high-quality ohmic contacts at the S/D regions. The commonly used metallization schemes on the β -Ga₂O₃ epitaxial layers include Ti/Au and Ti/Al/Ni/Au, followed by post-metallization annealing at 400–500 °C in nitrogen.¹³ The physical mechanisms for the ohmic contact formation between Ti/Au and Sn-doped β -Ga₂O₃ were investigated.¹⁰¹ It was found that at the junction between Ti and β -Ga₂O₃, a thin layer of Ti-TiO_x, which is partially lattice matched to the β -Ga₂O₃, can facilitate electron transport. Furthermore, the interdiffusion between Au and Ti can narrow the distance between the low-resistance Au and heavily doped β -Ga₂O₃.¹⁰¹ In addition to the metallization and annealing, high doping concentrations at the S/D regions are also critical to reduce the contact resistance. The commonly used doping methods include Si-ion implantation and Sn-doped spin-on-glass (SOG).^{102,103} After Si-ion implantation with the concentration 10^{19} – 10^{20} cm⁻³, the implanted β -Ga₂O₃ substrates were annealed at 900–1000 °C in nitrogen to achieve a high activation efficiency of more than 60%. With the annealed Ti/Au electrodes, the specific contact resistance can be as low as 4.6×10^{-6} Ω cm².¹⁰² In another MOSFET work, the Ti/Au contacts (annealed at 470 °C in nitrogen for 1 min after metallization) on top of a Si-ion implanted S/D regions (Si = 5×10^{19} cm⁻³, annealed at 925 °C in nitrogen for 30 min after implantation) can achieve a similar specific contact resistance of 8.1×10^{-6} Ω cm².⁸⁵ On the other hand, for the SOG doping, the S/D regions were first spin-coated with a 170-nm-thick layer of SOG (Sn = 4×10^{21} cm⁻³), followed by a 5 min and 1100 °C annealing process in nitrogen for the Sn ions to diffuse into the β -Ga₂O₃ layer. Lastly, the SOG layer was removed by a pH-buffered HF treatment.¹⁰³ The Sn doping concentration is 4×10^{21} cm⁻³ at the surface and decays exponentially with the depth into the β -Ga₂O₃ layer. Combined with the annealed Ti/Au electrodes, the specific contact resistance is 2.1×10^{-5} Ω cm², which is much higher than the contact resistance achieved by the Si-ion implantation method. This could be part of the reason why the β -Ga₂O₃ MOSFETs with the SOG S/D contacts have relatively high $R_{on,sp}$ and relatively low PFOM (Table 4E and F).^{89,103} Recently, Jeong et al. demonstrated that by using CF₄ plasma treatment, an ohmic contact can be formed between the Ti/Al/Ti electrode and the Si-doped β -Ga₂O₃ epitaxial layer grown on a *c*-plane sapphire substrate by HVPE (Table 4J).¹⁰⁴ The CF₄ plasma treatment was performed by using a reactive ion etcher with the RF power of 150 W and the slow introduction of CF₄ and O₂ gases into the chamber filled with nitrogen. Then, the Ti/Al/Ti metal stacks at the S/D regions were formed by evaporation, and the deposited electrodes are ohmic even without post-metallization annealing. However, the resulting specific contact resistance (2×10^{-3} Ω cm²) remains relatively high.¹⁰⁴

Recessed Gates and Self-Aligned Gates for RF Operation. So far, the high-breakdown electric field of β -Ga₂O₃ (8 MV cm⁻¹) has been mainly applied toward the

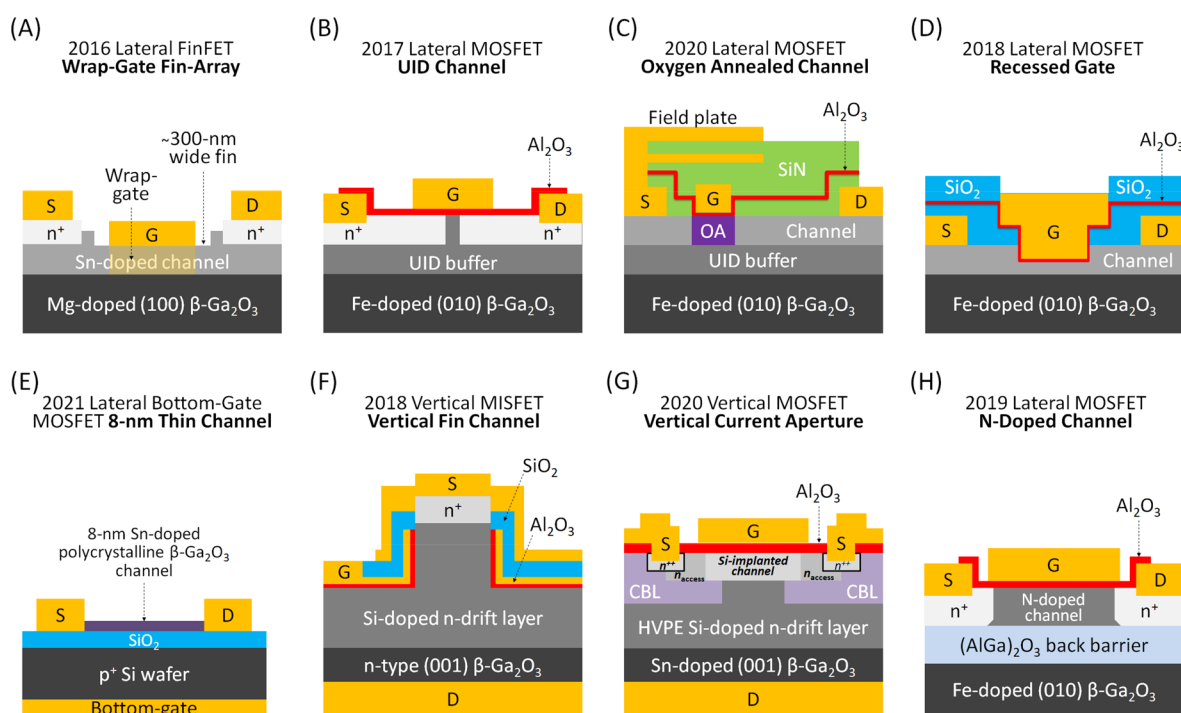


Figure 4. Cross-section illustrations of representative enhancement-mode β -Ga₂O₃ FETs, including (A) FinFET with a wrap-gate,¹¹² (B) MOSFET with a narrow UID channel,¹¹³ (C) MOSFET with an oxygen annealed channel and double source-connected field-plates,¹¹⁴ (D) MOSFET with a recessed gate,¹¹⁵ (E) bottom-gate MOSFET with an 8-nm-thin channel,¹¹⁶ (F) MISFET with a vertical fin channel,¹¹⁷ (G) MOSFET with a vertical current aperture,¹¹⁸ and (H) MOSFET with a N-doped channel.¹²²

power switching application, for which the power device performance is evaluated by the PFOM = $V_{br}^2/R_{on,sp}$ (Table 4). On the other hand, the high breakdown electric field of β -Ga₂O₃ is also advantageous in the JFOM = (breakdown electric field) \times (electron saturation velocity),⁸³ which describes the power-frequency product for the RF applications, such as RF amplifiers, RF switches, and power switching at GHz speed. Based on the combination of ab initio calculations and full band Monte Carlo simulations, a peak electron saturation velocity of 2×10^7 cm s⁻¹ is estimated at an electric field of 200 kV cm⁻¹ (Table 1).¹⁰⁵ Therefore, the JFOM of β -Ga₂O₃ can be higher than GaN and SiC (Table 1). In light of this, in 2017, Green et al. demonstrated depletion-mode β -Ga₂O₃ MOSFETs with recessed gates for small- and large-signal RF operations (Figure 3E).¹⁰⁶ The epitaxial layers, including a 180-nm-thick Si-doped channel layer (1×10^{18} cm⁻³) and a 25-nm-thick Si-doped ohmic layer (1×10^{19} cm⁻³), were grown on a (100) β -Ga₂O₃ substrate with a 6° miscut by MOCVD, followed by multiple steps of lithographic RIE for the mesa device isolation and the formation of S/D regions and recessed gate. For the DC operation, the β -Ga₂O₃ MOSFET exhibits maximum current density = 150 mA mm⁻¹ and maximum transconductance (g_m) of 21.2 mS mm⁻¹ at $V_{GS} = -3.5$ V and $V_{DS} = 40$ V. For the small-signal RF operation, the same device exhibits cutoff frequency (f_T) and maximum oscillating frequency (f_{MAX}) equal to 2.7 and 12.9 GHz, respectively, at the DC biasing condition of maximum g_m . For the large-signal CW RF operation, the same device achieves output power (P_{OUT}) of 0.23 W mm⁻¹ with power added efficiency (PAE) of 6.3% at 800 MHz using passive source and load tuning.¹⁰⁶ In 2019, Liddy et al. demonstrated depletion-mode β -Ga₂O₃ MOSFETs with self-aligned refractory metal gates (SAGs) for eliminating the source access resistance

(Figure 3F).¹⁰⁷ The device fabrication started with the depositions of a 22-nm-thick Si-doped β -Ga₂O₃ epitaxial layer on a Fe-doped (010) β -Ga₂O₃ substrate by MOCVD and then a 30-nm-thick Al₂O₃ gate dielectric by ALD, which can also serve as the implant cap. Next, the W/Cr gate electrode was formed by sputtering and lithographic RIE, followed by Si-ion implantation to define the S/D regions. Lastly, after removing the Al₂O₃ implant cap, the annealed Ti/Al/Ni/Au metals stacks formed ohmic contacts to the implanted regions. Due to the negligible source access resistance and the short channel length (2.5 μ m), the β -Ga₂O₃ MOSFET achieves maximum g_m of 35 mS mm⁻¹ at $V_{GS} = 4$ V and $V_{DS} = 10$ V.¹⁰⁷

Delta-Doped Channels and Oxygen Annealed UID Layers for RF Operation. For the power devices operating at high frequencies, the gate length usually needs to be scaled into the sub- μ m regime. However, such a small-sized gate would not be able to effectively control the channel if the channel thickness is higher than 200 nm. Therefore, approaches like recessed gates and thin channels with heavy doping have been adopted to alleviate this issue.^{93,94,106} In 2019, Xia et al. demonstrated β -Ga₂O₃ metal–semiconductor FETs (MES-FETs) with delta-doped channels for RF operations (Figure 3G).¹⁰⁸ A submonolayer of Si-ion dopants was implanted between two UID buffer layers, which were sequentially grown on a Fe-doped (010) β -Ga₂O₃ substrate by PA-MBE. Based on Hall measurements on an isolated van der Pauw structure, the delta-doped channel has a sheet electron density of 1.13×10^{13} cm⁻² with the electron mobility equal to 70 cm² V⁻¹ s⁻¹. The β -Ga₂O₃ MOSFET can achieve maximum g_m of 44 mS mm⁻¹ at $V_{GS} = 2$ V and $V_{DS} = 12$ V, and record high $f_T = 27$ GHz and $f_{MAX} = 16$ GHz.¹⁰⁸ In order to further improve the large-signal RF performance, it is critical to avoid current collapse at high

Table S. Representative Enhancement-Mode β -Ga₂O₃ FETs with Various Device Structures and Fabricated by Different Deposition Techniques^a

Enhancement-Mode β -Ga ₂ O ₃ FETs									
Features	Substrates/Gates	Epitaxial Layers	Carrier Concentrations	V_{br} (V)	$R_{on,sp}$ (m Ω cm ²)	$V_{dsat}/R_{on,sp}$ (MW cm ⁻²)	$I_{ds,sat}$	I_{on}/I_{off}	ref
(A) <ul style="list-style-type: none"> Lateral finFET Wrap-gate fin-array 	Dielectric Mg-doped (100) β -Ga ₂ O ₃ /20 nm Al ₂ O ₃	MOCVD <ul style="list-style-type: none"> 0.30 μm Sn-doped channel, followed by RIE with Cr hard mask to form fin-array 	Fin-array: 2.3×10^{17} cm ⁻³	612 ($V_{GS} = 0$ V) ($L_{SD} = 21$ μ m) ($W_G = 19$ μ m)	~ 1.6 ($V_{GS} = 4$ V) ($L_{SD} = 4$ μ m) ($W_G = 19$ μ m)	NR	$> \sim 0.18$ mA mm ⁻¹ ($V_{GS} = 4$ V) ($L_{SD} = 4$ μ m) ($W_G = 19$ μ m)	$> 10^5$	2016 ¹¹²
(B) <ul style="list-style-type: none"> Lateral MOSFET UID channel Si implantation for S/D and access regions 	Fe-doped (010) (β -Ga ₂ O ₃ /50 nm Al ₂ O ₃)	OA-MBE <ul style="list-style-type: none"> 1.20 μm UID buffer layer 	Channel: $< 4 \times 10^{-14}$ cm ⁻³ S/D: 5×10^{19} cm ⁻³	~ 40 ($V_{GS} = 0$ V) ($L_{SD} = 4$ μ m)	~ 22.5 ($V_{GS} = 38$ V) ($L_{SD} \sim 4$ μ m)	$\sim 7.1 \times 10^{-2}$	1.4 mA mm ⁻¹ ($V_{GS} = 38$ V) ($L_{SD} = 4$ μ m)	$\sim 10^6$	2017 ¹¹³
(C) <ul style="list-style-type: none"> Lateral MOSFET Oxygen annealing treated channel Double source-connected field-plates Fluorinert Immersion 	Fe-doped (010) β -Ga ₂ O ₃ /30 nm Al ₂ O ₃	MOCVD <ul style="list-style-type: none"> 0.20 μm Si-doped channel 0.60 μm UID buffer layer 	Channel (without oxygen annealing): 2×10^{17} cm ⁻³	> 3000 ($V_{GS} = 0$ V) ($L_{SD} = 17$ μ m)	163 ($V_{GS} = 9$ V) ($L_{SD} = 17$ μ m)	> 55.2	6.4 mA mm ⁻¹ ($V_{GS} = 9$ V) ($L_{SD} = 17$ μ m)	$\sim 10^8$	2020 ¹¹⁴
(D) <ul style="list-style-type: none"> Lateral MOSFET 1-μm-long and recessed gate 	Fe-doped (010) β -Ga ₂ O ₃ /20 nm SiO ₂	OA-MBE <ul style="list-style-type: none"> 0.20 μm Si-doped channel 0.14 μm recess depth 	Channel: $> 5.5 \times 10^{17}$ cm ⁻³	505 ($V_{GS} = 0$ V) ($L_{SD} = 8$ μ m)	17.2 ($V_{GS} = 8$ V) ($L_{SD} = 8$ μ m)	14.8	~ 40 mA mm ⁻¹ ($V_{GS} = 8$ V) ($L_{SD} = 8$ μ m)	$\sim 10^9$	2018 ¹¹⁵
(E) <ul style="list-style-type: none"> Lateral bottom-gate MOSFET 8-nm-thick Sn-doped polycrystalline channel 	Si+/300 nm SiO ₂	RF sputtering \rightarrow 900 °C for 1 h in open air \rightarrow SOG doping <ul style="list-style-type: none"> 8 nm Sn-doped channel 	Channel: $\sim 1.7 \times 10^{17}$ cm ⁻³	224 ($V_{GS} = 0$ V) ($L_{SD} = 8$ μ m)	1.8×10^7 ($V_{GS} = 90$ V) ($V_{TH} = 90$ V)	2.8×10^{-6}	~ 15 nA mm ⁻¹ ($V_{GS} = 90$ V) ($V_{GS} - V_{TH} = 90$ V)	$\sim 10^3$	2021 ¹¹⁶
(F) <ul style="list-style-type: none"> Vertical MISFET Low carrier concentration in the n-drift region 	n-type (001) β -Ga ₂ O ₃ /30 nm Al ₂ O ₃	HVPE <ul style="list-style-type: none"> 10 μm Si-doped n-drift region 	Source region: 5×10^{19} cm ⁻³ n-drift region: $< 2 \times 10^{16}$ cm ⁻³ Substrate: 2×10^{18} cm ⁻³	1057 ($V_{GS} = 0$ V)	~ 18 ($V_{GS} = 3$ V) (Source Area = 0.33 μ m \times 80 μ m)	~ 62.1	~ 350 A cm ⁻² ($V_{GS} = 3$ V) (Source Area = 0.33 μ m \times 80 μ m)	$\sim 10^8$	2018 ¹¹⁷
(G) <ul style="list-style-type: none"> Vertical MOSFET N-ion implanted CBLs to form vertical current apertures 	Sn-doped (001) β -Ga ₂ O ₃ /50 nm Al ₂ O ₃	HVPE <ul style="list-style-type: none"> 9 μm Si-doped n-drift region 	Source region: 5×10^{19} cm ⁻³ Channel: 5×10^{17} cm ⁻³ n-drift region: 1.5×10^{16} cm ⁻³ Substrate: 3×10^{18} cm ⁻³	263 ($V_{GS} = 0$ V)	135 ($V_{GS} = 6$ V)	0.5	26 A cm ⁻² ($V_{GS} = 6$ V)	2×10^7	2020 ¹¹⁸
(H) <ul style="list-style-type: none"> Lateral MOSFET N-doped p-type channel 	Fe-doped (010) β -Ga ₂ O ₃ /20 nm Al ₂ O ₃	PA-MBE <ul style="list-style-type: none"> 50 nm N-doped p-type UID channel 100 nm (AlGa)₂O₃ back barrier layer 	Channel: N: 1×10^{18} cm ⁻³ ; O: 2×10^{17} cm ⁻³ S/D: 5×10^{19} cm ⁻³	NR	NR	NR	1.2 μ A mm ⁻¹ ($V_{GS} = 8$ V) ($L_G = L_{SD} = 4$ μ m)	$> 10^5$	2019 ¹²²

^a For each power device, the parameters for evaluating the power switching performance are summarized, including the three-terminal off-state breakdown voltage (V_{br}), on-resistance normalized by the device area ($R_{on,sp}$), power figure of merit (PFOM = $V_{br}^2/R_{on,sp}$), maximum saturation drain current ($I_{ds,sat}$) and I_{on}/I_{off} ratio.

drain bias (V_{DS}). Therefore, a UID buffer layer is always needed to keep the channel away from the Fe- or Mg-doped insulating substrate. However, background donors, such as Si or hydrogen or oxygen vacancies due to imperfect epitaxy, may lead to a background electron concentration 10^{15} – 10^{16} cm^{-3} . To resolve the issue of conductive UID layers, in 2020, Lv et al. applied an oxygen annealing process for compensating and neutralizing the donors in the UID layer (Figure 3H).¹⁰⁹ After the epitaxial growth of a 0.2- μm -thick Si-doped channel and a 0.5- μm -thick UID buffer layer and the formation of ohmic contacts at the S/D regions, the channel region was deposited with a 0.2- μm -thick SiN passivation layer by plasma-enhanced CVD (PECVD), followed by lithographic etching to expose the gate foot region for the oxygen annealing process (500 °C for 5 min in oxygen atmosphere). The $\beta\text{-Ga}_2\text{O}_3$ MOSFET with the oxygen annealing treatment can achieve maximum g_m of 11 mS mm^{-1} at $V_{GS} = 10$ V and $V_{DS} = 20$ V, and $f_T = 1.8$ GHz, $f_{MAX} = 4.2$ GHz, $P_{OUT} = 0.4$ W mm^{-1} , and PAE = 10% for the large-signal CW RF operation at 1 GHz.¹⁰⁹

■ ENHANCEMENT-MODE $\beta\text{-Ga}_2\text{O}_3$ FETS

For mitigating off-state power loss and ensuring safe operation at high voltages, normally off enhancement-mode transistors are usually preferable to depletion-mode transistors, which require a negative V_{GS} to remain in the off-state. Several approaches have been investigated to shift the threshold voltage (V_{TH}) from negative to positive, as discussed below.

Nonplanar Fin-Shaped Channels. As revealed by the GaN and AlGaIn nanowire fin-shaped FETs (finFETs), the metal gate wrapping around the fins can partially or fully deplete the channels with enhanced electrostatics.^{110,111} Following this concept, in 2016, Chabak et al. demonstrated $\beta\text{-Ga}_2\text{O}_3$ wrap-gate finFETs capable of normally off operation with the V_{TH} between 0 and 1 V (Figure 4A).¹¹² The fabrication of the $\beta\text{-Ga}_2\text{O}_3$ fin-array started on a 300-nm-thick Sn-doped $\beta\text{-Ga}_2\text{O}_3$ epitaxial layer grown on a Mg-doped (100) $\beta\text{-Ga}_2\text{O}_3$ substrate by MOCVD, and then Cr hard mask arrays of ~ 300 -nm-wide fin channels separated with ~ 900 nm pitch were formed on the $\beta\text{-Ga}_2\text{O}_3$ epitaxial layer by electron beam lithography (EBL) and metal evaporation. Subsequently, a RIE step using BCl_3 chemistry, with the etching selectivity $\text{Ga}_2\text{O}_3:\text{Cr} \approx 2:1$, removed the entire Cr mask while creating triangular-shaped fins. The $\beta\text{-Ga}_2\text{O}_3$ wrap-gate finFET with the $L_{SD} = 4$ μm and $L_G = 2$ μm can achieve a I_{on}/I_{off} ratio larger than 10^5 but only a very limited $I_{ds,sat}$ of ~ 0.18 mA mm^{-1} . With the L_{GD} increased to 21 μm , the V_{br} can be as large as 612 V at $V_{GS} = 0$ V (Table 5A).¹¹²

UID or Oxygen Annealed Channels. Compared to the complex fin-shaped channels, in 2017, Wong et al. demonstrated that by using a relatively simple, 4- μm -long UID channel defined by Si-ion implantation, enhancement-mode $\beta\text{-Ga}_2\text{O}_3$ MOSFETs with positive V_{TH} can be realized (Figure 4B).¹¹³ Following the deposition of a 1.2- μm -thick UID buffer layer on a Fe-doped (010) $\beta\text{-Ga}_2\text{O}_3$ substrate by OA-MBE, the S/D regions as well as the access regions were formed by Si-ion implantation (5×10^{19} cm^{-3}), leaving a 4 μm undoped gap as the channel region. The background electron concentration was estimated to be less than 4×10^{14} cm^{-3} by C–V analysis on a Schottky barrier diode (SBD) comprising Pt/ $\beta\text{-Ga}_2\text{O}_3$ UID. The $\beta\text{-Ga}_2\text{O}_3$ MOSFET can achieve an I_{on}/I_{off} ratio nearly 10^6 and a decent $I_{ds,sat} = 1.4$ mA mm^{-1} . However, the V_{br} is only ~ 40 V, which is attributed to premature breakdown through the Al_2O_3 dielectric layer between the gate and drain

(Table 5B).¹¹³ Previously, an oxygen annealing process was applied for compensating and neutralizing the background donors in the UID layer, in order to improve the MOSFET's large-signal RF performance (Figure 3H).¹⁰⁹ Following the same concept, in 2020, Lv et al. demonstrated that the oxygen annealing treatment under the gate region can exhaust the electron concentration in the channel, leading to normally off operation (Figure 4C).¹¹⁴ A 0.6- μm -thick UID buffer layer and a 0.2- μm -thick Si-doped (2×10^{17} cm^{-3}) channel layer were epitaxially grown on a Fe-doped (010) $\beta\text{-Ga}_2\text{O}_3$ substrate by MOCVD. After the formation of ohmic contacts at the S/D regions, a 0.2- μm -thick SiN was deposited via PECVD, followed by lithographic etching to expose the gate foot region for the oxygen annealing process (500 °C for 5 min in oxygen atmosphere). The $\beta\text{-Ga}_2\text{O}_3$ MOSFET with the double source-connected field-plates and $L_{GD} = 17$ μm can achieve record high $V_{br} > 3000$ V in Fluorinert FC-770, $R_{on,sp} = 163$ $\text{m}\Omega \text{cm}^2$, and PFOM > 55.2 MW cm^{-2} (Table 5C).¹¹⁴

Recessed Gates or Ultrathin Channels. As described previously, small-sized and recessed gates are useful in rapidly controlling the channels for RF operations.^{94,106} In 2018, Chabak et al. demonstrated that if the active channel thickness, decreased by the recessed gate, is small enough, the gated region of the channel can be fully depleted at $V_{GS} = 0$ V (Figure 4D).¹¹⁵ The channel, a 0.2- μm -thick Si-doped $\beta\text{-Ga}_2\text{O}_3$ epitaxial layer, was grown on a Fe-doped (010) $\beta\text{-Ga}_2\text{O}_3$ substrate, followed by a similar recessed gate formation process as described previously.¹⁰⁶ The recess depth was ~ 140 nm, leaving the active channel thickness of ~ 60 nm in the gated region. Based on Hall measurements on several unetched van der Pauw structures, the undepleted channel layer has an average minimum free carrier concentration of 5.5×10^{17} cm^{-3} and an average sheet electron mobility of 106 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. The enhancement-mode $\beta\text{-Ga}_2\text{O}_3$ MOSFET, with the recessed gate design, $L_G = 1$ μm and $L_{SD} = 8$ μm , can achieve $V_{br} = 505$ V, $R_{on,sp} = 17.2$ $\text{m}\Omega \text{cm}^2$, and PFOM = 14.8 MW cm^{-2} (Table 5D).¹¹⁵ Following the concept of applying an ultrathin, fully depleted channel for enhancement-mode FETs, in 2021, Yoon et al. demonstrated that 8-nm-thin Sn-doped polycrystalline $\beta\text{-Ga}_2\text{O}_3$ thin films can serve as the channels of bottom-gate MOSFETs capable of normally off high-voltage operation (Figure 4E).¹¹⁶ The device fabrication started with the deposition of an amorphous 8 nm thin Ga_2O_3 thin film on a $\text{SiO}_2/\text{p}^+\text{Si}$ substrate by RF sputtering, followed by annealing at 900 °C for 1 h in an open atmosphere for crystallization into monoclinic $\beta\text{-Ga}_2\text{O}_3$. The n-type doping of the $\beta\text{-Ga}_2\text{O}_3$ thin film was accomplished by a similar SOG method as described previously.^{102,103} Finally, the S/D electrodes were formed by the deposition of Ti/TiN metal stacks by RF sputtering. The optical bandgap of the 8-nm-thin Sn-doped polycrystalline $\beta\text{-Ga}_2\text{O}_3$ thin film (5.77 eV) is higher than that of a 100-nm-thick $\beta\text{-Ga}_2\text{O}_3$ thin film (4.7 eV) due to the quantum confinement effect. The back-gate MOSFET with the nanomembrane channel can achieve high $V_{br} = 224$ V, but the $R_{on,sp}$ and $I_{ds,sat}$ are unsatisfactory compared to conventional $\beta\text{-Ga}_2\text{O}_3$ FETs fabricated by epitaxy (Table 5E).¹¹⁶

Vertical Fins or Current Apertures. In 2018, Hu et al. demonstrated high-voltage, vertical $\beta\text{-Ga}_2\text{O}_3$ MOSFETs which can remain in the off-state with $V_{GS} = 0$ V under $V_{DS} > 1$ kV (Figure 4F).¹¹⁷ A 10- μm -thick Si-doped ($N_d < 2 \times 10^{16}$ cm^{-3}) n-drift layer was grown on an n-type (001) $\beta\text{-Ga}_2\text{O}_3$ substrate by HVPE, followed by Si-ion implantation ($N_d = 5 \times 10^{19}$ cm^{-3}) on the epitaxial layer to form the source region. Then,

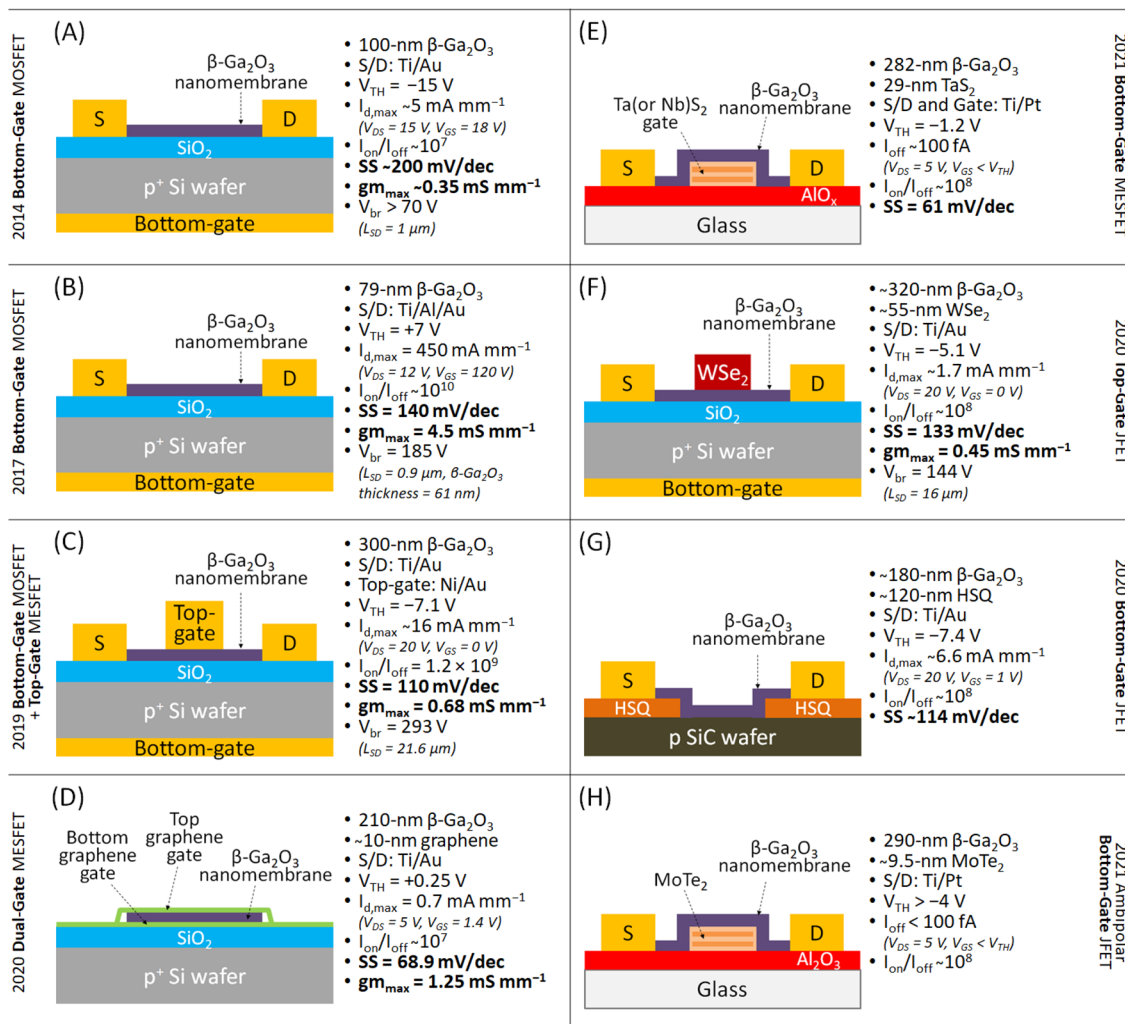


Figure 5. Schematic drawings of representative β -Ga₂O₃ nanomembrane FETs with various gating schemes, including (A, B) bottom-gate MOSFETs,^{123,127} (C) bottom-gate MOSFET and top-gate MESFET,¹³² (D) dual-gate MESFET,¹³³ (E) bottom-gate MESFET,¹³⁴ (F) top-gate JFET,¹³⁵ (G) bottom-gate JFET,¹³⁷ and (H) ambipolar bottom-gate JFET.¹³⁸ For each β -Ga₂O₃ nanomembrane FET, the parameters for evaluating the device performance are summarized, including the threshold voltage (V_{TH}), maximum drain current ($I_{d,max}$), I_{on}/I_{off} ratio, subthreshold slope (SS), maximum transconductance ($g_{m,max}$), and breakdown voltage (V_{br}).

the vertical channel was formed by RIE with the patterned Pt metal mask which defines the position and area of the source. A 30-nm-thick Al₂O₃ was deposited by ALD as the gate dielectric, followed by sputtering a 50-nm-thick Cr as the gate electrode. The vertical β -Ga₂O₃ MOSFET with the source area equal to 0.33 μ m \times 80 μ m can achieve V_{br} = 1057 V at V_{GS} = 0 V and $R_{on,sp}$ \sim 18 m Ω cm², resulting in PFOM \sim 62.1 MW cm⁻² (Table 5F).¹¹⁷ Following the concept of vertical fin channel, in 2020, Wong et al. used N-ion implanted current blocking layers (CBLs) to form vertical current apertures connecting between drain and source (Figure 4G).¹¹⁸ A 9- μ m-thick Si-doped (1.5×10^{16} cm⁻³) n-drift layer was formed on a Sn-doped (001) β -Ga₂O₃ substrate by HVPE, followed by chemical mechanical polishing. The 0.8- μ m-thick CBLs were formed in the epitaxial layer by N-ion implantation (1.5×10^{18} cm⁻³), followed by annealing at 1100 $^{\circ}$ C for 30 min in nitrogen to remove implantation damage and activate the implanted N as compensating acceptors. Subsequently, Si-ion implantation was conducted to form the channel regions, source access regions, and source contact layers, with the doping concentrations equal to 5×10^{17} cm⁻³, 2×10^{18} cm⁻³,

and 5×10^{19} cm⁻³, respectively, followed by annealing at 950 or 800 $^{\circ}$ C for 30 min in nitrogen for the donor activation. The vertical β -Ga₂O₃ MOSFET with the CBL formed vertical current aperture can achieve V_{br} = 263 V at V_{GS} = 0 V and $R_{on,sp}$ = 135 m Ω cm², resulting in PFOM = 0.5 MW cm⁻² (Table 5G).¹¹⁸

N-Doped p-Type Channel. Theoretically, N can act as deep acceptors in β -Ga₂O₃,^{119–121} while Si has been experimentally confirmed as shallow donors. In 2019, Kamimura et al. demonstrated that by controlling the doping concentration ratio between N and Si, the β -Ga₂O₃ UID layer can behave as a p-type channel, based on which an enhancement-mode β -Ga₂O₃ MOSFET can be obtained (Figure 4H).¹²² The device was based on a 50-nm-thick UID channel layer and a 100-nm-thick (AlGa)₂O₃ back barrier layer, both of which were grown on a Sn-doped (010) β -Ga₂O₃ substrate by PA-MBE, with the Ga beam flux constantly at 1.8×10^{-7} Torr and the O₂ flux at \sim 1 sccm, that is around the stoichiometry condition. According to the secondary ion mass spectroscopy (SIMS) analysis, in the UID channel the N concentration (1×10^{18} cm⁻³) was estimated to be much

higher than the Si concentration ($2 \times 10^{17} \text{ cm}^{-3}$), making the UID channel p-type. The enhancement-mode $\beta\text{-Ga}_2\text{O}_3$ MOSFET with the p-type UID channel and the $V_{\text{TH}} > +8 \text{ V}$ can achieve a $I_{\text{on}}/I_{\text{off}}$ ratio larger than 10^5 , but the $I_{\text{ds,sat}}$ remained low at $1.2 \mu\text{A mm}^{-1}$, since the V_{GS} swing was limited up to $+8 \text{ V}$ by the Al_2O_3 gate leakage (Table SH).¹²²

■ $\beta\text{-Ga}_2\text{O}_3$ NANOMEMBRANE FETS

Despite its UWBG (4.9 eV) and high breakdown electric field (8 MV cm^{-1}), one obvious drawback of $\beta\text{-Ga}_2\text{O}_3$ is the relatively low thermal conductivity ($21 \text{ W m}^{-1} \text{ K}^{-1}$ in [010]), compared to Si ($150 \text{ W m}^{-1} \text{ K}^{-1}$), SiC ($270 \text{ W m}^{-1} \text{ K}^{-1}$), and GaN ($210 \text{ W m}^{-1} \text{ K}^{-1}$) (Table 1). In 2014, Hwang et al. found that $\beta\text{-Ga}_2\text{O}_3$ nanomembranes can be easily synthesized by an exfoliation process similar to that of graphene and transferred to a different semiconductor platform.¹²³ Although $\beta\text{-Ga}_2\text{O}_3$ is not a layered material like graphene, the ease of exfoliation is likely attributed to the monoclinic structure and the higher lattice parameter along the [100] direction than the [010] and [001] directions.¹⁴ The integration scheme is beneficial for on-chip power management and enables the formation of heterojunctions, which may open the possibilities of new (opto) electronic applications. Particularly, in contrast to the low power switching applications demonstrated by other nanomaterials, such as graphene, MoS₂, and WSe₂,^{124–126} the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FETs aim at achieving high-power switching in low dimensions.

Shifting from Depletion- to Enhancement-Mode. As mentioned previously, the enhancement-mode power devices enable fail-safe operation and simplify circuit designs at the system level. For the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FETs, the V_{TH} can be shifted from negative to positive via various approaches. In 2017, Zhou et al. showed that the V_{TH} of bottom-gate MOSFETs ($\beta\text{-Ga}_2\text{O}_3/\text{SiO}_2/\text{p+ Si}$) can be increased from -120 V to $\sim 80 \text{ V}$, when the thickness of the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane channel was shrunk from 110 to 50 nm.¹²⁷ In 2019, Kim et al. found that by applying remote CF_4 plasma on part of the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane, the V_{TH} of the top-gate MOSFETs can be increased from -7.5 V without the treatment to $\sim 2 \text{ V}$ with the treatment.¹²⁸ In 2022, Wang et al. demonstrated that by forming a heterojunction between the p-type SnO and n-type $\beta\text{-Ga}_2\text{O}_3$ nanomembrane, the V_{TH} of the bottom-gate MOSFETs ($\text{SnO}/\beta\text{-Ga}_2\text{O}_3/\text{SiO}_2/\text{p+ Si}$) can be increased from -40 V without SnO to $\sim 5 \text{ V}$ with 12 nm SnO.¹²⁹

Bottom-Gate MOSFETs. To effectively control the channels of the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane MOSFETs, i.e., to decrease the subthreshold slope (SS, mV/dec) of the MOSFET, various gating schemes have been investigated. The most widely used scheme is the bottom-gate MOSFETs,^{123,127,130} in which a $\beta\text{-Ga}_2\text{O}_3$ membrane (as the channel), exfoliated from a (-201) bulk $\beta\text{-Ga}_2\text{O}_3$ crystal, is transferred to the surface of a SiO_2 dielectric layer (as the gate dielectric) deposited on a heavily doped Si substrate (as the bottom-gate). The $\beta\text{-Ga}_2\text{O}_3$ nanomembrane firmly adheres to the SiO_2 surface through the bond-free van der Waals force. Subsequently, the S/D regions are defined by EBL, followed by Ti/Al/Au or Ti/Au metallization and a lift-off process. Two representative bottom-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FETs and their electrical characteristics are shown in Figure SA and B.^{123,127} It is worth mentioning that an Ar plasma bombardment process prior to the S/D metallization step can effectively reduce the contact resistance. Without the Ar bombardment,

the contacts may show Schottky-like behaviors.¹²⁷ Furthermore, to achieve high drain currents, the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane channels need to have adequate electron concentrations. Therefore, heavily doped crystals ($2.7 \times 10^{18} \text{ cm}^{-3}$), from which the nanomembranes are exfoliated, are desirable.¹²⁷ The bottom-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FETs also exhibit much better temperature and air stabilities, compared to devices based on conventional 2D transition metal dichalcogenides. No degradation of electrical characteristics was observed when the operating temperature was elevated to $250 \text{ }^\circ\text{C}$ or after a month-long storage in ambient condition.¹³⁰ Moreover, the electrical properties of the bottom-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FETs can be improved by Al_2O_3 surface passivation, which reduces surface states and adsorbates at the nanomembrane surface.¹³¹

Dual-Gate FETs. To further enhance the channel control, dual-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FETs have been developed recently.^{132,133} In 2019, Ma et al. demonstrated a dual-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FET, comprising a top-gate MEFET and a bottom-gate MOSFET, as shown in Figure SC.¹³² Upon the bottom-gate MOSFET ($\beta\text{-Ga}_2\text{O}_3/\text{SiO}_2/\text{p+ Si}$), the top-gate electrode (Ni/Au) was deposited over a part of the $\beta\text{-Ga}_2\text{O}_3$ channel by EBL and lift-off processes. A Schottky contact is formed at the Ni/ $\beta\text{-Ga}_2\text{O}_3$ interface. Therefore, when a negative potential is applied to the top-gate, the depletion width of the Schottky junction expands, reducing the effective channel thickness. Compared to the bottom-gating mode, the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FET operating in the dual-gating mode exhibited a positively shifted V_{TH} , a much higher $g_{\text{m,max}}$ and a much lower SS.¹³² In 2020, Kim et al. demonstrated double graphene-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane MEFETs (graphene/ $\beta\text{-Ga}_2\text{O}_3$ /graphene), as shown in Figure SD.¹³³ The graphene and $\beta\text{-Ga}_2\text{O}_3$ nanomembranes were mechanically exfoliated from the pyrolytic graphite and (-201) $\beta\text{-Ga}_2\text{O}_3$ crystals, respectively, and subsequently integrated into the multilayered architecture via van der Waals heterojunctions on a $\text{SiO}_2/\text{p+ Si}$ substrate. The S/D electrodes were formed by EBL and lift-off processes, followed by a rapid thermal annealing step (1 min in Ar at $480 \text{ }^\circ\text{C}$) to form ohmic contacts with the $\beta\text{-Ga}_2\text{O}_3$ channel. Compared to the single graphene-gate device with a negative V_{TH} (-0.96 V), the double graphene-gate $\beta\text{-Ga}_2\text{O}_3$ MEFET operated with a positive V_{TH} ($+0.25 \text{ V}$) and achieved a low SS (68.9 mV/dec). The excellent electrical properties are attributed to the high crystallinity of each exfoliated nanomembrane and the high-quality interface between graphene and $\beta\text{-Ga}_2\text{O}_3$.¹³³

Bottom-Gate MEFETs. In addition to the Schottky junctions described previously (Ni/ $\beta\text{-Ga}_2\text{O}_3$ and graphene/ $\beta\text{-Ga}_2\text{O}_3$),^{132,133} in 2021, Kim et al. demonstrated bottom-gate nanomembrane MEFETs based on the Schottky junctions of Nb(or Ta)₂S₂/ $\beta\text{-Ga}_2\text{O}_3$, as shown in Figure SE.¹³⁴ The exfoliated Nb(or Ta)₂S₂ nanoflake as the bottom-gate was dry-transferred onto a AlO_x -coated glass substrate by polydimethylsiloxane (PDMS) stamping. Then the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane channel was precisely aligned and electrostatically transferred onto the Nb(or Ta)₂S₂ nanoflake. The S/D and gate electrodes (Ti/Pt) were defined by photolithography, sputtering deposition, and lift-off processes. Note that after the UV exposure and development, plasma treatment to the $\beta\text{-Ga}_2\text{O}_3$ was performed for improving the ohmic contacts. Due to TaS₂'s larger work function (5.6 eV) than usual novel metals, the TaS₂ bottom-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane MEFET achieved a record low (61 mV/dec) with a negative

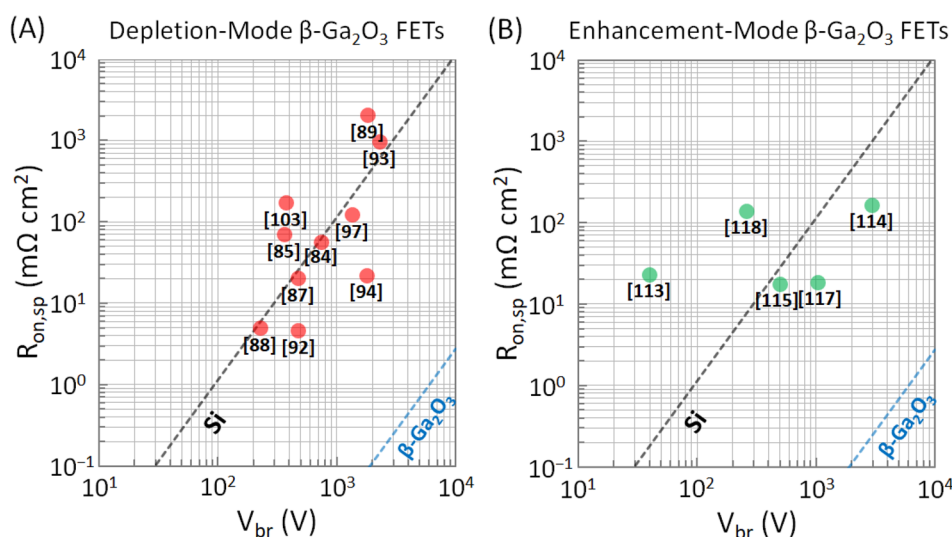


Figure 6. (A) Representative depletion-mode $\beta\text{-Ga}_2\text{O}_3$ FETs with the V_{br} and $R_{\text{on,sp}}$ listed in Table 4 (red circles). (B) Representative enhancement-mode $\beta\text{-Ga}_2\text{O}_3$ FETs with the V_{br} and $R_{\text{on,sp}}$ listed in Table 5 (green circles). The black and blue dashed lines represent the Baliga's theoretical limits for Si and $\beta\text{-Ga}_2\text{O}_3$, respectively.

V_{TH} (-1.2 V). When integrated as a switch into a green organic LED pixel circuit, the $\beta\text{-Ga}_2\text{O}_3$ nanomembrane MESFET exhibits almost the same or even superior low leakage (~ 100 fA) performance compared to conventional a-IGZO channel MOSFETs in the pixel switching.¹³⁴

Top-Gate JFETs. By taking advantage of the strain-free van der Waals heterojunctions between the exfoliated $\beta\text{-Ga}_2\text{O}_3$ nanomembranes and other two-dimensional semiconductor nanomaterials, junction FETs (JFETs) of various forms have been developed recently.^{135–138} In 2018, Kim et al. demonstrated heterojunction $\beta\text{-Ga}_2\text{O}_3$ nanomembrane JFETs through van der Waals bonding with exfoliated WSe_2 nanomembranes, as shown in Figure 5F.¹³⁵ The device fabrication was similar to the graphene/ $\beta\text{-Ga}_2\text{O}_3$ /graphene dual-gate MESFETs,¹³³ except that the graphene dual-gate was replaced by a WSe_2 top-gate. The rectifying current–voltage characteristic of the heterojunction comprising p-type WSe_2 and n-type $\beta\text{-Ga}_2\text{O}_3$ was clearly observed. When applied with a negative V_{GS} , the depletion width of the reverse-biased $\text{WSe}_2/\beta\text{-Ga}_2\text{O}_3$ heterojunction increases, narrowing the effective channel thickness. The WSe_2 top-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane JFET operated in the depletion-mode with the $V_{\text{TH}} = -5.1$ V, $\text{SS} = 68.9$ mV/dec, $\text{gm}_{\text{max}} = 0.45$ mS mm^{-1} , and $V_{\text{br}} = 144$ V. Moreover, the JFET exhibited outstanding long-term stability and was able to retain most of the transistor characteristics at high operating temperatures.¹³⁵ In 2020, Li et al. demonstrated a similar JFET but with the top-gate replaced by p-type black phosphorus (BP). The BP top-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane JFET also operated in the depletion-mode with the $V_{\text{TH}} = -20$ V, $\text{SS} = 260$ mV/dec, and $\text{gm}_{\text{max}} = 4.2$ mS mm^{-1} .¹³⁶

Bottom-Gate JFETs. Considering the low thermal conductivity of $\beta\text{-Ga}_2\text{O}_3$, integrating $\beta\text{-Ga}_2\text{O}_3$ nanomembrane FETs on a different material substrate can potentially achieve more efficient on-chip heat dissipation through the substrate. In 2020, Lee et al. demonstrated heterojunction $\beta\text{-Ga}_2\text{O}_3$ nanomembrane JFETs on 4H-SiC substrates through van der Waals bonding, as shown in Figure 5G.¹³⁷ The 4H-SiC can function as the bottom-gate as well as the thermal drain due to its relatively high thermal conductivity (Table 1). The device

fabrication started with the homoepitaxial growth of a p-type 4H-SiC layer (1 μm thick and doping concentration equal to 2×10^{17} cm^{-3}). Then, two hydrogen silsesquioxane (HSQ) covered regions, for insulating the S/D electrodes from the conductive 4H-SiC layer, were formed by EBL, followed by developing using 25% tetramethylammonium hydroxide. An exfoliated $\beta\text{-Ga}_2\text{O}_3$ nanomembrane was dry-transferred onto the HSQ and 4H-SiC to form the channel. Lastly, the S/D electrodes were fabricated by EBL, metallization, and lift-off, followed by rapid thermal annealing for creating ohmic contacts with the $\beta\text{-Ga}_2\text{O}_3$ channel. When applied with a negative V_{GS} , the depletion width of the heterojunction between the p-type 4H-SiC and n-type $\beta\text{-Ga}_2\text{O}_3$ increases, narrowing the effective channel thickness. The 4H-SiC bottom-gate $\beta\text{-Ga}_2\text{O}_3$ nanomembrane JFET operated in the depletion-mode with the $V_{\text{TH}} = -7.4$ V and $\text{SS} = 114$ mV/dec. Most importantly, for the same input power of 160 W m^{-1} , the JFET based on the 4H-SiC substrate exhibited a peak temperature at least 100 $^\circ\text{C}$ lower than based on a sapphire substrate, manifesting the stronger heat dissipation of the 4H-SiC substrate.¹³⁷ Interestingly, in 2021, Choi et al. demonstrated ambipolar JFETs based on van der Waals heterojunctions formed between exfoliated p-type MoTe_2 flakes and exfoliated n-type $\beta\text{-Ga}_2\text{O}_3$ nanomembranes, either of which can function as the channel, as shown in Figure 5H.¹³⁸ With the MoTe_2 as the bottom-gate and the $\beta\text{-Ga}_2\text{O}_3$ as the channel, the JFET operated in the depletion-mode with the $V_{\text{TH}} > -4$ V and $I_{\text{on}}/I_{\text{off}}$ ratio $\sim 10^8$.¹³⁸

CONCLUSION

Due to its UWBG (4.9 eV) and large breakdown electric field (8 MV cm^{-1}), $\beta\text{-Ga}_2\text{O}_3$ has attracted renewed attention as one of the next-generation semiconductors recently. Compared to the commercialized semiconductors, such as Si, GaN, and SiC, power devices based on $\beta\text{-Ga}_2\text{O}_3$ are capable of handling high voltages in smaller dimensions and with higher efficiencies. Furthermore, the $\beta\text{-Ga}_2\text{O}_3$ bulk crystals can be synthesized by the relatively low-cost melt growth methods, such as the FZ, CZ, and EFG methods, making the single-crystal substrates and epitaxial layers readily accessible. Several epitaxy

techniques have been investigated for the depositions of α -, ε -, and β -phase Ga_2O_3 , including MOCVD, LPCVD, PA-MBE, HVPE, and mist-CVD, among which MOCVD is most widely used while HVPE offers relatively high growth rates. For the homoepitaxy on the (100) β - Ga_2O_3 substrates, despite ultraflat surfaces obtained, stacking faults in the form of twin lamellae are usually observed in the epitaxial layers, which however can be avoided by using substrates with relatively large miscut angles. In contrast, the epitaxial layers based on the (010) β - Ga_2O_3 substrates possess better crystal qualities, and the heat transfer along the [010] direction is more efficient than along the [100] direction. Therefore, Fe-doped semi-insulating (010) β - Ga_2O_3 substrates are widely used for fabricating high-performance β - Ga_2O_3 MOSFETs. On the other hand, the β - Ga_2O_3 epitaxial layers grown on *c*-plane sapphire substrates, although showing clear (−201)-oriented XRD patterns, are not thoroughly single-crystal, because of the symmetry mismatch between the monoclinic β - Ga_2O_3 and hexagonal Al_2O_3 . The orthorhombic ε - Ga_2O_3 can be better matched to the sapphire substrates, but tends to transform into β - Ga_2O_3 upon high-temperature annealing. Therefore, so far the great majority of the β - Ga_2O_3 FETs have been built on the homoepitaxial layers, although heteroepitaxy on the sapphire substrates in the long term should be the more cost-effective solution.

For the power switching application, to exploit the full potential of β - Ga_2O_3 , many device-level approaches have been developed to increase V_{br} and decrease $R_{\text{on,sp}}$ for maximizing PFOM. The depletion-mode β - Ga_2O_3 FETs with gate- or source-connected field-plates, Fluorinert immersion, and SiN_x passivation can effectively avoid premature breakdown through the β - Ga_2O_3 channel and air, resulting in V_{br} higher than 1000 V. On the aspect of reducing $R_{\text{on,sp}}$, the Ge-doped β - Ga_2O_3 channels possess higher electron mobility than the Sn-doped channels, and the 2DEG channels of the heterostructure FETs also exhibit high electron mobility ($>100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) due to the absence of impurity scattering. In addition, ohmic contacts with the channels can be formed via Ti/Au metallization followed by annealing, and the heavily doped S/D regions can be obtained by Si-ion implantation or SOG. As shown in Figure 6A, although some depletion-mode β - Ga_2O_3 FETs have already achieved V_{br} higher than 1000 V, further reduction of $R_{\text{on,sp}}$ is necessary, so that the β - Ga_2O_3 FETs' PFOMs can advance closer to the Baliga's theoretical limit. For the RF amplification application, it is desirable for the power devices to have large transconductance gain (gm) and wide bandwidth (f_{T} and f_{MAX}). To better control the channels, which leads to high gm, recessed gates and delta-doped channels have been applied for the depletion-mode β - Ga_2O_3 FETs, resulting in gm higher than 20 mS mm^{-1} . For increasing the bandwidth, parasitic capacitance and resistance of the β - Ga_2O_3 FETs needs to be minimized. In light of this, the SAGs have been adopted for eliminating the source access resistance.

For mitigating off-state power loss and ensuring safe operation at high voltages, enhancement-mode FETs are usually preferable to depletion-mode ones. Despite the lack of p-type doping, several device-level approaches have been developed to shift the V_{TH} of the β - Ga_2O_3 FETs from negative to positive. The main idea is to deplete the gated region of the channel. For example, the metal wrap-gates of the finFETs can partly or fully deplete the narrow fin channels with enhanced electrostatics. Following the same idea, the enhancement-mode β - Ga_2O_3 FETs with ultrathin channels, recessed gates, vertical fin channels and vertical current apertures have been

demonstrated. In addition, the electron concentrations of the channels can be exhausted by using oxygen annealing or by simply adopting an UID channel. It is worth mentioning that p-type UID channels have been demonstrated by using N-ion implantation. However, the drain currents of such devices remained low. Despite the tremendous progress recently, as shown in Figure 6B, the performance of the enhancement-mode β - Ga_2O_3 FETs in general is still lagging the depletion-mode ones in terms of V_{br} and $R_{\text{on,sp}}$. Lastly, to resolve the low-thermal conductivity issue of β - Ga_2O_3 , exfoliated nanomembranes of β - Ga_2O_3 are integrated into multilayered structures on various semiconductor platforms for better heat dissipation. Based on the strain-free van der Waals heterojunctions which can control the effective channel thickness, the electrical characteristics of the β - Ga_2O_3 nanomembrane FETs can be easily modulated. Depending on the gating schemes, a great variety of β - Ga_2O_3 nanomembrane FETs have been explored, such as bottom-gate MOSFETs (β - $\text{Ga}_2\text{O}_3/\text{SiO}_2/\text{p}+\text{Si}$), top-gate MESFETs (Ni/β - Ga_2O_3), dual-gate MESFETs (graphene/ β - Ga_2O_3 /graphene), bottom-gate MESFET (β - $\text{Ga}_2\text{O}_3/\text{TaS}_2$), top-gate JFETs (p-type WSe_2/n -type β - Ga_2O_3 and p-type BP/ n -type β - Ga_2O_3), and bottom-gate JFETs (n -type β - $\text{Ga}_2\text{O}_3/\text{p}$ -type SiC and n -type β - $\text{Ga}_2\text{O}_3/\text{p}$ -type MoTe_2). In general, the β - Ga_2O_3 nanomembrane FETs possess strong channel control capability, with the SS lower than 200 mV/dec , which is favorable for the high-frequency power switching application. However, the V_{br} and gm of the β - Ga_2O_3 nanomembrane FETs are lower than the epitaxial β - Ga_2O_3 FETs.

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Notes

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