

CONDENSED MATTER PHYSICS

Controlling and visualizing Dirac physics in topological semimetal heterostructures

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A bulk crystal of cadmium arsenide is a three-dimensional Dirac semimetal, but, in a thin film, it can behave like a three-dimensional topological insulator. This tunability provides unique opportunities to manipulate and explore a topological insulator phase. However, an obstacle to engineering such tunability is the subtlety of transport-based discriminants for topological phases. In this work, the quantum capacitance of cadmium arsenide-based heterostructures provides two direct experimental signatures of three-dimensional topological insulator physics: an insulating three-dimensional bulk and a Landau level at zero energy that does not disperse in a magnetic field. We proceed to join our ability to see these fingerprints of the topological surface states with flexibility afforded by our epitaxial heterostructures to demonstrate a route toward controlling the energy of the Dirac nodes on each surface. These results point to new avenues for engineering topological insulators based on cadmium arsenide.

INTRODUCTION

Since its discovery as a three-dimensional (3D) Dirac semimetal (1), cadmium arsenide (Cd_3As_2) has been studied as an exemplar (2, 3). Its remarkable properties include its high mobility (4, 5) and the lack of massive energy bands near its 3D Dirac nodes. As a topological material, great interest has been directed toward devising ways of studying, controlling, and ultimately harnessing its surface states. Powerful experimental controls alongside ready integration into existing technology form the promise of epitaxial thin films as a setting for achieving these goals.

The growth direction of the Cd_3As_2 film determines the surface states relevant to transport. In 3D Dirac semimetals, Fermi arc-like surface states (6), which inhabit those surface Brillouin zones into which the bulk Dirac nodes project onto different points, are not topologically protected (7), although transport through such surface states may occur nonetheless (8, 9). The Cd_3As_2 (001) surface Brillouin zone, however, is distinguished from all others in that the two bulk Dirac nodes project onto the same point, eliminating the possibility of a Fermi arc-like surface state. The Cd_3As_2 (001) surface state is due to the band inversion in the film's bulk (1, 10) and is topologically protected (1). Thus, a (001)-oriented Cd_3As_2 film that demonstrates only surface state transport can be said to be a topological insulator (11). Experiments indicate that this regime prevails in films whose thickness falls between 10 and 50 nm, although the cutoffs on either end are not known precisely (11, 12).

The topologically protected nature of these surface states guarantees their presence, but not their accessibility or visibility in a device. For example, the energy of the 2D Dirac node on either surface may fall below the energy of a bulk band, obscuring the physics of the topological surface state. Previous work has demonstrated the sensitivity of the surface states to the chemical preparation of the film's top surface (13), and capped structures benefit from improved mobility, consistent carrier density, and higher reproducibility (12, 14). Nevertheless, a way to control the 2D surface Dirac nodes' energy has not yet been demonstrated.

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There are two main results of this work. In the first result, we directly visualize the nondispersing zeroth Landau level in the (001) Cd_3As_2 thin-film surface state, a fingerprint of its 2D Dirac nature. The technique we use, based on the system's quantum capacitance, allows us to separate the contributions of the two surface states. Together, these are powerful evidence for the 3D topological insulator picture in (001) Cd_3As_2 films (11). In addition, the quantum capacitance clarifies some longstanding features of the gated Hall bar transport in (001) Cd_3As_2 .

The concept of the quantum capacitance technique is that, for a capacitor where one plate is a metal and the other is a material with a finite density of states, there is a series-wise reduction of the total capacitance by that finite density of states, i.e.

$$C/A = \left\{ (C_{\text{geo}}/A)^{-1} + [e^2 D(E)]^{-1} \right\}^{-1} \quad (1)$$

where $C_{\text{geo}} = \epsilon_r \epsilon_0 A/d$, with A being the area of the parallel plate capacitor, d being the dielectric thickness, ϵ_r being the relative dielectric constant of the dielectric, and ϵ_0 being the dielectric constant; e is the electron charge; and $D(E)$ is the 2D density of states per area per energy in the material with the finite density of states (15, 16). For a 3D topological insulator thin film, the relation between the total capacitance measured, C , and the total density of states is slightly but measurably altered by the separation of the large surfaces by another dielectric, namely, the 3D insulating bulk (17). Comparing Eq. 1 with a model for the capacitance of a 3D topological insulator thus reveals the presence of its insulating bulk and topological surface states.

The second main result is the demonstration of the importance of the epitaxial setting, i.e., the composition of the full heterostructure in which the Cd_3As_2 film is embedded, which is enabled by the visualization of the low-energy density of states of the topological surface states. In particular, we demonstrate that our method is able to detect the differences in energy between the Dirac nodes on either surface and the fact that they are tuned according to the composition of the semiconductor layer beneath the Cd_3As_2 . This information is essential in realizing the highly sought-after quantum spin Hall insulator state in thin films of Cd_3As_2 , which depends on minimizing this energy difference (18). More broadly, the use of epitaxial

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heterostructures represents a new route to engineering topological insulator materials, using well-understood, highly controllable semiconductor materials as tools to optimize the topological properties of heterostructures and devices based on new materials.

RESULTS

We discuss data from three different samples, A, A', and B. The structure of sample A is shown in Fig. 1A. A 150-nm-thick buffer layer is composed of 100-nm GaSb and 50-nm AlSb, with the AlSb on top. The buffer layer of sample B (Fig. 1B) is a 50-nm AlSb that is sandwiched in between two 50-nm GaSb layers, so that the uppermost part of the buffer layer is GaSb, rather than AlSb; the thickness is held constant. The third sample (A') is similar to sample A, but with a 250-nm-thick AlGaSb layer lying beneath the sample A buffer layer. In all samples, a four-monolayer-thick (~ 1.2 nm) InAs wetting layer (not shown in the schematic) is added directly below the Cd_3As_2 film to facilitate (001) growth (19). Purely 2D transport has been demonstrated in films ranging from about 10 to 50 nm, across a wide range of carrier densities (11, 12, 19). The thickness of the Cd_3As_2 layer in each of these films is about 45 nm (see Materials and Methods), where we thus expect the bulk to be insulating.

Capacitors are fabricated on these structures, as shown in Fig. 1 (C to J). The result is a circular parallel plate capacitor with a metal top plate separated from a Cd_3As_2 bottom plate by an Al_2O_3

dielectric layer. Note that the mesa isolation (Fig. 1, E and F) involves etching past the bottom of the Cd_3As_2 film, and so, contacts are made to both the top and bottom surfaces of the Cd_3As_2 film (Fig. 1, I and J). Details about sample growth and device fabrication can be found in Materials and Methods.

Figure 2 shows different low-field $C(V)$ traces for sample A (Fig. 2A) and sample B (Fig. 2B) at different temperatures. Both traces have qualitatively the same shape. The pronounced dip at negative bias is asymmetric: The negative bias side of the dip rises more steeply than the positive bias side. The capacitance levels out on both ends, but the apparent asymptotes are different on either side of the dip. The bias voltage at which the dip occurs is device—rather than sample—dependent, even in devices on the same sample showing otherwise identical characteristics (see fig. S1), and so, we draw no conclusions about its value across different devices.

As a function of temperature, the $C(V)$ traces hardly change. The main correction is an increasing background level. This can be seen directly in the right-hand panels (Fig. 2, C and D), which plot the same data as in the corresponding left-hand ones, with the lowest-temperature (1.8 K) $C(V)$ trace subtracted. Besides this flat increase, a small kink appears at a voltage slightly more negative (<0.5 V) than where the dip appears. (In the sample B data, reranging by the bridge produces a square edge at a particular value of C , which produces a

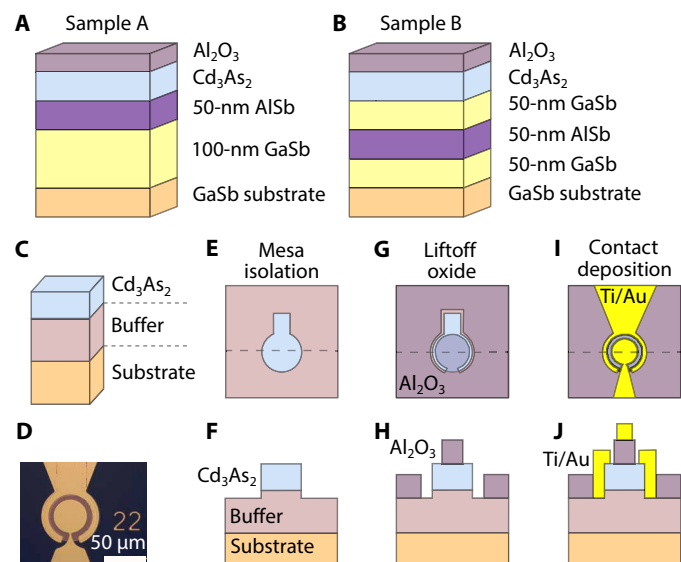


Fig. 1. Heterostructures and devices. (A) Structure of sample A. The thin InAs wetting layer (1.2 nm) is not shown. All layers, except the Al_2O_3 gate dielectric, are deposited in situ. (B) Structure of sample B. Note that 50 nm of AlSb is placed below 50 nm of GaSb. (C) Generic schematic to describe all the samples, color-coded as to aid in the understanding of the remaining panels. (D) An optical microscope image of a device with a radius of 22 μm (central conductor). (E) Schematic of the mesa isolation process. The Cd_3As_2 is overetched. (F) Cross section of the mesa isolation schematic. (G) Plan-view and (H) cross-sectional schematic of the oxide lift-off process. A ring is exposed around the edge of the mesa; an extension of the mesa is fully exposed to increase reproducibility related to mask alignment. (I) Plan-view and (J) cross-sectional schematic of the device after contact deposition. Metal is deposited on the edge of the mesa, which forms the bottom plate of the capacitor, and above the oxide to make the top plate of the capacitor. The final capacitor area is the area under the central metal disk.

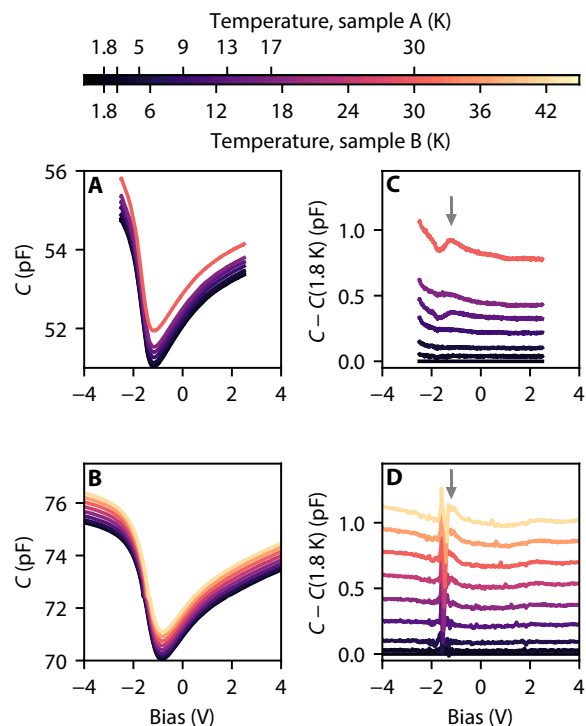


Fig. 2. Temperature dependence of the low-field $C(V)$ for samples A and B. Capacitance measured as a function of dc bias for different temperatures for sample A (A) and sample B (B). The different traces are not offset, and their color corresponds to the temperature, as indicated by the scale at the top. In (C) and (D), the 1.8-K trace is subtracted, and the data are shown for sample A (C) and sample B (D). These data are also not offset. The gray arrows indicate the kink in the capacitance data where the zeroth Landau level develops under the application of the magnetic field. A step-like artifact near 72 pF in (B) is generated by the bridge, which occurs at the same capacitance on both sides of the sweep. In (D), the artifact from (B) falls to the left of the kink.

large, artificial spike directly to the left of this feature in Fig. 2D.) In addition, the capacitance at the most negative voltages increases slightly more than across the rest of the trace. We discuss these features more below, but it is relevant here that the applied test voltage (25 mV root mean square amplitude) smears out fine features in the $C(V)$ trace, preventing the observation of its thermal broadening as the temperature increases.

The addition of a magnetic field is critical to understanding the zero-field $C(V)$ traces, because the effect of Landau quantization on the density of states is distinctive and provides a crucial, independent consistency check of our understanding of the zero-field data. Figure 3 shows capacitance data from three different Cd_3As_2 -based heterostructures. Figure 3A shows $C(V, B)$ data from sample A. To better visualize the quantum oscillations, Fig. 3B shows the same data, with the low-field capacitance subtracted at each voltage step, $\delta C = C(V, B) - C(V, B < 1 \text{ T})$. Here, $C(V, B < 1 \text{ T})$ is the average value of the capacitance for each voltage point at $0 < B < 1 \text{ T}$, i.e., what is plotted in Fig. 2 (A and B), because the dip feature discussed above dominates the color scale. The same two plots are shown for sample A' (Fig. 3, C and D, respectively) and sample B (Fig. 3, E and F).

The subtracted data are similar for the three samples. The Landau level spectrum is not a single dispersing fan of states at a single fulcrum. This is apparent from features that appear as branching for some Landau levels; others appear to be interleaved. There is also a complex hierarchy in how distinct some of the levels appear, with some streaks that are more intense than their neighbors. Qualitatively, this is consistent with the picture developed elsewhere that two separate sets of states, offset in energy and residing on the bottom and top surfaces, respectively, generate the Landau level spectrum (11, 12).

A large horizontal level is visible in each plot of the subtracted data and obscured in the full data. It is central to the discussion below that this level in δC does not coincide with the minimum of the measured capacitance C , as can be directly verified by inspection of Fig. 3. Rather, it appears on the negative bias side of the dip. We

discuss this level, which we identify as a zeroth Landau level, in more detail below.

Last, a notable feature of these data is the extreme similarity of the Landau level spectrum in samples A and A' and the difference with that of sample B. As indicated in Fig. 3, differences include the relative spacing between the nondispersing (horizontal) Landau level and the pair of levels above it; note as well that the apparent high-field pairing of some of the levels is likewise preserved between Fig. 3 (B and D) but not Fig. 3F. These points are discussed in more detail below.

DISCUSSION

The zeroth Landau level

Why does the zeroth Landau level not appear at the global minimum of the capacitance? For comparison, in the compensated 3D topological insulator BiSbTeSe_2 , the zero- B capacitance looks very similar to that shown in Fig. 2 (A and B), but the zeroth Landau level appears as a peak that develops at or very near the center of the dip feature (20, 21). The same is true for graphene (22), and more broadly is an obvious consequence of Eq. 1, because the Dirac point corresponds to a minimum of the density of states, and that is the energy where we find the zeroth Landau level.

Here, the crucial difference is that we see contributions from states on both (001) surfaces of the Cd_3As_2 film (top and bottom). Critically, when the surfaces are separated by an insulating 3D bulk, the separate contributions of each surface can be distinguished by the capacitance measurement. That is, in the band structure schematized in Fig. 4A, it is possible to identify the top and bottom states. To see this, consider the situation where two fans originate from the same confined well or interface. This gives a different result, where the quantum capacitance of the whole system is the parallel sum of the quantum capacitance of each state, i.e., $C_q = C_{q,1} + C_{q,2}$, where $C_{q,(1,2)} = A e^2 D_{(1,2)}(E)$, with $D_{(1,2)}(E)$ being the density of states for either state and A being area of the parallel plate capacitor. This

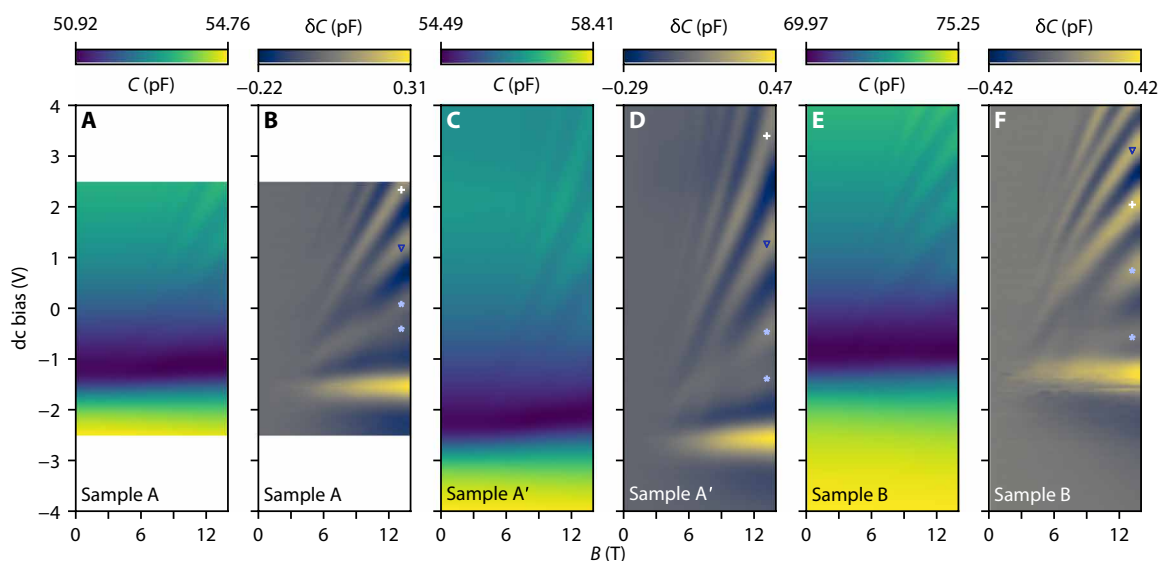


Fig. 3. Measured Landau level spectra for samples A, A', and B. Capacitance data as a function of magnetic field and dc bias voltage for sample A (A and B), sample A' (C and D), and sample B (E and F). For each sample, the right panels (B, D, and F) show the same data, but with the low-field capacitance subtracted. The scales are shown above the plots. The Landau levels indicated with symbols (*, +, and ∇) are referred to in the main text.

situation, whose equivalent circuit is shown as model 1 in Fig. 4B, is not observed, as discussed below. Note that model 1 is also hard to rationalize: It would amount to saying that the electric field in the bulk of the film has the same value as in the Al_2O_3 dielectric. More sensibly, we can model the full capacitance as a series-wise reduction of the geometrical capacitance between the top electrode and

the top surface state (C_{tg}) by the quantum capacitance of the top surface state (C_{qt}). C_{qt} is itself in parallel with the series-wise reduction of the geometrical capacitance due to the insulating bulk of the Cd_3As_2 film (C_{tb}) by the quantum capacitance of the bottom surface state (C_{qb}). The result is shown as model 2 in Fig. 4B (17). (Further rationalization for model 2 is shown in fig. S3.) The resulting capacitance is

$$C = \left\{ C_{\text{tg}}^{-1} + \left[C_{\text{qt}} + (C_{\text{tb}}^{-1} + C_{\text{qb}}^{-1})^{-1} \right]^{-1} \right\}^{-1} \quad (2)$$

Note that the potential on the right side of the equivalent circuit is held to be the same by the low contact of the capacitor.

We seek to understand why only one of the “per surface” zeroth Landau levels is prominent and why the minimum of the $C(V)$ trace does not fall in the same place. For the moment, we take the Dirac node of the top surface to be at lower energy, assuming that its zeroth Landau level should be easier to observe. (The analysis is repeated for the opposite situation in figs. S4 and S5.) Besides the two-surface model of the capacitance (model 2, shown in Fig. 4B), we find two more ingredients that are necessary for understanding the data. One is that the Fermi velocities on each surface must differ, as is expected where, as here, the interfaces are affected by materials with different bandgaps and chemical potentials (23). The second, and a main finding, is that, when the Fermi velocity on the top surface is not higher than that on the bottom surface, the global minimum of the capacitance falls at an energy identified with the Dirac node of the bottom surface. The reasoning is shown in Fig. 4 (C to K). The left column shows the per surface and total density of states for a 3D topological insulator with its 2D Dirac cones, one per surface, at different energies. The middle column shows the resulting capacitance in three configurations: Model 1 takes into account only the top gate dielectric, and the quantum capacitance contribution is simply the sum of the density of states on each surface; model 2 is calculated using Eq. 2. Model 2 traces shown are for slightly different thicknesses of the oxide and Cd_3As_2 layers, respectively. The right column is the same as the center column, but the density of states has been subjected to Gaussian broadening, which can arise because of disorder, and is not unusual in quantum oscillation measurements (24), but here also accounts for the nonnegligible oscillating test voltage we apply in the bridge measurement (see Materials and Methods). Each row of the figure corresponds to different relative values of the Fermi velocity. In Fig. 4 (D, E, J, and K), but not Fig. 4 (G and H), the global minimum of the capacitance appears at the energy of the bottom surface Dirac node, and the top surface Dirac node lies to the negative energy side of the dip, partway up the slope. Crucially, this is consistent with what we observe in Fig. 3, where the nondispersing zeroth Landau level consistently appears to the negative bias side of the large dip in the capacitance.

Supporting evidence comes from the temperature dependence shown in Fig. 2. As discussed above, besides the flat background that increases with temperature, there is a kink that develops at negative bias with increasing temperature. This kink is at the bias where we observe the zeroth Landau level. Last, the identification of the horizontal feature as a Landau level is also consistent with the increasing density of states as a function of field (see the Supplementary Materials), further supporting the two-surface model, model 2.

Last, note that a conductive bulk is inconsistent with these data, even without the supporting evidence of transport (11, 12, 19). We expect a weakly conducting, disordered bulk to have a more marked

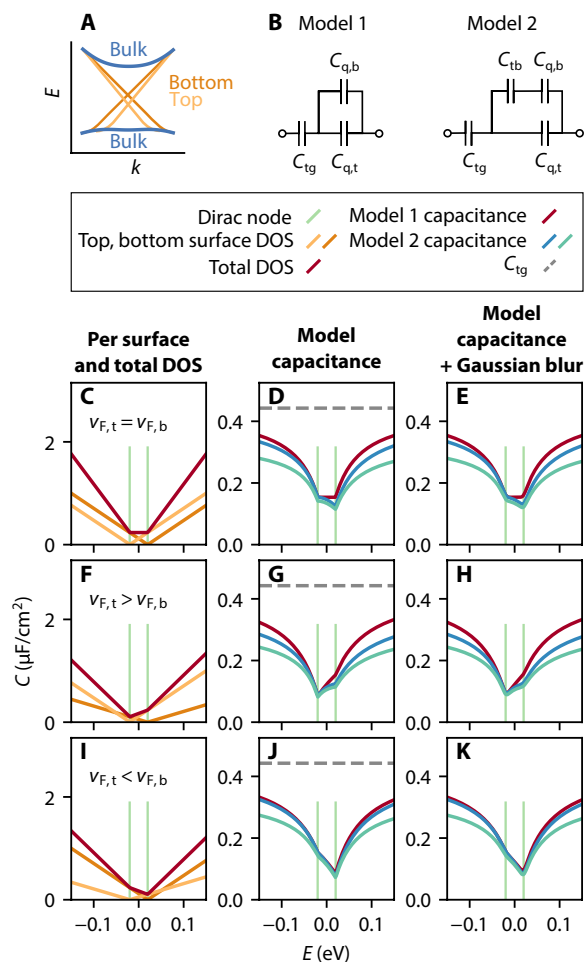


Fig. 4. Modeling two different surfaces that contribute separately to the total capacitance. (A) Schematic band diagram. Two surface states, one on each surface, lie between the bulk bands, and their Dirac nodes are at different energies. (B) Circuit diagrams for models 1 and 2. The Dirac node for the top surface is in all cases placed at a lower (negative) energy, while the bottom surface Dirac node is placed at a higher (positive) energy (the opposite situation is shown in fig. S4). (C) The density of states calculated for two Dirac cones, one on each surface, and their sum. The energy of each cone is indicated with a vertical line in all the panels. The Fermi velocity is set to 10^6 m/s on each surface. The density of states is shown in units of capacitance, i.e., as $C = e^2 D(E)$, to have the same units as the other panels. (D) The capacitance calculated for this situation using model 1 (red, symmetric trace) and model 2 (blue traces). We use the parameters $\epsilon_r = 10$ for Al_2O_3 and $\epsilon_r = 30$ for Cd_3As_2 . The two model 2 traces are shown for different thicknesses: 20-nm Al_2O_3 , 40-nm Cd_3As_2 (darker blue) and 25-nm Al_2O_3 , 45-nm Cd_3As_2 (lighter blue). A dashed horizontal line indicates the gate capacitance (20-nm Al_2O_3), which we use for model 1 as well. (E) Same as (D), but after convolution of the density of states with a Gaussian with a width parameter of 4 meV. (F to H) The same panels as the row above, but with the Fermi velocity on the top surface $v_{F,t} = 1.5 \times 10^6$ m/s and the Fermi velocity on the bottom surface $v_{F,b} = 10^6$ m/s. (I to K) The same as the above row, except $v_{F,t} = 10^6$ m/s and $v_{F,b} = 1.5 \times 10^6$ m/s.

dependence on temperature and bias voltage than we observe, as more impurity states lying within the bandgap are activated.

The bottom surface

The preceding paragraphs describe why the nondispersing zeroth Landau level for the top surface lies away from the global minimum of the $C(V)$ trace, but what about the nondispersing Landau level of the bottom surface? From the above discussion, we know that it is at higher energy than the strong zeroth Landau level feature in the data. We also know that it should fall at or very near the global minimum of the capacitance. Here, we show that the suppression of the bottom surface capacitance may render this Landau level invisible. Figure 5 shows schematic Landau level spectra, using plausible parameters for $v_{F(t,b)}$ and a large energy difference between the two nodes, as in Fig. 4, to better illuminate the discussion. The top two panels, Fig. 5 (A and B), have also had a similar subtraction procedure performed as for the data shown in Fig. 3. With no background density of states and no bulk effects, the difference between model 1 (Fig. 5A) and model 2 (Fig. 5B) can be seen by eye and is most pronounced for the nondispersing Landau level on each surface. The line cut at 15 T (Fig. 5C) reveals the suppression of the bottom surface Landau level versus the top surface one. With a smaller energy separation between the Landau levels, the ability to distinguish them disappears.

The combination of this analysis with the zero-field behavior of the capacitance models (Fig. 4) allows us to identify model 2, and not model 1, as consistent with the data, with the energy of the Dirac node of the bottom surface higher than that of the top surface, and the Fermi velocity on the top surface equal to or lower than the Fermi velocity on the bottom surface, i.e., $E_{D,t} < E_{D,b}$ and $v_{F,t} \leq v_{F,b}$. A similar analysis, assuming $E_{D,b} > E_{D,t}$, is shown in the Supplementary Materials (figs. S4 and S5). In that case, while some of the zero-field traces are consistent with the zero-field data, none are then consistent with the relative prominence of the right zeroth Landau level.

Bulk effects

There is minimal thermal activation of the bulk bandgap, as is clear from the weak temperature dependence of the $C(V)$ traces in Fig. 2. This is in contrast to recent results in the 3D topological insulator

BiSbTeSe₂, in which suppression of the bulk conductivity is achieved by charge compensation of the bulk, which gives rise to a complicated temperature dependence involving nearly immobile spatial charge fluctuations (20). Here, the bulk is mostly featureless: Besides a nearly flat increase in a background density of states (unaffected by the bias voltage), the temperature dependence of the low-field $C(V)$ trace is unremarkable, even to such high temperatures as 42 K. This is consistent with the Cd₃As₂ 3D bulk having a sizeable gap that is much larger than band structure calculations (1, 10) predict. A thermal mismatch strain is one possible explanation for the existence of a relatively large gap in thin films. From these data, we can estimate the size of the bulk bandgap using the spacing of the Landau levels assuming that the carrier cyclotron mass is $0.03m_e$, where m_e is the bare electron mass (3): At 10 T, 1-V gate bias tunes 40 meV. If surface states are visible across less than approximately 6 V of bias, we estimate an approximate upper bound for the bulk bandgap of 240 meV.

The other bulk effect of note is the suppression of the hole-like Landau levels at energies lower than the zeroth Landau level. The absence of these Landau levels suggests that the p-type carriers are much more massive and have much lower mobility than the n-type carriers. These more massive p-type carriers have elsewhere been ascribed to the Cd₃As₂ bulk (25), and their increasing relevance at high negative bias is one explanation for the disappearance of the Landau levels.

Controlling the Dirac node using molecular beam epitaxy

It has been argued (11, 12) that a key experimental parameter in determining the energy of Dirac nodes of the topological surface states and, as a result, the full Landau level spectrum in a (001) Cd₃As₂ film is the band alignments on either side of the junction. The importance of the band alignment was first pointed out for related systems such as the inverted PbTe/SnTe system (26, 27), now understood as a topological crystalline insulator (28), and, more recently, in strained HgTe films (23, 29, 30). In our (001) Cd₃As₂ films, the bottom and top interfaces are dissimilar: The bottom interface is with a compound semiconductor, and the top interface is an amorphous insulator. The differences between the Landau level spectra in Fig. 3 (E and F) versus those in Fig. 3 (A to D) are then due to the different band offsets of the underlying GaSb (samples A and A') and AlSb (sample B) layer, as discussed next.

The reproducibility of the measured spectra between devices and samples is high. The Landau level spectra across devices on the same sample are, up to measurement noise and an offset in the voltage scale, identical (see fig. S1). In the same vein, samples A and A', on which devices were fabricated in different process runs and which have slightly different structures (sample A' has the same buffer layer as sample A, plus an insulating spacer at the bottom of the stack), show identical or nearly identical Landau level spectra [compare Fig. 3 (A and B) with Fig. 3 (C and D)]. Features that differ across the samples are (i) the voltage offset, i.e., the position of the global minimum of the capacitance with respect to the bias voltage, and (ii) the apparent curvature of the Landau levels, which we ascribe to hysteretic effects related to the voltage sweep direction (see Materials and Methods).

We turn our attention to differences between the Landau level spectrum of sample B (Fig. 3, E and F) and samples A and A'. One clear difference is the proximity of the first dispersing Landau level relative to the nondispersing one. In samples A and A', the level is paired with the higher one, whereas in sample B, it lies appreciably

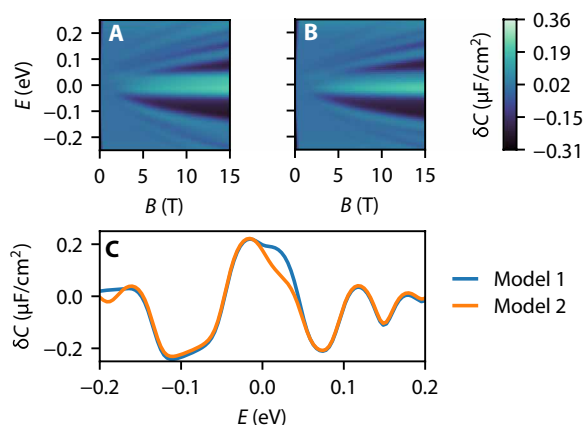


Fig. 5. Model comparison in a magnetic field. The Landau level spectra are calculated using model 1 (A) and model 2 (B). The capacitance has undergone the same low-field subtraction procedure as the data in Fig. 3. In these plots, $v_{F,t} = 1 \times 10^6$ m/s and $v_{F,b} = 1.5 \times 10^6$ m/s. (C) Line cut at 15 T showing the suppression of the zeroth Landau level on the bottom surface.

lower in energy. The two Landau levels above the nondispersing level are indicated (with an asterisk *) in Fig. 3 (B, D, and F). Second, the next level up (indicated with a +) is more prominent in sample B than in samples A and A'; the opposite is true of the next one up (indicated with a ∇). This alternation then continues for the next several Landau levels and suggests a shift by approximately one Landau level of the whole spectrum, caused by the Dirac node at the $\text{Cd}_3\text{As}_2/\text{InAs}/\text{AlSb}$ interface lying closer in energy to the Dirac node at the $\text{Cd}_3\text{As}_2/\text{Al}_2\text{O}_3$ interface than does the Dirac node at the $\text{Cd}_3\text{As}_2/\text{InAs}/\text{GaSb}$ interface.

Band offset tuning, and, thus, Dirac node engineering, should be possible on either interface. The primary concern on the top interface is reducing interfacial trap densities at the oxide/ Cd_3As_2 interface (31). In addition, deposition of layers is constrained by the thermal stability of Cd_3As_2 . By contrast, the bottom interface can be tuned extremely reliably, because Cd_3As_2 can be grown on a wide range of different buffer layers and substrates, including the III-V and II-VI alloy systems (19, 32–34).

MATERIALS AND METHODS

Sample growth

Thin (001)-oriented Cd_3As_2 films were grown by molecular beam epitaxy, following a scheme discussed in more detail elsewhere (19). On a Te-doped GaSb (001) substrate, following a thermal oxide desorption under Sb flux, a III-Sb buffer layer was grown, whose composition varies across samples A, A', and B. A thin InAs wetting layer, which has been shown to facilitate smooth (001) Cd_3As_2 film growth (19), intervenes before the growth of the Cd_3As_2 layer, which is performed at low temperature (<200°C on the sample manipulator thermocouple) and high flux ($>2 \times 10^{-6}$ torr on a flux monitoring ion gauge), supplied from two molecular sources. The Cd_3As_2 film thickness of samples A, A', and B was determined by cross-sectional transmission electron microscopy to be 42, 46, and 41 nm, respectively.

Device fabrication

Devices were defined using a conventional photolithography process. First, a mesa for each device was etched using Ar ion milling. The mesa was disk-shaped with a rectangular extension to increase the contact area for the metal layer. Overetching poses no problems because of the insulating buffer layer. Next, a thin Al_2O_3 layer was deposited via atomic layer deposition at low temperature (120°C), which served as the capacitor dielectric. The oxide was lifted off the edge of the circular mesa, plus the entire rectangular extension region, minus a thin bridge that served for routing the capacitor top plate to a pad for wire bonding. Last, metal contacts (Ti/Au) were deposited using electron beam evaporation. One disk defined the top plate of the capacitor, and contact to the bottom plate was made through the exposed annular region on the edge of the mesa. In transmission electron microscopy, the oxide thicknesses of samples A, A', and B were found to be 21, 25, and 23 nm, respectively.

Capacitance measurements

Measurements of the capacitance as a function of voltage bias, magnetic field, and temperature were performed in Quantum Design Physical Property Measurement System DynaCool equipped with a 14-T magnet, using a purpose-built sample platform consisting of a shielded canister, into which coaxial cables were routed, allowing the shielding of the cables to continue and enclose the entire capacitor.

A 25-mV ac test voltage from an Andeen-Hagerling 2700A capacitance bridge, transmitted on the pins of two cables, was patched from the feedthroughs on the enclosure to the capacitor plates. The measurement frequency was chosen between 5 and 10 kHz as a trade-off between the loss measured on the bridge and measurement speed. A dc voltage bias across the plates was supplied by a Keithley 2400 SourceMeter and swept during the experiment. This maximally shielded configuration enabled the bridge circuit to more accurately reject the parallel capacitance between each pin, i.e., the capacitor high or low, and its corresponding (grounded) shield. Thermalization of the sample was not problematic down to 1.8 K, the lowest temperature achieved here. The shielded enclosure was screwed onto a Quantum Design universal sample puck, and the sample substrate was in thermal contact with the enclosure via the wire leads. Furthermore, at 1.8 K, the sample sat in approximately 500 mtorr of ^4He gas, which allowed for thermal exchange with the cold isothermal region at the bottom of the cryostat. Nevertheless, our practice was to allow for more than 20 min of equilibration time following a change of temperature.

The plots in Figs. 2 and 3 were acquired by setting the magnetic field and sweeping the bias voltage from zero to one end of the sweep range, sweeping back to the opposite end, and sweeping back to zero and then stepping the magnetic field and repeating. The data shown are from the long sweep; the sweep direction was different for sample A' relative to the other two samples. Some hysteresis was present in the gate, although all qualitative features are present in both sweep directions. The main feature that differs between the sweep directions, besides a voltage offset, is an artifact that appears as a curvature of the Landau levels in Fig. 3: This is why the Landau levels appear to drift slightly upward in Fig. 3 (C and D) and downward in Fig. 3 (E and F). Note that, for the smaller voltage sweep range shown in Fig. 3 (A and B), the effect is much reduced.

Capacitance data processing

The data from the long sweep were binned at each voltage set point in the sweep (e.g., 10 mV)—the bridge acquires data continuously—and averaged in each bin. The data were then subjected to smoothing by a moving average along the B axis. The plotting routine for Fig. 3 involved a bilinear interpolation of the color at each pixel. To perform the subtraction, the $B < 1$ T data are averaged along the B axis and subtracted from the smoothed data. The data plotted in Fig. 2 are these low-field average data, i.e., what is subtracted from the subtracted data.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at <https://science.org/doi/10.1126/sciadv.abn4479>

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Acknowledgments: We thank A. Suslov for helpful discussions about probe design and P. Perez for work on the first iteration of the apparatus. A portion of this work was performed at the UCSB Nanofabrication Facility, an open access laboratory. **Funding:** This work was supported by the U.S. Department of Defense through the Vannevar Bush Faculty Fellowship program (grant no. N00014-16-1-2814). Additional support (to R.K.) was provided by the CATS Energy Frontier Research Center, which is funded by the Department of Energy, Basic Energy Sciences, under contract DE-AC02-06CH11357. The microscopy work was supported by the U.S. Department of Energy (grant no. DEFG02-02ER45994). T.N.P. acknowledges the U.S. National Science Foundation Graduate Research Fellowship Program for support (grant no. 1650114). This research made use of shared facilities of the UCSB MRSEC, which is supported by the National Science Foundation (grant no. DMR 1720256). **Author contributions:** Experiments were performed by D.A.K. and R.K. D.A.K. and R.K. analyzed the data. D.O. assisted in the construction of the capacitance probe. T.N.P. carried out the transmission electron microscopy study. D.A.K. wrote the manuscript, and all authors commented on it and/or edited it. S.S. supervised the project. **Competing interests:** The authors declare that they have no competing interests. **Data and materials availability:** All data needed to evaluate the conclusions in the paper are present in the paper and/or the Supplementary Materials. Additional data related to this paper are available at <https://doi.org/10.5281/zenodo.6610055>.

Submitted 26 November 2021

Accepted 25 May 2022

Published 8 July 2022

10.1126/sciadv.abn4479