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Silicon-organic hybrid slot waveguide based three-input multicasted optical hexadecimal addition/subtraction

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By exploiting multiple non-degenerate four-wave mixing in a silicon-organic hybrid slot waveguide and 16-ary phase-shift keying signals, we propose and simulate three-input (A, B, C) multicasted 40-Gbaud (160-Gbit/s) optical hexadecimal addition/subtraction (A + B − C, A + C − B, B + C − A, A + B + C, A − B − C, B − A − C). The error vector magnitude (EVM) and dynamic range of signal power are analyzed to evaluate the performance of optical hexadecimal addition/subtraction.

Optical signal processing is regarded as an important technique for next-generation high-speed optical networks. Optical nonlinearities are promising candidates to enable various optical signal processing functions, such as logic gate, switching, (de)multiplexing, and coding/decoding[1]. Previously, optical binary logic gates were reported in various platforms for on-off keying (OOK) and phase-shift keying (PSK) formats, including highly nonlinear fiber (HNLF), semiconductor optical amplifier (SOA), periodically poled lithium niobate (PPLN) waveguide, chalcogenide (As_2S_3) waveguide, and silicon waveguide[2–4]. With unabated exponential growth of data traffic, advanced multi-level modulation formats become of great importance to increase the capacity and spectral efficiency of communication systems. In addition, multi-level modulation formats with multiple constellation points in the I/Q plane can be used to represent high-base (quaternary, octal, hexadecimal) numbers. Hence, there might be interest to enable optical signal processing for high-base numbers using multi-level modulation formats, e.g., m-ary quadrature amplitude modulation (m-QAM) and m-ary phase-shift keying (m-PSK). Recently, we demonstrated optical computing and coding/decoding for high-base numbers using HNLFs with length longer than 100 m[5–8]. Driven by the trend of large-scale integration, it is highly desirable to perform these functions using compact devices. The promising compact devices include high-index-contrast silicon waveguide, slot waveguide, surface plasmon polariton (SPP) waveguide, hybrid slot waveguide, and hybrid plasmonic waveguide. Using hybrid slot guiding mechanism (hybrid SPP and dielectric), hybrid plasmonic waveguides incorporating metallic features were proposed to provide enhanced mode confinement with moderate loss[9–12]. To further improve the loss, long-range low-loss hybrid plasmonic waveguides were also proposed with favorable performance[13–15]. Those hybrid plasmonic waveguides guide the light in the subwavelength nano slot region for highly confined light transport at telecom wavelength. The tight light confinement and enhanced nonlinearity might lead to high-performance optical communications applications such as nonlinear optical signal processing. In addition to hybrid plasmonic waveguides, silicon waveguide is of great interest owing to its compactness and potential for complementary metal-oxide-semiconductor (CMOS) compatibility. Silicon-organic hybrid slot waveguide has recently attracted lots of interest for its capability of confining light in the nano-scale low-index slot region filled with high nonlinear organic material[16,17]. The significantly reduced mode area and enhanced nonlinearity, together with negligible two-photon absorption (TPA) and free-carrier absorption (FCA) of nonlinear organic slot, make silicon-organic hybrid slot waveguide suitable for efficient high-speed optical signal processing[16,17]. However, there has been little research on silicon waveguide based optical signal processing for high-base numbers, e.g., hexadecimal addition/subtraction. Also, multi-input operation (e.g., three-input) of hexadecimal addition/subtraction has not yet been reported so far.

In this paper, we present a silicon-organic hybrid slot waveguide with tight light confinement, enhanced nonlinearity, and reduced TPA and FCA. Using multiple non-degenerate FWM processes and 16-ary PSK (16-PSK), we propose and simulate three-input (A, B, C) multicasted 40-Gbaud (160-Gbit/s) optical hexadecimal addition/subtraction (A + B − C, A + C − B, B + C − A, A + B + C, A − B − C, B − A − C). The error vector magnitude (EVM) and dynamic range of signal power are analyzed for performance evaluation.

Results

Silicon-organic hybrid slot waveguide. Figure 1(a) depicts the 3D structure of a silicon-organic hybrid slot waveguide. It features a sandwich structure with a low-refractive-index PTS [polymer poly (bis para-toluene sulfonate) of 2, 4-hexadiyne-1, 6 diol] layer surrounded by two high-refractive-index silicon layers. The cladding is air and the substrate is silicon dioxide. The typical geometry parameters are as follows: waveguide width W = 250 nm, upper silicon height Hu = 180 nm, lower silicon height Hl = 180 nm, and slot height Hs = 25 nm. The quasi-TM mode distribution and its normalized power density along x and y directions are shown in Figs. 1(b)–(d). One can clearly see the tight light confinement in the nano-scale nonlinear organic slot which also offers high nonlinearity and instantaneous Kerr response without impairments by TPA and FCA. Using finite-element method, we assess the effective mode area and nonlinearity to be 7.7×10^{-14} m^2 and 5500 $w^{-1}m^{-1}$, which can potentially facilitate efficient optical signal processing (e.g., hexadecimal addition/ subtraction).

Concept and principle of three-input hexadecimal addition/ subtraction. Figure 2 illustrates the concept and principle of three-input hexadecimal addition/subtraction. As shown in Fig. 2(a), hexadecimal numbers (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, b, c, d, e, f) are represented by 16 phase levels (0, $\pi/8$, $2\pi/8$, $3\pi/8$, $4\pi/8$, $5\pi/8$, $6\pi/8$, $7\pi/8$, π, $-7\pi/8$, $-6\pi/8$, $-5\pi/8$, $-4\pi/8$, $-3\pi/8$, $-2\pi/8$, $-\pi/8$) of 16-PSK. Three input hexadecimal numbers (A, B, C or −C) are coupled into a silicon-organic hybrid slot waveguide. Multicasted three outputs are achieved carrying hexadecimal addition/subtraction results (A + B − C or A + B + C, A + C − B or A − B − C, B + C − A or B − A − C). As shown in Fig. 2(b), the working principle relies on multiple non-degenerate FWM processes. When three 16-PSK signals are fed into the waveguide, three converted idlers (idler1, idler2, idler3) are generated by three non-degenerate FWM

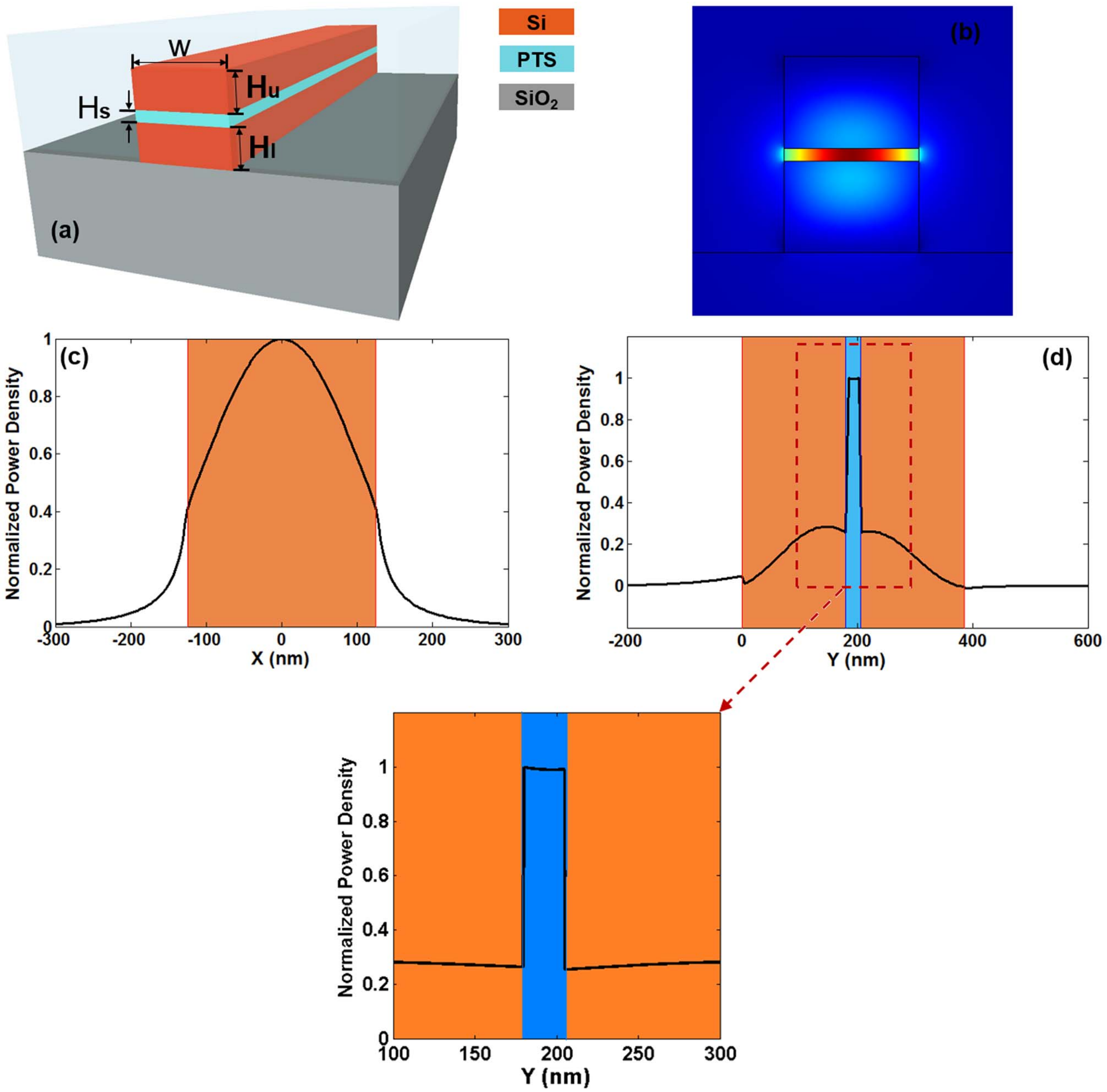

Figure 1 | (a) 3D structure, (b) mode distribution, (c) (d) normalized power density along x and y directions of a silicon-organic hybrid slot waveguide.

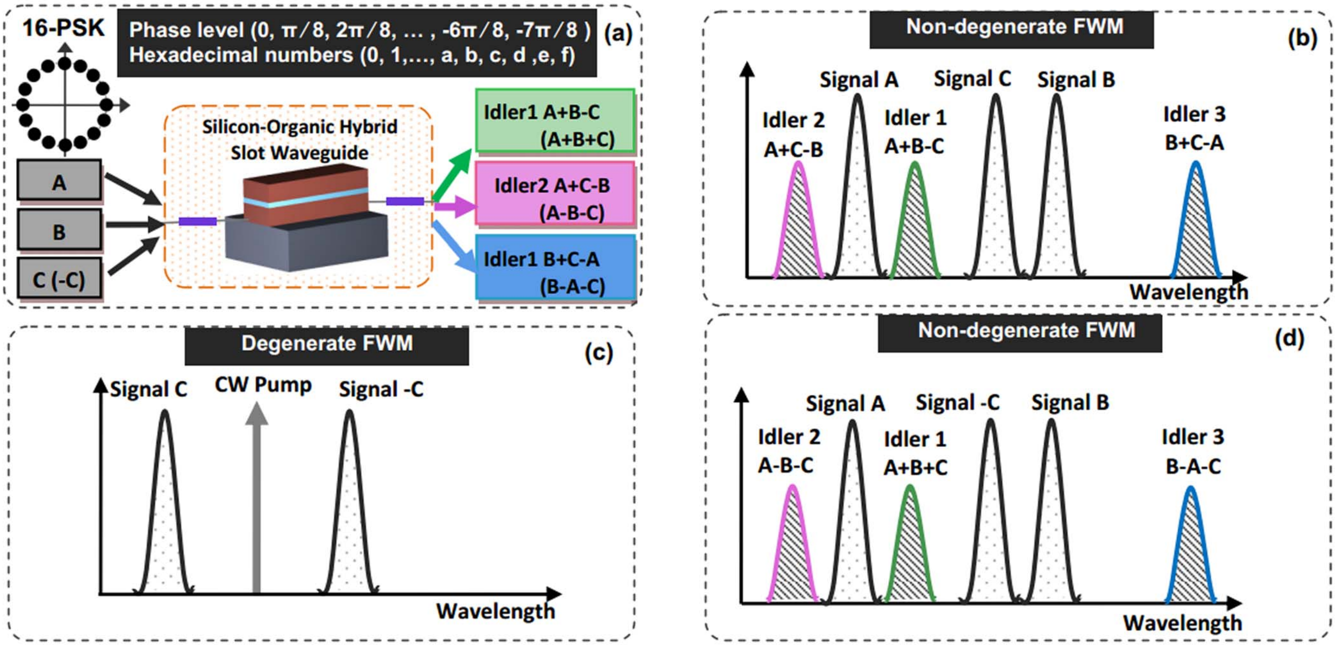

Figure 2 | (a) Concept and (b) (c) (d) operation principle of three-input hexadecimal addition/subtraction.

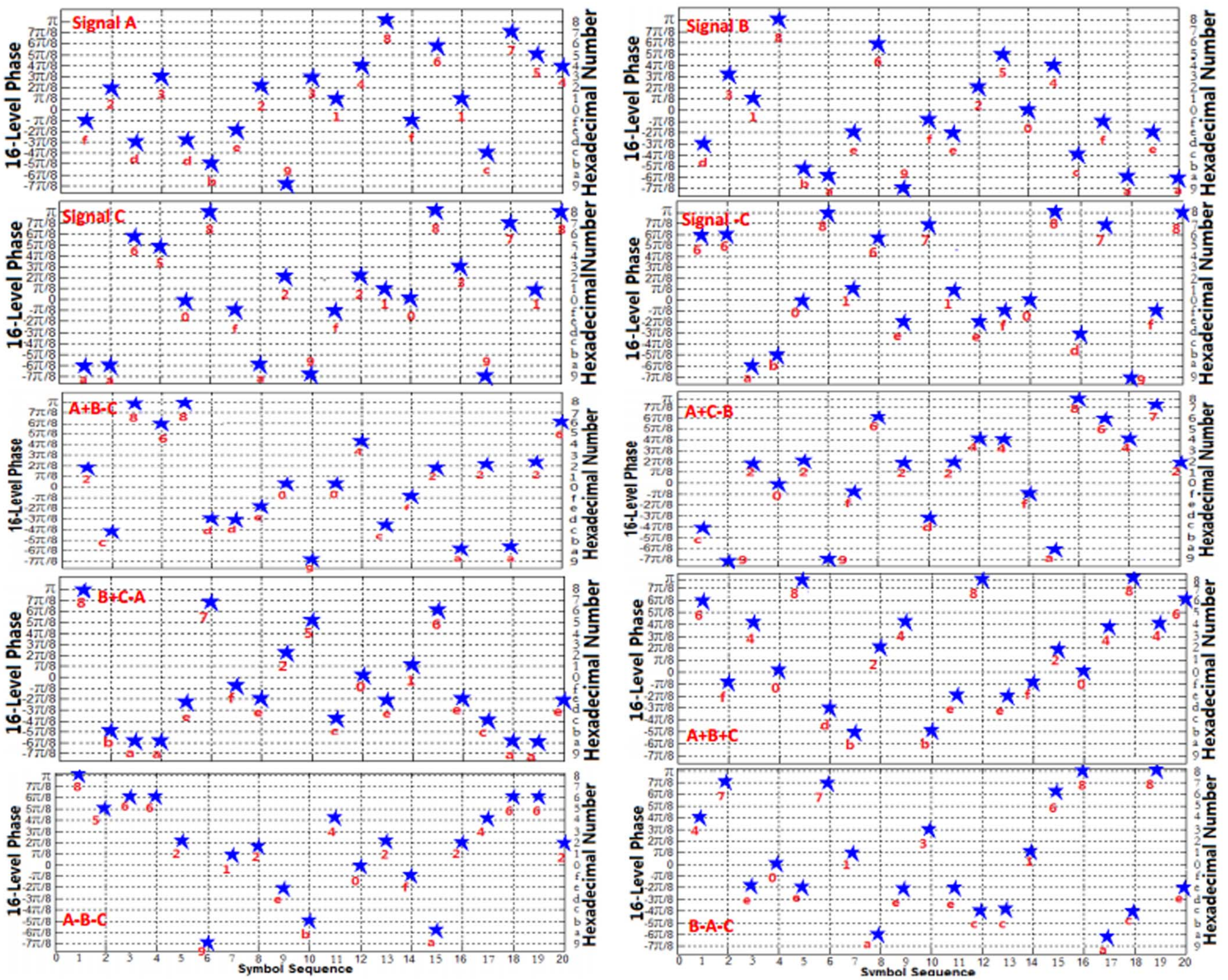

Figure 3 | Simulated symbol sequence for three-input multicasted 40-Gbaud (160-Gbit/s) hexadecimal addition/subtraction using a silicon-organic hybrid slot waveguide.

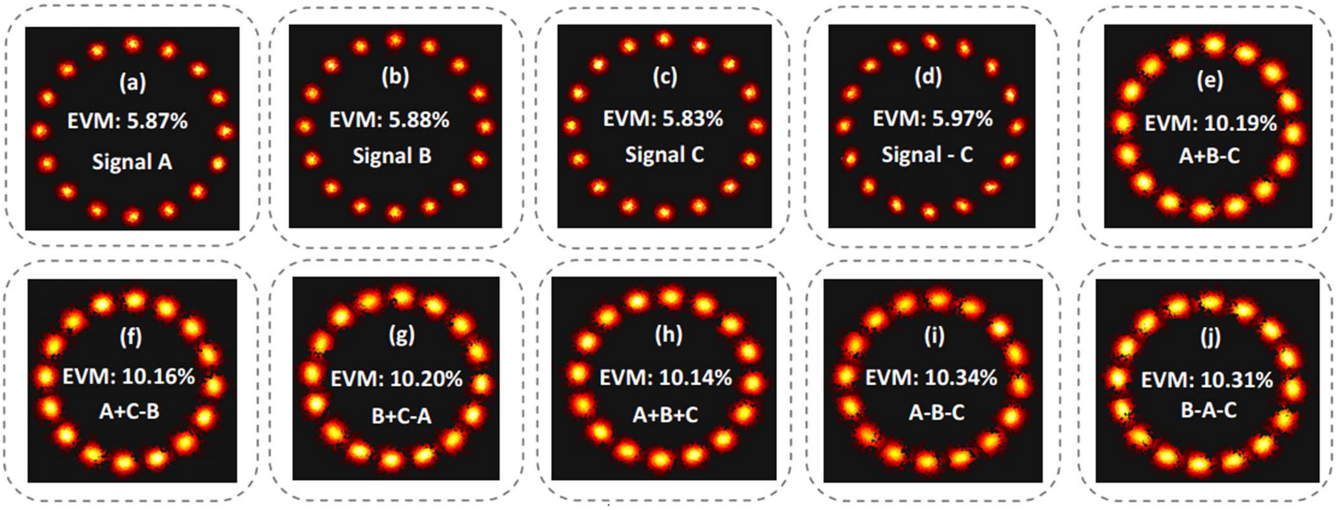

Figure 4 | Simulated constellations for three-input multicasted 40-Gbaud (160-Gbit/s) hexadecimal addition/subtraction using a silicon-organic hybrid slot waveguide.

processes[7]. Owing to the 2π phase wrap characteristic, the linear phase relationships indicate that three converted idlers correspond to module 16 operations of hexadecimal addition/subtraction of A + B − C, A + C − B and B + C − A, respectively. When using A, B and -C as three inputs, where -C is obtained from C through an additional degenerate FWM process in a silicon-organic hybrid slot waveguide, as shown in Fig. 2(c) and (d), multicasted three output hexadecimal addition/subtraction of A + B + C, A − B − C and B − A − C are achieved.

Operation performance of three-input hexadecimal addition/subtraction. The proposed silicon-organic hybrid slot waveguide based three-input hexadecimal addition/subtraction is simulated using nonlinear coupled-mode equations. Group-velocity mismatching (GVM) and group-velocity dispersion (GVD) are considered. In the simulations, three 40-Gbaud 2^{13}-1 pseudorandom binary sequence (PRBS) 16-PSK signals (λ_A: 1546 nm, λ_B: 1552 nm, λ_C: 1550 nm) are adopted. The peak power of three-input signals is 10 mW. A 1-mm long silicon-organic hybrid slot waveguide is employed. The operation performance is evaluated by error vector amplitude (EVM)[18,19].

Figure 3 depicts simulation results for three-input multicasted 40-Gbaud (160-Gbit/s) hexadecimal addition/subtraction. 20-symbol sequences are plotted in Fig. 3, which confirms the successful implementation of three-input hexadecimal addition/subtraction (A + B − C, A + C − B, B + C − A, A + B + C, A − B − C, B − A − C). The constellations are also shown in Fig. 4 with assessed EVM under an optical signal-to-noise ratio (OSNR) of 28 dB for input signals. The observed degradation of EVM for hexadecimal addition/subtraction can be ascribed to the accumulated noise from input 16-PSK signals and impairments from nonlinear interactions inside the silicon-organic hybrid slot waveguide.

We further investigate the EVM of input signals and output idlers against the OSNR of input signals as shown in Fig. 5(a) and (b). The EVM penalties are assessed to be less than 4.5 for hexadecimal addition/subtraction under an OSNR of 28 dB. Figure 6(a) and (b) depict EVM of hexadecimal addition/subtraction as a function of input signal power ranging from 0.1 to 200 mW. Note that EVM increases slightly (<0.8 dB) with input signal power <50 mW, which implies a large available dynamic range (~27 dB) of input signal. EVM rises rapidly as input signal power is larger than 50 mW, which might be ascribed to the impairments from other spurious nonlinear effects beyond non-degenerate FWM inside the silicon-organic hybrid slot waveguide.

Discussion

We present optical hexadecimal addition/subtraction using a silicon-organic hybrid slot waveguide with tight light confinement, enhanced nonlinearity, and reduced TPA and FCA. By employing multiple non-degenerate FWM processes and 16-PSK signals, we simulate and implement three-input (A, B, C) multicasted 40-Gbaud (160-Gbit/s) optical hexadecimal addition/subtraction (A + B − C, A + C − B, B + C − A, A + B + C, A − B − C, B − A

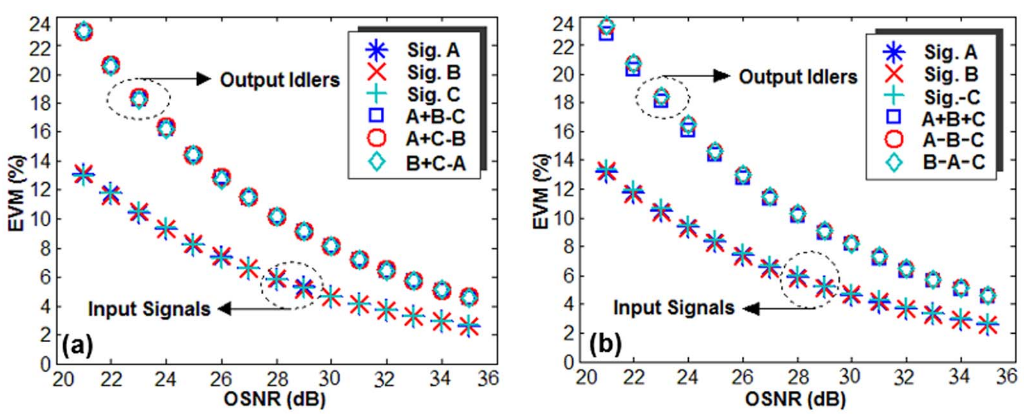

Figure 5 | Simulated EVM vs. OSNR for 40-Gbaud (160-Gbit/s) hexadecimal addition/subtraction using a silicon-organic hybrid slot waveguide.

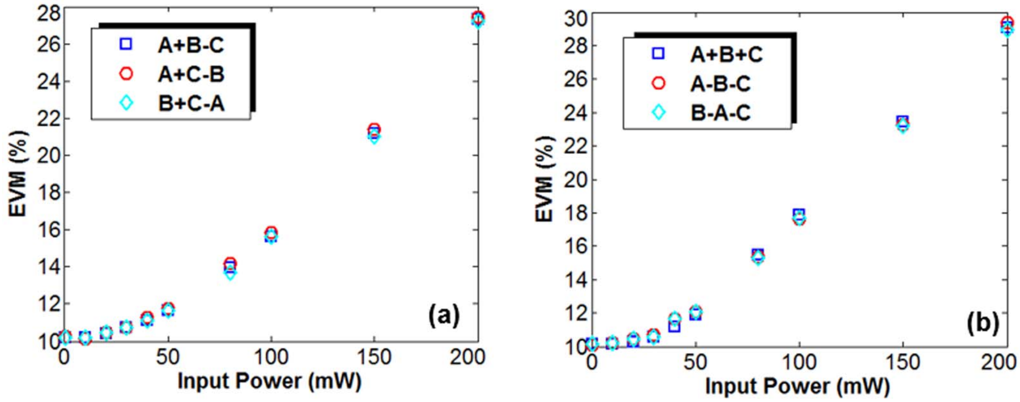

Figure 6 | Simulated dynamic range of signal power for 40-Gbaud (160-Gbit/s) hexadecimal addition/subtraction using a silicon-organic hybrid slot waveguide.

− C). The operation performance is characterized by EVM and dynamic range of signal power. The EVM penalties are evaluated to be less than 4.5 for hexadecimal addition/subtraction under an OSNR of 28dB. The presented optical hexadecimal addition/subtraction features good performance tolerance to input signal power with a large available dynamic range of ~27 dB. With future improvement, other ultracompact devices with even tighter light confinement and higher nonlinearity such as hybrid plasmonic waveguides might also be considered to enable wide highly efficient optical signal processing applications.

Methods

Under the non-depletion approximation, one can derive the electrical field and optical phase relationships of three non-degenerate FWM processes expressed as

$$E_{i1} \propto E_A \cdot E_B \cdot E_C^*, \quad \Phi_{i1} = \Phi_A + \Phi_B - \Phi_C \tag{1}$$

$$E_{i2} \propto E_A \cdot E_C \cdot E_B^*, \quad \Phi_{i2} = \Phi_A + \Phi_C - \Phi_B \tag{2}$$

$$E_{i3} \propto E_B \cdot E_C \cdot E_A^*, \quad \Phi_{i3} = \Phi_B + \Phi_C - \Phi_A \tag{3}$$

According to the linear phase relationships in Eqs. (1)–(3), for three input 16-PSK signals (A, B, C), it is expected that the three converted idlers take module 16 operations of hexadecimal addition/subtraction of A + B − C, A + C − B and B + C − A, respectively. By employing –C instead of C, three converted idlers correspond to module 16 operations of hexadecimal addition/subtraction of A + B + C, A − B − C and B − A − C, respectively.

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Author contributions

J.W. developed the concept and conceived the design. C.G. performed the numerical simulations. C.G. and J.W. analyzed the data. C.G. and J.W. contributed to writing and finalizing the paper.

Additional information

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