Review

Heterogeneous Wafer Bonding Technology and Thin-Film Transfer Technology-Enabling Platform for the Next Generation Applications beyond 5G

Zhihao Ren [1,2,3,†]**, Jikai Xu** [1,2,3,†]**, Xianhao Le** [1,2] **and Chengkuo Lee** [1,2,3,4,*]

1   Department of Electrical & Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117576, Singapore; elerz@nus.edu.sg (Z.R.); e0496474@u.nus.edu (J.X.); elelexia@nus.edu.sg (X.L.)
2   Center for Intelligent Sensors and MEMS (CISM), National University of Singapore, 5 Engineering Drive 1, Singapore 117608, Singapore
3   National University of Singapore Suzhou Research Institute (NUSRI), Suzhou Industrial Park, Suzhou 215123, China
4   NUS Graduate School for Integrative Science and Engineering, National University of Singapore, Singapore 117456, Singapore
*   Correspondence: elelc@nus.edu.sg
†   These authors contribute equally.

Abstract: Wafer bonding technology is one of the most effective methods for high-quality thin-film transfer onto different substrates combined with ion implantation processes, laser irradiation, and the removal of the sacrificial layers. In this review, we systematically summarize and introduce applications of the thin films obtained by wafer bonding technology in the fields of electronics, optical devices, on-chip integrated mid-infrared sensors, and wearable sensors. The fabrication of silicon-on-insulator (SOI) wafers based on the Smart Cut^{TM} process, heterogeneous integrations of wide-bandgap semiconductors, infrared materials, and electro-optical crystals via wafer bonding technology for thin-film transfer are orderly presented. Furthermore, device design and fabrication progress based on the platforms mentioned above is highlighted in this work. They demonstrate that the transferred films can satisfy high-performance power electronics, molecular sensors, and high-speed modulators for the next generation applications beyond 5G. Moreover, flexible composite structures prepared by the wafer bonding and de-bonding methods towards wearable electronics are reported. Finally, the outlooks and conclusions about the further development of heterogeneous structures that need to be achieved by the wafer bonding technology are discussed.

Keywords: heterogeneous integration; wafer bonding; thin-film transfer; System-in-Package (SiP); sensor; 5G; 6G; photonics; power electronics; Internet of Thing (IoT); Artificial Intelligence of Thing (AIoT); wearable electronics

1. Introduction

Wafer bonding is a popular technology that can integrate two or more kinds of materials into one heterogeneous system. It has been successfully applied to system-in-package (SiP) and fabrication of heterogeneous structures [1–7]. Traditional wafer bonding technology is mainly based on silicon (Si)-based materials and is oriented to the microelectromechanical system (MEMS) packaging [8–10]. Due to the high-quality bonding interface, wafer bonding can satisfy meet the strict requirements of MEMS devices in terms of airtightness, bonding strength, and interface corrosion in extreme environments. Combined with the ion implantation, a Smart Cut^{TM} technology (Soitec, Bernin, France), has been proposed and used for the fabrication of high-quality single-crystal thin film onto different substrates. Correspondingly, the application of wafer bonding technology has been dramatically expanded. Among them, Si-on-insulator (SOI) wafers that have been widely used in various electronic products and photonic devices are one of the most

successful commercial cases. The top Si thin film can serve as the functional layer for both electrical and optical designs. With the rapid rise of new energy vehicles, wafer bonding technology of wide-bandgap semiconductors, such as gallium nitride (GaN), silicon carbide (SiC), and gallium oxide (Ga_2O_3), for power electronics is gradually being developed and improved [11–13]. Due to the advantages of being able to transfer high-quality single-crystal thin film without consideration of lattice mismatch, wafer bonding combined with ion implantation or laser irradiation possess more flexible features in the processing and heterogeneous integration of power chips.

Currently, we are on the cusp of communication technology innovation. The development of the fifth-generation (5G) communication technology and alternative communication technologies beyond 5G will affect the technology landscape of countries worldwide. The communication technologies aim to be a revolutionary leap forward in data rates, latency, massive connectivity, network reliability, and energy efficiency [14–17]. Therefore, high data-transmission requirements force a rapid improvement in the performance of terminal products. The arrival of the 5G era is inseparable from the development of radio frequency (RF) front-ends for telecom infrastructure, and the core of the RF front-ends are the filters composed of piezoelectric resonators. Piezoelectric resonators with high electromechanical coupling will improve the performance of the RF front-end, e.g., increase in the bandwidth and reduce the loss. Among the piezoelectric resonators using various structures and piezoelectric materials, the piezoelectric resonator based on lithium niobate ($LiNbO_3$) thin film has a significantly high electromechanical coupling. However, it is currently not possible to achieve the preparation of $LiNbO_3$ film on the substrate/insulator through conventional deposition processes. Exploiting the transfer technique to move a slice of the bulk $LiNbO_3$ and bond to a carrier substrate is the most common and effective method [18,19]. Moving into the era of 5G and beyond 5G, among diversified components and devices that integrate on the chip in the wafer fabrication process, the thin-film $LiNbO_3$ electro-optic modulator has shown outstanding advantages in terms of the speed of information transmission and bandwidth modulation [20]. As for the fabrication of the $LiNbO_3$-on-insulator (LNOI) platform, wafer bonding provides effective technical support for the on-chip heterogeneous integration of $LiNbO_3$ thin film. This idea has been confirmed to be feasible by designing and preparing high-speed modulators on LNOI wafers, which are fabricated using the wafer direct bonding technology to peel off the single-crystal thin film from the bulk $LiNbO_3$ crystals [21,22]. This will be beneficial for the next generation applications beyond 5G communication.

In addition to the above mentioned on-chip integrated applications, thin-film transfer relying on the combination of bonding and de-bonding methods can also be used to fabricate wearable electronics. With the continuous improvement of life quality for human beings, wearable sensors and human-machine interfaces have been considered essential for future multi-functional sensors related to human health [23–28]. However, flexible substrates, such as polydimethylsiloxane (PDMS) and polyimide (PI) cannot tolerate high-temperature treatment. Therefore, functional thin films are difficult to prepare on the flexible substrates without damages by sputtering, evaporation, and deposition methods. One of the most effective solutions is to deposit the targeted film onto the Si substrate cladding with hundreds of nanometers of silicon dioxide (SiO_2). Then, thin films can be transferred onto flexible substrates using the combination of sacrificial removal processes by hydrofluoric acid solution and hot-press bonding processes. Due to the bonding and de-bonding processes compatible with the complementary metal-oxide-semiconductor (CMOS) technology can provide large-scale and stable substrates for subsequent device fabrication. Meanwhile, in the era of big data and artificial intelligence, next-generation wearable sensors will enable human beings to interact with other objects in more and more applications. Driven by such trends, the Internet of Things (IoTs) and artificial intelligence of things (AIoTs) are indispensable considerations for future sensor design and development [29].

In this review, we summarized the high-quality thin films fabricated using wafer bonding technologies and transferred methods in different fields. Divided by materials, we reviewed electronics devices, optoelectronics devices, on-chip integrated mid-infrared sensors, and wearable sensors for communication and sensing applications. The schematic diagram of the article structure is shown in Figure 1. Firstly, we introduce the X-on-insulator platforms fabricated by the Smart Cut^{TM} process, including wafer bonding and ion implantation processes. Additionally, applications of different platforms in the on-chip integration are presented. Secondly, the different wide-bandgap semiconductor thin-film transfer progress based on the wafer bonding methods for high-power electronics is reported. Thirdly, achievements of LiNbO$_3$ thin-film transfer for high-speed electro-optical modulators towards the next generation of communication technology are summarized. Fourthly, film transfer of infrared materials and their applications in molecular sensors are systematically introduced. Finally, we emphasize the methods on the functional thin-film transfer onto flexible substrates for the next generation of wearable sensors, which are related to human health monitoring.
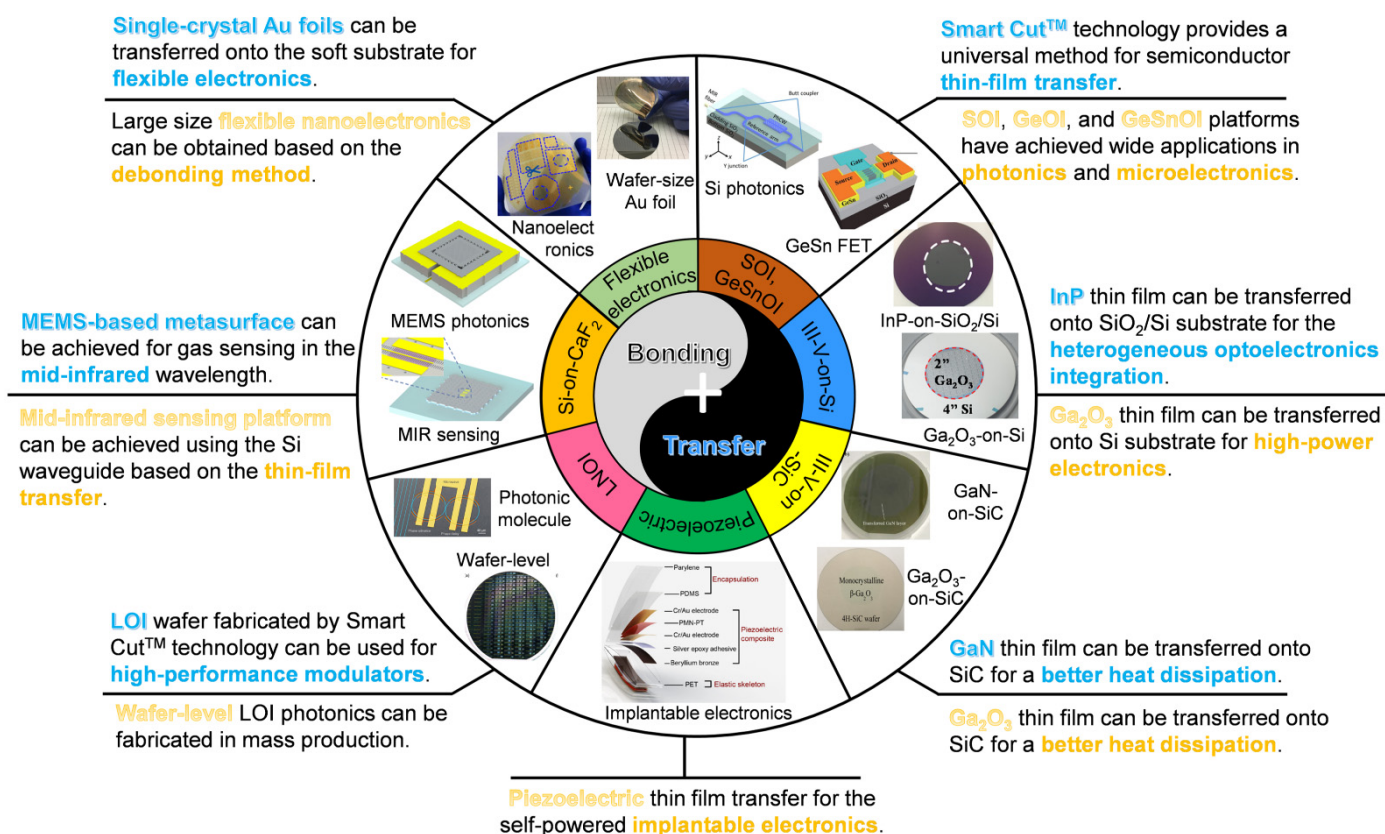

Figure 1. Schematic illustration for the classification of thin-film transfer via bonding methods and their applications in photonics, power electronics, and flexible electronics.

2. Fabrication of Si- and Ge-Based Thin Film-on-Insulators via Wafer Bonding Method

Semiconductors are fundamental for all kinds of photonic and electronic components. They are the basic platform for device design and fabrication. Si- and Ge-based materials are the most popular among numerous semiconductors due to the advances in mature fabrication, low cost, and mass production [30,31]. Therefore, most complementary-metal-oxide-semiconductor (CMOS) process development depends on them. However, the device layers used for active and passive devices are usually nanometer- or micrometer-level in thickness. To avoid signal crosstalk or element diffusion, the insert barrier layer is indispensable between the adjacent device layers. Therefore, the fabrication of Si- or Ge-based thin film on insulators is urgently needed to solve. Although such films can be grown on specific substrates via sputtering, chemical vapor deposition (CVD), plasma-

enhanced chemical vapor deposition (PECVD), and so on, amorphous or polycrystalline crystal structures are challenging to maximize the excellent material performance. A wafer bonding method combined with ion implantation (known as Smart Cut[TM] technology) has been developed [32,33]. This technology makes it possible to transfer a thin layer from a single-crystal donor substrate to the supporting wafer, overcoming physical limitations and changing the face of the substrate industry.

2.1. Smart Cut[TM] Technology for the Fabrication of Si-on-Insulator and Its Applications

Today, most industry-leading Si-on-insulator (SOI) wafers destined for chip manufacturing are made by Smart Cut[TM] technology. The standard Smart Cut process for the SOI fabrication is shown in Figure 2a. Surface oxidation is first applied to both cleaned Si wafers. One of them is used as the supporting substrate, which is used for the thin-film donor wafer. Then, hydrogen ion (H^+) implantation creates a destroyed layer (i.e., bubble layer) on the subsurface. There are several advantages to implant the light element (i.e., H^+) into the donor wafers. The transferred layer can be engineered with no defects. By controlling the implantation energy of H^+, the thickness of the transferred layer can be determined with a high degree of precision. After finishing the ion implantation, the oxidized wafers are bonded together via an activated bonding method. Then, an annealing process is performed on the bonded pairs. On the one hand, the donor wafer will be completely cracked from the bubble layer, making the thin film peel off and remain on the supporting wafer. On the other hand, high-temperature treatment will be beneficial for strengthening the bonding interface between the thin film and supporting substrate. Finally, chemical-mechanical polishing (CMP) is used for flattening and smoothing surfaces to satisfy practical production requirements. For the donor wafers, substrates can be refreshed and reused after each layer transfer operation. The cross-section image of the fabricated SOI wafer is shown in Figure 2b [34]. A dense and sharp interface without any defects can be observed by transmission electron microscopy (TEM), proofing the advantages of Smart Cut technology. We should note that wafer bonding is suitable for a few kinds of materials and a wide range of temperatures, opening the way to enable any thin-film materials onto other substrates while maintaining initial crystallographic properties. For example, Ge is another basic material in the electronics industry [35–39]. GeOI is also an essential platform for high-performance field-effect transistors (FET). Based on the Smart Cut technology, single-crystal Ge thin film can be transferred to other substrates. TEM study indicates that the bonding interface is void-free, as shown in Figure 2c, confirming this process can be applied to the thin-film transfer beyond Si material [40]. Besides, Smart Cut technology is based on standard semiconductor equipment and allows different sizes of products. The thickness of top thin-film layers and buried oxide layers can also be adjusted with substantial flexibility. Moreover, the excellent quality in terms of uniformity, bonding interfaces, and precise control of thickness variability cannot be achieved by other methods. This technology also provides new opportunities for growing and emerging fields, such as sensors, energy harvesting, flexibles electronics, photonics, and MEMS, etc. [41–52].
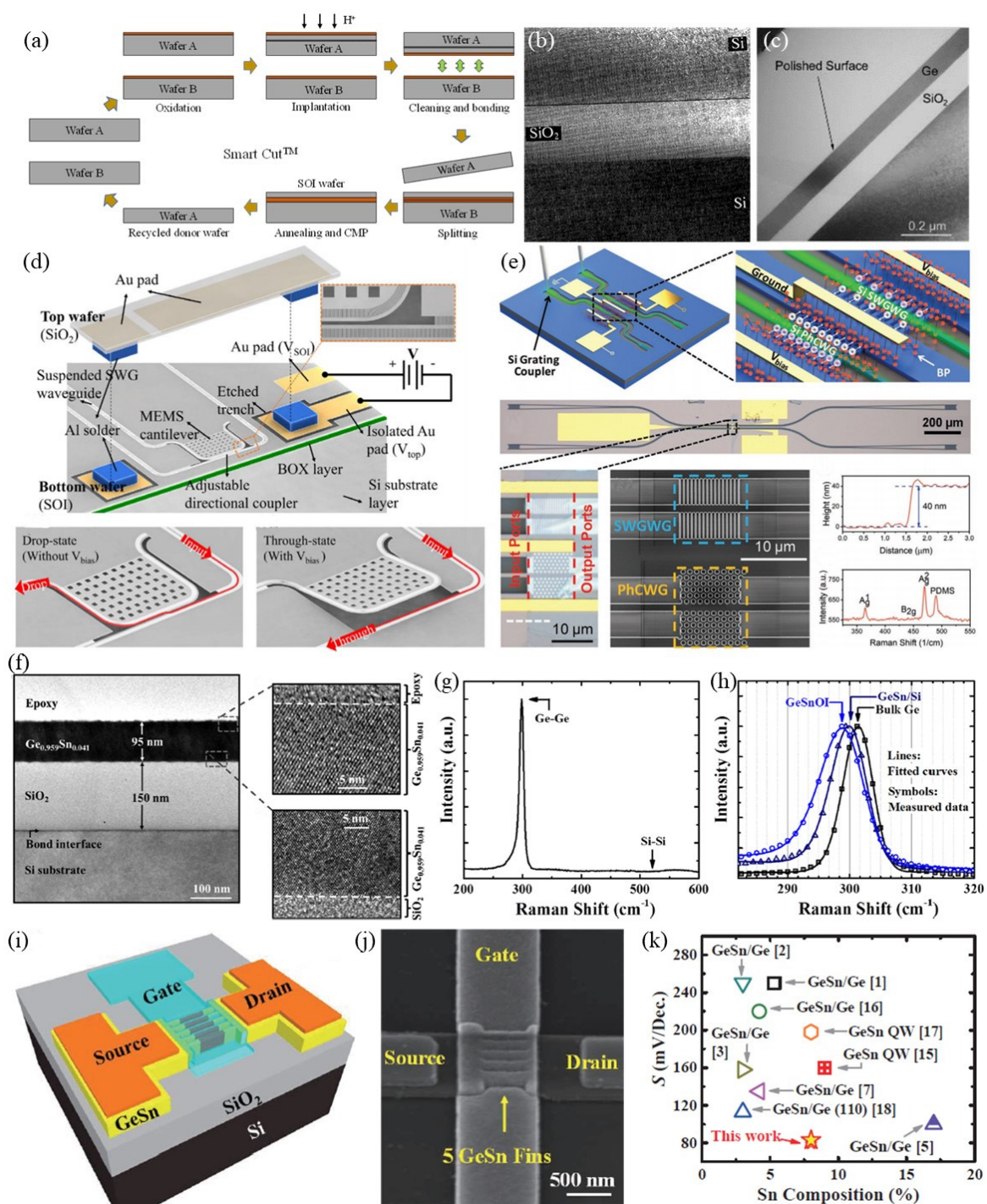
Figure 2. Smart Cut^TM process for the fabrication of SOI, GeOI, and GeSnOI, as well as their applications in photonics and electronics. (**a**) Flow chart of the Smart Cut^TM process for the thin-film transfer. (**b**) TEM image of the transferred SOI interface [34]. (**c**) Transferred GeOI interface observed by TEM [40]. (**d**) A typical application of SOI in MEMS-based tunable waveguide coupler [53]. (**e**) A traditional application of SOI wafer in MIR slow light waveguide photodetector [54]. (**f**) Interfacial characterization for the GeSnOI wafer fabricated by the direct bonding method [55]. (**g**) Interface studies for the bonded GeSnOI wafer [55]. (**h**) Strain calculation for the GeSnOI wafer based on the comparison of Raman spectra [55]. (**i**–**k**) Application of the bonded GeSnOI wafer in the GeSn FinFET [56]. Reprinted with permission from ref. [34]. Copyright 1997 Japan Society of Applied Physics. Reprinted with permission from ref. [40]. Copyright 2004 Springer. Reprinted with permission from ref. [53]. Copyright 2020 The Optical Society. Reprinted with permission from ref. [54]. Copyright 2020 Wiley-VCH. Reprinted with permission from ref. [55]. Copyright 2016 American Institute of Physics.

Recently, a typical multifunctional photonic switch on the SOI platform operating in the mid-infrared (MIR) wavelength range (from 3.85 μm to 4.05 μm) has been reported [53]. They used suspended waveguides with sub-wavelength cladding and MEMS to tune the waveguide coupler. The schematic diagram of the proposed device is shown in Figure 2d. SiO$_2$ wafer and SOI wafer are the upper and lower layers of the device, respectively. Microstructures patterned on the two parts are fabricated separately and assembled via the flip-chip bonding method. The optical waveguide couplers are prepared on the bottom SOI wafer, including suspended subwavelength grating (SWG) waveguides, grating couplers, and a tunable waveguide coupler with a MEMS cantilever. To make the MEMS cantilever move up and down, a single-side cladding for the suspended SWG waveguide is used to replace double-side cladding in the cantilever region. Leveraging the advantage of this change, the movement of the MEMS cantilever and optical signal transmission along the waveguide can be simultaneously realized with less crosstalk. The Au pad is fabricated on the top SiO$_2$ wafer and covers the cantilever region. Al solders are used for the intermediate bonding of the top SiO$_2$ wafer and bottom SOI wafer and the spacers and electrical interconnections. The MEMS cantilever can be actuated by applying a voltage between the top and bottom electrodes. The light propagates in the waveguide and couples from the input-port to drop-port in the lack of voltage bias. Correspondingly, the power-splitting ratio can be continuously tuned in the range of 0% and 100%. Based on the advances of the SOI platform and design, an optical attenuator with 25 dB depth using DC voltage actuation has been realized. With the actuation of AC voltage, the 1×2 optical switches with a response time of 8.9 μs and -3 dB bandwidth up to 127 kHz has been demonstrated.

Due to the excellent infrared properties of Si, another important application for the SOI platform is used for the photodetectors combining with two-dimension materials (e.g., black phosphorus, BP) [54]. A design for the shared-BP photonic system composed of photonic crystal waveguides (PhCWCs) with a slow light effect for the responsivity enhancement has been proposed. The schematic diagram and physical images of the device structures are shown in Figure 2e. A PhCWC and a subwavelength grating waveguide (SWGWG) with equal length are designed to highlight the slow-light enhancement. The BP covers the waveguide surfaces and is shared by the PhCWC and SWGWG at the same time. In the 3.8 μm wavelength, a responsive enhancement by more than tenfold in BP photodetector has been demonstrated. Such a slow light waveguide photodetector shows great potential for the on-chip MIR system in a wide range of applications, including environmental monitoring, industrial process control, and medical diagnostics.

2.2. GeSn-on-Insulator Platform Fabrication and Its Applications in FETs

Germanium-tin (Ge$_{1-x}$Sn$_x$) alloy is a famous Group IV semiconductor for potential applications in both electronics and photonics [57–61]. By controlling the content of Sn, the bandgap of Ge$_{1-x}$Sn$_x$ can be tuned. The combination of Group IV-based optical components with high-speed CMOS circuits can be desirable in future integrated chips. Therefore, the high-quality Ge$_{1-x}$Sn$_x$ layer on the insulator is an essential platform for monolithic integration. Currently, Ge$_{1-x}$Sn$_x$ thin film with a surface roughness of 0.528 nm can be grown on the (001)-oriented Si substrate using a molecular beam epitaxy (MBE) system. To fabricate the Ge$_{1-x}$Sn$_x$ on insulator structure, a 500 nm-thickness SiO$_2$ layer is deposited on the Ge$_{1-x}$Sn$_x$ using the PECVD. To make the SiO$_2$ denser, a 350 °C thermal treatment for 7 h in an N$_2$ environment is conducted. Subsequently, the CMP process is performed on the SiO$_2$ surface to reduce the surface roughness. The root-mean-square (RMS) value smaller than 0.2 nm has been achieved, which can satisfy the requirement for wafer direct bonding [62–74]. Then, both SiO$_2$/Ge$_{1-x}$Sn$_x$/Si and Si supporting wafer surfaces are activated by the O$_2$ plasma for 15 s and contacted at room temperature. A post-annealing at 300 °C in an N$_2$ environment is carried out to further enhance the bonding strength. Finally, the top Si is removed by soaking the bonded pair into tetramethylammonium hydroxide (TMAH) solution with an 80 °C heating treatment, while the bottom Si supporting wafer is spin-coated by a protective layer to avoid being etched. The cross-sectional TEM image of

the obtained GeSnOI is shown in Figure 2f [55]. The bonding interface is flat and void-free. The thickness of the $Ge_{1-x}Sn_x$ layer is 95 nm which is the same as the one grown by MBE, revealing the high etching selectivity of TMAH for the Si and $Ge_{1-x}Sn_x$.

To characterize the chemical bonds and strain of the fabricated GeSnOI wafers, Raman spectra are used for the component analysis, as shown in Figure 2g,h [55]. It can be seen that a peak assign to be Ge-Ge vibration mode at 300 cm^{-1} is appeared, while the peak at 520 cm^{-1} is contributed by the Si-Si vibration mode nonexistent. This indicates that the Si has been entirely removed by the TMAH solution, as presented in Figure 2g. By comparing the Raman shifts among the GeSnOI, GeSn/Si, and bulk Ge wafers, a compressive strain of GeSnOI substrate is calculated to be 0.10% which is smaller than 0.26% in the original $Ge_{1-x}Sn_x$ substrate, as shown in Figure 2h. The high-quality transferred GeSn thin film will bring enormous benefits for the fabrication of high-performance GeSn PFET. Based on the GeSnOI platform, a GeSn FinFET has been reported. The schematic diagram of the device structure is shown in Figure 2i [56]. The scanning electron microscopy (SEM) image of the device is shown in Figure 2j [56]. The channel lengths and fin width are down to 50 nm and 20 nm, respectively. Compared with other reported GeSn p-FETs, record-low S of 79 mV/decade and record-high $G_{m,int}$ of 807 μs/m (V_{DS} of −0.5 V), as well as highest $G_{m,int}/S_{sat}$ are realized. The result of the comparison for S in GeSn p-FET is shown in Figure 2k [56]. These results are the world's first GeSn FinFETs demonstrated on a GeSnOI substrate with excellent electrical performance. The enablements mentioned above are attributed to the high-quality GeSnOI heterogeneous structure obtained by the layer transfer. The encouraging achievements show that the GeSnOI platform holds promise for future advanced applications.

3. Heterogeneous Bonding for III-V and Wide Bandgap Semiconductor Thin-Film Transfer onto Si Substrate

As mentioned above, Si-based CMOS is one of the most fundamental components in semiconductor products. Driven by Moore's Law in the past year, device miniaturization and multifunction are the goals of chip development and pursuit. As the feature size continues to scale down, many advantages, such as improved operation speed, reduced power consumption, and production cost, gradually emerges [75–77]. Unfortunately, device reliability issues, such as short channel effects and random fluctuations, become more severe when the size approaches the limitation of Si-CMOS [78]. Besides, the substantial increase in the cost of lithography and etching processes makes the price of devices no longer dominant. The device design and its performance will be more and more materials-driven, along with the benefits of scaling subside. Therefore, the development of heterogeneous material systems compatible with the Si-CMOS platform can be the next generation of semiconductor technologies to break through the bottleneck of Si-CMOS scaling. Among numerous semiconductors, III-V compound materials, such as InP, GaAs, and GaN, receive widespread attention due to the excellent electrical properties and high-electron-mobility in transistors [79–82]. Compared with Si, most III-V compounds have a direct bandgap, making them can be used as light-emitting diodes (LEDs) and lasers [83–87]. The combination of III-V materials with the Si-CMOS platform can be used as a hybrid solution for the on-chip integration of Si-based photonics. Although they can directly grow on the Si substrate via epitaxial growth, many issues, such as significant mismatch in the lattice and coefficient of thermal expansion (CTE), still need to solve and improve. In contrast, direct wafer bonding is an efficient method to join hetero/homogeneous materials into one composite at low temperatures. Based on the Smart Cut^{TM} technology, it is possible to integrate thin film of III-V compounds onto the Si-CMOS platform. In addition to compound semiconductors, wide-bandgap materials, such as Ga_2O_3, are also popular in optoelectronic devices.

3.1. InP Thin-Film Transfer Based on the Modified Smart Cut^{TM} Technology

The InP thin-film transfer via wafer bonding is similar to the Smart Cut^{TM} technology. However, the generated gas originated from the InP/Si bonding will cause unavoidable bubbles in the interface, reducing the usage of integrated heterogeneous wafers. A modified method using surface trenches to eliminate interfacial voids has been proposed [88]. The schematic diagram of the modified Smart Cut^{TM} technology for InP thin-film transfer is shown in Figure 3a. Before the wafer bonding, trenches are patterned on the SiO$_2$ layer using photolithography followed by the plasma etching process. By optimizing the parameter of trench space, the bubbles can be efficiently inhibited. To highlight the effect of trenches, half of the SiO$_2$-on-Si wafer with channels and a half without channels are used for InP heterogeneous bonding. The bonding results after annealing are shown in Figure 3b. Experimental results show that there are many bubbles in the non-trench region, while the trench region is void-free. The interfacial SEM image shows that the InP/SiO$_2$/Si bonding interface across the trench region is tight. TEM observation also confirms that the atomic bonding between InP and SiO$_2$ has been achieved. Relying on this modified method, InP thin film with 2-in can be successfully transferred onto the SiO$_2$-on-Si wafer. The whole area of the InP/SiO$_2$/Si heterogeneous substrates is uniform, flat, and high-quality, can be used for practical device fabrication. We should note that the lateral outgassing surface trenches (LOTs) mechanism to facilitate the generated gas diffusion out of the bonding interface is a physical effect, only relying on the design of LOTs. This modified Smart Cut^{TM} technology might be a promising method to remove the bubbles at the bonding interface for all III-V compound semiconductors when integrated with the SiO$_2$, SiO$_2$-on Si, or Si substrates.
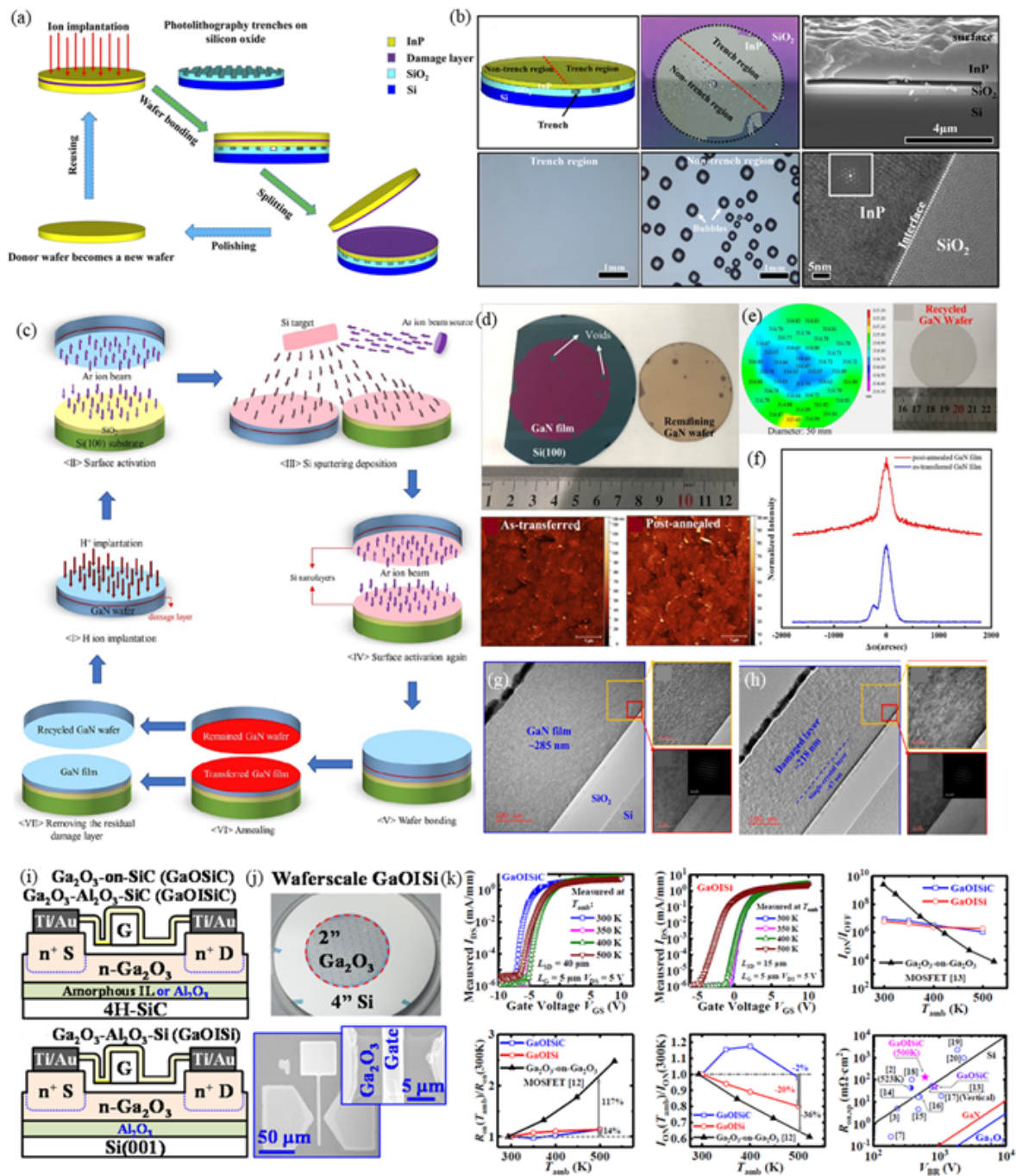
Figure 3. Heterogeneous bonding for III-V and wide bandgap semiconductor thin-film transfer onto Si substrate and their applications. (**a**) Schematic diagram of the modified Smart Cut^{TM} technology for InP thin-film transfer [88]. (**b**) Optical and SEM images for the transferred InP thin film onto Si substrate [88]. (**c**) Schematic diagram of the modified Smart Cut^{TM} technology for GaN thin-film transfer [89]. (**d**) Optical image of the transferred GaN thin film onto Si substrate [89]. (**e**) Thickness and AFM measurements for the transferred GaN thin film [89]. (**f**) XRD characterization for the GaN thin film before and after the annealing treatment [89]. (**g**,**h**) TEM observation for the bonding interface before and after the annealing treatment [89]. (**i**) Schematic diagram of the Ga$_2$O$_3$-based MOSFET [90]. (**j**) Optical image of the transferred wafer-level GaOISi and SEM image of the device structure [90]. (**k**) Performance characterizations of the Ga$_2$O$_3$-based MOSFET [90]. Reprinted with permission from ref. [88]. Copyright 2020 American Institute of Physics. Reprinted with permission from ref. [89]. Copyright 2020 Institute of Physics. Reprinted with permission from ref. [90]. Copyright 2020 Institute of Electrical and Electronics Engineers.

3.2. Wide Bandgap Semiconductor Thin-Film Transfer and Its Applications in MOSFETs

Gallium nitride (GaN) is an ideal material to apply in wireless communications and optical communications because it can operate in high power and frequency [91–93]. Thus, the heterogeneous integration of GaN with Si-CMOS substrate has attracted wide attention [94]. However, due to the significant lattice mismatch between GaN and Si, joining two kinds of materials into one system is challenging. Recently, direct epitaxy growth of GaN film on the (100)-oriented Si substrate has been reported. The generated GaN thin film is usually polycrystalline with a two-domain structure because of the asymmetric surface domains of the Si substrate. A modified surface activated bonding (SAB) method has been proposed to achieve the GaN thin film transfer combining with the Smart Cut^{TM} process [89]. The schematic diagram of the GaN thin-film transfer onto the Si substrate is shown in Figure 3c. Because of the high bonding strength of modified SAB, the GaN/SiO$_2$/Si bonding interface can keep stable during the post-annealing to peel off the GaN thin film from the bulk GaN wafer. The optical image of the transferred GaN-on-insulator (GaNOI) wafer is shown in Figure 3d. The area ratio of the transferred thin film to the donor GaN wafer is more than 90%. A small number of bubbles are caused by the particles adsorbed on the wafer surfaces. The deep cleaning process can avoid this kind of defect. Comparing the surface roughness before and after annealing treatment, the RMS values are 6.81 nm and 6.95 nm, respectively, in the area of 5 μm × 5 μm, demonstrating the modified SAB method can obtain sufficient bonding strength to resist the interfacial stress. The thickness mapping of the transferred thin film shows that the thickness is nearly uniform in the whole wafer, as presented in Figure 3e. After griding and CMP for the remaining GaN wafer, the color recovered from golden brown to transparent. It indicates that the damaged layer formed during the peel-off process has been removed. XRD and TEM experiments also confirm that the high-quality GaN thin film transferred process has been achieved, as shown in Figure 3f–h.

In addition to GaN semiconductor, Ga$_2$O$_3$ with ultra-wide bandgap has been considered a promising material for next-generation power electronics [95–102]. Unlike the GaN thin-film transfer, the modified SAB process uses nanometer-scale Al$_2$O$_3$ as the intermediate layer to perform the Smart Cut^{TM} process [90]. The transferred Ga$_2$O$_3$/Si heterogeneous structure can be used for the fabrication of MOSFETs. The schematic structure of the proposed Ga$_2$O$_3$ MOSFET on (001)-oriented Si substrate is shown in Figure 3i. An optical image of the transferred wafer-level Ga$_2$O$_3$ thin film and SEM image of the MOSFET microstructure is presented in Figure 3j. Due to the high-quality bonding, the device structure has been well prepared. The integrated wafers also bring lots of benefits in performance, as shown in Figure 3k. A device V_{br} above 600 V is achieved at 500 K, which is weakly dependent on the temperatures. It shows a significant improvement in thermal stability compared with the Ga$_2$O$_3$-on-SiC devices. Therefore, it proves that thin-film transfer via wafer bonding is a promising method to overcome the thermal limitation in Ga$_2$O$_3$ power electronic applications.

4. Heterogeneous Bonding for Wide-Bandgap Semiconductors Thin-Film Transfer onto SiC or Diamond Substrates for High Heat Dissipation

Although the heterogeneous integration of wide-bandgap semiconductors and Si-CMOS can bring many benefits, applications of GaN and Ga$_2$O$_3$ are mainly high-power or high-frequency electronic devices because of their excellent material properties [103,104]. However, the high channel temperatures induced by self-heating usually degrade the device's performance and reliability. One of the most effective methods is to use the heat dissipation substrates to remove the heat in time. SiC is used for heat dissipation substrates for GaN due to its high thermal conductivity and small lattice mismatch with GaN [13,105–109]. Unfortunately, the existence of the thermal boundary conductance (TBC) between GaN and SiC limits heat transport, making significant errors in theoretical calculations and experiments [110,111]. The GaN can grow on the SiC substrate with the assistance of the AlN intermediate layer, which is vital to growing high-quality GaN thin

film. The issue, such as dislocation density, usually appears, making the interface thermal resistance more serious. In addition to MBE and metal-organic chemical vapor deposition, wafer bonding technology is another feasible method for fabricating heterogeneous GaN/SiC structures. Compared with thin-film growth and deposition, wafer bonding has many advantages, such as insensitive to lattice mismatch, low temperatures, wafer-scale, etc. [112–119].

To achieve a reliable bonding between GaN and SiC, the SAB method has been used for direct wafer bonding [12]. Different from the Smart Cut^{TM} technology, the laser lift-off is used for the GaN thin-film transfer. The schematic diagram of the experimental process is shown in Figure 4a. The GaN is grown on the sapphire wafer and used as the donor substrate. After the GaN/SiC bonding, the 248 nm laser irradiates on the bonded wafer pair to make GaN and sapphire separate. Optical images of the bonded wafer pair and transferred GaN thin film are shown in Figures 4b and 4c, respectively. Atomic bonding has been confirmed by TEM, and the bonding interface is only 3 nm, as shown in Figure 4d. This indicates that a high-quality GaN/SiC heterogeneous structure can be obtained by the SAB method combined with a laser lift-off process. Diamond is another popular substrate for thermal management [120]. The GaN thin film can also be transferred onto the diamond substrate via the bonding method [11]. Instead of the intermediate-free SAB method, nanometer-scale amorphous Si layers are used for the GaN/diamond bonding. The Si is sputtered to the GaN and diamond substrates before the surface activation. The followed processes are the same as the GaN thin-film transfer onto the SiC wafer. Atomic bonding between GaN and diamond has been realized, as shown in Figure 4e–g. The bonding interface is smooth and void-free, demonstrating the effectiveness of the GaN thin-film transfer to the heat sink substrates.

Not only limited to the GaN, the SAB method for the thin-film transfer is also suitable for the Ga_2O_3 [90,121,122]. The Ga_2O_3 thin-film transferred procedure is the same as the Smart Cut^{TM} process, as shown in Figure 4h. However, the bonding method is using nanometer-scale Al_2O_3 layers as the intermediate for the modified SAB method. Optical images of the Ga_2O_3/SiC bonded wafer pair and transferred Ga_2O_3 thin film are shown in Figures 4i and 4j, respectively. TEM observation shows that atomic bonding between Ga_2O_3 and SiC has been achieved bridging by Al_2O_3, as presented in Figure 4k. The thickness mapping of the transferred thin film shows that the thickness is nearly uniform in the whole Ga_2O_3/SiC wafer, as presented in Figure 4l. The surface roughness can also satisfy the high requirements of device fabrication after a CMP surface treatment confirmed by multi-point testing. The RMS values are stable at ~0.5 nm with a measured area of 5 μm × 5 μm. After a 900 °C post-annealing treatment, the FWHM of XRD rocking curves for the Ga_2O_3/SiC heterogeneous wafer is reduced to 130 arcsec, demonstrating the high crystallinity of the Ga_2O_3 layer.
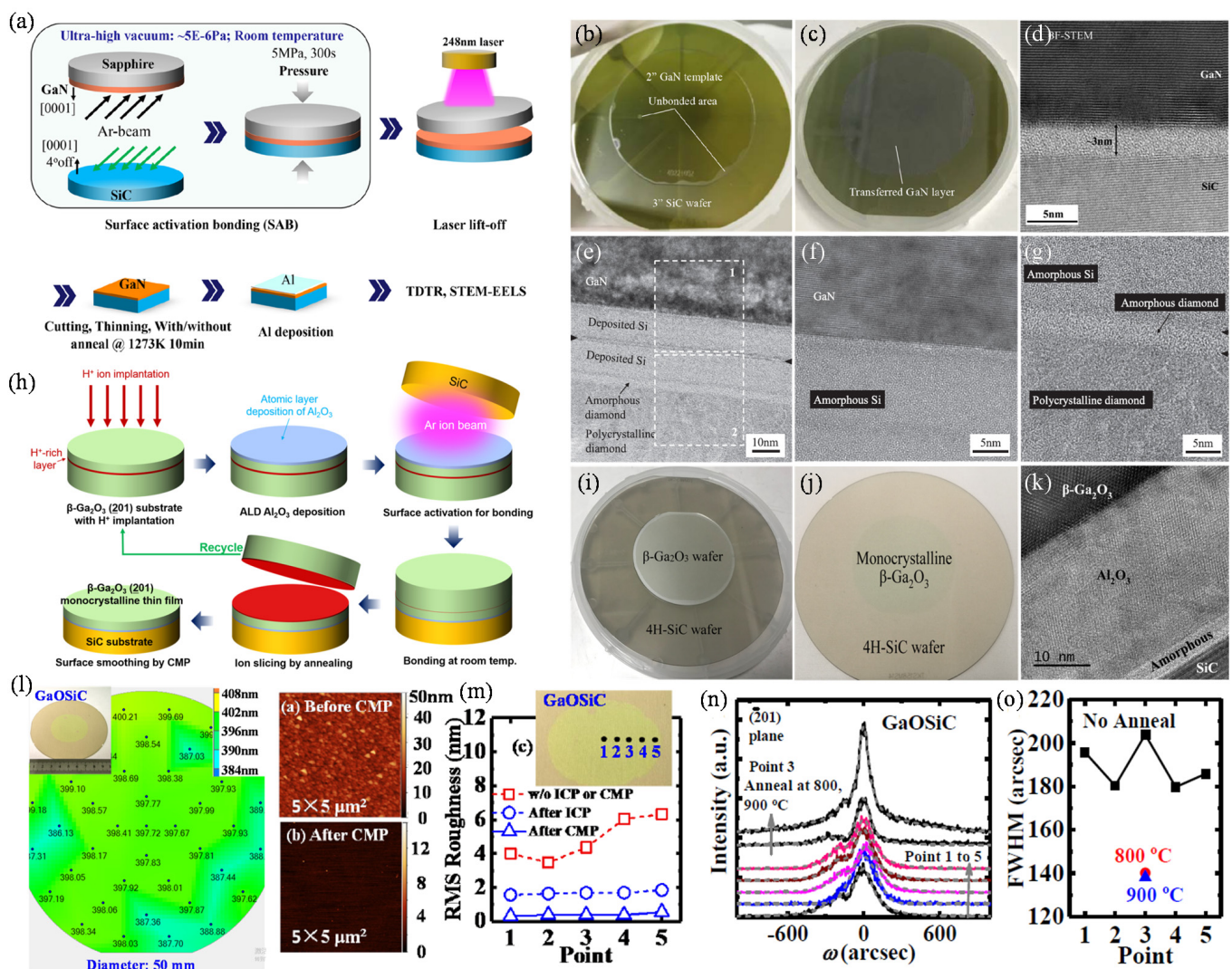
Figure 4. Heterogeneous bonding for wide-bandgap semiconductors thin-film transfer onto SiC or diamond substrates for high heat dissipation. (**a**) The schematic diagram for GaN thin-film transfer onto the SiC substrate via Si-modified SAB method [12]. (**b**) Optical image of the bonded GaN and SiC wafers via Si-modified SAB method [12]. (**c**) Optical image of the transferred GaN thin film onto SiC substrate [12]. (**d–g**) TEM images of the GaN/SiC bonding interface [12]. (**h**) The schematic diagram for Ga_2O_3 thin-film transfer onto the SiC substrate via Al_2O_3-modified SAB method [121]. (**i**) Optical image of the bonded Ga_2O_3 and SiC wafers via Al_2O_3-modified SAB method [121]. (**j**) Optical image of the transferred Ga_2O_3 thin film onto SiC substrate [121]. (**k**) TEM images of the Ga_2O_3/SiC bonding interface [121]. (**l**) Thickness and AFM measurements for the transferred Ga_2O_3 thin film onto SiC substrate [90]. (**m–o**) Material characterizations of the transferred Ga_2O_3 thin film [90]. Reprinted with permission from ref. [12]. Copyright 2019 American Chemical Society. Reprinted with permission from ref. [121]. Copyright 2020 American Chemical Society. Reprinted with permission from ref. [90]. Copyright 2020 Institute of Electrical and Electronics Engineers.

5. Piezoelectric Thin Transfer for the Self-Powered Implantable Electronics

Implantable electronics have important research significance for human health detection, disease diagnosis, and treatments. Several intelligent automatic devices have been applied in clinical practice to improve patients' health. Although many self-powered devices, such as triboelectric- or electrochemical-based devices, can detect the human body's dynamics, they cannot be applied in-vivo because of the limited biocompatibility of materials [29,123–133]. Among many kinds of materials, piezoelectric materials have always attracted much attention due to their mature preparation processes and high-efficiency responses to the deformation [134–136]. Although (K, Na)NbO_3 (KNN) is more friendly to the human body and environment because it is lead-free, lead zirconate titanite (PZT) has

more advantages in the performance and fabrication of implanted devices due to the higher piezoelectric effect [137–144]. Therefore, by transferring the PZT thin film to a flexible substrate with good biocompatibility, such as polydimethylsiloxane (PDMS) and polyimide (PI), it can be used for the fabrication of self-powered implantable electronics with different functions. Herein, methods for the piezoelectric thin film transfer onto PDMS and PI will be introduced.

The PZT thin film transfer onto different flexible substrates is based on the debonding method of hydrofluoric (HF) acid to remove the SiO_2 layer [145]. The final exploded view, and top view of the flexible mechanical energy harvester (MEH) based on thin ribbons of PZT are shown in Figure 5a. The schematic illustration for the fabrication of MEH composite structures is displayed in Figure 5b. Firstly, the composite PZT with metal electrodes is deposited onto the SiO_2-on-Si wafers by the CMOS-compatible process. The device structures have also been transferred at the same time. Secondly, the photoresist is spin-coated on the wafer surfaces to prevent the device structure from being corroded by subsequent HF solutions. After the immersion treatment, the deposited PZT thin film with photoresist protection will be separated from the SiO_2-on-Si wafer. Finally, the functional thin film will be stamped by the PDMS onto the PI substrate for the implantable electronics. Based on this process and composite structures, implantable devices that enable high-efficiency mechanical-to-electrical energy conversion have been proposed. The device parameters and structures are shown in Figure 5c. With the excitation of bending treatment, the PZT thin film will generate an electrical signal responded to the deformation. Optical images of a PZT MEH clamped on a bending stage in flat and bent conditions are presented in Figures 5d and 5e, respectively. Due to PI has good biocompatibility, such kind of device can be used for self-powered implant devices in the organism [146]. Photographs of PZT MEHs on the right ventricle (RV), left ventricle (LV), and free wall of a bovine heart are shown in Figure 5f–h. Different signal outputs will be produced under different monitoring systems. It demonstrates the effectiveness of PZT thin film transfer and the feasibility of biocompatible electronics relying on such composite structures.

The same process can also be used for the piezoelectric composite thin film transfer onto the PDMS substrate [147]. Recently, an implantable piezoelectric generator (iPEG) has been proposed to monitor and treat severe diseases. The device structures are shown in Figure 5i. It can be used for the battery-free implantable cardiac pacemaker. As shown in Figure 5j, different signal outputs will show up with different shape changes, as presented in Figure 5k. Therefore, information about heartbeats will be recorded and output as electrical signals.

Moreover, the biocompatibility of the iPEG has also been tested, as shown in Figure 5l. The fabricated composite device has almost no adverse effects on biological tissues. The live heartbeat test has also been performed, as shown in Figure 5m,n. The heart beating will compress the device to varying degrees to record information for the subsequent health monitoring and disease diagnosis. Since the device fabrication process is CMOS compatible, the device possesses excellent stability and can be applied for mass production.
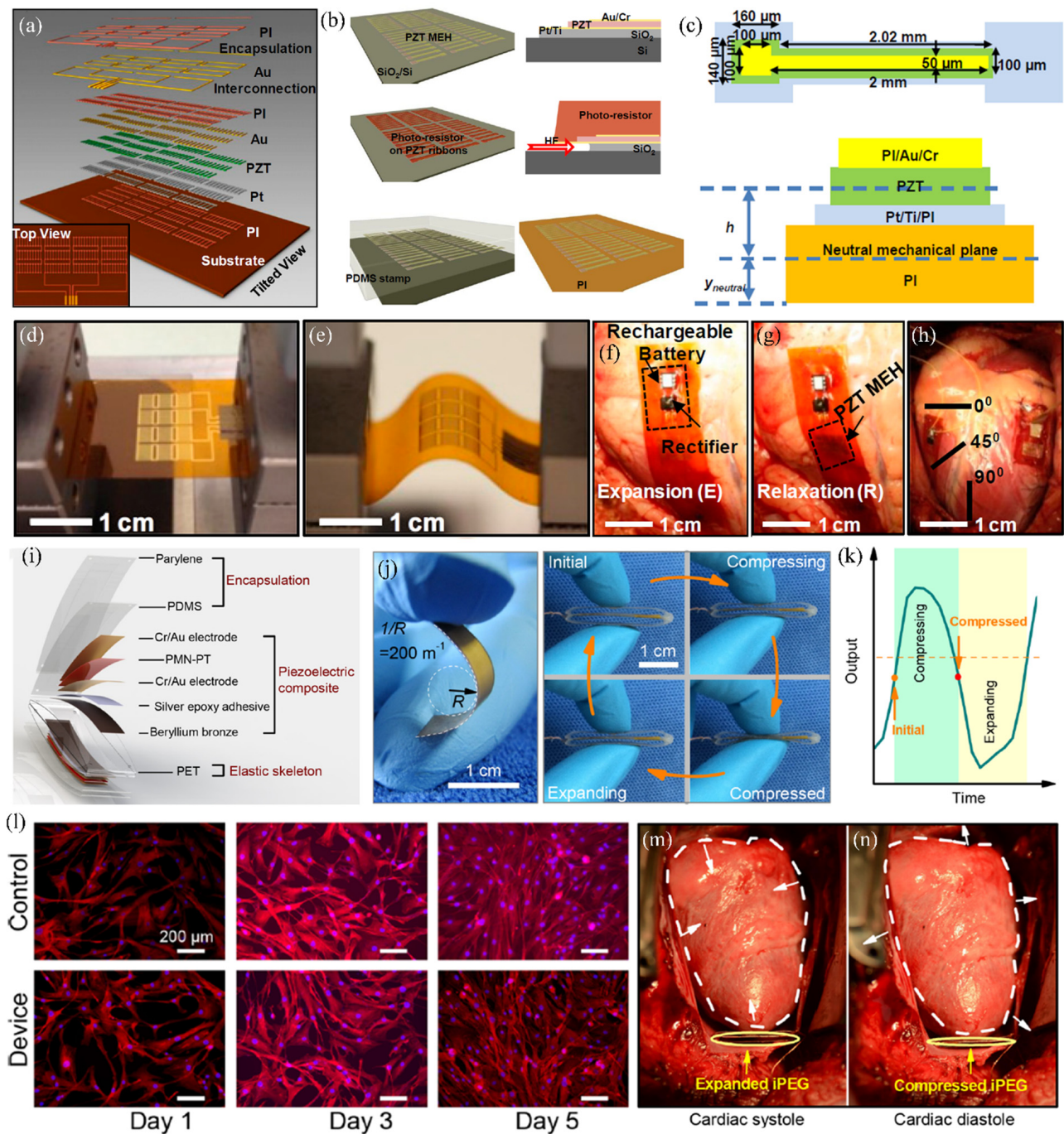
Figure 5. Piezoelectric thin transfer for the self-powered implantable electronics. (**a**) Exploded view and top view of the flexible MEH based on thin ribbons of PZT [145]. (**b**) Schematic illustration of procedures for fabricating a PZT MEH on a polyimide (PI) substrate [145]. (**c**) Top and cross-section view of a single PZT ribbon capacitor structure [145]. (**d**,**e**) Optical recordings of a PZT MEH clamped on a bending stage in flat and bent configurations [145]. (**f**,**g**) Images of PZT MEHs on the RV, LV, and free wall of a bovine heart [145]. (**h**) PZT MEH cointegrated with a rectifier and rechargeable battery [145]. (**i**) Exploded view of the detailed composited structures for the implantable piezoelectric generator [147]. (**j**,**k**) Piezoelectric composite bending by human fingers and corresponding output signals [147]. (**l**) Biocompatibility tests of the implantable piezoelectric generator using human pericardial fibroblasts [147]. (**m**,**n**) Optical images for the real-time monitoring of heart test using the proposed implantable device [147]. Reprinted with permission from ref. [145]. Copyright 2014 United States National Academy of Sciences. Reprinted with permission from ref. [147]. Copyright 2019 American Chemical Society.

6. LiNbO$_3$ Thin-Film Transfer for High-Performance Electro-Optical Modulators

LiNbO$_3$ is a popular material due to its excellent piezoelectric property, electro-optic and nonlinear optical effects. However, traditional bulk LiNbO$_3$-based optical devices suffer from large volume, expensive, low bandwidth, and high operating voltages. To overcome this problem, thin-film LiNbO$_3$ is a good choice. Currently, there are already several kinds of commercial LiNbO$_3$ thin-film wafers, such as LiNbO$_3$-on-Si, LiNbO$_3$-on-sapphire, LiNbO$_3$-on-glass, etc. Fabrication of the above LiNbO$_3$-based heterogeneous wafers is based on the Smart Cut^{TM} technology [148]. The process is shown in Figure 6a. He$^+$ implantation is performed to create a damage layer in the LiNbO$_3$ sub-surface. After surface activation, the activated surfaces of LiNbO$_3$ and handle substrate are contacted to form the pre-bonded pair. With an annealing treatment, the donor LiNbO$_3$ wafer is cracked from the damage layer. At the same time, the bonding interface between the LiNbO$_3$ thin film and handle wafer will be strengthened because of the higher temperatures. After the CMP process, heterogeneous wafers can be used for device fabrication. However, LiNbO$_3$ is a kind of chemically inert material. The large propagation loss caused by the rough sidewalls is due to the imperfect fabrication. A rib configuration for the LiNbO$_3$-based optical devices has been proposed to better confine the waveguide light, as shown in Figure 6b–g [22]. Electro-optic (EO) modulators and EO comb generators are essential building blocks for modern telecommunication networks, quantum photonics, and microwave-photonic systems. The excellent properties of LiNbO$_3$ can satisfy the requirements of high-performance EO devices. Recently, a 50:50 Y-junction Mach-Zehnder interferometer and an EO comb generator have been proposed, as shown in Figures 6h and 6i, respectively [20,21]. The EO modulator can work at a CMOS-compatible voltage (1.4 V) with high bandwidth. The transmission speed of data can reach 210 Gbit/s. As for the LiNbO$_3$-based EO comb generator, the frequency range covering the entire telecommunication L-band has been achieved. Both demos demonstrate that the LiNbO$_3$-based EO devices have huge potential in applying 5G and even the next generation of communication technology.

Transducers are promising platforms that may enable large-scale quantum networks because of the direct conversion, low-noise operation, and large bandwidth. A superconducting cavity EO transducer based on the LiNbO$_3$ thin film has been proposed [149]. The schematic diagram and working mechanism of the designed device are shown in Figure 6j. The optical pump signal can be tuned to the red optical at a specific frequency because two microring resonators are evanescently coupled. The simulated and measured results for the piezoelectric loss in LiNbO$_3$ are shown in Figure 6k. It can be seen that frequencies near the bulk acoustic wave modes present strong loss, while low loss is observed for frequencies far detuned from the bulk acoustic modes. For the detuning dependence of microwave-to-optical photon transduction, the results are shown in Figure 6l. The experimental measurements are in good agreement with the theory. Therefore, the LiNbO$_3$-based EO transducer shows system simplicity and low-noise operation, showing opportunities for the on-chip filter integration and further improvement of the transduction efficiency.
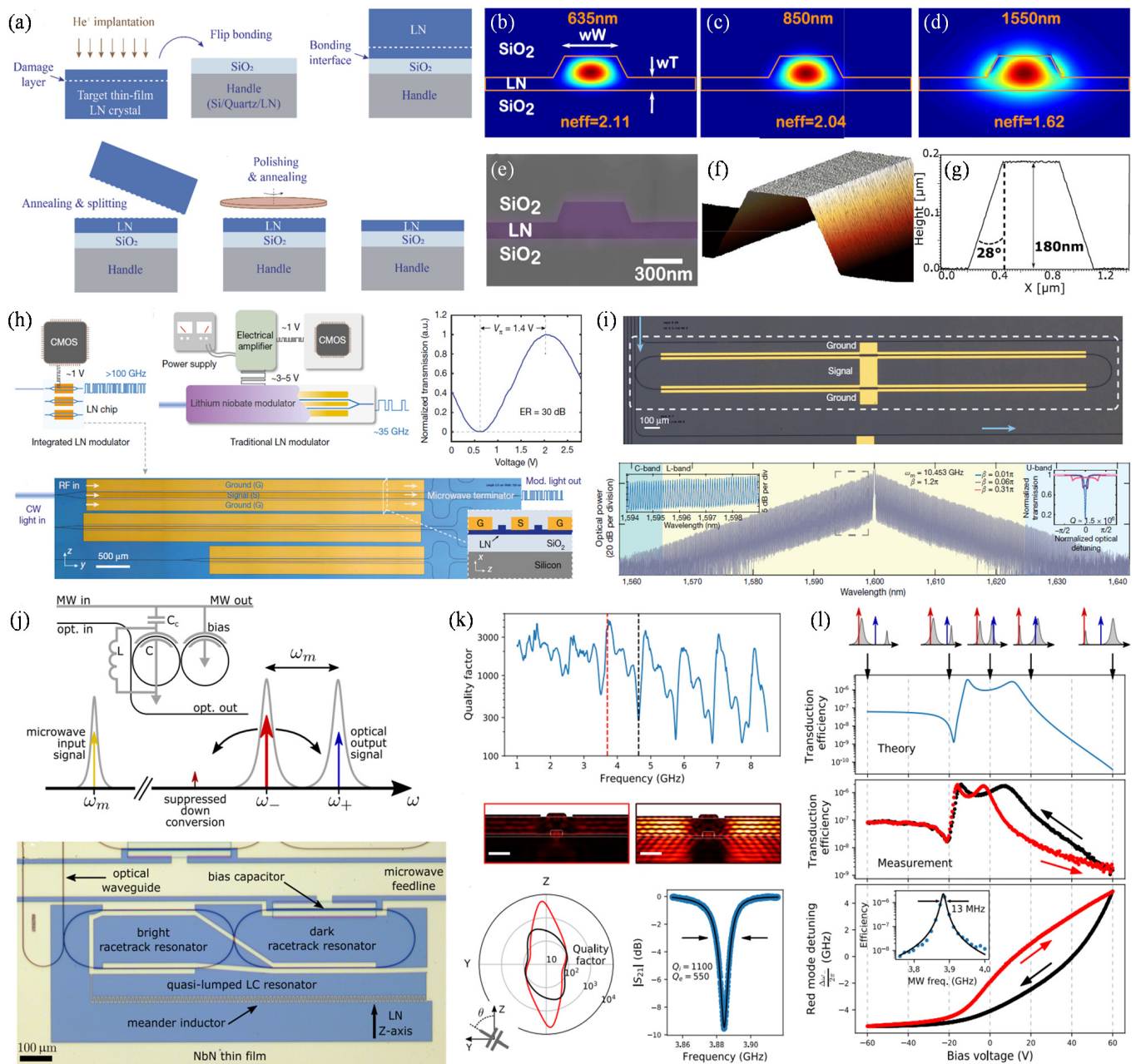
Figure 6. LiNbO$_3$ thin-film transfer for high-performance electro-optical modulators. (**a**) Schematic diagram of the LiNbO$_3$ thin-film transfer for the fabrication of LNOI wafer [148]. (**b–d**) Finite element simulation of the TE$_{00}$ waveguide mode near the wavelengths of 635 nm, 850 nm, and 1550 nm [22]. (**e**) SEM image of the cross-sectional waveguide [22]. (**f,g**) Surface morphology and surface profile of the LiNbO$_3$ waveguide [22]. (**h**) Schematic diagram and optical images of the nanophotonics LiNbO$_3$ modulator compatible with CMOS drive voltages [21]. (**i**) Optical image of the fabricated LiNbO$_3$-based comb generator [20]. (**j**) Schematic diagram and optical image of the designed superconducting cavity electro-optic transducer based on the LNOI platform [149]. (**k**) Performance test of the piezoelectric loss in LiNbO$_3$ [149]. (**l**) Performance measurements for the detuning dependence of microwave-to-optical photon transduction [149]. Reprinted with permission from ref. [148]. Copyright 2020 World Scientific. Reprinted with permission from ref. [22]. Copyright 2019. The Optical Society. Reprinted with permission from ref. [21]. Copyright 2018 Springer Nature. Reprinted with permission from ref. [20]. Copyright 2019 Springer Nature. Reprinted with permission from ref. [149]. Copyright 2020 The Optical Society.

7. Si-on-CaF$_2$ Platform Fabrication for MIR Sensors

There are many fingerprints for gases, liquids, and biomolecules in the MIR wavelength [150–159]. Correspondingly, the working wavelengths of many sensors are designed in the range of MIR [160–170]. In addition to microelectronics, Si is also one of the most popular materials in photonics [171,172]. Due to its high refractive index, excellent transparent properties in the spectral range from 1.2 μm to 8.0 μm, and high-quality commercial product of SOI platform, all kinds of Si-based sensors have been well developed. Although SOI has good confinement for light due to the significant differences in the refractive index between Si ($n = 3.48$) and SiO$_2$ ($n = 1.40$), the existence of SiO$_2$ limits the operating wavelength range of Si photonics because of the light absorption. To make Si-based devices have better performance when the working wavelength is larger than 4 μm, transferring Si thin film to infrared substrates with lower refractive indexes, such as sapphire, MgF$_2$, CaF$_2$, and BaF$_2$, is a good choice.

The primary fabrication process for developed Si thin-film transfers onto the CaF$_2$ substrate is shown in Figure 7a [173]. The SOI platform is composed of a top Si layer, buried silicon dioxide (BOX) layer, and Si substrate, the donor wafer for the Si thin film. Before the thin-film transferred process, an array of holes is patterned on the top Si layer using photolithography and dry etching methods. These holes are used for the hydrofluoric acid solution to access the BOX and removing the SiO$_2$ layer. Due to the existence of photoresist, the underlying cured and baked photoresist become pedestals to support the top Si layer on the supporting substrate after completely releasing the BOX. Subsequently, a polydimethylsiloxane (PDMS) film with a thickness of several micrometers is used to stick on the surface of the released top Si thin film. We should note that the contact between PDMS and Si thin film mainly depends on the adhesion force, which can be regarded as temporary bonding, but the bonding strength is stronger than the fracture strength of the photoresist. Therefore, the Si membrane can be peeled off from the SOI platform. After that, the Si/PDMS composite is pressed on the receiving CaF$_2$ substrate, and PDMS is slowly removed. Consequently, the Si thin film is bonded onto the CaF$_2$ substrate with the assistance of surface forces. Although the bonding of Si and CaF$_2$ is under the effects of van der Waals and other temporary bonds, experiments have verified that the substrate can withstand the erosion of chemical solutions.

The above-mentioned method is capable of transferring Si thin film with an area of several square centimeters. Based on this process, the first Si photonic device integrated on the CaF$_2$ substrate has been fabricated and published [173]. Figure 7b shows the optical image of the microring arrays fabricated on the transferred Si-on-CaF$_2$ substrate. It can be seen that the surface is flat and smooth. The microstructures of the Si microring resonators coupled with bus waveguides are shown in Figure 7c. The waveguides are inversely tapered toward the edge of the chip to facilitate butt-coupling with infrared fibers. Due to the working wavelengths that can be designed beyond 4.0 μm, the mixed ethanol and toluene ratio can be distinguished. Moreover, the high-performance MIR resonator based on this transferred platform can be used to analyze organic chemicals with a limit of detection of less than 0.1 ng.

The heterogeneous integration of waveguide photodetectors towards chip-scale zero-bias long-wave infrared (LWIR) spectroscopic sensing has also been demonstrated [174]. The schematic diagram of the proposed on-chip LWIR spectroscopic sensor is shown in Figure 7d. The graphene overlays the waveguide as a photodetector. When the light with different wavelengths propagates along the multiple waveguide channels, the analytes will extensively interact with the evanescent field. Then, both light intensity and photoresponse are decreased at the specific absorption peaks. The measured device performances are shown in Figure 7e–g. Experimental results show that the photocurrent changes linearly with the increased light power. In addition to the passive device, the functional system design, such as MEMS-based tuning spectra, is shown in Figure 7k [175]. To avoid the limitation of stress in device fabrication, double layers of thin PCS reflectors are transferred to form the Fabry–Pérot filter (FPF). By applying different voltages, the transferred Si thin

film can be deformed to different degrees. The simulation and experimental results show that the spectra can be tuned with different voltages, as presented in Figure 7h–n. When the applied voltage is 70 V, the peak position is decreased from 5.61 μm to 4.13 μm. By reconstructing the tunable spectra, this kind of device can be used for sensing applications. As a proof of concept, CO_2 molecules have been introduced for measurement. A dip recovering with a full width at half maximum of 170 nm at 4.26 μm has been observed. More high-performance passive or active miniaturized MIR devices will be developed based on the technology of Si thin-film transfer onto the CaF_2 substrate.
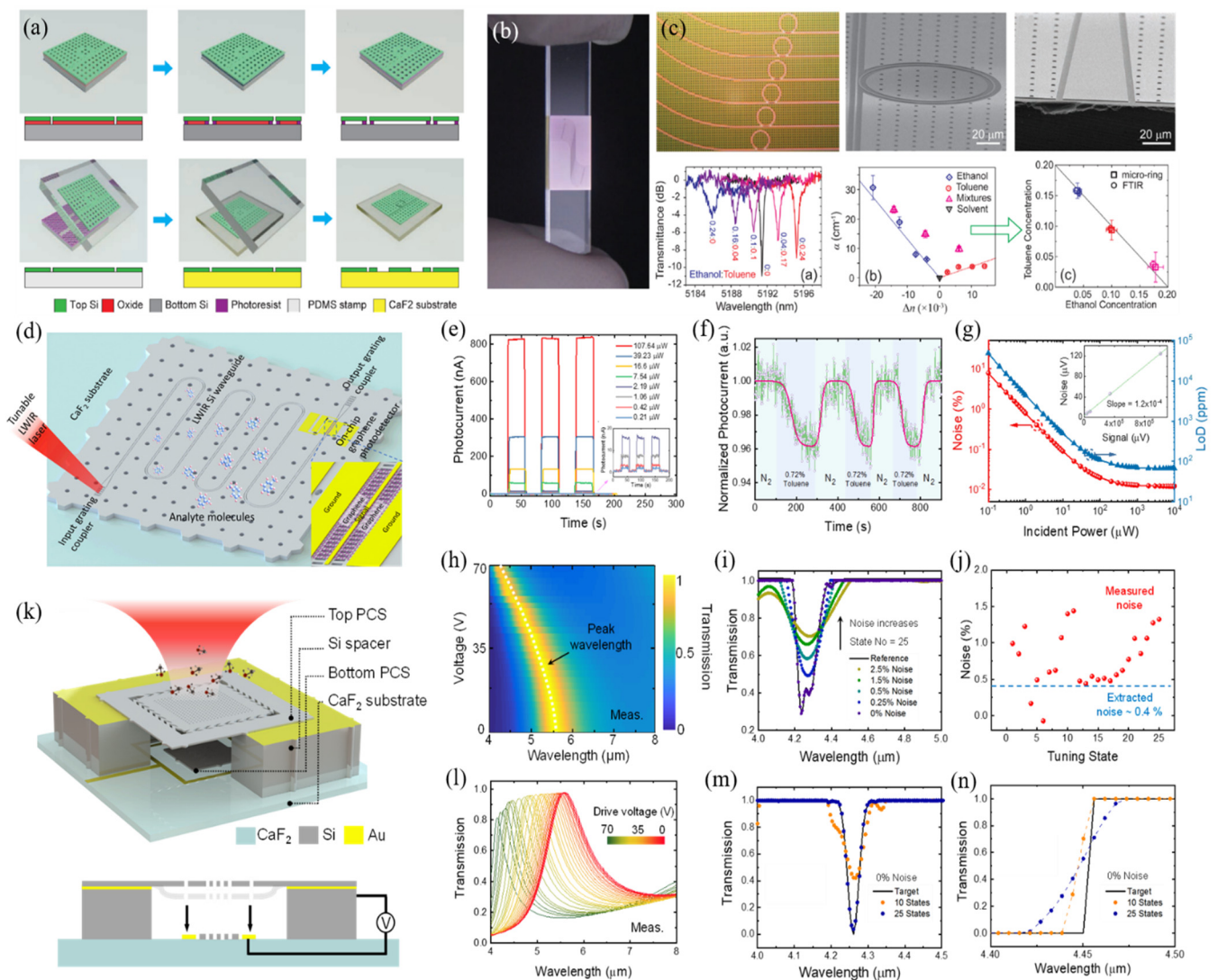

Figure 7. Si thin-film transfer onto the CaF_2 substrate for the MIR sensing applications. (**a**) Schematic illustration of the Si thin film transfer process [173]. (**b**) Optical image of the fabricated Si photonic device on a CaF_2 substrate [173]. (**c**) Optical and SEM images of the fabricated microring sensors with their performance test [173]. (**d**) Schematic illustration of the heterogeneously integrated graphene/Si/halide Si-based MIR photodetectors [174]. (**e–g**) Dynamic on-chip sensing demonstration [174]. (**h–j**) Simulation and experimental results for the spectral tuning and gas sensing [175]. (**k**) Schematic diagram of the MEMS-based tuning optical gas sensor [175]. (**l–n**) Simulation and experimental results for the spectral tuning and gas sensing. Reprinted with permission from ref. [173]. Copyright 2014 American Chemical Society.Reprinted with permission from ref. [174]. Copyright 2021 American Chemical Society. Reprinted with permission from ref. [175]. Copyright 2021 Institute of Electrical and Electronics Engineers.

8. High-Quality Thin Film Obtained via the Debonding Method for Flexible Electronics

Flexible and wearable electronics are an inevitable trend in the development of real-time and dynamic monitoring for human health since the thin-film electronics can offer better performance than traditional bulk systems, being lightweight, low-cost, and visible [17,23,24,28,176–180]. Although significant progress in the fabrication of thin-film materials and optimization of structure design, the realization for high-performance thin-film electronics compatible with a wafer-level batch process is still limited [181–188]. Thus, the development of transfer printing technology in the wafer-level for thin-film micro/nanoelectronics is important for high-yield production. In the above sections, we have introduced several thin-film transferred technologies combined with bonding and debonding methods based on the Smart Cut^{TM} technology. In such situations, bonding is more critical to achieving reliable fabrication for electronic and photonic devices. However, for the thin-film transfer printing process at the wafer level, debonding is more critical to obtain flexible substrates with large size and fewer surface damages. In this part, we introduce two kinds of technologies (i.e., SiO_2 layer released and water-induced layer separation) to fabricate high-quality thin-film substrates.

Nano-thickness metal films possess excellent properties in optical transmittance, flexibility, and sheet resistance. Most of them are generated on the substrates by evaporation, sputtering, or other deposition methods, making the thin films polycrystalline. However, the grain boundaries often make electronics suffer from electron-hole recombination, which will degrade their performance. To overcome this problem, introducing a single-crystal Au film on the Si surface as a substrate for epitaxial growth of other single-crystal metal thin films has been developed [189]. The schematic diagram for the Au foil transferred process is shown in Figure 8a. Wafer-scale single-crystal Au film is grown on the Si substrate by the epitaxial growth method. With the help of light irradiation, a sacrificial SiO_x layer sandwiched by the Au foil and Si template is generated due to the photoelectrochemically oxidizing. Then, a polymer adhesive is attached to the Au surface for the subsequent thin-film separation. By immersing the composite layer in the hydrofluoric acid solution, the SiO_x layer is removed to achieve the peeling. The interfacial microstructures in each step are shown in Figure 8b. Both single-crystal Au film and oxidized SiO_2 have been confirmed by TEM. A 28 nm-thickness Au foil with a sheet resistance of 7 ohms per square shows only a 4% increase after 4000 bending cycles. Besides, the grown ZnO nanowires also show flexibility with the nanowires intact up to 500 bending cycles. X-ray diffraction and pole figures have been used to study the in-plane and out-of-plane orientation, as shown in Figure 8c. High-quality single-crystal metal films have been confirmed. Therefore, this process provides a universal method for the production of ordered substrates for flexible electronics.

The schematic illustrations of critical steps for the thin film transfer based on the water-induced layer separation are shown in Figure 8d [190]. Nanometer-thickness Ni and dilute polyimide are deposited on a SiO_2/Si wafer to serve as the separation and glue layer, respectively. With water molecules' assistance, the glue layer dissolves, and the device layer peels off from the substrate. Additionally, the SiO_2/Si wafer can be repeatedly used. Optical images of the n-doped Si thin-film capacitor arrays on a thermally releasable tape, and device performance test are shown in Figure 8e. Due to the robust structures, the transferred flexible electronics can be pasted on objects with different shapes. Moreover, the preset functions of the device can be well realized. This debonding method can be effectively performed in wafer-recyclable, environmentally friendly transfer printing for large-scale thin-film nanoelectronics.
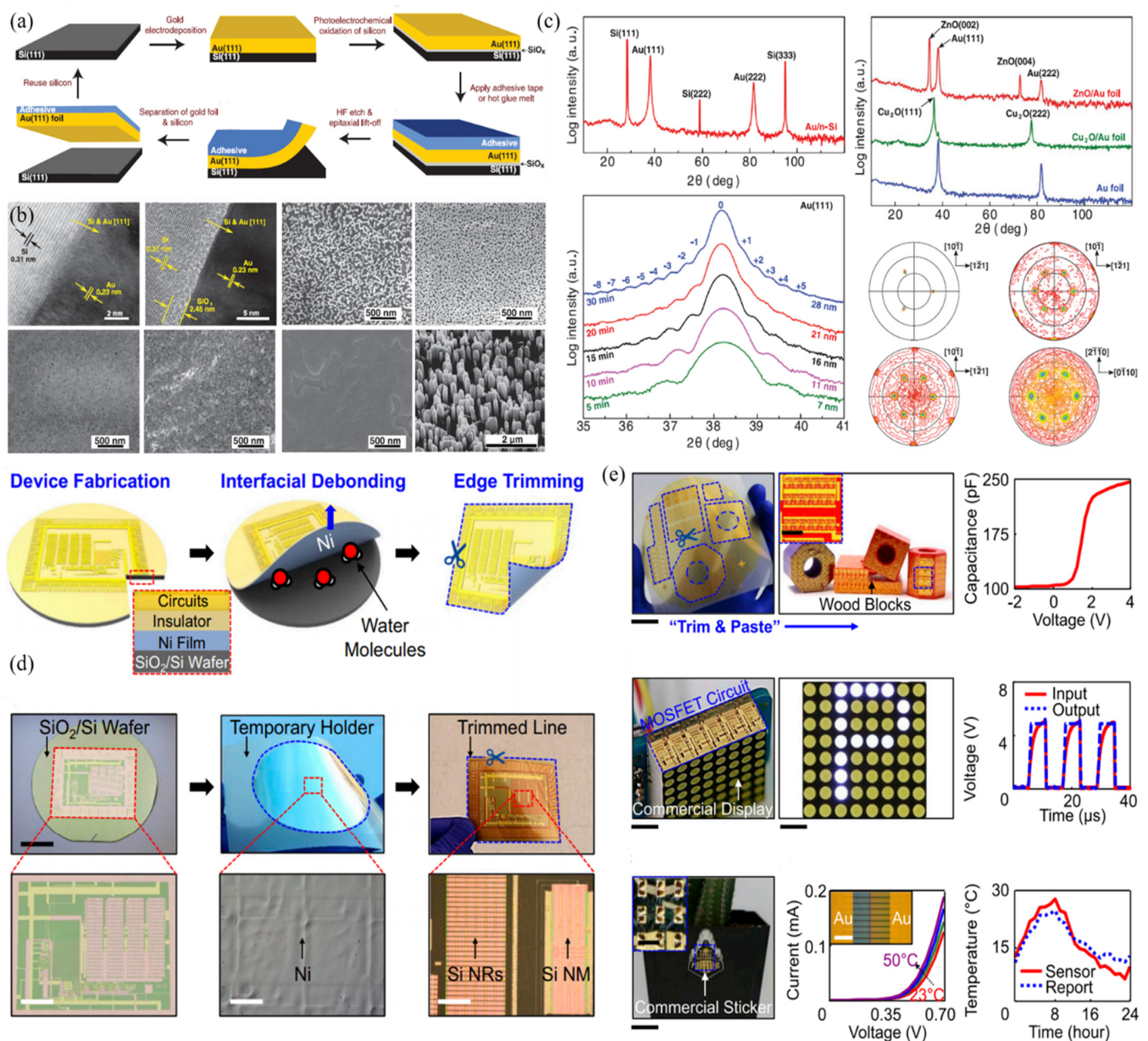
Figure 8. The high-quality thin film is obtained by the debonding method for flexible electronics. (**a**) The schematic diagram for the epitaxial lift-off of single-crystal Au foil by the release of SiO₂ layer [189]. (**b**) Comparison for the high-resolution TEM studies of the epitaxial grown and transferred Au film with the application of Cu₂O and ZnO growth [189]. (**c**) In-plane and out-of-plane orientation studies by the X-ray diffraction and pole figure for the transferred Au foil [189]. (**d**) Schematic illustration of the thin-film transfer for large-area nanoelectronics based on the SiO₂ layer releasable method [190]. (**e**) Device fabrication on the transferred thin film and its performance characterizations [190]. Reprinted with permission from ref. [189]. Copyright 2017 American Association for the Advancement of Science. Reprinted with permission from ref. [190]. Copyright 20118 United States National Academy of Sciences.

9. Concluding Remarks and Perspectives

In the past few decades, wafer bonding technology has made remarkable achievements in SiP and the fabrication of heterogeneous structures for electronics. Although it is only one step in developing various platforms, wafer bonding is one of the most essential and indispensable steps in obtaining reliable interfaces among device layers and substrates. Thanks to the extraordinary performance by thin-film, the micro/nano devices show great enhancement in many applications of electronics devices, optoelectronics devices, infrared nanophotonic sensors, and wearable sensors compared with their counterpart

made by bulk materials. Although the cost for the wafer increases at the current stage, the gain of device performance is requesting the industry to lower down the cost by developing mature processes for mass production. With the rapid development of 5G technology and IoTs, the fabrication of new heterostructures suitable for various functional devices ushered in both challenges and opportunities. Compared with the developments of bonding methods for semiconductors, more work needs to contribute to infrared material bonding. With the emerging rise of metasurfaces in molecular sensing, more heterogeneous composites for infrared materials need to be developed to satisfy the theoretical research and experimental requirements. In the future, wearable and multifunctional system-level integration combined with extensive data analysis and artificial intelligence is an inevitable trend for sensing applications. Wafer bonding is one of the feasible and effective methods for such a large and complex heterogeneous integration.

References

1. Lee, C.; Xie, J. Design and Optimization of Wafer Bonding Packaged Microelectromechanical Systems Thermoelectric Power Generators with Heat Dissipation Path. *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **2009**, *27*, 1267. [CrossRef]
2. Lee, C.; Huang, W.-F.; Shie, J.-S. Wafer Bonding by Low-Temperature Soldering. *Sens. Actuators A Phys.* **2000**, *85*, 330–334. [CrossRef]
3. Lee, C.; Yu, A.; Yan, L.; Wang, H.; He, J.H.; Zhang, Q.X.; Lau, J.H. Characterization of Intermediate In/Ag Layers of Low Temperature Fluxless Solder Based Wafer Bonding for MEMS Packaging. *Sens. Actuators A Phys.* **2009**, *154*, 85–91. [CrossRef]
4. Niklaus, F.; Stemme, G.; Lu, J.Q.; Gutmann, R.J. Adhesive Wafer Bonding. *J. Appl. Phys.* **2006**, *99*, 031101. [CrossRef]
5. Lin, Y.-S.; Xu, Z. Reconfigurable Metamaterials for Optoelectronic Applications. *Int. J. Optomechatronics* **2020**, *14*, 78–93. [CrossRef]
6. Yu, D.Q.; Lee, C.; Yan, L.L.; Thew, M.L.; Lau, J.H. Characterization and Reliability Study of Low Temperature Hermetic Wafer Level Bonding Using In/Sn Interlayer and Cu/Ni/Au Metallization. *J. Alloy. Compd.* **2009**, *485*, 444–450. [CrossRef]
7. Da-Quan, Y.; Li, L.Y.; Chengkuo, L.; Won, K.C.; Thew, S.; Chin, K.F.; Lau, J.H. Wafer-Level Hermetic Bonding Using Sn/In and Cu/Ti/Au Metallization. *IEEE Trans. Compon. Packag. Technol.* **2009**, *32*, 926–934. [CrossRef]
8. Tian, R.; Hang, C.; Tian, Y.; Wu, B.; Liu, Y.; Zhao, J. Interfacial Intermetallic Compound Growth in Sn-3Ag-0.5Cu/Cu Solder Joints Induced by Stress Gradient at Cryogenic Temperatures. *J. Alloy. Compd.* **2019**, *800*, 180–190.
9. Made, R.I.; Gan, C.L.; Yan, L.L.; Yu, A.; Yoon, S.W.; Lau, J.H.; Lee, C. Study of Low-Temperature Thermocompression Bonding in Ag-In Solder for Packaging Applications. *J. Electron. Mater.* **2009**, *38*, 365–371. [CrossRef]
10. Tian, R.; Hang, C.; Tian, Y.; Feng, J. Brittle Fracture Induced by Phase Transformation of Ni-Cu-Sn Intermetallic Compounds in Sn-3Ag-0.5Cu/Ni Solder Joints under Extreme Temperature Environment. *J. Alloy. Compd.* **2019**, *777*, 463–471. [CrossRef]
11. Cheng, Z.; Mu, F.; Yates, L.; Suga, T.; Graham, S. Interfacial Thermal Conductance across Room-Temperature-Bonded GaN/Diamond Interfaces for GaN-on-Diamond Devices. *ACS Appl. Mater. Interfaces* **2020**, *12*, 8376–8384. [CrossRef]
12. Mu, F.; Cheng, Z.; Shi, J.; Shin, S.; Xu, B.; Shiomi, J.; Graham, S.; Suga, T. High Thermal Boundary Conductance across Bonded Heterogeneous GaN-SiC Interfaces. *ACS Appl. Mater. Interfaces* **2019**, *11*, 33428–33434. [CrossRef] [PubMed]
13. Kang, Q.; Wang, C.; Zhou, S.; Xu, J.; An, R.; Tian, Y. Fabrication of SiC-on-Insulator Substrate via a Low-Temperature Plasma Activated Bonding Process. In Proceedings of the 2019 20th International Conference Electronic Packaging Technology, Hong Kong, China, 12–15 August 2019; pp. 4–7.
14. Cai, Y.; Qin, Z.; Cui, F.; Li, G.Y.; McCann, J.A. Modulation and Multiple Access for 5G Networks. *IEEE Commun. Surv. Tutor.* **2018**, *20*, 629–646. [CrossRef]
15. Pham, Q.V.; Fang, F.; Ha, V.N.; Piran, M.J.; Le, M.; Le, L.B.; Hwang, W.J.; Ding, Z. A Survey of Multi-Access Edge Computing in 5G and Beyond: Fundamentals, Technology Integration, and State-of-the-Art. *IEEE Access* **2020**, *8*, 116974–117017. [CrossRef]
16. Niu, Y.; Li, Y.; Jin, D.; Su, L.; Vasilakos, A.V. A Survey of Millimeter Wave Communications (MmWave) for 5G: Opportunities and Challenges. *Wirel. Netw.* **2015**, *21*, 2657–2676. [CrossRef]
17. Shi, Q.; Dong, B.; He, T.; Sun, Z.; Zhu, J.; Zhang, Z.; Lee, C. Progress in Wearable Electronics/Photonics—Moving toward the Era of Artificial Intelligence and Internet of Things. *InfoMat* **2020**, *2*, 1131–1162. [CrossRef]

18. Yang, Y.; Lu, R.; Gao, L.; Gong, S. 4.5 GHz Lithium Niobate MEMS Filters With 10% Fractional Bandwidth for 5G Front-Ends. *J. Microelectromech. Syst.* **2019**, *28*, 575–577. [CrossRef]

19. Lu, R.; Yang, Y.; Link, S.; Gong, S. A1 Resonators in 128° Y-Cut Lithium Niobate with Electromechanical Coupling of 46.4%. *J. Microelectromech. Syst.* **2020**, *29*, 313–319. [CrossRef]

20. Zhang, M.; Buscaino, B.; Wang, C.; Shams-Ansari, A.; Reimer, C.; Zhu, R.; Kahn, J.M.; Lončar, M. Broadband Electro-Optic Frequency Comb Generation in a Lithium Niobate Microring Resonator. *Nature* **2019**, *568*, 373–377. [CrossRef]

21. Wang, C.; Zhang, M.; Chen, X.; Bertrand, M.; Shams-Ansari, A.; Chandrasekhar, S.; Winzer, P.; Lončar, M. Integrated Lithium Niobate Electro-Optic Modulators Operating at CMOS-Compatible Voltages. *Nature* **2018**, *562*, 101–104. [CrossRef] [PubMed]

22. Desiatov, B.; Shams-Ansari, A.; Zhang, M.; Wang, C.; Lončar, M. Ultra-Low-Loss Integrated Visible Photonics Using Thin-Film Lithium Niobate. *Optica* **2019**, *6*, 380. [CrossRef]

23. Wen, F.; Sun, Z.; He, T.; Shi, Q.; Zhu, M.; Zhang, Z.; Li, L.; Zhang, T.; Lee, C. Machine Learning Glove Using Self-Powered Conductive Superhydrophobic Triboelectric Textile for Gesture Recognition in VR/AR Applications. *Adv. Sci.* **2020**, *7*, 1–15. [CrossRef]

24. Wen, F.; He, T.; Liu, H.; Chen, H.Y.; Zhang, T.; Lee, C. Advances in Chemical Sensing Technology for Enabling the Next-Generation Self-Sustainable Integrated Wearable System in the IoT Era. *Nano Energy* **2020**, *78*, 105155. [CrossRef]

25. He, T.; Guo, X.; Lee, C. Flourishing Energy Harvesters for Future Body Sensor Network: From Single to Multiple Energy Sources. *iScience* **2021**, *24*, 101934. [CrossRef]

26. Zhu, M.; He, T.; Lee, C. Technologies toward next Generation Human Machine Interfaces: From Machine Learning Enhanced Tactile Sensing to Neuromorphic Sensory Systems. *Appl. Phys. Rev.* **2020**, *7*, 031305. [CrossRef]

27. Shi, Q.; Sun, Z.; Zhang, Z.; Lee, C. Triboelectric Nanogenerators and Hybridized Systems for Enabling Next-Generation IoT Applications. *Research* **2021**, *2021*, 1–30.

28. He, T.; Wang, H.; Wang, J.; Tian, X.; Wen, F.; Shi, Q.; Ho, J.S.; Lee, C. Self-Sustainable Wearable Textile Nano-Energy Nano-System (NENS) for Next-Generation Healthcare Applications. *Adv. Sci.* **2019**, *6*, 1901437. [CrossRef]

29. Zhu, J.; Liu, X.; Shi, Q.; He, T.; Sun, Z.; Guo, X.; Liu, W.; Sulaiman, O.B.; Dong, B.; Lee, C. Development Trends and Perspectives of Future Sensors and MEMS/NEMS. *Micromachines* **2020**, *11*, 7. [CrossRef] [PubMed]

30. Taraschi, G.; Pitera, A.J.; Fitzgerald, E.A. Strained Si, SiGe, and Ge on-Insulator: Review of Wafer Bonding Fabrication Techniques. *Solid. State. Electron.* **2004**, *48*, 1297–1305. [CrossRef]

31. Zhou, J.; Wu, Z.; Han, G.; Kanyang, R.; Peng, Y.; Li, J.; Wang, H.; Liu, Y.; Zhang, J.; Sun, Q.; et al. Frequency Dependence of Performance in Ge Negative Capacitance PFETs Achieving Sub-30 MV/Decade Swing and 110 MV Hysteresis at MHz. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 15.5.1–15.5.4.

32. Maszara, W.P. Silicon-On-Insulator by Wafer Bonding: A Review. *J. Electrochem. Soc.* **1991**, *138*, 341–347. [CrossRef]

33. Maleville, C.; Aspar, B.; Poumeyrol, T.; Moriceau, H.; Bruel, M.; Auberton-Hervè, A.J.; Barge, T. Wafer Bonding and H-Implantation Mechanisms Involved in the Smart-Cut® Technology. *Mater. Sci. Eng. B* **1997**, *46*, 14–19. [CrossRef]

34. Bruel, M.; Aspar, B.; Auberton-Hervé, A.J. Smart-Cut: A New Silicon on Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding. *Jpn. J. Appl. Phys. Part 1 Regul. Pap. Short Notes Rev. Pap.* **1997**, *36*, 1636–1641. [CrossRef]

35. Wang, T.; Lou, L.; Lee, C. A Junctionless Gate-All-Around Silicon Nanowire FET of High Linearity and Its Potential Applications. *IEEE Electron Device Lett.* **2013**, *34*, 478–480. [CrossRef]

36. Zhou, J.; Peng, Y.; Han, G.; Li, Q.; Liu, Y.; Zhang, J.; Liao, M.; Sun, Q.Q.; Zhang, D.W.; Zhou, Y.; et al. Hysteresis Reduction in Negative Capacitance Ge PFETs Enabled by Modulating Ferroelectric Properties in HfZrOx. *IEEE J. Electron Devices Soc.* **2017**, *6*, 41–48. [CrossRef]

37. Zhou, J.; Han, G.; Li, J.; Peng, Y.; Liu, Y.; Zhang, J.; Sun, Q.Q.; Zhang, D.W.; Hao, Y. Comparative Study of Negative Capacitance Ge PFETs with HfZrOx Partially and Fully Covering Gate Region. *IEEE Trans. Electron Devices* **2017**, *64*, 4838–4843. [CrossRef]

38. Zhou, J.; Han, G.; Xu, N.; Li, J.; Peng, Y.; Liu, Y.; Zhang, J.; Sun, Q.Q.; Zhang, D.W.; Hao, Y. Experimental Validation of Depolarization Field Produced Voltage Gains in Negative Capacitance Field-Effect Transistors. *IEEE Trans. Electron Devices* **2019**, *66*, 4419–4424. [CrossRef]

39. Zhou, J.; Han, G.; Xu, N.; Li, J.; Peng, Y.; Liu, Y.; Zhang, J.; Sun, Q.Q.; Zhang, D.W.; Hao, Y. Incomplete Dipoles Flipping Produced Near Hysteresis-Free Negative Capacitance Transistors. *IEEE Electron Device Lett.* **2019**, *40*, 329–332. [CrossRef]

40. Tracy, C.J.; Fejes, P.; Theodore, N.D.; Maniar, P.; Johnson, E.; Lamm, A.J.; Paler, A.M.; Malik, I.J.; Ong, P. Germanium-on-Insulator Substrates by Wafer Bonding. *J. Electron. Mater.* **2004**, *33*, 886–892. [CrossRef]

41. Zhu, J.; Zhu, M.; Shi, Q.; Wen, F.; Liu, L.; Dong, B.; Haroun, A.; Yang, Y.; Vachon, P.; Guo, X.; et al. Progress in TENG Technology—A Journey from Energy Harvesting to Nanoenergy and Nanosystem. *EcoMat* **2020**, *2*, 1–45. [CrossRef]

42. Shi, Q.; Zhang, Z.; He, T.; Sun, Z.; Wang, B.; Feng, Y.; Shan, X.; Salam, B.; Lee, C. Deep Learning Enabled Smart Mats as a Scalable Floor Monitoring System. *Nat. Commun.* **2020**, *11*, 4609. [CrossRef]

43. Chang, Y.; Dong, B.; Ma, Y.; Wei, J.; Ren, Z.; Lee, C. Vernier Effect-Based Tunable Mid-Infrared Sensor Using Silicon-on-Insulator Cascaded Rings. *Opt. Express* **2020**, *28*, 6251. [CrossRef]

44. Wei, J.; Ren, Z.; Lee, C. Metamaterial technologies for miniaturized infrared spectroscopy: Light sources, sensors, filters, detectors and integration. *J. Appl. Phys.* **2020**, *128*, 240901. [CrossRef]

45. Ren, Z.; Chang, Y.; Ma, Y.; Shih, K.; Dong, B.; Lee, C. Leveraging of MEMS Technologies for Optical Metamaterials Applications. *Adv. Opt. Mater.* **2020**, *8*, 1900653. [CrossRef]

46. Chang, Y.; Hasan, D.; Dong, B.; Wei, J.; Ma, Y.; Zhou, G.; Ang, K.W.; Lee, C. All-Dielectric Surface-Enhanced Infrared Absorption-Based Gas Sensor Using Guided Resonance. *ACS Appl. Mater. Interfaces* **2018**, *10*, 38272–38279. [CrossRef]

47. Ma, Y.; Dong, B.; Li, B.; Ang, K.-W.; Lee, C. Dispersion Engineering and Thermo-Optic Tuning in Mid-Infrared Photonic Crystal Slow Light Waveguides on Silicon-on-Insulator. *Opt. Lett.* **2018**, *43*, 5504. [CrossRef] [PubMed]

48. Ma, Y.; Dong, B.; Lee, C. Progress of Infrared Guided-Wave Nanophotonic Sensors and Devices. *Nano Converg.* **2020**, *7*, 12. [CrossRef] [PubMed]

49. Sun, F.; Dong, B.; Wei, J.; Ma, Y.; Tian, H.; Lee, C. Demonstration of Mid-Infrared Slow Light One-Dimensional Photonic Crystal Ring Resonator with High-Order Photonic Bandgap. *Opt. Express* **2020**, *28*, 30736. [CrossRef]

50. Yazici, M.S.; Dong, B.; Hasan, D.; Sun, F.; Lee, C. Integration of MEMS IR Detectors with MIR Waveguides for Sensing Applications. *Opt. Express* **2020**, *28*, 11524. [CrossRef]

51. Qin, X.; Peng, Y.; Li, P.; Cheng, K.; Wei, Z.; Liu, P.; Cao, N.; Huang, J.; Rao, J.; Chen, J.; et al. Silk Fibroin and Ultra-Long Silver Nanowire Based Transparent, Flexible and Conductive Composite Film and Its Temperature-Dependent Resistance. *Int. J. Optomechatron.* **2019**, *13*, 41–50. [CrossRef]

52. Liu, W.; Ma, Y.; Chang, Y.; Dong, B.; Wei, J.; Ren, Z.; Lee, C. Suspended Silicon Waveguide Platform with Subwavelength Grating Metamaterial Cladding for Long-Wave Infrared Sensing Applications. *Nanophotonics* **2021**, *10*, 1861–1870. [CrossRef]

53. Qiao, Q.; Yazici, M.S.; Dong, B.; Liu, X.; Lee, C.; Zhou, G. Multifunctional Mid-Infrared Photonic Switch Using a MEMS-Based Tunable Waveguide Coupler. *Opt. Lett.* **2020**, *45*, 5620. [CrossRef]

54. Ma, Y.; Dong, B.; Wei, J.; Chang, Y.; Huang, L.; Ang, K.W.; Lee, C. High-Responsivity Mid-Infrared Black Phosphorus Slow Light Waveguide Photodetector. *Adv. Opt. Mater.* **2020**, *8*, 1–12. [CrossRef]

55. Lei, D.; Lee, K.H.; Bao, S.; Wang, W.; Wang, B.; Gong, X.; Tan, C.S.; Yeo, Y.C. GeSn-on-Insulator Substrate Formed by Direct Wafer Bonding. *Appl. Phys. Lett.* **2016**, *109*, 2–6. [CrossRef]

56. Lei, D.; Lee, K.H.; Bao, S.; Wang, W.; Masudy-Panah, S.; Yadav, S.; Kumar, A.; Dong, Y.; Kang, Y.; Xu, S.; et al. The first GeSn FinFET on a novel GeSnOI substrate achieving lowest S of 79 mV/decade and record high Gm, int of 807 μs/μm for GeSn P-FETs. In Proceedings of the 2017 Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017; pp. T198–T199.

57. Huang, L.J.; Chu, J.O.; Canaperi, D.F.; D'Emic, C.P.; Anderson, R.M.; Koester, S.J.; Wong, H.S.P. SiGe-on-Insulator Prepared by Wafer Bonding and Layer Transfer for High-Performance Field-Effect Transistors. *Appl. Phys. Lett.* **2001**, *78*, 1267–1269. [CrossRef]

58. Langdo, T.A.; Currie, M.T.; Lochtefeld, A.; Hammond, R.; Carlin, J.A.; Erdtmann, M.; Braithwaite, G.; Yang, V.K.; Vineis, C.J.; Badawi, H.; et al. SiGe-Free Strained Si on Insulator by Wafer Bonding and Layer Transfer. *Appl. Phys. Lett.* **2003**, *82*, 4256–4258. [CrossRef]

59. Zhou, J.; Han, G.; Peng, Y.; Liu, Y.; Zhang, J.; Sun, Q.Q.; Zhang, D.W.; Hao, Y. Ferroelectric Negative Capacitance GeSn PFETs With Sub-20 MV/Decade Subthreshold Swing. *IEEE Electron Device Lett.* **2017**, *38*, 1157–1160. [CrossRef]

60. Zhou, J.; Han, G.; Li, Q.; Peng, Y.; Lu, X.; Zhang, C.; Zhang, J. Ferroelectric HfZrO x Ge and GeSn PMOSFETs with Sub-60 MV/Decade Subthreshold Swing, Negligible Hysteresis, and Improved I DS. In *2016 IEEE International Electron Devices Meeting (IEDM)*; IEEE: New York, NY, USA, 2016; pp. 310–313.

61. Xu, S.; Han, K.; Huang, Y.C.; Kang, Y.; Masudy-Panah, S.; Wu, Y.; Lei, D.; Zhao, Y.; Gong, X.; Yeo, Y.C. High Performance GeSn Photodiode on a 200 Mm Ge-on-Insulator Photonics Platform for Advanced Optoelectronic Integration with Ge CMOS Operating at 2 Mm Band. In Proceedings of the 2019 Symposium on VLSI Technology, Kyoto, Japan, 9–14 June 2019; pp. T176–T177.

62. Xu, J.; Wang, C.; Ji, X.; An, Q.; Tian, Y.; Suga, T. Direct Bonding of High Dielectric Oxides for High-Performance Transistor Applications. *Scr. Mater.* **2020**, *178*, 307–312. [CrossRef]

63. Xu, J.; Wang, C.; Wang, T.; Liu, Y.; Tian, Y. Direct Bonding of Silicon and Quartz Glass Using VUV/O3 Activation and a Multistep Low-Temperature Annealing Process. *Appl. Surf. Sci.* **2018**, *453*, 416–422. [CrossRef]

64. Xu, J.; Wang, C.; Li, D.; Cheng, J.; Wang, Y.; Hang, C.; Tian, Y. Fabrication of SiC/Si, SiC/SiO$_2$, and SiC/Glass Heterostructures via VUV/O$_3$ Activated Direct Bonding at Low Temperature. *Ceram. Int.* **2019**, *45*, 4094–4098. [CrossRef]

65. Xu, J.; Wang, C.; Kang, Q.; Zhou, S.; Tian, Y. Direct Heterogeneous Bonding of SiC to Si, SiO$_2$, and Glass for High-Performance Power Electronics and Bio-MEMS. In Proceedings of the 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA; 2019; pp. 1266–1271.

66. Xu, J.; Wu, B. VUV/O$_3$ Activated Bonder for Low-Temperature Direct Bonding of Si-Based Materials. In Proceedings of the 2018 19th International Conference on Electronic Packaging Technology (ICEPT), Shanghai, China, 8–11 August 2018; pp. 1448–1452.

67. Xu, J.; Wang, C.; Tian, Y.; Wu, B.; Wang, S.; Zhang, H. Glass-on-LiNbO$_3$ Heterostructure Formed via a Two-Step Plasma Activated Low-Temperature Direct Bonding Method. *Appl. Surf. Sci.* **2018**, *459*, 621–629. [CrossRef]

68. Wang, C.; Xu, J.; Guo, S.; Kang, Q.; Wang, Y.; Wang, Y.; Tian, Y. A Facile Method for Direct Bonding of Single-Crystalline SiC to Si, SiO$_2$, and Glass Using VUV Irradiation. *Appl. Surf. Sci.* **2019**, *471*, 196–204. [CrossRef]

69. Xu, J.; Wang, C.; Zhang, R.; Cheng, J.; Li, G.; Xiang, J.; Tian, Y. VUV/O$_3$ Activated Direct Heterogeneous Bonding towards High-Performance LiNbO$_3$-Based Optical Devices. *Appl. Surf. Sci.* **2019**, *495*, 1–11. [CrossRef]

70. Xu, J.; Wang, C.; Wu, B.; Tian, Y.; Qi, X. Communication—Defect-Free Direct Bonding for High-Performance Glass-On-LiNbO$_3$ Devices. *J. Electrochem. Soc.* **2018**, *165*, B727–B729. [CrossRef]

71. Xu, J.; Wang, C.; Wang, T.; Wang, Y.; Kang, Q.; Liu, Y.; Tian, Y. Mechanisms for Low-Temperature Direct Bonding of Si/Si and Quartz/Quartz: Via VUV/O_3 Activation. *RSC Adv.* **2018**, *8*, 11528–11535. [CrossRef]

72. Mu, F.; He, R.; Suga, T. Room Temperature GaN-Diamond Bonding for High-Power GaN-on-Diamond Devices. *Scr. Mater.* **2018**, *150*, 148–151. [CrossRef]

73. Takigawa, R.; Utsumi, J. Direct Bonding of LiNbO3 and SiC Wafers at Room Temperature. *Scr. Mater.* **2020**, *174*, 58–61. [CrossRef]

74. Xu, J.; Wang, C.; Zhou, S.; Zhang, R.; Tian, Y. Low-Temperature Direct Bonding of Si and Quartz Glass Using the APTES Modification. *Ceram. Int.* **2019**, *45*, 16670–16675. [CrossRef]

75. Klinkert, C.; Szabó, Á.; Stieger, C.; Campi, D.; Marzari, N.; Luisier, M. 2-D Materials for Ultrascaled Field-Effect Transistors: One Hundred Candidates under the Ab Initio Microscope. *ACS Nano* **2020**, *14*, 8605–8615. [CrossRef]

76. Zhao, J.; Occhipinti, L.G.; Anthopoulos, T.D.; Pecunia, V.; Portilla, L.; Wang, Y.; Sun, L.; Li, F.; Robin, M.; Wei, M.; et al. Ambipolar Deep-Subthreshold Printed-Carbon-Nanotube Transistors for Ultralow-Voltage and Ultralow-Power Electronics. *ACS Nano* **2020**, *14*, 14036–14046.

77. Si, M.; Andler, J.; Lyu, X.; Niu, C.; Datta, S.; Agrawal, R.; Ye, P.D. Indium-Tin-Oxide Transistors with One Nanometer Thick Channel and Ferroelectric Gating. *ACS Nano* **2020**, *14*, 11542–11547. [CrossRef] [PubMed]

78. Dai, T.; Chen, C.; Huang, L.; Jiang, J.; Peng, L.M.; Zhang, Z. Ultrasensitive Magnetic Sensors Enabled by Heterogeneous Integration of Graphene Hall Elements and Silicon Processing Circuits. *ACS Nano* **2020**, *14*, 17606–17614. [CrossRef] [PubMed]

79. Tedeschi, D.; Fonseka, H.A.; Blundo, E.; Granados Del Águila, A.; Guo, Y.; Tan, H.H.; Christianen, P.C.M.; Jagadish, C.; Polimeni, A.; de Luca, M. Hole and Electron Effective Masses in Single InP Nanowires with a Wurtzite-Zincblende Homojunction. *ACS Nano* **2020**, *14*, 11613–11622. [CrossRef]

80. Jiménez, J.J.; Mánuel, J.M.; Bartsch, H.; Breiling, J.; García, R.; Jacobs, H.O.; Müller, J.; Pezoldt, J.; Morales, F.M. Comprehensive (S)TEM Characterization of Polycrystalline GaN/AlN Layers Grown on LTCC Substrates. *Ceram. Int.* **2019**, *45*, 9114–9125. [CrossRef]

81. Ohno, Y.; Liang, J.; Shigekawa, N.; Yoshida, H.; Takeda, S.; Miyagawa, R.; Shimizu, Y.; Nagai, Y. Chemical Bonding at Room Temperature via Surface Activation to Fabricate Low-Resistance GaAs/Si Heterointerfaces. *Appl. Surf. Sci.* **2020**, *525*, 146610. [CrossRef]

82. Mu, F.; Morino, Y.; Jerchel, K.; Fujino, M.; Suga, T. GaN-Si Direct Wafer Bonding at Room Temperature for Thin GaN Device Transfer after Epitaxial Lift Off. *Appl. Surf. Sci.* **2017**, *416*, 1007–1012. [CrossRef]

83. Liang, Y.; Li, C.; Huang, Y.Z.; Zhang, Q. Plasmonic Nanolasers in On-Chip Light Sources: Prospects and Challenges. *ACS Nano* **2020**, *14*, 14375–14390. [CrossRef]

84. Luo, X.; Cao, Y.; Song, J.; Hu, X.; Cheng, Y.; Li, C.; Liu, C.; Liow, T.Y.; Yu, M.; Wang, H.; et al. High-Throughput Multiple Dies-to-Wafer Bonding Technology and III/V-on-Si Hybrid Lasers for Heterogeneous Integration of Optoelectronic Integrated Circuits. *Front. Mater.* **2015**, *2*, 1–21. [CrossRef]

85. Lee, K.H.; Wang, Y.; Wang, B.; Zhang, L.; Sasangka, W.A.; Goh, S.C.; Bao, S.; Lee, K.E.; Fitzgerald, E.A.; Tan, C.S. Monolithic Integration of Si-CMOS and III-V-on-Si through Direct Wafer Bonding Process. *IEEE J. Electron Devices Soc.* **2017**, *6*, 571–578. [CrossRef]

86. Khayrudinov, V.; Remennyi, M.; Raj, V.; Alekseev, P.; Matveev, B.; Lipsanen, H.; Haggren, T.; Haggren, T. Direct Growth of Light-Emitting III-V Nanowires on Flexible Plastic Substrates. *ACS Nano* **2020**, *14*, 7484–7491. [CrossRef]

87. Bao, S.; Wang, Y.; Lina, K.; Zhang, L.; Wang, B.; Sasangka, W.A.; Lee, K.E.K.; Chua, S.J.; Michel, J.; Fitzgerald, E.; et al. A Review of Silicon-Based Wafer Bonding Processes, an Approach to Realize the Monolithic Integration of Si-CMOS and III-V-on-Si Wafers. *J. Semicond.* **2021**, *42*, 023106. [CrossRef]

88. Lin, J.; You, T.; Jin, T.; Liang, H.; Wan, W.; Huang, H.; Zhou, M.; Mu, F.; Yan, Y.; Huang, K.; et al. Wafer-Scale Heterogeneous Integration InP on Trenched Si with a Bubble-Free Interface. *APL Mater.* **2020**, *8*, 051110. [CrossRef]

89. Shi, H.; Huang, K.; Mu, F.; You, T.; Ren, Q.; Lin, J.; Xu, W.; Jin, T.; Huang, H.; Yi, A.; et al. Realization of Wafer-Scale Single-Crystalline GaN Film on CMOS-Compatible Si(100) Substrate by Ion-Cutting Technique. *Semicond. Sci. Technol.* **2020**, *35*, 125004. [CrossRef]

90. Xu, W.; Wang, X.; Wang, Y.; You, T.; Ou, X.; Han, G.; Hu, H.; Zhang, S.; Mu, F.; Suga, T.; et al. First Demonstration of Waferscale Heterogeneous Integration of Ga_2O_3 MOSFETs on SiC and Si Substrates by Ion-Cutting Process. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 274–277.

91. Ren, K.; Liang, Y.C.; Huang, C.F. Physical Mechanism on the Suppression of Dynamic Resistance Degradation by Multi-Mesa-Channel in AlGaN/GaN High Electron Mobility Transistors. *Appl. Phys. Lett.* **2019**, *115*, 262101. [CrossRef]

92. Li, H.; Xiang, H.; Huang, H.; Zeng, Z.; Peng, X. Interface Structure and Deformation Mechanisms of AlN/GaN Multilayers. *Ceram. Int.* **2020**, *46*, 11556–11562. [CrossRef]

93. Li, N.; Labat, S.; Leake, S.J.; Dupraz, M.; Carnis, J.; Cornelius, T.W.; Beutier, G.; Verdier, M.; Favre-Nicolin, V.; Schülli, T.U.; et al. Mapping Inversion Domain Boundaries along Single GaN Wires with Bragg Coherent X-ray Imaging. *ACS Nano* **2020**, *14*, 10305–10312. [CrossRef] [PubMed]

94. Matsumae, T.; Fengwen, M.; Fukumoto, S.; Hayase, M.; Kurashima, Y.; Higurashi, E.; Takagi, H.; Suga, T. Heterogeneous GaN-Si Integration via Plasma Activation Direct Bonding. *J. Alloy. Compd.* **2021**, *852*, 156933. [CrossRef]

95. Yang, H.; Qian, Y.; Zhang, C.; Wuu, D.S.; Talwar, D.N.; Lin, H.H.; Lee, J.F.; Wan, L.; He, K.; Feng, Z.C. Surface/Structural Characteristics and Band Alignments of Thin Ga_2O_3 Films Grown on Sapphire by Pulse Laser Deposition. *Appl. Surf. Sci.* **2019**, *479*, 1246–1253. [CrossRef]

96. Lee, H.K.; Yun, H.J.; Shim, K.H.; Park, H.G.; Jang, T.H.; Lee, S.N.; Choi, C.J. Improvement of Dry Etch-Induced Surface Roughness of Single Crystalline β-Ga_2O_3 Using Post-Wet Chemical Treatments. *Appl. Surf. Sci.* **2020**, *506*, 144673. [CrossRef]

97. Yuan, H.; Su, J.; Guo, R.; Tian, K.; Lin, Z.; Zhang, J.; Chang, J.; Hao, Y. Contact Barriers Modulation of Graphene/β-Ga_2O_3 Interface for High-Performance Ga_2O_3 Devices. *Appl. Surf. Sci.* **2020**, *527*, 146740. [CrossRef]

98. Xiao, Y.; Liu, W.; Liu, C.; Yu, H.; Liu, H.; Han, J.; Liu, W.; Zhang, W.; Wu, X.; Ding, S.; et al. Large-Area Vertically Stacked MoTe2/β-Ga_2O_3 p-n Heterojunction Realized by PVP/PVA Assisted Transfer. *Appl. Surf. Sci.* **2020**, *530*, 147276. [CrossRef]

99. Rodrigues, A.V.; Orlandi, M.O. Study of Intense Photoluminescence from Monodispersed β-Ga_2O_3 Ellipsoidal Structures. *Ceram. Int.* **2019**, *45*, 5023–5029. [CrossRef]

100. Wang, D.; He, L.; Le, Y.; Feng, X.; Luan, C.; Xiao, H.; Ma, J. Characterization of Single Crystal β-Ga_2O_3 Films Grown on $SrTiO_3$ (100) Substrates by MOCVD. *Ceram. Int.* **2020**, *46*, 4568–4572. [CrossRef]

101. Jiang, J.; Zhang, J. Temperature-Resolved Photoluminescence, Raman and Electrical Properties of Li Doped Ga_2O_3 Nanostructure. *Ceram. Int.* **2020**, *46*, 2409–2412. [CrossRef]

102. Wang, Y.B.; Xu, W.H.; You, T.G.; Mu, F.W.; Hu, H.D.; Liu, Y.; Huang, H.; Suga, T.; Han, G.Q.; Ou, X.; et al. β-Ga_2O_3 MOSFETs on the Si Substrate Fabricated by the Ion-Cutting Process. *Sci. China Phys. Mech. Astron.* **2020**, *63*, 1–4. [CrossRef]

103. Zeng, C.; Shen, J.; He, C.; Chen, H. High Thermal Conductivity in Bi-In-Sn/Diamond Composites. *Scr. Mater.* **2019**, *170*, 140–144. [CrossRef]

104. Wang, K.; Ruan, K.; Hu, W.; Wu, S.; Wang, H. Room Temperature Bonding of GaN on Diamond Wafers by Using Mo/Au Nano-Layer for High-Power Semiconductor Devices. *Scr. Mater.* **2020**, *174*, 87–90. [CrossRef]

105. Mu, F.; Xu, Y.; Shin, S.; Wang, Y.; Xu, H.; Shang, H.; Sun, Y.; Yue, L.; Tsuyuki, T.; Suga, T.; et al. Wafer Bonding of SiC-AlN at Room Temperature for All-SiC Capacitive Pressure Sensor. *Micromachines* **2019**, *10*, 635. [CrossRef] [PubMed]

106. Mu, F.; Uomoto, M.; Shimatsu, T.; Wang, Y.; Iguchi, K.; Nakazawa, H.; Takahashi, Y.; Higurashi, E.; Suga, T. De-Bondable SiC–SiC Wafer Bonding via an Intermediate Ni Nano-Film. *Appl. Surf. Sci.* **2019**, *465*, 591–595. [CrossRef]

107. Zhang, L.; Diallo, L.; Fnidiki, A.; Lechevallier, L.; Declémy, A.; Lefebvre, W.; Juraszek, J. Probing the Origins of Magnetism in 2 At% Fe-Implanted 4H-SiC. *Scr. Mater.* **2020**, *188*, 157–163. [CrossRef]

108. Kondo, S.; Seki, K.; Maeda, Y.; Yu, H.; Fukami, K.; Kasada, R. Contribution of Dangling-Bonds to Polycrystalline SiC Corrosion. *Scr. Mater.* **2020**, *188*, 6–9. [CrossRef]

109. Olson, D.H.; Gaskins, J.T.; Tomko, J.A.; Opila, E.J.; Golden, R.A.; Harrington, G.J.K.; Chamberlain, A.L.; Hopkins, P.E. Local Thermal Conductivity Measurements to Determine the Fraction of α-Cristobalite in Thermally Grown Oxides for Aerospace Applications. *Scr. Mater.* **2020**, *177*, 214–217. [CrossRef]

110. Lee, E.; Luo, T. Thermal Transport across Solid-Solid Interfaces Enhanced by Pre-Interface Isotope-Phonon Scattering. *Appl. Phys. Lett.* **2018**, *112*, 011603. [CrossRef]

111. Ziade, E.; Yang, J.; Brummer, G.; Nothern, D.; Moustakas, T.; Schmidt, A.J. Thermal Transport through GaN-SiC Interfaces from 300 to 600 K. *Appl. Phys. Lett.* **2015**, *107*, 1–5. [CrossRef]

112. Xu, J.; Du, Y.; Tian, Y.; Wang, C. Progress in Wafer Bonding Technology towards MEMS, High-Power Electronics, Optoelectronics, and Optofluidics. *Int. J. Optomechatron.* **2020**, *14*, 94–118. [CrossRef]

113. Ko, C.T.; Chen, K.N. Wafer-Level Bonding/Stacking Technology for 3D Integration. *Microelectron. Reliab.* **2010**, *50*, 481–488. [CrossRef]

114. Gijsele, U. Invited Review Semiconductor. *Interface* **1994**, *37*, 101–127.

115. You, A.; Be, M.A.Y.; In, I. Fundamental Issues in Wafer Bonding. *J. Vac. Sci. Technol. A Vac. Surf. Film.* **2013**, *17*, 1145–1152.

116. Kang, Q.; Wang, C.; Niu, F.; Zhou, S.; Xu, J.; Tian, Y. Single-Crystalline SiC Integrated onto Si-Based Substrates via Plasma-Activated Direct Bonding. *Ceram. Int.* **2020**, *46*, 22718–22726. [CrossRef]

117. Xu, Y.; Wang, S.K.; Yao, P.; Wang, Y.; Chen, D. An Air-Plasma Enhanced Low-Temperature Wafer Bonding Method Using High-Concentration Water Glass Adhesive Layer. *Appl. Surf. Sci.* **2020**, *500*, 144007. [CrossRef]

118. Li, W.; Liang, T.; Liu, W.; Lei, C.; Hong, Y.; Li, Y.; Li, Z.; Xiong, J. Interface Characteristics Comparison of Sapphire Direct and Indirect Wafer Bonded Structures by Transmission Electron Microscopy. *Appl. Surf. Sci.* **2019**, *494*, 566–574. [CrossRef]

119. Masteika, V.; Kowal, J.; Braithwaite, N.S.J.; Rogers, T. A Review of Hydrophilic Silicon Wafer Bonding. *ECS J. Solid State Sci. Technol.* **2014**, *3*, Q42–Q54. [CrossRef]

120. Matsumae, T.; Kurashima, Y.; Umezawa, H.; Takagi, H. Hydrophilic Low-Temperature Direct Bonding of Diamond and Si Substrates under Atmospheric Conditions. *Scr. Mater.* **2020**, *175*, 24–28. [CrossRef]

121. Cheng, Z.; Mu, F.; You, T.; Xu, W.; Shi, J.; Liao, M.E.; Wang, Y.; Huynh, K.; Suga, T.; Goorsky, M.S.; et al. Thermal Transport across Ion-Cut Monocrystalline β-Ga_2O_3 Thin Films and Bonded β-Ga_2O_3-SiC Interfaces. *ACS Appl. Mater. Interfaces* **2020**, *12*, 44943–44951. [CrossRef]

122. Xu, Y.; Mu, F.; Wang, Y.; Chen, D.; Ou, X.; Suga, T. Direct Wafer Bonding of Ga_2O_3–SiC at Room Temperature. *Ceram. Int.* **2019**, *45*, 6552–6555. [CrossRef]

123. Sun, Z.; Zhu, M.; Zhang, Z.; Chen, Z.; Shi, Q.; Shan, X.; Yeow, R.C.H.; Lee, C. Artificial Intelligence of Things (AIoT) Enabled Virtual Shop Applications Using Self-Powered Sensor Enhanced Soft Robotic Manipulator. *Adv. Sci.* **2021**, *8*, 2100230. [CrossRef]

124. Zhang, Z.; He, T.; Zhu, M.; Sun, Z.; Shi, Q.; Zhu, J.; Dong, B.; Yuce, M.R.; Lee, C. Deep Learning-Enabled Triboelectric Smart Socks for IoT-Based Gait Analysis and VR Applications. *NPJ Flex. Electron.* **2020**, *4*, 1–12. [CrossRef]

125. Zhu, M.; Sun, Z.; Zhang, Z.; Shi, Q.; He, T.; Liu, H.; Chen, T.; Lee, C. Haptic-Feedback Smart Glove as a Creative Human-Machine Interface (HMI) for Virtual/Augmented Reality Applications. *Sci. Adv.* **2020**, *6*, 1–15. [CrossRef] [PubMed]

126. Wang, J.; He, T.; Lee, C. Development of neural interfaces and energy harvesters towards self-powered implantable systems for healthcare monitoring and rehabilitation purposes. *Nano Energy* **2019**, *65*, 104039. [CrossRef]

127. Anaya, D.V.; He, T.; Lee, C.; Yuce, M.R. Self-powered eye motion sensor based on triboelectric interaction and near-field electrostatic induction for wearable assistive technologies. *Nano Energy* **2020**, *72*, 104675. [CrossRef]

128. Hassani, F.A.; Shi, Q.; Wen, F.; He, T.; Haroun, A.; Yang, T.; Feng, Y.; Lee, C. Smart materials for smart healthcare-moving from sensors and actuators to self-sustained nanoenergy nanosystems. *Smart Mater. Med.* **2020**, *1*, 92–124.

129. Cho, Y.; Park, J.; Lee, C.; Lee, S. Recent progress on peripheral neural interface technology towards bioelectronic medicine. *Bioelectron. Med.* **2020**, *6*, 23.

130. Liu, L.; Guo, X.; Lee, C. Promoting smart cities into the 5G era with multi-field Internet of Things (IoT) applications powered with advanced mechanical energy harvesters. *Nano Energy* **2021**, *88*, 106304. [CrossRef]

131. Wen, F.; Wang, H.; He, T.; Shi, Q.; Sun, Z.; Zhu, M.; Zhang, Z.; Cao, Z.; Dai, Y.; Zhang, T.; et al. Battery-Free Short-Range Self-Powered Wireless Sensor Network (SS-WSN) Using TENG Based Direct Sensory Transmission (TDST) Mechanism. *Nano Energy* **2020**, *67*, 104266. [CrossRef]

132. Zhu, M.; Sun, Z.; Chen, T.; Lee, C. Low Cost Exoskeleton Manipulator Using Bidirectional Triboelectric Sensors Enhanced Multiple Degree of Freedom Sensory System. *Nat. Commun.* **2021**, *12*, 1–16. [CrossRef]

133. Zhang, Q.; Liang, Q.; Nandakumar, D.K.; Qu, H.; Shi, Q.; Alzakia, F.I.; Tay, D.J.J.; Yang, L.; Zhang, X.; Suresh, L.; et al. Shadow Enhanced Self-Charging Power System for Wave and Solar Energy Harvesting from the Ocean. *Nat. Commun.* **2021**, *12*, 1–11.

134. Hu, G.; Yi, Z.; Lu, L.; Huang, Y.; Zhai, Y.; Liu, J.; Yang, B. Self-Powered 5G NB-IoT System for Remote Monitoring Applications. *Nano Energy* **2021**, *87*, 106140. [CrossRef]

135. Dong, X.; Yi, Z.; Kong, L.; Tian, Y.; Liu, J.; Yang, B. Design, Fabrication, and Characterization of Bimorph Micromachined Harvester with Asymmetrical PZT Films. *J. Microelectromech. Syst.* **2019**, *28*, 700–706. [CrossRef]

136. Lu, L.; Jiang, C.; Hu, G.; Liu, J.; Yang, B. Flexible Noncontact Sensing for Human–Machine Interaction. *Adv. Mater.* **2021**, *33*, 1–10.

137. Funakubo, H.; Dekkers, M.; Sambri, A.; Gariglio, S.; Shklyarevskiy, I.; Rijnders, G. Epitaxial PZT Films for MEMS Printing Applications. *MRS Bull.* **2012**, *37*, 1030–1038. [CrossRef]

138. Kim, S.G.; Priya, S.; Kanno, I. Piezoelectric MEMS for Energy Harvesting. *MRS Bull.* **2012**, *37*, 1039–1050. [CrossRef]

139. Shibata, K.; Wang, R.; Tou, T.; Koruza, J. Applications of Lead-Free Piezoelectric Materials. *MRS Bull.* **2018**, *43*, 612–616. [CrossRef]

140. Eom, C.B.; Trolier-McKinstry, S. Thin-Fi lm Piezoelectric MEMS. *MRS Bull.* **2012**, *37*, 1007–1017. [CrossRef]

141. Rödel, J.; Li, J.F. Lead-Free Piezoceramics: Status and Perspectives. *MRS Bull.* **2018**, *43*, 576–580. [CrossRef]

142. Wang, K.; Malič, B.; Wu, J. Shifting the Phase Boundary: Potassium Sodium Niobate Derivates. *MRS Bull.* **2018**, *43*, 607–611. [CrossRef]

143. Damjanovic, D.; Rossetti, G.A. Strain Generation and Energy-Conversion Mechanisms in Lead-Based and Lead-Free Piezoceramics. *MRS Bull.* **2018**, *43*, 588–594. [CrossRef]

144. Hu, W.; Kalantar-Zadeh, K.; Gupta, K.; Liu, C.P. Piezotronic Materials and Large-Scale Piezotronics Array Devices. *MRS Bull.* **2018**, *43*, 936–940. [CrossRef]

145. Dagdeviren, C.; Yang, B.D.; Su, Y.; Tran, P.L.; Joe, P.; Anderson, E.; Xia, J.; Doraiswamy, V.; Dehdashti, B.; Feng, X.; et al. Conformal Piezoelectric Energy Harvesting and Storage from Motions of the Heart, Lung, and Diaphragm. *Proc. Natl. Acad. Sci. USA* **2014**, *111*, 1927–1932. [CrossRef]

146. Song, E.; Li, J.; Won, S.M.; Bai, W.; Rogers, J.A. Materials for Flexible Bioelectronic Systems as Chronic Neural Interfaces. *Nat. Mater.* **2020**, *19*, 590–603. [CrossRef]

147. Li, N.; Yi, Z.; Ma, Y.; Xie, F.; Huang, Y.; Tian, Y.; Dong, X.; Liu, Y.; Shao, X.; Li, Y.; et al. Direct Powering a Real Cardiac Pacemaker by Natural Energy of a Heartbeat. *ACS Nano* **2019**, *13*, 2822–2830. [CrossRef] [PubMed]

148. Wang, C.; Zhang, M.; Lončar, M. High- Q Lithium Niobate Microcavities. *Ultra-High-Q Opt. Microcavities* **2020**, *1*, 1–35.

149. Holzgrafe, J.; Sinclair, N.; Zhu, D.; Shams-Ansari, A.; Colangelo, M.; Hu, Y.; Zhang, M.; Berggren, K.K.; Lončar, M. Cavity Electro-Optics in Thin-Film Lithium Niobate for Efficient Microwave-to-Optical Transduction. *Optica* **2020**, *7*, 1714–1720. [CrossRef]

150. Yesilkoy, F.; Arvelo, E.R.; Jahani, Y.; Liu, M.; Tittl, A.; Cevher, V.; Kivshar, Y.; Altug, H. Ultrasensitive Hyperspectral Imaging and Biodetection Enabled by Dielectric Metasurfaces. *Nat. Photonics* **2019**, *13*, 390–396. [CrossRef]

151. Wei, J.; Li, Y.; Wang, L.; Liao, W.; Dong, B.; Xu, C.; Zhu, C.; Ang, K.-W.; Qiu, C.-W.; Lee, C. Zero-Bias Mid-Infrared Graphene Photodetectors with Bulk Photoresponse and Calibration-Free Polarization Detection. *Nat. Commun.* **2020**, *11*, 6404. [CrossRef] [PubMed]

152. Rodrigo, D.; Tittl, A.; Ait-bouziad, N.; John-herpin, A.; Limaj, O.; Kelly, C.; Yoo, D.; Wittenberg, N.J.; Oh, S.; Lashuel, H.A.; et al. Resolving molecule-specific information in dynamic lipid membrane processes with multi-resonant infrared metasurfaces. *Nat. Commun.* **2018**, *9*, 2160. [CrossRef]

153. Leitis, A.; Tittl, A.; Liu, M.; Lee, B.H.; Gu, M.B.; Kivshar, Y.S.; Altug, H. Angle-Multiplexed All-Dielectric Metasurfaces for Broadband Molecular Fingerprint Retrieval. *Sci. Adv.* **2019**, *5*, eaaw2871. [CrossRef] [PubMed]

154. Tittl, A.; Leitis, A.; Liu, M.; Yesilkoy, F.; Choi, D.-Y.; Neshev, D.N.; Kivshar, Y.S.; Altug, H. Imaging-Based Molecular Barcoding with Pixelated Dielectric Metasurfaces. *Science* **2018**, *360*, 1105–1109. [CrossRef] [PubMed]

155. Rodrigo, D.; Limaj, O.; Janner, D.; Etezadi, D.; De Abajo, F.J.G.; Pruneri, V.; Altug, H. Mid-Infrared Plasmonic Biosensing with Graphene. *Science* **2015**, *349*, 165–168. [CrossRef]

156. Dong, B.; Hu, T.; Luo, X.; Chang, Y.; Guo, X.; Wang, H.; Kwong, D.L.; Lo, G.Q.; Lee, C. Wavelength-Flattened Directional Coupler Based Mid-Infrared Chemical Sensor Using Bragg Wavelength in Subwavelength Grating Structure. *Nanomaterials* **2018**, *8*, 893. [CrossRef] [PubMed]

157. Dong, B.; Luo, X.; Hu, T.; Guo, T.X.; Wang, H.; Kwong, D.L.; Lo, P.G.Q.; Lee, C. Compact Low Loss Mid-Infrared Wavelength-Flattened Directional Coupler (WFDC) for Arbitrary Power Splitting Ratio Enabled by Rib Waveguide Dispersion Engineering. *IEEE J. Sel. Top. Quantum Electron.* **2018**, *24*, 1–8. [CrossRef]

158. Dong, B.; Luo, X.; Zhu, S.; Hu, T.; Li, M.; Hasan, D.; Zhang, L.; Chua, S.J.; Wei, J.; Chang, Y.; et al. Thermal Annealing Study of the Mid-Infrared Aluminum Nitride on Insulator (AlNOI) Photonics Platform. *Opt. Express* **2019**, *27*, 19815. [CrossRef]

159. Dong, B.; Ma, Y.; Ren, Z.; Lee, C. Recent Progress in Nanoplasmonics-Based Integrated Optical Micro/Nano-Systems. *J. Phys. D Appl. Phys.* **2020**, *53*, 213001. [CrossRef]

160. Wei, J.; Lee, C. Anomalous Plasmon Hybridization in Nanoantennas near Interfaces. *Opt. Lett.* **2019**, *44*, 6041. [CrossRef] [PubMed]

161. Wei, J.; Li, Y.; Chang, Y.; Hasan, D.M.N.; Dong, B.; Ma, Y.; Qiu, C.-W.; Lee, C. Ultrasensitive Transmissive Infrared Spectroscopy via Loss Engineering of Metallic Nanoantennas for Compact Devices. *ACS Appl. Mater. Interfaces* **2019**, *11*, 47270–47278. [CrossRef] [PubMed]

162. Shih, K.; Ren, Z.; Wang, C.; Lee, C. MIR Plasmonic Liquid Sensing in Nano-Metric Space Driven by Capillary Force. *J. Phys. D Appl. Phys.* **2019**, *52*, 394001. [CrossRef]

163. Wei, J.; Sun, F.; Dong, B.; Ma, Y.; Chang, Y.; Lee, C. Deterministic Aperiodic Photonic Crystal Nanobeam Supporting Adjustable Multiple Mode-Matched Resonances. *Opt. Lett.* **2018**, *43*, 5407–5410. [CrossRef]

164. Adato, R.; Aksu, S.; Altug, H. Engineering Mid-Infrared Nanoantennas for Surface Enhanced Infrared Absorption Spectroscopy. *Mater. Today* **2015**, *18*, 436–446. [CrossRef]

165. Hasan, D.; Ho, C.P.; Lee, C. Thermally Tunable Absorption-Induced Transparency by a Quasi 3D Bow-Tie Nanostructure for Nonplasmonic and Volumetric Refractive Index Sensing at Mid-IR. *Adv. Opt. Mater.* **2016**, *4*, 943–952. [CrossRef]

166. Hasan, D.; Lee, C. Hybrid Metamaterial Absorber Platform for Sensing of CO2 Gas at Mid-IR. *Adv. Sci.* **2018**, *5*, 1700581. [CrossRef]

167. Hasan, D.; Pitchappa, P.; Pei Ho, C.; Lee, C. High Temperature Coupling of IR Inactive C=C Mode in Complementary Metal Oxide Semiconductor Metamaterial Structure. *Adv. Opt. Mater.* **2017**, *5*, 1600778. [CrossRef]

168. Hasan, D.; Pitchappa, P.; Wang, J.; Wang, T.; Yang, B.; Ho, C.P.; Lee, C. Novel CMOS-Compatible Mo-AlN-Mo Platform for Metamaterial-Based Mid-IR Absorber. *ACS Photonics* **2017**, *4*, 302–315. [CrossRef]

169. Xu, J.; Ren, Z.; Dong, B.; Liu, X.; Wang, C.; Tian, Y.; Lee, C. Nanometer-Scale Heterogeneous Interfacial Sapphire Wafer Bonding for Enabling Plasmonic-Enhanced Nanofluidic Mid-Infrared Spectroscopy. *ACS Nano* **2020**, *14*, 12159–12172. [CrossRef]

170. Zhou, H.; Hui, X.; Li, D.; Hu, D.; Chen, X.; He, X.; Gao, L.; Huang, H.; Lee, C.; Mu, X. Metal–Organic Framework-Surface-Enhanced Infrared Absorption Platform Enables Simultaneous On-Chip Sensing of Greenhouse Gases. *Adv. Sci.* **2020**, *7*, 2001173. [CrossRef]

171. Ma, Y.; Dong, B.; Li, B.; Wei, J.; Chang, Y.; Ho, C.P.; Lee, C. Mid-Infrared Slow Light Engineering and Tuning in 1-D Grating Waveguide. *IEEE J. Sel. Top. Quantum Electron.* **2018**, *24*, 6101608. [CrossRef]

172. Chang, Y.; Wei, J.; Lee, C. Metamaterials-from Fundamentals and MEMS Tuning Mechanisms to Applications. *Nanophotonics* **2020**, *9*, 3049–3070. [CrossRef]

173. Chen, Y.; Lin, H.; Hu, J.; Li, M. Heterogeneously Integrated Silicon Photonics for the Mid-Infrared and Spectroscopic Sensing. *ACS Nano* **2014**, *8*, 6955–6961. [CrossRef]

174. Ma, Y.; Chang, Y.; Dong, B.; Wei, J.; Liu, W.; Lee, C. Heterogeneously Integrated Graphene/Silicon/Halide Waveguide Photodetectors toward Chip-Scale Zero-Bias Long-Wave Infrared Spectroscopic Sensing. *ACS Nano* **2021**, *15*, 10084–10094. [CrossRef] [PubMed]

175. Chang, Y.; Xu, S.; Dong, B.; Wei, J.; Le, X.; Ma, Y.; Zhou, G.; Lee, C. Transfer-printed NEMS tunable Fabry Pérot filter for mid-infrared computational spectroscopy. In Proceedings of the 21st International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers 2021) Virtual Conference, 20–25 June 2021; pp. 553–556.

176. Zhang, H.; Tian, Y.; Wang, S.; Huang, Y.; Wen, J.; Hang, C.; Zheng, Z.; Wang, C. Highly Stable Flexible Transparent Electrode via Rapid Electrodeposition Coating of Ag-Au Alloy on Copper Nanowires for Bifunctional Electrochromic and Supercapacitor Device. *Chem. Eng. J.* **2020**, *399*, 125075. [CrossRef]

177. Zhang, H.; Wang, S.; Tian, Y.; Wen, J.; Hang, C.; Zheng, Z.; Huang, Y.; Ding, S.; Wang, C. High-Efficiency Extraction Synthesis for High-Purity Copper Nanowires and Their Applications in Flexible Transparent Electrodes. *Nano Mater. Sci.* **2020**, *2*, 164–171. [CrossRef]

178. Zhang, H.; Wang, S.; Tian, Y.; Liu, Y.; Wen, J.; Huang, Y.; Hang, C.; Zheng, Z.; Wang, C. Electrodeposition Fabrication of Cu@Ni Core Shell Nanowire Network for Highly Stable Transparent Conductive Films. *Chem. Eng. J.* **2020**, *390*, 124495. [CrossRef]

179. Zhu, M.; Yi, Z.; Yang, B.; Lee, C. Making Use of Nanoenergy from Human–Nanogenerator and Self-Powered Sensor Enabled Sustainable Wireless IoT Sensory Systems. *Nano Today* **2021**, *36*, 101016. [CrossRef]
180. Wang, H.; Wu, T.; Zeng, Q.; Lee, C. A Review and Perspective for the Development of Triboelectric Nanogenerator (TENG)-Based Self-Powered Neuroprosthetics. *Micromachines* **2020**, *11*, 865. [CrossRef]
181. Eisenhaure, J.D.; Xie, T.; Varghese, S.; Kim, S. Microstructured Shape Memory Polymer Surfaces with Reversible Dry Adhesion. *ACS Appl. Mater. Interfaces* **2013**, *5*, 7714–7717. [CrossRef] [PubMed]
182. Yang, Y.; Hwang, Y.; Cho, H.A.; Song, J.H.; Park, S.J.; Rogers, J.A.; Ko, H.C. Arrays of Silicon Micro/Nanostructures Formed in Suspended Configurations for Deterministic Assembly Using Flat and Roller-Type Stamps. *Small* **2011**, *7*, 484–491. [CrossRef] [PubMed]
183. Meitl, M.A.; Zhu, Z.T.; Kumar, V.; Lee, K.J.; Feng, X.; Huang, Y.Y.; Adesida, I.; Nuzzo, R.G.; Rogers, J.A. Transfer Printing by Kinetic Control of Adhesion to an Elastomeric Stamp. *Nat. Mater.* **2006**, *5*, 33–38. [CrossRef]
184. Keum, H.; Carlson, A.; Ning, H.; Mihi, A.; Eisenhaure, J.D.; Braun, P.V.; Rogers, J.A.; Kim, S. Silicon Micro-Masonry Using Elastomeric Stamps for Three-Dimensional Microfabrication. *J. Micromech. Microeng.* **2012**, *22*, 055018. [CrossRef]
185. Carlson, A.; Bowen, A.M.; Huang, Y.; Nuzzo, R.G.; Rogers, J.A. Transfer Printing Techniques for Materials Assembly and Micro/Nanodevice Fabrication. *Adv. Mater.* **2012**, *24*, 5284–5318. [CrossRef] [PubMed]
186. Pham, T.A.; Nguyen, T.K.; Vadivelu, R.K.; Dinh, T.; Qamar, A.; Yadav, S.; Yamauchi, Y.; Rogers, J.A.; Nguyen, N.T.; Phan, H.P. A Versatile Sacrificial Layer for Transfer Printing of Wide Bandgap Materials for Implantable and Stretchable Bioelectronics. *Adv. Funct. Mater.* **2020**, *30*, 1–10. [CrossRef]
187. Zhang, S.; Ling, H.; Chen, Y.; Cui, Q.; Ni, J.; Wang, X.; Hartel, M.C.; Meng, X.; Lee, K.J.; Lee, J.; et al. Hydrogel-Enabled Transfer-Printing of Conducting Polymer Films for Soft Organic Bioelectronics. *Adv. Funct. Mater.* **2020**, *30*, 1–8. [CrossRef]
188. Park, J.; Yoon, H.; Kim, G.; Lee, B.; Lee, S.; Jeong, S.; Kim, T.; Seo, J.; Chung, S.; Hong, Y. Highly Customizable All Solution–Processed Polymer Light Emitting Diodes with Inkjet Printed Ag and Transfer Printed Conductive Polymer Electrodes. *Adv. Funct. Mater.* **2019**, *1902412*, 1–9. [CrossRef]
189. Mahenderkar, N.K.; Chen, Q.; Liu, Y.; Duchild, A.R.; Hofheins, S.; Chason, E.; Switzer, J.A. Epitaxial Lift-off of Electrodeposited Single-Crystal Gold Foils for Flexible Electronics. *Science* **2017**, *1206*, 1203–1206. [CrossRef]
190. Wie, D.S.; Zhang, Y.; Kim, M.K.; Kim, B.; Park, S.; Kim, Y.J.; Irazoqui, P.P.; Zheng, X.; Xu, B.; Lee, C.H. Wafer-Recyclable, Environment-Friendly Transfer Printing for Large-Scale Thin-Film Nanoelectronics. *Proc. Natl. Acad. Sci. USA* **2018**, *115*, E7236–E7244. [CrossRef] [PubMed]