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Review

Ion-Movement-Based Synaptic Device for Brain-Inspired Computing

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Abstract: As the amount of data has grown exponentially with the advent of artificial intelligence and the Internet of Things, computing systems with high energy efficiency, high scalability, and high processing speed are urgently required. Unlike traditional digital computing, which suffers from the von Neumann bottleneck, brain-inspired computing can provide efficient, parallel, and low-power computation based on analog changes in synaptic connections between neurons. Synapse nodes in brain-inspired computing have been typically implemented with dozens of silicon transistors, which is an energy-intensive and non-scalable approach. Ion-movement-based synaptic devices for brain-inspired computing have attracted increasing attention for mimicking the performance of the biological synapse in the human brain due to their low area and low energy costs. This paper discusses the recent development of ion-movement-based synaptic devices for hardware implementation of brain-inspired computing and their principles of operation. From the perspective of the device-level requirements for brain-inspired computing, we address the advantages, challenges, and future prospects associated with different types of ion-movement-based synaptic devices.

Keywords: ion movement; synaptic device; brain-inspired computing

1. Introduction

Explosively increasing data set sizes in artificial intelligence (AI) and the Internet of Things have resulted in us facing limitations in energy efficiency and the challenges of the von Neumann bottleneck approaching the end of Moore's law [1–5]. In more detail, the AI algorithm that runs on the complementary metal oxide semiconductor (CMOS)-based von Neumann hardware seems to be somewhat inefficient [6], since: (1) the separation of processor and memory causes heavy data traffic between devices, especially in data-intensive tasks; (2) CMOS uses a "0" and "1" binary logic system rather than a gradual weight change; (3) the connections of transistors in silicon chips are usually in two dimensions; (4) CMOS-based computers consume a thousand times as much energy as the human brain to perform the same task [6,7]. For example, a supercomputer (IBM Watson) [8] has 2880 computing cores (10 refrigerators' worth in size and space) and requires about 80 kW of power and 20 tons of air-conditioned cooling capacity, while the human brain occupies a space of less than 2 *l* and consumes low power, of the order of 10 W [9,10]. Additionally, if data storage and communication continue to increase at the current rate, the total energy consumed by binary operations using CMOS will reach ~10^{27} J in 2040, surpassing the total energy produced worldwide [11,12]. In order to improve the performance of computing systems in the so-called "big data" era [13], it is necessary to fundamentally change the way computing is executed [14]. We need to shift to a data-centric paradigm rather than a computer-centric one [14].

The growth of computational power, the availability of big data, and the rapid development of training methods have resulted in significant advances in data-centric computing methods, such as the artificial neural network (ANN), which is inspired by the co-location

of logic and memory, tolerance to local failures, hyper-connectivity, and parallel processing present in the human brain [12,15,16]. The human brain is a massively parallel computing structure that processes input information by synaptic transmission. Each synaptic event consumes only around 1–10 fJ [5,17]. The hardware in brain-inspired computing architecture is required to mimic stochastic behaviors by introducing a new logic device such as an orthogonator gate and to physically emulate synapses in the human brain at the small circuit or device levels, consuming significantly reduced energy [12,18–24].

Recently, synaptic devices based on various types of resistive switching devices have been utilized for brain-inspired computing [25–30]. Brain-inspired computing based on synaptic devices has achieved particular progress from ion-movement-based resistive switching mechanisms such as cation-movement-based filaments [31–36], anion-movement-based filaments [37–43], cation-movement-based ferroelectric polarization reversal [44–49], and ion-movement-based electrochemical electrolytes [50–57]. These ion-movement-based resistive switching devices can show a gradual change in conductance and nonvolatile characteristics, which have not been implemented in Mott-insulator-based resistive switching devices. Resistive switching based on the phase transition of Mott insulators under an electric field shows an abrupt change in conductance and volatile behaviors, which are suitable for neuron devices [58–60]. In this review, we summarize in detail the different ion-movement-based mechanisms and discuss the advances in the development of ion-movement-based resistive switching devices for artificial synaptic elements. In addition, we discuss the challenges that need to be addressed in future research on synaptic devices towards developing brain-inspired computing systems.

2. Biological Synapses

2.1. Properties of Biological Synapses

The brain contains billions of neurons, which are highly connected by trillions of synapses [6]. Synapses are small gaps (20–40 nm) between the axon end of the presynaptic neuron and the dendrites of the postsynaptic neuron (Figure 1a) [61]. Neurons generate action potentials (spikes) with amplitudes of approximately 100 mV and durations in the range of 0.1–1 ms in their soma. The spikes propagate through the axon and are transmitted to the postsynaptic neurons through the synapses [10]. The connection weights of the synapses between neurons can become stronger (potentiation) or weaker (depression) through a process called synaptic plasticity, as the brain adapts to new information. Synaptic plasticity is widely believed to play a key role in the learning and memory processes of the brain [61].

2.2. Biological Synaptic Plasticity

Biological synaptic plasticity, which enables learning and memory, is the ability to continuously modulate synaptic weights in response to action potentials. In more detail, biological synaptic plasticity is the changed connection strength of a biological synapse, which is caused by the activities of a presynaptic neuron and a postsynaptic neuron. [10] It includes long-term potentiation/depression, short-term potentiation/depression, and spike-timing-dependent plasticity (STDP). The biological synaptic weight can be persistently changed by modulating the amount of neurotransmitter presynaptically released across the synapse or the number of receptors present postsynaptically; this is so-called long-term plasticity. Specifically, the increases and decreases in synaptic weight are called long-term potentiation (LTP) and long-term depression (LTD), respectively (Figure 1b) [5,62]. Short-term potentiation (STP) and short-term depression (STD) are temporary increases and decreases in synaptic weight, respectively. STP and STD generally last from seconds to tens of minutes and then fade away to the initial values, in biological systems (Figure 1c) [5,63]. Spike-timing-dependent plasticity (STDP), a form of Hebbian learning, emerged as a new concept of cellular learning in the late 1990s [10,64–66]. Different types of STDP exhibit different forms of dependency on the spiking time $\Delta t = t_{pre} - t_{post}$, where t_{pre} and t_{post} are

the arrival times of presynaptic and postsynaptic spikes, respectively. As the amplitude of Δt becomes shorter, the change in synaptic weight becomes larger (Figure 1d).
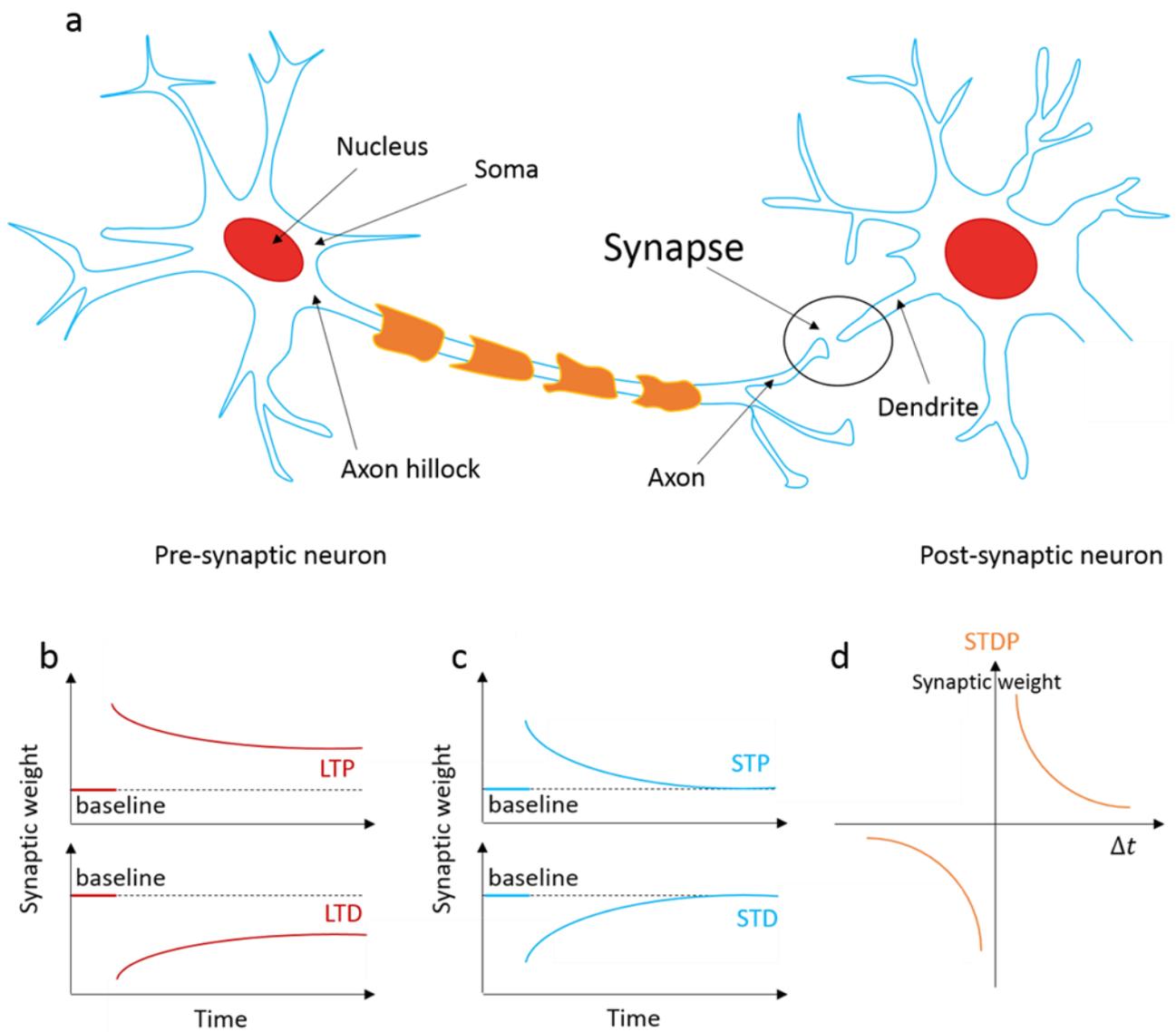

Figure 1. Properties of a biological synapse. (**a**) Schematic image of the biological synapse structure. Typical synaptic weight changes in the cases of (**b**) LTP and LTD, (**c**) STP and STD, and (**d**) STDP.

3. Resistive Switching Devices Applicable to Synaptic Devices

3.1. Synaptic Devices for ANNs

3.1.1. Brain-Inspired Computing with ANNs

The implementation of brain-inspired computing with ANNs could overcome the challenge for software-based computing where the algorithm is essentially run by conventional sequential machines with limited parallelism [29]. An ANN generally consists of a massive number of synapses that connect between groups of neurons, which requires a large volume of memory and thus results in extremely high hardware costs. Therefore, it is beneficial to develop more compact synaptic devices with high performance [67]. Figure 2a shows the vector matrix multiplication (VMM) required for typical ANN learning. The processing of an ANN architecture includes two phases: forward and backward propagation. First, the input data x are unwrapped to a row vector ($1 \times n$), and each input datum is connected to each value (weight w) of the next layer, which is arranged in a matrix for VMM. During forward propagation, the VMM $y_m = \sum_n w_{nm}x_n$ is required and can be

calculated by $I_m = \sum_n G_{nm} V_n$ in a crossbar array of synaptic devices, where G_{nm} is the weight (conductance) of the synaptic devices at node (n, m) and V_n is the input voltage of row n. During backward propagation, the weight of the synaptic device is modulated to reduce the gap between the real output and the target output. The error at the jth node is calculated as $e_j = t_j - y_j$, where y_j is the real output and t_j is the target output. In addition, e_j is used to guide the adjustment of the weight, as $\Delta w_{ij} = \alpha e_j x_i$, where $\alpha > 0$ is a constant learning rate and x_i is the ith input. Synaptic devices must have controllable multistate and analog conductance for processing a huge amount of information like a biological brain [5]. The other method is brain-inspired computing with a spiking neural network (SNN), which consists of STDP-based learning rules. In SNN, the biological system is more closely mimicked than in ANN. SNN is believed to be computationally powerful. However, SNN has still not been able to reach the accuracy of ANN trained with backpropagation, due to the lack of efficient learning algorithms [68]. Therefore, suitable STDP-based learning rules for the improved accuracy of SNN must form the subject of further research. Consequently, this review focuses on ANNs with synaptic devices, which are relatively far from real synapses and brain mimicking but use the power of parallel inference to drastically reduce the energy requirements for hardware operating with a large neural network [68].

3.1.2. Synaptic Devices

Many studies have attempted to implement synaptic devices emulating the brain's synaptic plasticity and functions such as memory, learning, and recognition. Synaptic devices modulate their conductance values in a way that is analogous to the modulation of synaptic weights in biological systems. In synaptic devices, the conductance is generally measured using the current between two electrodes, as shown in Figure 2b. A synaptic device's conductance is equivalent to the biological synaptic weight and can be increased or decreased by an external voltage signal leading to potentiation or depression characteristics, respectively. In analogous conductance behavior such as potentiation and depression in the synaptic device, the functional parameters should be checked with respect to the goal of reducing accuracy loss in the ANN. The accuracy loss in ANNs in the implementation of a brain-inspired computing system is a critical factor for quantifying the reliability metrics and can be attributed to two main factors: the nonideal effect in analog resistive switching, which causes the hardware training accuracy to be lower than the software training accuracy [68,69], and the conductance drift or fluctuation of the analog resistive switching devices, which causes the accuracy after training to degrade with time [68,70].

3.2. Required Specifications of a Synaptic Device for ANNs

The functional metrics of analog resistive switching behavior corresponding to linearity, precision, cycle-to-cycle variation, device-to-device variation, and dynamic range have direct influences on the training accuracy in brain-inspired computing, as shown in Figure 2c. The negative effect or error in the training accuracy shown by the degradation of these functional metrics during repeated operations should be taken into careful consideration. Many simulation studies have reported how much these functional metrics impact on the training accuracy in ANNs. Based on previous valuable simulation studies, we discuss the definitions of functional metrics and their impacts on training accuracy.
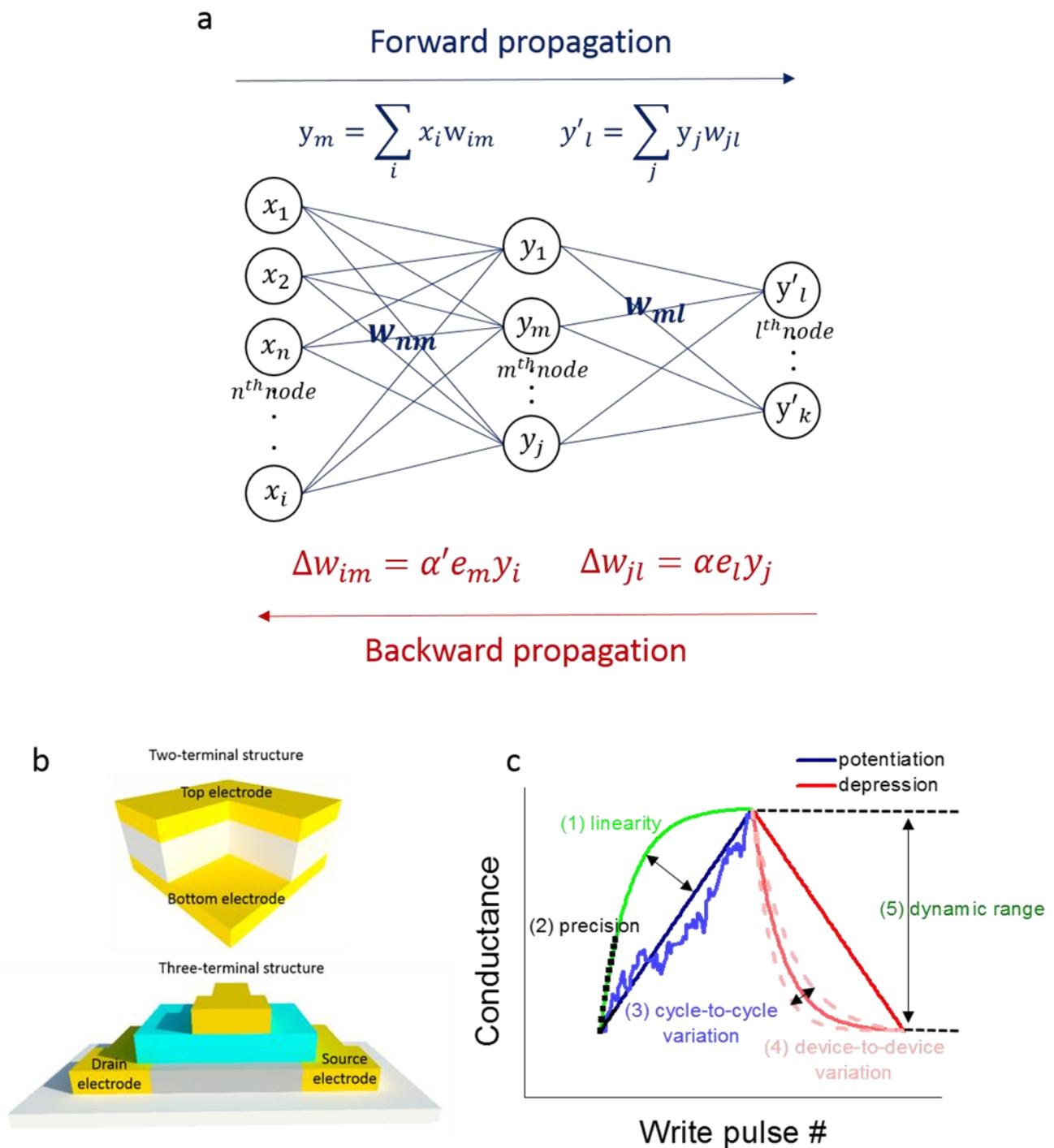
Figure 2. (**a**) Schematic structure of fully connected ANN. (**b**) Schematic structure of two-terminal- and three-terminal-based synaptic devices. (**c**) An overview of functional metrics of analog resistive switching for improved learning capability.

3.2.1. Linearity

The linearity of weight updates represents how linearly the conductance changes with the number of applied pulses. Ideally, the amount of potentiation and depression should be linearly proportional to the number of applied pulses [71]. Lower linearity of potentiation (depression) results in greater difficulty in tuning the conductance to the target value, leading to worse convergence rates during training [67,68,70]. Hence, higher nonlinearity directly causes more accuracy loss. However, the dependence of training accuracy on

linearity changes with the type of learning algorithm. For learning with backpropagation algorithms, the linearity of the weight update dramatically affects the online training accuracy. High accuracy can only be achieved with small nonlinearity [72]. In contrast, on-chip learning with sparse coding algorithms demonstrates only a small accuracy loss of ~4%, even at the maximum nonlinearity [67,73]. This implies that linearity has a less critical impact on learning accuracy when sparse coding algorithms are used rather than backpropagation algorithms.

3.2.2. Precision

Precision is defined as the number of conductance levels that the synaptic device can achieve [67,68,71]. High precision is known to bring advantages in terms of network capacity and robustness, although the requirement for the precision remains application-specific [10]. If the precision is smaller than 4 bits, the classification accuracy in a single-layer perceptron neural network with a compressed modified National Institute of Science and Technology (MNIST) data set decreases abruptly [74]. Even for sparse coding algorithms for on-chip learning and backpropagation algorithms with emerging nonvolatile memory, the learning accuracy decreases when the precision is smaller than 6 bits [67,72].

3.2.3. Cycle-to-Cycle Variation

In the potentiation and depression process, hardware systems based on resistive switching devices suffer from random noise addition. The cycle-to-cycle variation is defined as pulse-to-pulse noise at every weight update operation in the synaptic device during potentiation or depression. Cycle-to-cycle variation can cause unregulated changes in the conductance after applying each pulse. Due to the large number of weight update operations during training, cycle-to-cycle variation results in increased cost of training and serious accuracy loss [67,68,75].

3.2.4. Device-to-Device Variation

The effect of device-to-device variation can be analyzed by introducing variation in the linearity baseline for each synaptic device. This functional metric has a smaller impact on learning accuracy than other functional metrics. On-chip learning with a sparse coding algorithm can tolerate a device-to-device variation of up to 30% [67,73]. In the case of nonvolatile memory-based synaptic devices with a backpropagation algorithm, the neural network is resilient to device-to-device variation, except where there is high nonlinearity in the weight update [72].

3.2.5. Dynamic Range (Analog on/off Ratio)

The dynamic range, also known as the analog on/off ratio, can be defined as the ratio of the high resistive state (HRS) conductance and the low resistive state (LRS) conductance in analog switching. The dynamic range varies with the materials and structures of analog resistive switching devices. The learning accuracy for the synaptic device dramatically decreases when the dynamic range becomes smaller [67,73,76]. In addition, a large dynamic range in a synaptic device results in improved tolerance to cycle-to-cycle and device-to-device variation [63].

3.3. Ion-Movement-Based Mechanisms of Different Resistive Switching Devices

3.3.1. Cation-Movement-Based Filamentary Two-Terminal Resistive Switching Devices

Resistive switching devices based on cation migration are usually termed electrochemical metallization (ECM) cells or conductive-bridge random-access memories (CBRAMs) in the literature [77–81]. The ECM cell is a promising approach for brain-inspired computing devices due to its short switching time (~ns), scalability to the nanometer regime, and ultra-low power consumption (~nW) [82]. A typical ECM cell utilizes an insulator as a switching layer sandwiched between the top and bottom electrodes. One of the two electrodes should be an electrochemically active metal (e.g., Ag, Cu, or Ni) and the other

should be an inert metal (e.g., Pt, W, or Au) [78,81,83,84]. The insulator layer acts as a solid electrolyte for Ag, Cu, or Ni cation migration. Insulator layer materials include chalcogenide glasses [85], oxide layers [86], epitaxy layers [35], polymers [34], and even two-dimensional (2D) materials [31].

During resistive switching, essentially new materials are produced in the insulator layer through electrochemical reactions and ion movement. When a positive bias is applied to the active electrode, three steps are normally involved in this material reconfiguration process called set switching: ionization, movement, and the reduction of cations to form conductive filaments (CFs) [77,79,81,84,87]. The active metal used as an anode is ionized to a cation under an external voltage bias (Figure 3a) [77,88,89]. The cation moved by the applied electric field travels through the solid electrolyte toward the inactive cathode electrode. The speed of ion movement depends exponentially on the applied electric field due to the barrier lowering effect, as shown in Equation (1) [77,81,90].

$$v_\mathrm{c} = a \cdot f \cdot \exp\left(- E_\mathrm{a}/k_\mathrm{B}T\right) \cdot \sinh\left(qaE/2k_\mathrm{B}T\right) \tag{1}$$

where v_c is the drift velocity of the cation, a is the hopping distance (the distance between the potential wells), f is the attempt frequency, E_a is the energy barrier for ion migration, E is the applied electric field, k_B is Boltzmann's constant, q is the ion's charge, and T is the absolute temperature. Electrocrystallization is caused by the reduction of cations with the aid of electrons provided by the inert metal cathode, leading to the formation of CFs [79,81,83,84]. On the other hand, when a negative bias is applied to the active electrode, the formed CFs can be ruptured due to thermally assisted electrochemical reactions, and this is called reset switching [91]. The front of the CF has the thinnest cross-sectional area and hence the highest current density, leading to a high temperature. Under the negative voltage applied to the active electrode, which prevents the supply of cations, the dissolution reaction at the front of the CF will be accelerated by the high temperature [33]. In addition, the cation-movement-based mechanism should consider the time evolution of the memory characteristic after the set process. The memory characteristic degradation relies on the diffusion of metal atoms toward the lower concentration region over time [68].

3.3.2. Anion-Movement-Based Filamentary Two-Terminal Resistive Switching Devices

An anion-movement-based filamentary two-terminal device, also known as valence change memory (VCM), is quite similar to a cation-movement-based filamentary two-terminal device (Figure 3b), except that the CF formed in the insulating thin film is a chain of oxygen defects within an oxide (rather than a chain of metallic atoms of the reactive electrode through an insulating solid electrolyte) [82]. When a positive bias is applied to the top electrode, anions hop among the energy potential wells (assumed to have hopping distance a and energy barrier E_a), where the applied electric field E lowers the energy barrier by a factor of qaE. The anion drift velocity shows the same exponential dependence on qaE as that of the cation drift velocity presented in Equation (1) [39]. The anions drift toward the top electrode leading to the movement of oxygen defects to the bottom electrode and the growth of defect-based CFs. On the other hand, when a negative bias is applied to the top electrode, the formed defect-based CF ruptures from the top electrode. The anion-movement-based filamentary system is attractive because it requires only metal oxides such as HfO_x, AlO_x, WO_x, FeO_x, GdO_x, TaO_x, TiO_x, and mixtures of such films, many of which are already used in CMOS processes. The underlying metal–insulator–metal structure is simple, compact, CMOS-compatible, and highly scalable, and its energy consumption and programming current can be made ultra-low, up to sub-pJ and <1 µA, respectively [82].
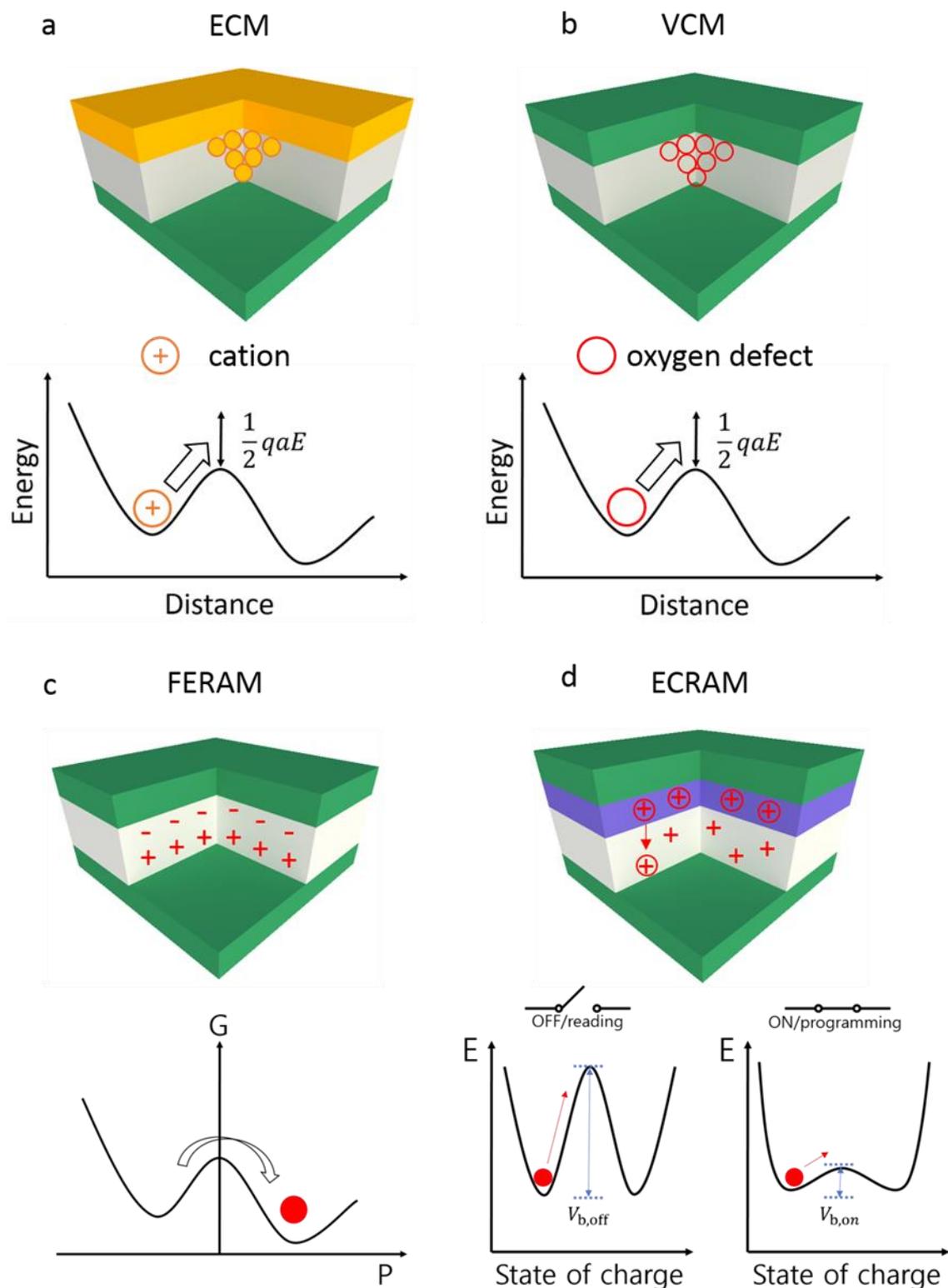
Figure 3. Ion-movement-based resistive switching devices. (**a**) Schematic of structure and of the field-driven acceleration of cation transport for ECM-based resistive switching device. (**b**) Schematic of structure and of the field-driven acceleration of defect transport for VCM-based resistive switching device. (**c**) Schematic of structure and of the field-driven cation movement for FERAM-based resistive switching device. G and P denote Gibbs energy and polarization, respectively. (**d**) Schematic of structure and of operation-specific change in blocking barrier for ECRAM-based resistive switching device. E denotes energy barrier.

3.3.3. Cation-Movement-Based Ferroelectric Two-Terminal Resistive Switching Devices

In a prototypical ferroelectric material, the charge centroids of positive and negative ions do not overlap. Ferroelectricity arises from the spontaneous displacement of the positively charged cations from the negatively charged oxygen anions in crystal structures such as ABO_3-type perovskites [92]. Mesoscopic one-dimensional free energy potentials can model 180° switching processes with two energy wells and one local maximum between the two wells, as shown in Figure 3c. The model is based on a mesoscopic lattice element, which comprises a large number of microscopic lattice cells. The application of an electric field distorts the energy landscape, and a dipole switch occurs when the equilibrium value determining the B-ion position exceeds the unstable equilibrium due to the central O^{2-} ion [93]. As a consequence, by application of a sufficiently high external electrical field, the B ion can equivalently move towards the "top" or the "bottom" of the lattice, thereby leading to the "up" or "down" states, respectively. A permanent dipole moment resulting from B-ion movement can be maintained even in the absence of an external electric bias [92,93]. A ferroelectric material such as $Pb(Zr,Ti)O_3$ [33], $(Hf,Zr)O_2$ [94], $BiFeO_3$ [45], or $BaTiO_3$ [44,46,95] acts as an active layer in cation-movement-based ferroelectric two-terminal resistive switching devices, which are also known as ferroelectric random-access memory (FERAM).

3.3.4. Ion-Movement-Based Electrochemical Three-Terminal Resistive Switching Devices

More recently, researchers proposed a cation-movement-based electrochemical transistor system, also called electrochemical random-access memory (ECRAM), comprising an ion-conducting/electron-blocking gate in combination with a channel layer (Figure 3d) [96]. The charge in the channel is manipulated during the "write" operation, which allows both electrons (through the external circuit) and ions (through the electrolyte) to be exchanged between the channel and the reference electrode under a small bias [97]. During the "read" operation, where the channel resistance is sensed, the circuit between the channel and the reference electrode is open, and the electronic charge of the channel remains unaltered by virtue of an ion-conducting/electron-blocking electrolyte [61,97]. Hence, a cation-movement-based electrochemical system is a type of nonvolatile redox cell in which the state of charge in the channel determines the electronic conductivity [61]. Typical materials systems used in ion-movement-based electrochemical three-terminal resistive switching devices are MoO_3/ionic liquid [98], MoO_3/LiClO4:PEO [62], $SmNiO_3$/ionic liquid [99], graphene/$LiClO_4$ [97], and MoS_2/PTCDA [100]. Organic materials are widely used in ion-movement-based electrochemical devices, and thus they are also known as organic electrochemical transistors [61–63,101].

4. Synaptic Devices

4.1. Cation-Movement-Based Filamentary Two-Terminal Synaptic Devices

To mimic biological synaptic plasticity, it is essential to demonstrate repeatable analog switching with ultra-low power or energy consumption. The attractive characteristics of the ECM cell such as short switching time, scalability, and ultra-low power or energy consumption have driven the development of synaptic devices. To improve the performance of energy-efficient analog switching, emerging electrolytes for ECM cells such as 2D materials, nanowires, polymers, and ultra-thin films have been used [31–34,102].

The Cu/MoS_2 bilayer/Au system has been reported for a synaptic device with ultra-low switching voltage (Figure 4a,b) [31]. In the MoS_2 bilayer between an active Cu top electrode and an inert Au bottom electrode, Cu has a lower migration barrier and diffusion activation energy than sulfur vacancies, leading to the operation of the synaptic device at ultra-low switching voltages. A pulse with a small amplitude of 0.6 V can cause a gradual increase and decrease in the device resistance, resulting in potentiation–depression curves (Figure 4b). Such low switching voltages are important, especially for neuromorphic computing, which strives to operate with a power far lower than that required for digital computing [31]. In addition, the STDP of the cation-movement-based filamentary

two-terminal synaptic device was experimentally confirmed, as shown in Figure 4c. The developed device reveals consistent analog switching and thus exhibits synapse-like learning behavior such as STDP, which was demonstrated for the first time in 2D-material-based vertical memristors. This demonstration of STDP combined with low switching voltage is promising for applications in neuromorphic circuits.

Fu et al. demonstrated a type of diffusive memristor which is fabricated using protein nanowires harvested from the bacterium Geobacter sulfurreducens and operates at biological voltages of 40–100 mV [32]. They demonstrated that a reduction in the switching voltage is obtained by using protein nanowires. The influx and efflux of Ag in the CF can also emulate Ca^{2+} influx and extrusion in a biological synapse. The steady-state evolution of the CF and the resultant change in conductance can be used to emulate synaptic plasticity. Figure 4d shows frequency-dependent paired-pulse facilitation (PPF) and paired-pulse depression (PPD) in a synaptic device operating at biological voltages. The features of the protein-nanowire-based filamentary devices are very similar to those of biological synapses in terms of signal amplitude and/or frequency range.

It has been reported that a synaptic $Ag/PbZr_{0.52}Ti_{0.48}O_3$ (PZT)$/La_{0.8}Sr_{0.2}MnO_3$ (LSMO) device with an ultra-thin ferroelectric PZT layer (~4 nm) serving as an electrolyte for cation migration can achieve very low energy consumption [33]. The ferroelectric barrier width becomes thinner due to the growth of an uncompleted CF of Ag, leading to a higher tunneling transmittance and switching to a low on-state resistance, as shown in Figure 4e. The rupture of the Ag CF takes place due to a thermally assisted electrochemical reaction (Figure 4f). Then, the tunneling barrier width becomes thicker, and the device switches back to a high off-state resistance. The gradual change in the direct tunneling current of the Ag/PZT/LSMO is enabled by barrier-width control originating from the Ag ion migration. Both potentiation and depression can be induced in the Ag/PZT/LSMO device by short stimulation pulses with a duration of 100 ns, which are enabled by the combination of applied voltage and polarization bound charge, as shown in Figure 4g. This characteristic could result in low programming energy (a potentiation energy consumption of ~22 aJ and a depression energy consumption of ~2.5 pJ) by minimizing the programming time.

Jang et al. demonstrated that the transition of the operation mode in a poly(1,3,5-trivinyl-1,3,5-trimethyl cyclotrisiloxane) (pV3D3)-based flexible memristor from conventional binary switching to synaptic analog switching can be achieved simply by reducing the size of the formed filament [34]. The flexible pV3D3 memristor operates through the formation and rupture of the Cu CF inside the pV3D3, resulting in the LRS and HRS, respectively, as shown in Figure 5a. Potentiation and depression curves can be induced by the conductance updates of the pV3D3 memristor under the application of consecutive pulses, as shown in Figure 5b. Conductance updates with linear behavior are achieved by utilizing pulse trains with increasing amplitude in the range of 2~4 V (-1.2~-1.4 V) with a width of 60 ns (100 ns) for the potentiation (depression) process.
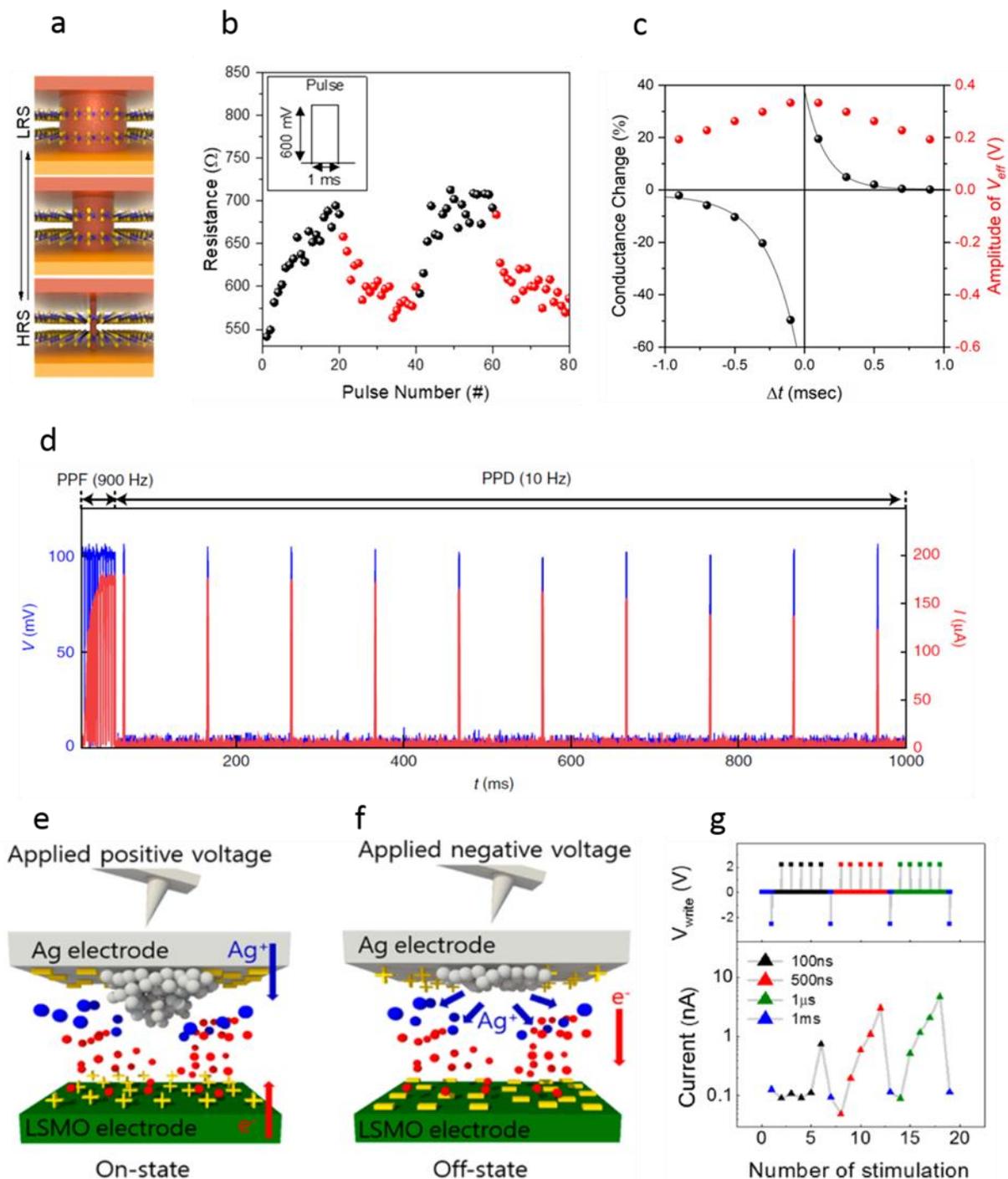
Figure 4. (**a**) Schematic of the change in the cation–movement–based filament for the Cu/MoS$_2$ double-layer/Au with switching between HRS and LRS. (**b**) Potentiation–depression curve obtained by consecutive pulses with a small amplitude of 0.6 V and (**c**) STDP behaviors obtained by low–amplitude spiking for the Cu/MoS$_2$ double–layer/Au. Reprinted/adapted with permission from Ref. [31]. 2019, American Chemical Society. (**d**) The current response of frequency–dependent PPF and PPD obtained by input pulses (100 mV, 1 ms) in a cation–movement–based filamentary two–terminal synaptic device with protein nanowires. Reprinted/adapted with permission from Ref. [32]. 2020, Springer Nature. (**e**,**f**) Schematic illustrations of growth and rupture of an uncompleted CF of Ag in an Ag/PZT/LSMO device in LRS and HRS, respectively. (**g**) Potentiation behaviors obtained by stimulation pulses with different durations for an Ag/PZT/LSMO device. Reprinted/adapted with permission from Ref. [33]. 2017, American Chemical Society.
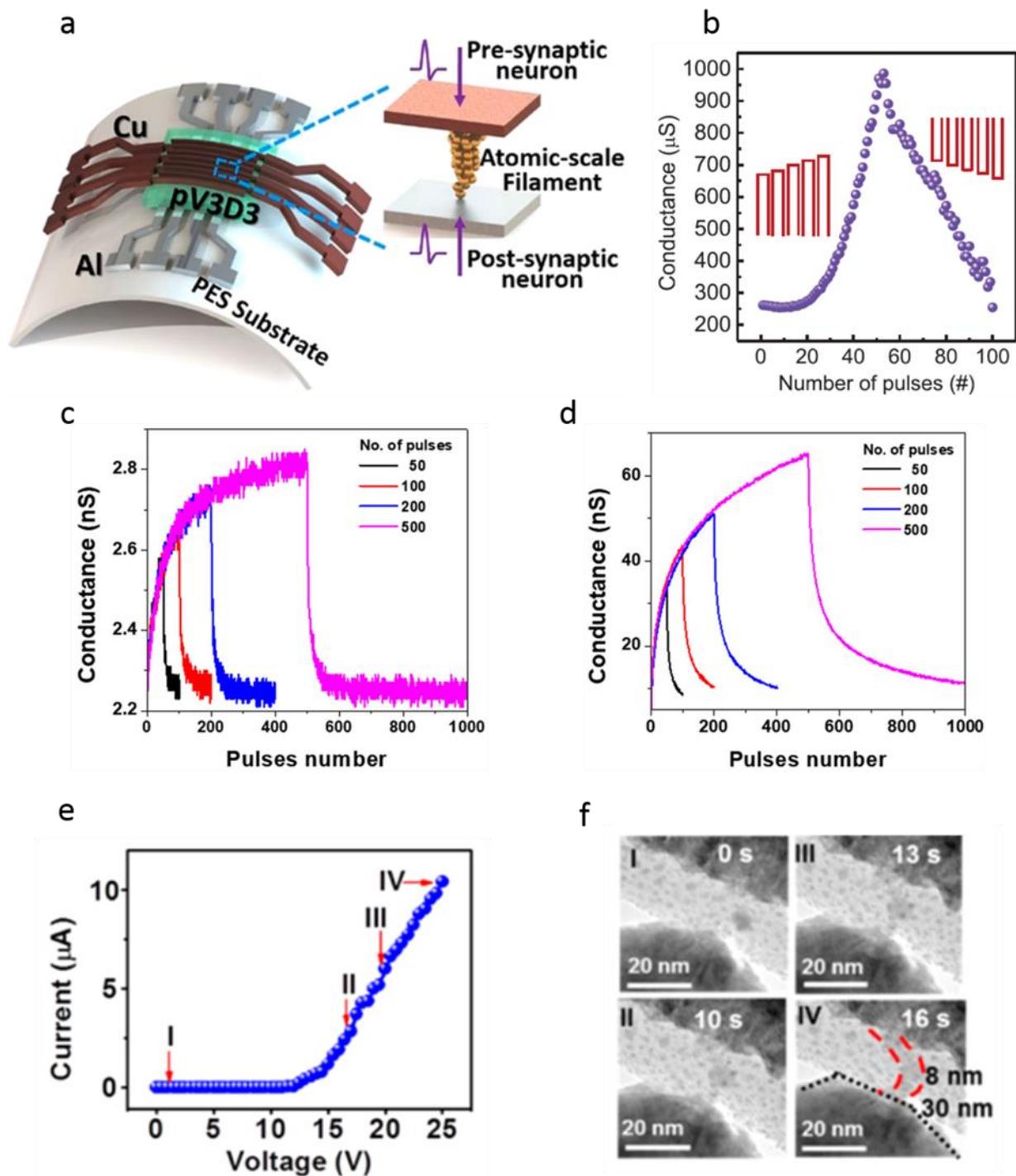
Figure 5. (**a**) Schematic image of pV3D3-based flexible synaptic device using the formation and rupture of Cu ion-movement-based filament. (**b**) Potentiation (depression) curve obtained by smart pulse scheme with increasing amplitude in the range of 2~4 V (−1.2~−1.4 V) with a width of 60 ns (100 ns) for a pV3D3-based flexible synaptic device. Reprinted/adapted with permission from Ref. [34]. 2018, American Chemical Society. (**c**,**d**) A comparison of potentiation–depression curves of the Ag/SiN$_x$/a-Si/p^{++} Si-based devices with unimplanted (**c**) and implanted (**d**) devices under varying numbers of stimulation pulses of 7.0 (−3.0) V for potentiation (depression). Reprinted/adapted with permission from Ref. [36]. 2020, Springer Nature. (**e**) Gradual current change and (**f**) simultaneously obtained transmission electron microscope image of a Cu tip/SiO$_2$/W cell during injection of voltage with increased amplitude. Reprinted/adapted with permission from Ref. [86]. 2017, American Chemical Society.

Challenges for Cation-Movement-Based Filamentary Two-Terminal Synaptic Devices

Reproducible gradual switching and controllable formation of the CF in cation-movement-based filamentary synaptic devices has been challenging to achieve due to the abrupt and stochastic nature of the switching mechanism, especially in the set process [61,82,103]. Therefore, a cation-movement-based filamentary two-terminal synaptic device typically shows nonlinear and asymmetric conductive responses, as well as large device variations, which can deteriorate the performance of an ANN [104,105]. The nonlinear and asymmetric conductivity can be overcome by introducing smart pulse schemes with varying amplitudes or durations of pulses, producing a large number of intermediate states and a symmetric/linear response [67,106]. However, smart pulse schemes with non-identical pulses require a read-before-write step to first identify the conductance state and then apply the correct pulse amplitude or duration to the device, which inevitably increases the complexity of the peripheral circuitry design as well as the latency and energy consumption [67]. As an alternative way to improve the symmetry and linearity of the conductance response, lateral growth of the CF has been used [31,34]. However, this method leads to a lowered analog on/off ratio, which is an important parameter for high recognition accuracy [35,67,76,104,105].

Kim et al. reported improved conductance linearity and dynamic range in a Ag/SiN$_x$/a-Si/p^{++} Si-based ECM device through Ge implantation [36]. Ge implantation induces structural defects in the bulk and surface regions of the a-Si layer, which enables spatially uniform Ag migration and nanocluster formation in the upper SiN$_x$ layer, leading to enhanced synaptic behavior. Figure 5c,d show analog switching profiles for unimplanted and implanted devices, respectively. The dynamic range of the implanted device is higher than that of the unimplanted device for the overall pulse numbers. An increased current flow in an implanted a-Si layer can enhance Ag migration, which leads to increased Ag clustering in the SiN$_x$ thin film and can improve the dynamic range of analog switching. In addition, the lower linearity in the depression of the unimplanted device, which has small-sized nanoclusters, is induced by the volatility characteristic, while the large-sized nanoclusters of the implanted device can improve the linearity for depression.

On the other hand, nanoclusters can form a CF with a curved shape in a Cu tip/SiO$_2$/W cell, leading to a gradual increase in the current level, as reported by Yuan et al. [86]. Figure 5e,f show the gradual current change and the simultaneously obtained transmission electron microscope (TEM) image, respectively, where the diameter of the Cu tip close to the SiO$_2$ is around 30 nm. With a bias sweep to +14 V, the device remains in the HRS (state I). A dark region corresponding to a Cu nanocluster suddenly appears when the bias is swept to +16 V. The existing Cu nanocluster starts to enlarge, which indicates that more Cu atoms migrate into the SiO$_2$, and the device gradually switches to intermediate states (states II and III). In these states, the current gradually increases to the μA level. With an increase in bias, more and more nanoclusters emerge inside the oxide layer close to one another and gradually grow in a curved path toward the inert W electrode. When the sweep bias reaches +25 V, the nanoclusters finally form the shape of a curved CF with a diameter of 8 nm at the widest part. Simultaneously, the current reaches a high level, leading to set switching of the device to the LRS (state IV).

Choi et al. reported an improvement in conductance linearity, endurance, and device variability without a large loss in analog on/off ratio using CFs confined in one-dimensional dislocations of an epitaxial SiGe layer [35]. The defect-selective etching provides additional sites for Ag occupation along the pipeline for ion migration, which increases the analog on/off ratio to above 100, using the same pulse train conditions as those used for the unetched epitaxial SiGe layer with a low analog on/off ratio of 3. It was confirmed that securing enough space at dislocations also contributes to improving the linearity in the conductance response. The diameter of the dislocation is estimated to be few nanometers, which offers enough space to accommodate Ag ions. This technique of fabricating a pathway for cation movement can reduce the device variability with high endurance.

In order to implement large-scale neuromorphic systems, ECM devices should be incorporated into crossbar array structures. The main challenges for ECM devices in crossbar array structures are high on-state current, energy inefficiency, and overheads of the sensing circuits. In addition, there are non-negligible voltage drops across lines in the array, which lead to significant degradation of the dot-product computing precision. In order to reduce the on-state current of an ECM in a crossbar array, a one-transistor (1T)–one-resistor (1R) structure has been introduced. However, the introduction of a three-terminal transistor increases the energy and size cost. The formation of a tunnel barrier through an incomplete filament or stacking of a selector are better solutions to enhance the energy efficiency and scalability.

4.2. Anion-Movement-Based Filamentary Two-Terminal Synaptic Devices

The key advantages of anion-movement-based filamentary two-terminal synaptic devices include the compact structure, the CMOS compatibility, and the capability for hybrid or 3D integration, making them attractive for a broad range of applications including memory, analog devices, and reconfigurable circuits, as well as brain-inspired computing [37,38].

Gong et al. implemented an anion-movement-based filamentary two-terminal synaptic device through a HfO_2-based resistive switching device [41]. This device shows analog switching behavior, as shown in Figure 6a. The conductance of the device gradually increases and decreases under 1000 consecutive positive and negative pulses, respectively. The progressive change in conductance in the HfO_2-based synaptic device is attributed to the modulation of the oxygen-vacancy-based filament by pulse stimulation. Figure 6b shows a schematic of its operation mechanism. The movement of the oxygen vacancies in response to an electrical signal has a probabilistic nature, which emerges as an inherent randomness in the conductance weight updates, superimposed on the expected signal.

Gao et al. developed a synaptic device based on a 3D vertical structure including several parallel oxide-based resistive switching devices on the same nanopillar, for the application of brain-inspired computing with high device density and low energy consumption [42]. Figure 6c shows a TEM image of a two-layer resistive switching device which has top and bottom HfO_x-based cells on the same pillar. The analog switching behavior is obtained through only a gradual reset process to mimic biological depression. The abrupt set process is considered as positive feedback between the oxygen vacancy generation rate and the temperature/local field strength, while the gradual reset process is considered as negative feedback [37]. Figure 6d shows the gradual reset processes of the device, induced from two initial resistance states (~100 kΩ and 1 MΩ) by applying 500 consecutive negative identical pulses. For the case of an initial resistance state of ~1 MΩ, the maximum energy per spike drops to ~0.29 pJ. The reduced energy consumption is mainly attributed to the higher initial resistance of the device.

Yu et al. implemented an anion-movement-based filamentary two-terminal synaptic device with low energy consumption by stacking multiple layers of $Pt/HfO_x/TiO_x/HfO_x/TiO_x/TiN$ [37]. The analog switching behavior is obtained through only a gradual reset process to mimic biological depression. The abrupt set process is considered as positive feedback between the oxygen vacancy generation rate and the temperature/local field strength, while the gradual reset process is considered as negative feedback. The gradual reset processes of five different devices were induced from two initial resistance states (~500 Ω and ~20 kΩ) by applying 400 consecutive negative identical pulses. A system-level simulation using these device-level experimental results revealed that the brain-inspired computing system may be robust against synaptic device variation. In addition, the synaptic device operates with very low energy consumption, which decreases from 24 pJ to 0.85 pJ as the initial resistance increases.
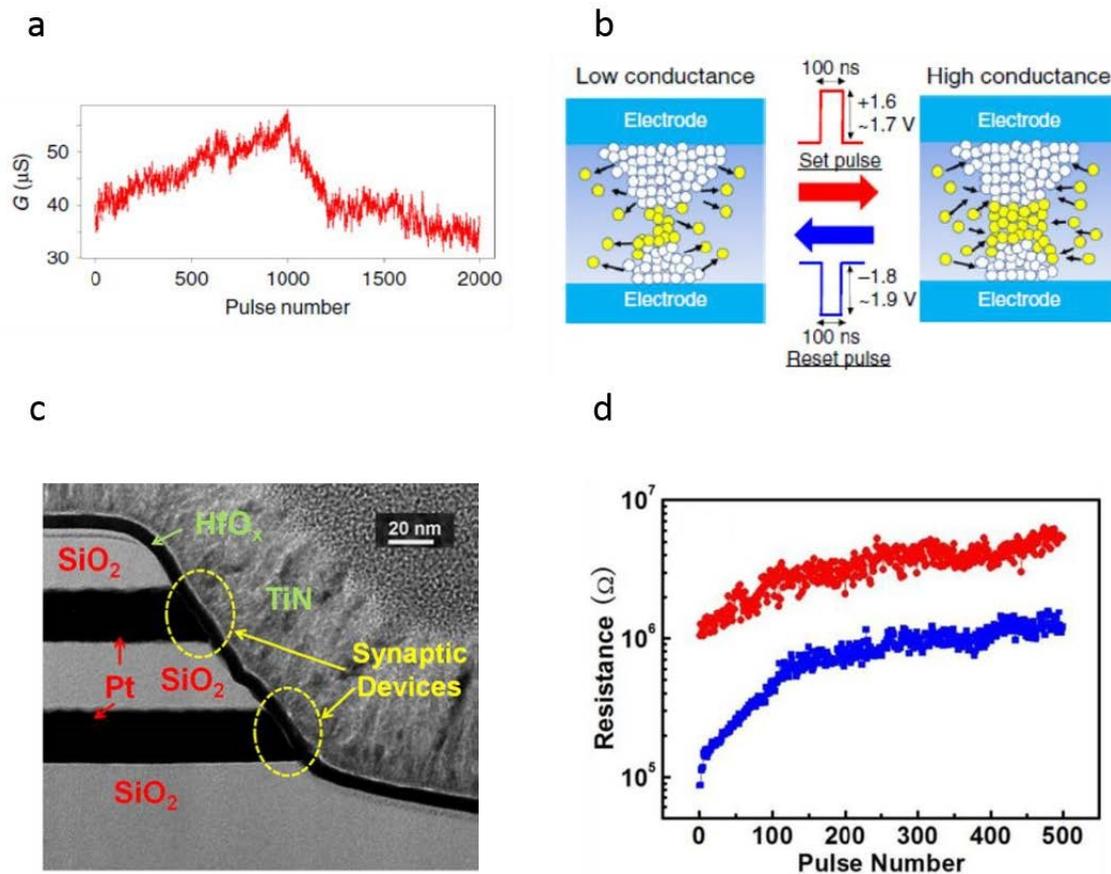
Figure 6. (**a**) Gradual increase (decrease) in conductance behavior in the HfO_2-based resistive switching device induced by 1000 consecutive identical set (reset) pulses. (**b**) A conceptual schematic of a CF confined in the HfO_2-based resistive switching device during switching corresponding to set and reset. Reprinted/adapted with permission from Ref. [41]. 2018, Springer Nature. (**c**) Cross-sectional TEM image of a 3D vertical structure based on HfO_x cells. (**d**) Synaptic behavior with different initial resistances (~100 kΩ and 1 MΩ) of the HfO_2-based 3D vertical synaptic device. In the initial resistance of the 1 MΩ device, the energy consumption decreases below 1 pJ. Reprinted/adapted with permission from Ref. [42]. 2014, American Chemical Society.

Challenges for Anion-Movement-Based Filamentary Two-Terminal Synaptic Devices

In an anion-movement-based filamentary two-terminal synaptic device, as in a cation-movement-based filamentary two-terminal synaptic device, the filament formation process and set switching is inherently abrupt and difficult to control. Hence, anion-movement-based filamentary two-terminal synaptic devices usually employ analog switching in the reset process, where the gradual rupture of CFs is involved [37,42]. However, in order that brain-inspired computing can be efficiently implemented using bidirectional analog switching of the synaptic device, the CF formation process should be controllable, leading to gradual set switching [40]. In addition, a large dynamic range is a critical parameter for high learning accuracy in brain-inspired computing and can provide improved tolerance to cycle-to-cycle and device-to-device variation [63].

The fundamental atomic-level design of the active layer for switching can directly affect the transport of anions and optimize the switching characteristics. Kim et al. demonstrated that the dynamic range can be increased by controlling the ionic hopping parameters such as the hopping distance and drift velocity, based on atomic engineering of the active layer through doping with Si atoms [39]. Figure 7a shows a schematic of the potential energy landscape for the nonlinear transport of anions under a high electric field. The drift velocity of anions is strongly affected by the hopping distance *a*, which can be modulated by Si

doping. Figure 7b exhibits the measured analog switching behaviors of Ta_2O_{5-x} layers with different Si doping concentrations under pulse trains. It can be clearly observed that the dynamic range increases with the doping concentration of Si. Furthermore, an increased Si doping level results in a higher dynamic range but more digital-like switching, due to the larger hopping distance.
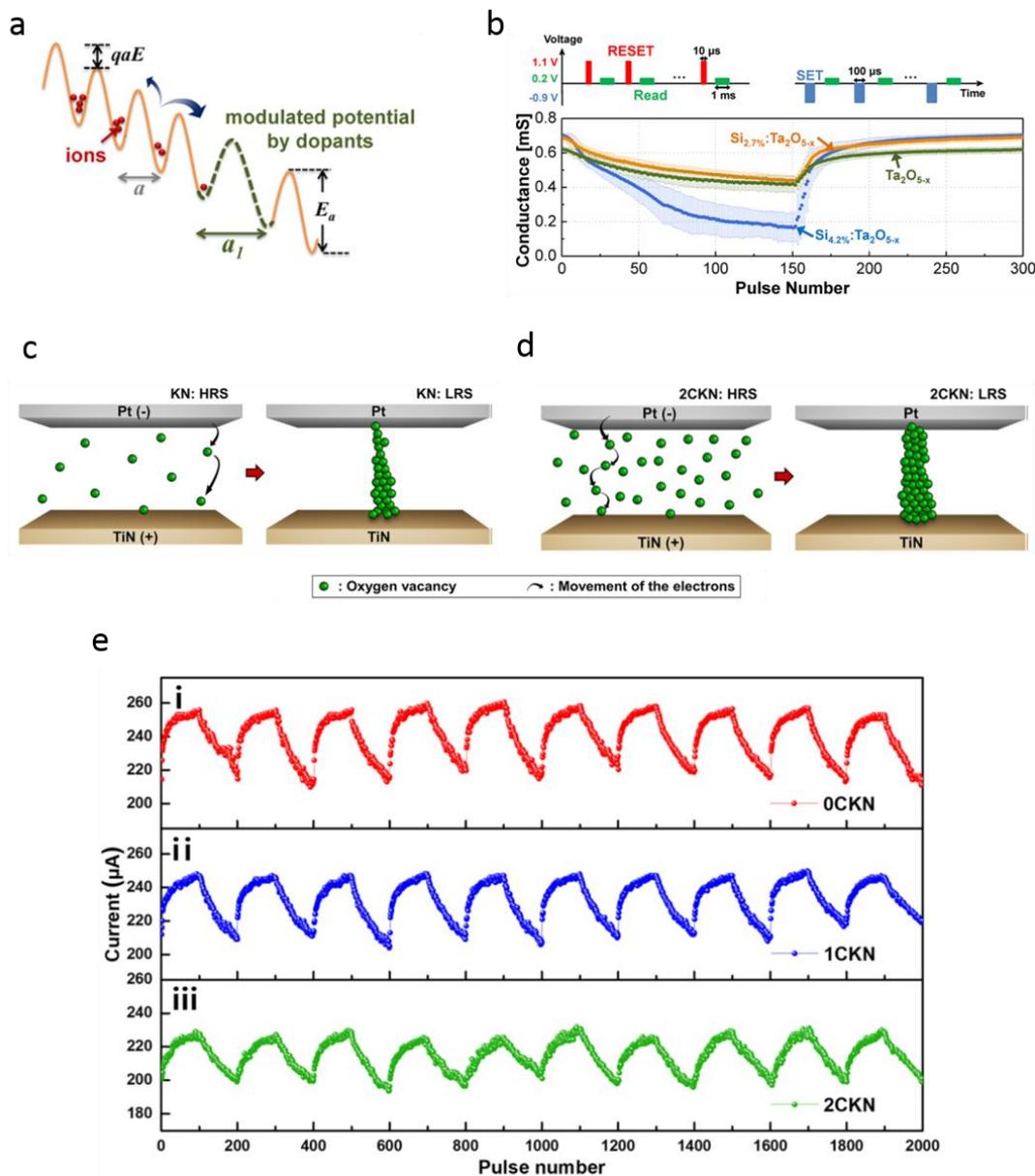

Figure 7. (**a**) Schematic illustration of nonlinear transport of different field−driven anions through the modulated hopping distances (*a* and a_1) for Ta_2O_{5-x} layers with different Si doping concentrations. (**b**) The dynamic range of analog switching depending on the Ta_2O_{5-x} layers with different Si doping concentrations under the same pulse train condition. The upward figure shows the consecutive reset and set pulse cycles applied to obtain depression and potentiation curves, respectively. Reprinted/adapted with permission from Ref. [39]. 2014, American Chemical Society. (**c**,**d**) Schematics of comparison of HRS and LRS in a $Pt/KNbO_3/TiN/Si$ with undoped (**c**) and Cu^{2+}−doped (**d**) $KNbO_3$ layers. (**e**) Potentiation–depression curves of $Pt/KNbO_3/TiN/Si$ with different Cu^{2+} doping concentrations ((i) 0.0, (ii) 1.0, and (iii) 2.0 mol %) in $KNbO_3$ layer with a stimulation number of 100 for potentiation and depression, respectively. Reprinted/adapted with permission from Ref. [43]. 2020, American Chemical Society.

Park et al. reported that the growth/dissolution of CFs in a $KNbO_3$ film is mainly influenced by the redox process of oxygen vacancies, and the linearity of synaptic weight updates in a $Pt/KNbO_3/TiN/Si$ synaptic device is improved when the number of oxygen vacancies in the KNbO3 switching layer is increased through doping with Cu^{2+} ions [43]. Figure 7c,d show schematic illustrations of HRS and LRS in synaptic devices with un-doped and Cu^{2+}-doped $KNbO_3$ layers, respectively. The increased oxygen vacancies in the synaptic device with a Cu^{2+}-doped $KNbO_3$ layer cause the formation of CFs with increased radius during the LRS. Furthermore, it is demonstrated that an increase in the number of oxygen vacancies enhances both the effect of the redox process on the variation of the filaments and the linearity of the synaptic weight updates, as shown in Figure 7e. In addition, the potentiation–depression curves in the 2 mol % Cu^{2+}-doped $KNbO_3$ (2CKN)-based synaptic device are well maintained after 10 cycles, indicating that it has good potentiation–depression cycling properties.

VCM has great potential for applications at circuit or system levels due to fab-friendly materials and the Si-compatible low-temperature processing of the active layer. However, VCM has a high on-state current range, which can lead to energy inefficiency. In addition, the variability problem is yet to be solved. The variability in ECM cells is reduced through formation and modulation of the pathway for cations, while the variability in VCM is hard to solve, because valence is vulnerable to the ambient environment. In order to implement large-scale neuromorphic systems, it is required to develop VCM devices with low on-state current and variability.

4.3. Cation-Movement-Based Ferroelectric Two-Terminal Synaptic Devices

An ultra-thin ferroelectric material can act as a switching layer in cation-movement-based ferroelectric two-terminal resistive switching devices. The attractive advantages of ferroelectric two-terminal resistive switching devices such as fast switching speed and ultra-low power/energy consumption can lead to high performance in the synaptic devices based on them.

Ma et al. reported that a synaptic device with an ultra-short switching time (600 ps) can be implemented by using a $Ag/BaTiO_3$ (~2.4 nm)/$Nb:SrTiO_3$ ferroelectric tunnel junction [47]. The upward and downward ferroelectric polarization directions correspond to the LRS and HRS, respectively. The switching between the two states is bipolar and, interestingly, not abrupt, leading to a broad range of intermediate resistance states. Figure 8a shows the gradual resistance versus voltage pulse behaviors obtained under different negative voltage ranges (−18, −16, −14, and −12 V) with a fixed pulse duration of 600 ps. The ultra-short switching time can be induced by both the high Nb concentration in the $Nb:SrTiO_3$ semiconducting electrode and the low work function of the metal electrode. Figure 8b shows 32 distinct resistive states of the device which can be maintained with no degradation for 10^4 s. To mimic biological synaptic plasticity, the sub-nanosecond (600 ps)-driven conductance change is measured, as shown in Figure 8c. A gradual change in the conductance similar to biological synaptic plasticity can be induced by increasing the amplitude of the negative or positive voltage pulses.

Boyn et al. reported that STDP with an operation time of a few hundred ns can be emulated through ferroelectric domain dynamics [45]. To mimic the various types of STDP shown in Figure 8d–f, they applied different pulse waveforms to a synaptic device based on ferroelectric switching. This procedure allows the generation of biologically realistic, accelerated (Figure 8d,e), or artificially designed (Figure 8f) STDP learning curves. In addition, Figure 8d–f show the excellent agreement between the conductance changes predicted using the nucleation-limited model of ferroelectric domains and the measured conductance variations associated with the various types of STDP.
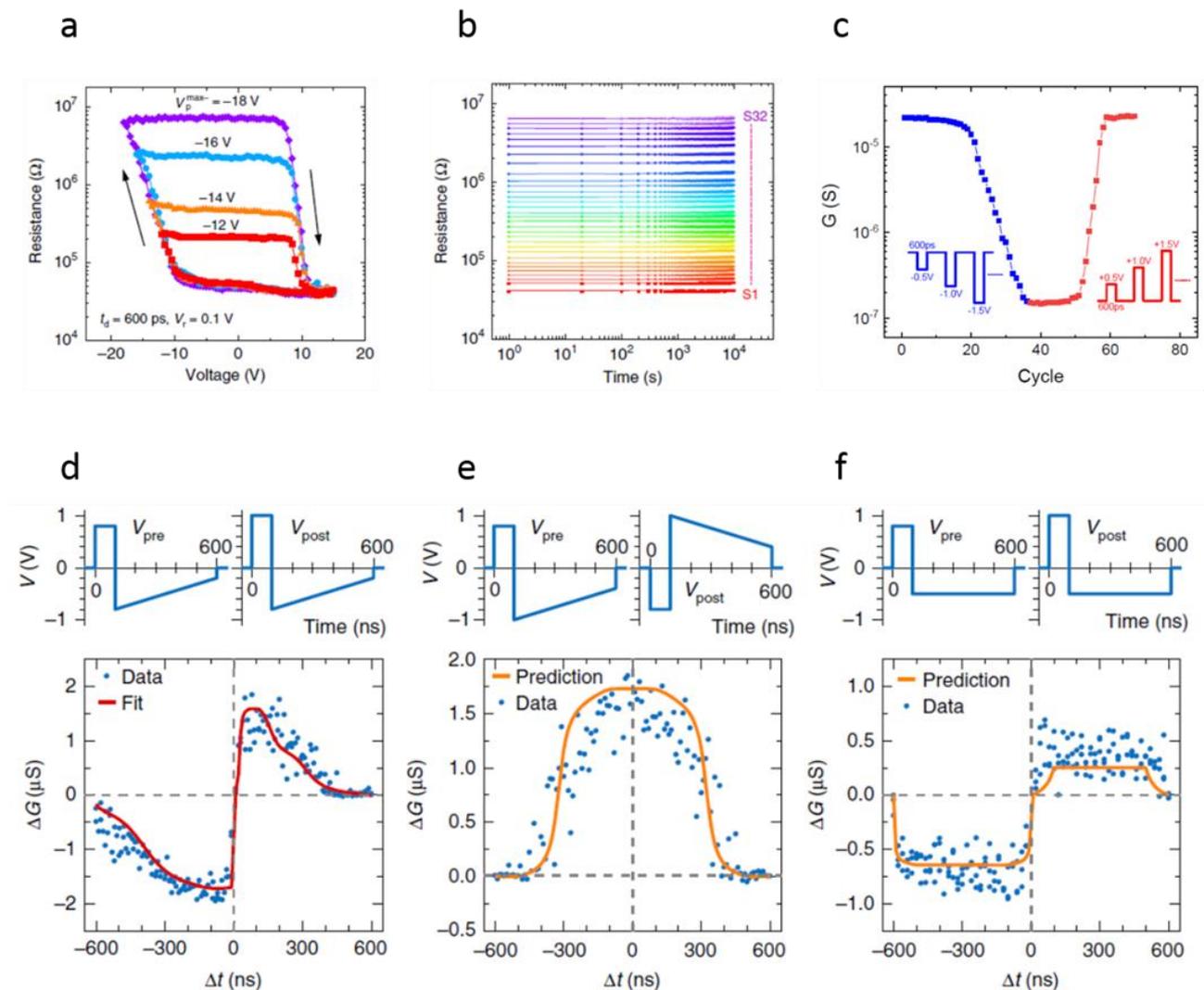
Figure 8. (**a**) Resistive switching with gradual change in $Ag/BaTiO_3$ (~ 2.4 nm)/$Nb:SrTiO_3$ ferroelectric tunnel junction under consecutive pulses (writing voltage = –18, –16, –14, and –12 V, fixed pulse duration = 600 ps). (**b**) Retention characteristics of the $Ag/BaTiO_3$ (~ 2.4 nm)/$Nb:SrTiO_3$ ferroelectric tunnel junction. (**c**) Analog switching behaviors of an ultra-thin ferroelectric-film-based synaptic device ($Ag/BaTiO_3$ (~ 2.4 nm)/$Nb:SrTiO_3$) under consecutive non-identical pulses with a sub-nanosecond (600 ps) duration. Reprinted/adapted with permission from Ref. [47]. 2020, Springer Nature. (**d**–**f**) STDP curves of different forms in an ultra-thin ferroelectric-film-based synaptic device (Co/BFO/CCMO). The top and bottom panels show presynaptic and postsynaptic spikes and the change in conductance, respectively. Reprinted/adapted with permission from Ref. [45]. 2017, Springer Nature.

Chanthbouala et al. reported that a ferroelectric synapse with ultra-short switching time (in the 10–200 ns range) can be implemented by using a Co (10 nm)/Au (10 nm)/$BaTiO_3$ (2 nm)/$La_{0.67}Sr_{0.33}MnO_3$ (30 nm) structure [44]. The upward and downward ferroelectric polarization directions correspond to the LRS and HRS, respectively. The switching between the two states is bipolar and, interestingly, not abrupt; a broad range of intermediate resistance states are observed. The nucleation and growth of ferroelectric domains by systematic variation of the pulse can lead to various resistance states, resulting in synaptic plasticity. Synaptic behaviors based on ferroelectric switching are demonstrated by applying consecutive pulses with a fixed amplitude.

Challenges for Cation-Movement-Based Ferroelectric Two-Terminal Synaptic Devices

A ferroelectric two-terminal synaptic device consists of an ultra-thin ferroelectric barrier inserted between two electrodes. It has attractive characteristics such as ultra-short switching time, nonvolatility, and ultra-low power/energy consumption. However, modulation of the barrier width in these synaptic devices is very limited, leading to a low dynamic range, although the tunneling transmittance depends exponentially on the barrier width [48,95]. The learning accuracy for the synaptic device dramatically decreases for a lower dynamic range [67,73,76]. In addition, to implement low-cost and large-scale arrays of synaptic devices based on ferroelectric switching, we must find suitable ferroelectric materials compatible with silicon or flexible substrates.

Wen et al. proposed a ferroelectric two-terminal resistive switching device employing a metal/ferro-electric/semiconductor heterostructure [95]. The potential energy profiles of the metal/ferroelectric/semiconductor for the LRS and HRS, respectively, depend on the ferroelectric polarization direction. Via polarization reversal in the ultra-thin ferroelectric barrier, the semiconductor surface can be switched between accumulation and depletion of the majority carriers as a result of a ferroelectric field effect. Hence, along with the switching of the barrier height in response to the polarization reversal in the ferroelectric barrier, additional tuning exists via the width of the barrier. The tunneling electrons experience an extra barrier over the space charge region if the semiconductor surface is depleted and the device is switched to the HRS. If the ferroelectric polarization points to the semiconductor, positive bound charges in the ferroelectric/semiconductor interface drive the n-type semiconductor surface into accumulation. This depolarization field lowers the barrier height and generates a higher tunneling transmittance, leading to the LRS. The semiconductor-based ferroelectric tunnel junction exhibits nonvolatile resistive switching behavior with a high dynamic range of above 10^4.

Xi et al. proposed a ferroelectric two-terminal resistive switching device with a dynamic range of 6.0×10^6 employing a $Pt/BaTiO_3/Nb$:$SrTiO_3$ heterostructure [48]. Figure 9a–c show the potential energy profiles of the $Pt/BaTiO_3/Nb$:$SrTiO_3$ in the LRS and HRS, respectively, which depend on the Nb concentration (1.0, 0.1, and 0.01 wt.%) in the Nb:$SrTiO_3$ semi-conducting electrode. For heavily doped Nb:$SrTiO_3$ with a Nb concentration of 1.0 wt.%, the synaptic device shows direct electron tunneling through the ultra-thin $BaTiO_3$ ferro-electric layer, leading to a large current in the LRS. When the Nb concentration decreases to 0.1 wt.%, a Schottky barrier in the $BaTiO_3/Nb$:$SrTiO_3$ appears, and thermally assisted tunneling is still pronounced, leading to a large LRS current comparable to direct tunneling. The device with a Nb concentration of 0.01 wt.% shows a low LRS current resulting from the suppression of thermally assisted tunneling, caused by a high and wide Schottky barrier. In the HRS, the device with a Nb concentration of 1.0 wt.% still shows a thermally assisted tunneling current due to the weak Schottky barrier, while the device with a Nb concentration of 0.1 wt.% has a Schottky barrier high and wide enough to suppress the thermally assisted tunneling. Therefore, the device with a Nb concentration of 0.1 wt.% can achieve a high dynamic range of 6.0×10^6.

Tian et al. fabricated a resistive switching device based on an organic ferroelectric copolymer, poly(viny-lidene fluoride-trifluoroethylene) (P(VDF-TrFE)), which can be applied to large-scale arrays on silicon or flexible substrates [49]. Figure 9d–g show piezoresponse force microscopy (PFM) images of the out-of-plane ferroelectric polarization domains written on bilayer (4.4 nm) and monolayer (2.2 nm) P(VDF-TrFE), respectively. The bright (dark) PFM phase images in Figure 9d–e correspond to upward (downward) polarization after the writing process, indicating polarization reversal in bilayer and mono-layer P(VDF-TrFE) via external bias. Figure 9h shows a schematic illustration of a resistive switching device with an ultra-thin P(VDF-TrFE) film fabricated on a Si substrate. The resistive switching behaviors between HRS and LRS were observed for devices with bilayer and monolayer P(VDF-TrFE), as shown in Figure 9i.
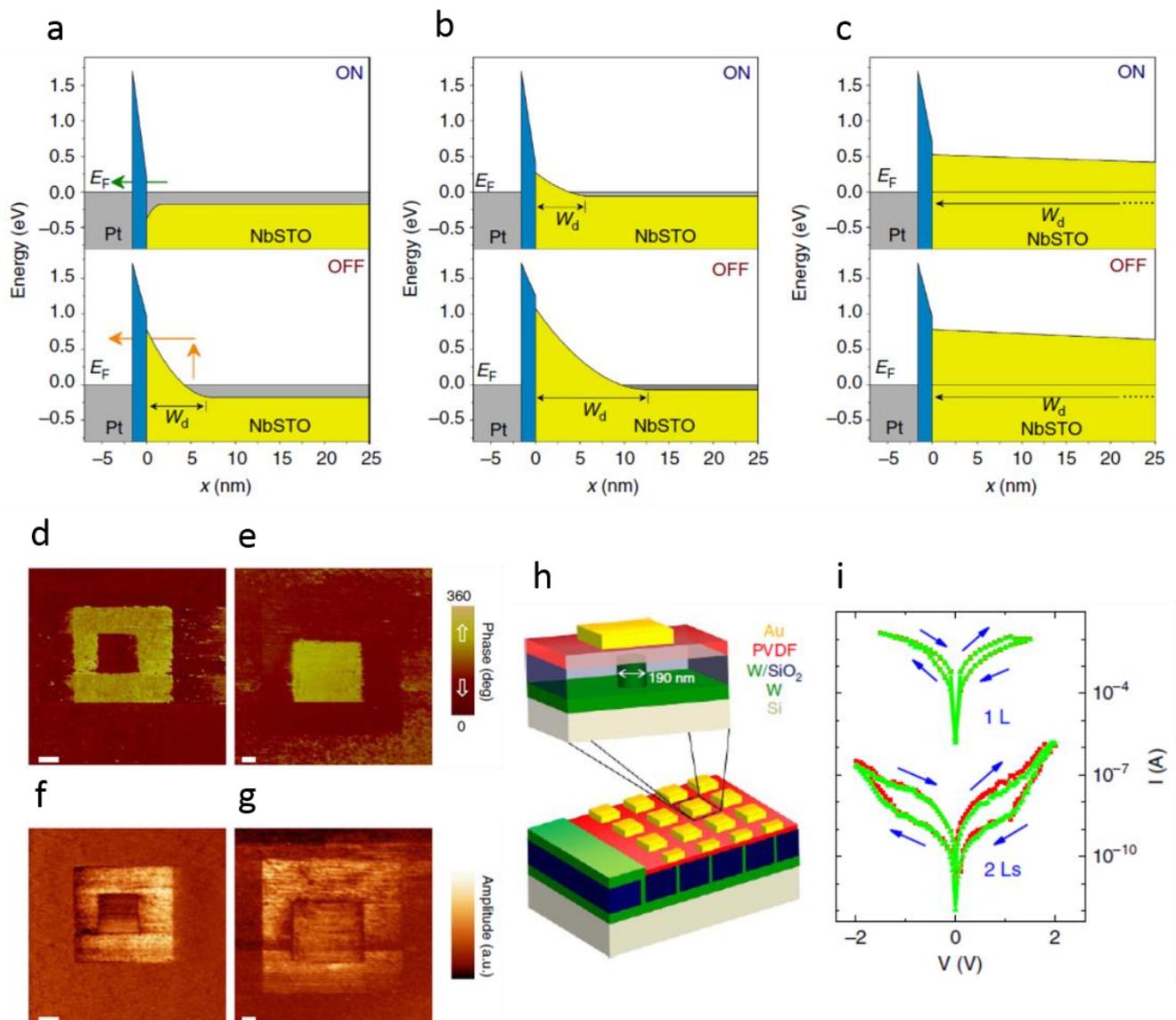
Figure 9. (**a**–**c**) Schematic illustration of potential energy profiles corresponding to the LRS and HRS in the Pt/BaTiO$_3$/Nb:SrTiO$_3$ structures with different Nb concentrations (1.0, 0.1, and 0.01 wt.%) in Nb:SrTiO$_3$ semiconducting electrode. Reprinted/adapted with permission from Ref. [48]. 2017, Springer Nature. (**d**–**g**) PFM phase (**d**,**e**) and amplitude (**f**,**g**) images of bilayer (4.4 nm) and monolayer (2.2 nm) P(VDF-TrFE), respectively. (**h**) Schematics of the Au/ P(VDF-TrFE)/W ferroelectric tunnel-junction-based device. (**i**) Resistance switching behaviors in the 1- and 2-layer P(VDF-TrFE)-based ferroelectric tunnel junction devices. Reprinted/adapted with permission from Ref. [49]. 2016, Springer Nature.

Recently, Li et al. demonstrated a cation-movement-based ferroelectric two-terminal synaptic device with high performance using a metal/ferroelectric/semiconductor heterostructure which has an extra depletion region on the semiconductor surface in the HRS [46]. The potentiation–depression curve for domain switching of the ferroelectric has a dynamic conductance range of 12–150 μS for 200 identical ultra-short pulses with a duration of 50 ns. The linearity of the potentiation–depression curve is the best among two-terminal synaptic devices.

Although FeRAM devices show good performances as synaptic devices, finding a Si-compatible process for the FeRAM is a big challenge. FeRAM devices with good performances usually consist of single-crystal or epitaxial ferroelectric materials. The high

crystallinity requires high growth temperatures or special substrates. Hafnia-based ferro-electric materials show good performances, although they are grown at low temperatures by using atomic layer deposition [107]. In addition, a Si-compatible process for a hafnia-based ferroelectric has been demonstrated [108]. Therefore, a great deal of effort has been focused on realizing neural networks through a hafnia-based ferroelectric.

4.4. Ion-Movement-Based Electrochemical Three-Terminal Synaptic Devices

The ion-movement-based electrochemical three-terminal synaptic device operates in a fundamentally different way from filamentary and ferroelectric synaptic devices. It creates an ion diffusion profile at the surface of the channel, which can be better controlled than the stochastic formation/rupture of CFs and can be more robust to cycle-to-cycle and device-to-device variations [61,96,109].

Burgt et al. fabricated a three-terminal device which comprises a postsynaptic electrode, a poly(3,4-ethylene-dioxythiophene):polystyrene sulfonate (PEDOT:PSS) film partially reduced with poly(ethylenimine) (PEI), interfaced with a PEDOT:PSS presynaptic electrode, and an electrolyte (Nafion) [61]. The potentiation and depression can be induced by a series of 500 pulses with ultra-low amplitude (~1 mV), resulting in 500 distinct conductance states. In addition, this device can be operated by injecting a presynaptic current pulse, displaying a nearly perfect linearity and low cycle-to-cycle variability. The developed flexible device has the potential for low-cost fabrication of arrays, which enables the integration of on-board neuromorphic computing and learning in implantable prosthetics, neural electrode arrays, or any other flexible large-area electronic system.

Ji et al. fabricated an electrochemical three-terminal synaptic device employing a poly(3,4-ethylene-dioxythiophene):tosylate (PEDOT:Tos)/polytetrahydrofu-ran (PTHF) composite as the active channel [65]. Figure 10a shows schematics of the electrochemical three-terminal synaptic device corresponding to a biological synapse and the chemical structures of $PEDOT^+$, Tos^-, and PTHF. The PEDOT:Tos/PTHF composite, as the active channel, is fabricated by the vapor-phase polymerization method. Different mass ratios of PTHF are adopted, and the resulting films are annotated as P-x% PTHF (x = 0, 20, 50, 80, 90) (in the film, x% is the PTHF by mass). The electrochemical three-terminal synaptic device with P-80% PTHF reveals potentiation–depression behaviors with discrete resistance states which are induced by a gating pulse train with a low voltage (<0.8 V) and are maintained over a long time (>200 min), as shown in Figure 10b,c.

Li et al. reported that an inorganic electrochemical three-terminal synaptic device with a Li_xTiO_2 diffusive memristor displays high linearity at both low current level and low writing pulse amplitude [66]. Moreover, the developed device does not need a read-select metal oxide semiconductor (MOS) transistor to switch the device between reading and writing operations. Figure 10d shows a schematic illustration of the inorganic electrochemical three-terminal synaptic device consisting of an inorganic redox transistor and a diffusive memristor selector. To check the conductance updates, a pulse train with a fixed amplitude of ±300 mV and 10 ms duration was applied to the device. Figure 10e shows the gradual change in the device conductance, with high linearity, symmetry, and a precision of 250 with an identical pulse train.

α-MoO_3 is a layered 2D material which allows the reversible intercalation of cations (e.g., H+ and Li+), via a Faradaic reaction involving the reduction/oxidation of Mo ions [51]. Yang et al. reported an all-solid-state electrochemical transistor consisting of a Li-ion-based solid dielectric and 2D α-MoO_3 nanosheets as the channel [51]. The devices can achieve nonvolatile conductance modulation through reversible intercalation of Li ions into the α-MoO_3 lattice. The channel conductance shows nonvolatile characteristics, where each channel conductance obtained after pulse stimulation decays to a stable value different from the previous one. To check the linearity, the asymmetric ratio (AR) was calculated from the 50-cycle LTP and LTD results. The obtained AR value was 0.31 ± 0.12, which is well below those of two-terminal memristive devices triggered by identical pulses (0.55–0.88). In

addition, potentiation–depression curves were measured for 15 electrochemical transistors with a device-to-device variation of <12%, indicating good device-to-device uniformity.
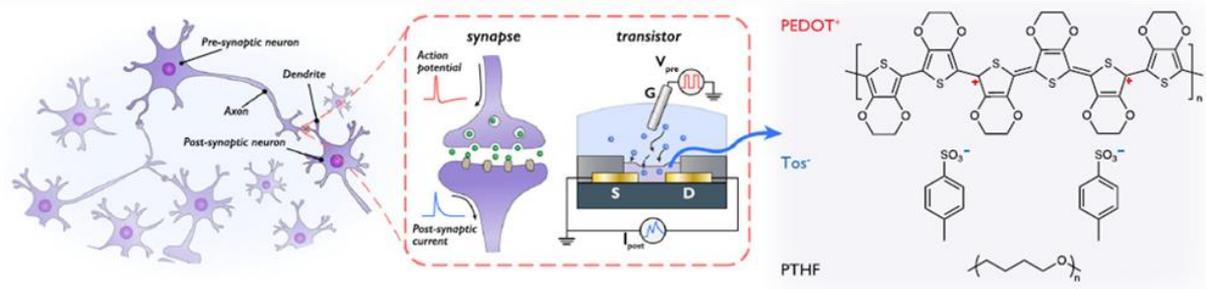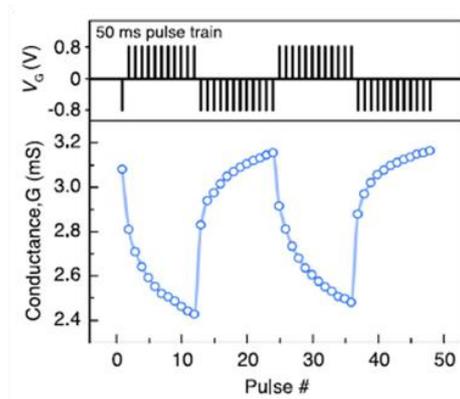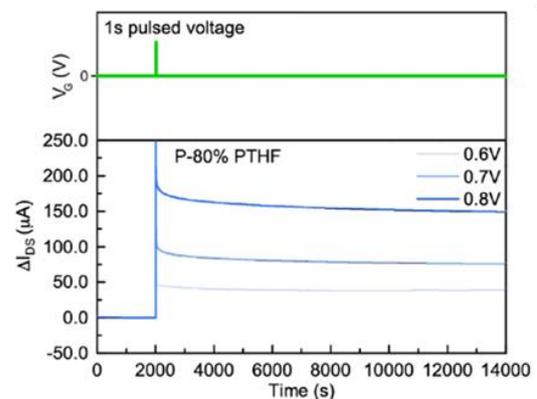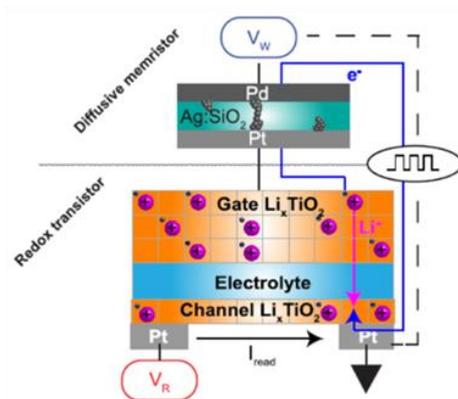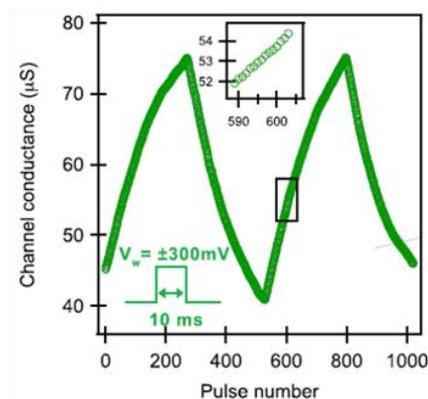

Figure 10. (**a**) Biological synapses and ECRAM–based synaptic device and the chemical structures of PEDOT$^+$, Tos$^-$, and PTHF. (**b**) Potentiation–depression curves of an ECRAM–based synaptic device with PEDOT:Tos/P–80 % PTHF as the active channel. These curves show 12 discrete states by injecting a writing voltage with ultra-low amplitude (+0.8 and −0.8 V). (**c**) Nonvolatile characteristic of the ECRAM-based synaptic device with PEDOT:Tos/P–80 % PTHF as the active channel under pulse stimulation with different amplitudes (0.6, 0.7, and 0.8 V). Reprinted/adapted with permission from Ref. [54]. 2021, Springer Nature. (**d**) Schematic illustration of a composite system of an inorganic redox transistor and a diffusive memristor. (**e**) Potentiation–depression curves of a composite system of an inorganic redox transistor and a diffusive memristor displaying nearly perfect linearity and low cycle-to-cycle variability under an injected pulse train with a fixed ±300 mV amplitude and 10 ms duration. Reprinted/adapted with permission from Ref. [55]. 2019, American Chemical Society.

Challenges for Ion-Movement-Based Electrochemical Three-Terminal Synaptic Devices

Electrochemical three-terminal synaptic devices can induce better modulation of the conductance than two-terminal synaptic devices, due to the separation of the read and write processes. The major challenge preventing the scale-up of inorganic electrochemical three-terminal synaptic devices is the utilization of Li as the doping ion. Li is not compatible with current CMOS processing due to its high volatility and concerns over manufacturing tool contamination [67,68]. In addition, the organic nature of the active channel material in organic electrochemical three-terminal synaptic devices presents challenges for Si-compatible device fabrication and long-term stability [68].

Onen et al. fabricated an electrochemical three-terminal synaptic device using a CMOS-compatible nonvolatile protonic programmable resistor enabled by the phosphosilicate glass electrolyte layer [67]. Figure 11a,b show the schematic illustration and the top-view scanning electron microscope image of the device, respectively. To mimic biological synaptic plasticity, the pulse stimulation is applied to the gate of the developed electrochemical three-terminal synaptic device for the writing process. The conductance of the channel in the device is modulated with high linearity during the writing process, with 100 consecutive pulses with ± 3 V amplitude and 1s duration, as shown in Figure 11c. In addition, the current response of the channel as a function of time, shown in Figure 11d, shows switching between multiple discrete current levels during potentiation and depression processes, as well as good retention during the read operation without gate pulses.

Yao et al. demonstrated an inorganic electrochemical three-terminal synaptic device based on proton intercalation instead of Li-ion movement in a WO_x channel, which is CMOS-compatible [68]. The synaptic device consists of a source (Au), drain (Au), gate (Pd), proton-conductive solid-polymer electrolyte (Nafion-117), and WO_x channel, as shown in Figure 11e. The Pd gate electrode serves the dual role of a reservoir of protons and electrons. After the deposition of Pd, hydrogen is introduced to form PdH_x. The electrolyte has a thickness of 300–400 nm and is fabricated by a spin-coating method (Figure 11f). The device is operated using positive or negative gate-current pulses which are applied in order to migrate protons into or out of the WO_x channel, respectively. Under positive current pulses, PdH_x is electrochemically oxidized, releasing protons that can move through the Nafion-117 electrolyte and intercalate into the WO_x. As a result, the conductance of the WO_x channel is gradually increased, similarly to the potentiation of biological synapses, as shown in Figure 11g. On the other hand, the conductance of the channel is decreased due to the release of protons from the channel during the application of negative current pulses to the gate electrode, leading to depression. In addition, the developed synaptic device shows high linearity, a large dynamic range, and high precision.

Organic electrochemical three-terminal synaptic devices suffer from a limited dynamic range ($<2\times$) between the highest and lowest conductance states induced using short (~1 μs or less) write pulses [63]. The intrinsic semiconducting polymer poly(2-(3,3-bis(2-(2-(2-methoxyethoxy)ethoxy)ethoxy)-[2,2-bithiophene]-5-yl)thieno[3,2-*b*]thiphene) [p(g2T-TT)] was introduced to improve the performances of organic electrochemical transistors [110]. Melianas et al. used ion gel electrolytes by mixing the polymeric insulator poly (vinylidene fluoride-co-hexafluoropropylene) (PVDF-HFP) with common ionic liquids such as 1-ethyl-3-methylimidazolium bis (trifluoromethylsulfonyl)imide (EMIM:TFSI) or 1-ethylimidazolium bis(trifluoromethylsul-fonyl)imide (EIM:TFSI).44. The p(g2T-TT) channel device enables a higher dynamic range (~4×) even under considerably shorter (300 ns) write pulses with an amplitude of 1 V than those needed for PEDOT:PSS channel devices.

ECRAM was recently developed, motivated by a battery system. Therefore, the development of device-level ECRAM presents an open field of research into tasks such as searching for materials, developing device architectures, and optimizing processes. Recently, ECRAM devices fabricated with a Si-compatible process have shown significant potential as synaptic devices. It is expected that large neural networks based on ECRAM produced using the Si-compatible process will be investigated.
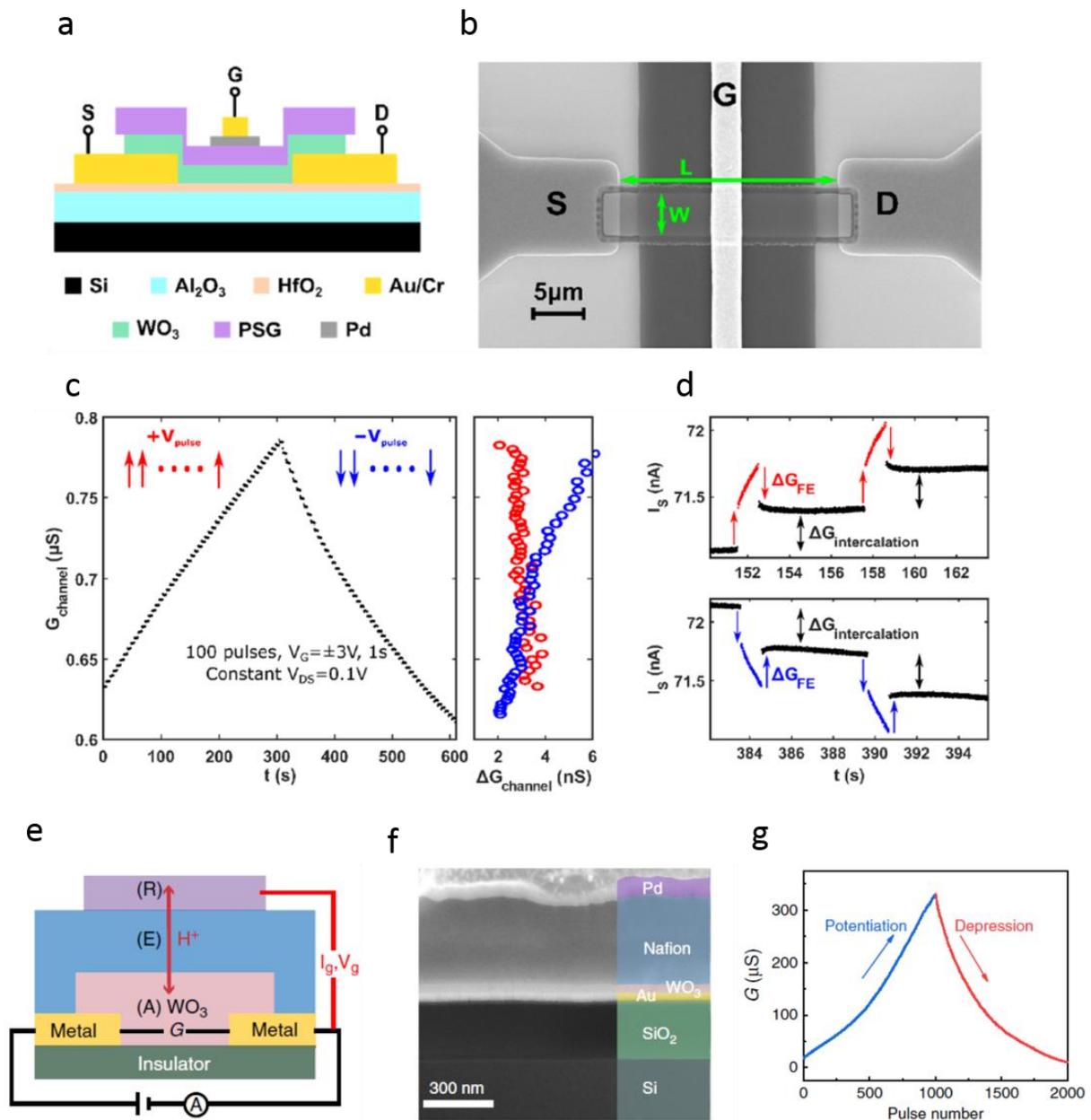
Figure 11. (**a**) Schematic illustration of the protonic programmable resistor for CMOS–compatible electrochemical three–terminal synaptic device. (**b**) The top–view scanning electron microscope image of an electrochemical three–terminal synaptic device with phosphosilicate glass as an electrolyte layer. (**c**) Potentiation–depression curve of a CMOS–compatible electrochemical three–terminal synaptic device consisting of phosphosilicate glass as an electrolyte layer obtained by injecting 100 consecutive pulses with ±3 V amplitude and 1s duration. This curve shows high linearity and low cycle–to–cycle variability. (**d**) The current response of the channel for multiple discrete currents with nonvolatile behavior in a CMOS–compatible electrochemical three–terminal synaptic device with phosphosilicate glass. Reprinted/adapted with permission from Ref. [56]. 2021, American Chemical Society. (**e**,**f**) Cross–sectional schematic illustration (**e**) and scanning electron microscopy image (**f**) of an inorganic electrochemical three–terminal synaptic device based on proton intercalation in a WO_x channel. (**g**) Potentiation–depression curves of an inorganic electrochemical three–terminal synaptic device with the proton–conductive solid–polymer electrolyte (Nafion–117) as electrolyte, via operation spikes of ±200 nA amplitude with 5 ms duration. The curves reveal high linearity, a large dynamic range, and high precision. Reprinted/adapted with permission from Ref. [57]. 2020, Springer Nature.

5. Conclusions

The development of synaptic devices for brain-inspired computing has progressed in the last few years. In this review, we discussed the fact that ion-movement-based synaptic devices of different types can be used to realize brain-inspired computing. In addition, we reviewed the strengths and weaknesses of each of these synaptic devices when applied to ANNs in brain-inspired computing. However, each device has remaining issues to be resolved for fully satisfying the specifications of a synaptic device for ANN: (1) linearity and cycle-to-cycle variation for a filamentary system based on cation and anion movement; (2) linearity and device-to-device variation for a cation-movement-based ferroelectric; and (3) dynamic range for an ion-movement-based electrochemical three-terminal device. To address these issues, various fields must be involved, from materials science to device design. In addition, synaptic devices should be optimized using circuit- or system-level simulators based on a compact model of reliability degradation for performance benchmarking and circuit design. If the challenges for each of the different types of synaptic devices are resolved, large-scale integration based on ion-movement-based synaptic devices will be realized in the near future, leading to the implementation of brain-inspired computing chips with low energy consumption, high scalability, and high processing speed. Therefore, ion-movement-based synaptic devices for brain-inspired computing continue to represent a potentially attractive solution to the problem of highly parallel and distributed processing of massive amounts of data, and thus can be expected to remain an active area of research.

References

1. Atzori, L.; Iera, A.; Morabito, G. The internet of things: A survey. *Comput. Netw.* **2010**, *54*, 2787–2805. [CrossRef]
2. Zanella, A.; Bui, N.; Castellani, A.; Vangelista, L.; Zorzi, M. Internet of things for smart cities. *IEEE Internet Things J.* **2014**, *1*, 22–32. [CrossRef]
3. Gubbi, J.; Buyya, R.; Marusic, S.; Palaniswami, M. Internet of things (IoT): A vision, architectural elements, and future directions. *Future Gener. Comput. Syst.* **2013**, *29*, 1645–1660. [CrossRef]
4. Hu, M.; Graves, C.E.; Li, C.; Li, Y.; Ge, N.; Montgomery, E.; Davila, N.; Jiang, H.; Williams, R.S.; Yang, J.J.; et al. Memristor-based analog computation and neural network classification with a dot product engine. *Adv. Mater.* **2018**, *30*, 1705914. [CrossRef]
5. Park, H.L.; Lee, Y.; Kim, N.; Seo, D.G.; Go, G.T.; Lee, T.W. Flexible Neuromorphic Electronics for Computing, Soft Robotics, and Neuroprosthetics. *Adv. Mater.* **2020**, *32*, 1903558. [CrossRef]
6. Xu, M.; Mai, X.; Lin, J.; Zhang, W.; Li, Y.; He, Y.; Tong, H.; Hou, X.; Zhou, P.; Miao, X. Recent Advances on Neuromorphic Devices Based on Chalcogenide Phase-Change Materials. *Adv. Funct. Mater.* **2020**, *30*, 2003419. [CrossRef]
7. Silver, D.; Schrittwieser, J.; Simonyan, K.; Antonoglou, I.; Huang, A.; Guez, A.; Hubert, T.; Baker, L.; Lai, M.; Bolton, A.; et al. Mastering the game of Go without human knowledge. *Nature* **2017**, *550*, 354. [CrossRef]
8. Ferrucci, D.; Brown, E.; Chu-Carroll, J.; Fan, J.; Gondek, D.; Kalyanpur, A.A.; Lally, A.; Murdock, J.W.; Nyberg, E.; Prager, J. Building Watson: An overview of the DeepQA progect. *AI Mag.* **2010**, *31*, 59–79.
9. Rachlin, H. Making IBM's computer, Watson, human. *Behav. Anal.* **2012**, *35*, 1–16. [CrossRef]
10. Kuzum, D.; Yu, S.; Wong, H.P. Synaptic electronics: Materials, devices and applications. *Nanotechnology* **2013**, *24*, 382001. [CrossRef]
11. Jeong, D.S.; Kim, K.M.; Kim, S.; Choi, B.J.; Hwang, C.S. Memristors for Energy-Efficient New Computing Paradigms. *Adv. Electron. Mater.* **2016**, *2*, 1600090. [CrossRef]
12. Sangwan, V.K.; Hersam, M.C. Neuromorphic nanoelectronic materials. *Nat. Nanotechnol.* **2020**, *15*, 517–528. [CrossRef] [PubMed]
13. Zokopoulos, P.C.; Eaton, C.; Deroos, D.; Deutsch, T.; Lapis, G. *Understanding Big Data: Analytics for Enterprise Class Hadoop and Streaming Data*; McGraw-Hill: New York, NY, USA, 2012.

14. Upadhyay, N.K.; Jiang, H.; Wang, Z.; Asapu, S.; Xia, Q.; Yang, J.J. Emerging Memory Devices for Neuromorphic Computing. *Adv. Mat. Technol.* **2019**, *4*, 1800589. [CrossRef]
15. Goodfellow, I.; Bengio, Y.; Courville, A. *Deep Learning*; The MIT Press: Cambridge, MA, USA, 2016.
16. LeCun, Y.; Bengio, Y.; Hinton, G. Deep learning. *Nature* **2015**, *521*, 436–444. [CrossRef] [PubMed]
17. Sengupta, B.; Stemmler, M.B. Power consumption during neuronal computation. *Proc. IEEE* **2014**, *102*, 738–750. [CrossRef]
18. James, C.D.; Aimone, J.B.; Miner, N.E.; Vineyard, C.M.; Rothganger, F.H.; Carlson, K.D.; Mulder, S.A.; Draelos, T.J.; Faust, A.; Marinella, M.J.; et al. A historical survey of algorithms and hardware architectures for neural-inspired and neuromorphic computing applications. *Biol. Insp. Cog. Arch.* **2017**, *19*, 49–64. [CrossRef]
19. Schuman, C.D.; Potok, T.E.; Patton, R.M.; Birdwell, J.D.; Dean, M.E.; Rose, G.S.; Plank, J.S. A survey of neuromorphic computing and neural networks in hardware. *arXiv* **2017**, arXiv:1705.06963.
20. Bear, M.F.; Connors, B.W.; Paradiso, M.A. *Neuroscience: Exploring the Brain*; Wolters Kluwer Health: Philadelphia, PA, USA, 2015.
21. Indiveri, G.; Chicca, E.; Douglas, R.J. Artificial Cognitive systems: From VLSI networks of spiking neurons to neuromorphic cognition. *Cogn. Comput.* **2009**, *1*, 119–127. [CrossRef]
22. Indiveri, G.; Linares-Barranco, B.; Hamilton, T.J.; Schaik, A.; Etienne-Cummings, R.; Delbruck, T.; Liu, S.C.; Dudek, P.; Häfliger, P.; Renaud, S.; et al. Neuromorphic silicon neuron circuit. *Front. Neurosci.* **2011**, *5*, 73. [CrossRef]
23. Bezrukov, S.M.; Kish, L.B. Deterministic multivalued logic scheme for information processing and routing in the brain. *Phys. Lett. A* **2009**, *375*, 2338–2342. [CrossRef]
24. Gingl, Z.; Kish, L.B.; Khatri, S.P. Towards brain-inspired computing. *Fluct. Noise Lett.* **2010**, *9*, 403–412. [CrossRef]
25. Chandrasekar, A.; Rakkiyappan, R. Impulsive controller design for exponential synchronization of delayed stochastic memristor-based recurrent neural networks. *Neurocomputing* **2016**, *173*, 1348–1355. [CrossRef]
26. Sun, J.; Han, J.; Wang, Y.; Liu, P. Memristor-based neural network circuit of emotion congruent memory with mental fatigue and emotion inhibition. *IEEE Trans. Biomed. Circuits Syst.* **2021**, *15*, 606. [CrossRef] [PubMed]
27. Wang, L.; Shen, Y. Design of controller on synchronization of memristor-based neural networks with time-varying delays. *Neurocomputing* **2015**, *147*, 372–379. [CrossRef]
28. Sun, J.; Han, J.; Liu, P.; Wang, Y. Memristor-based neural network circuit of pavlov associative memory with dual mode switching. *Int. J. Electron. Commun. AEÜ* **2021**, *129*, 153552. [CrossRef]
29. Sun, J.; Han, G.; Zeng, Z.; Wang, Y. Memristor-based neural network circuit of full-function pavlov associative memory with time delay and variable learning rate. *IEEE Trans. Cybern.* **2020**, *50*, 2935. [CrossRef]
30. Jo, S.H.; Chang, T.; Ebong, I.; Bhadviya, B.B.; Mazumder, P.; Lu, W. Nanoscale memristor device as synapse in neuromorphic system. *Nano Lett.* **2010**, *10*, 1297–1301. [CrossRef]
31. Xu, R.; Jang, H.; Lee, M.H.; Amanov, D.; Cho, Y.; Kim, H.; Park, S.; Shin, H.; Ham, D. Vertical MoS$_2$ Double-Layer Memristor with Electrochemical Metallization as an Atomic-Scale Synapse with Switching Thresholds approaching 100 mV. *Nano Lett.* **2019**, *19*, 2411–2417. [CrossRef]
32. Fu, T.; Liu, X.; Gao, H.; Ward, J.E.; Liu, X.; Yin, B.; Wang, Z.; Zhuo, Y.; Walker, D.J.F.; Yang, J.J.; et al. Bioinspired bio-voltage memristors. *Nat. Commun.* **2020**, *11*, 1861. [CrossRef]
33. Yoon, C.; Lee, J.H.; Lee, S.; Jeon, J.H.; Jang, J.T.; Kim, D.H.; Kim, Y.H.; Park, B.H. Synaptic plasticity selectively activated by polarization-dependent energy-efficient ion migration in an ultrathin ferroelectric tunnel junction. *Nano Lett.* **2017**, *17*, 1949–1955. [CrossRef]
34. Jang, B.C.; Kim, S.; Yang, S.Y.; Park, J.; Cha, J.H.; Oh, J.; Choi, J.; Im, S.G.; Dravid, V.P.; Choi, S.Y. Polymer analog memristive synapse with atomic-scale conductive filament for flexible neuromorphic computing system. *Nano Lett.* **2018**, *19*, 839–849. [CrossRef]
35. Choi, S.; Tan, S.H.; Li, Z.; Kim, Y.; Choi, C.; Chen, P.Y.; Yeon, H.; Yu, S.; Kim, J. SiGe epitaxial memory for neuromorphic computing with reproducible high performance based on engineered dislocations. *Nat. Mater.* **2018**, *17*, 335–340. [CrossRef] [PubMed]
36. Kim, K.; Park, S.; Hu, S.M.; Song, J.; Lim, W.; Jeong, Y.; Kim, J.; Lee, S.; Kwak, J.Y.; Pakr, J.; et al. Enhanced analog synaptic behavior of SiNx/a-Si bilayer memristors through Ge implantation. *NPG Asia Mater.* **2020**, *12*, 77. [CrossRef]
37. Yu, S.; Gao, B.; Fang, Z.; Yu, H.; Kang, J.; Wong, H.S. A low energy oxide-based electronic synaptic device for neuromorphic visual systems with tolerance to device variation. *Adv. Mater.* **2013**, *25*, 1774–1779. [CrossRef] [PubMed]
38. Du, C.; Ma, W.; Chang, T.; Sheridan, P.; Lu, W.D. Biorealistic implementation of synaptic functions with oxide memristors through internal ionic dynamics. *Adv. Funct. Mater.* **2015**, *25*, 4290–4299. [CrossRef]
39. Kim, S.; Choi, S.; Lee, J.; Lu, W.D. Tuning resistive switching characteristics of tantalum oxide memristors through Si doping. *ACS Nano* **2014**, *10*, 10262–10269. [CrossRef]
40. Wu, H.; Yao, P.; Gao, B.; Wu, W.; Zhang, Q.; Zhang, W.; Deng, N.; Wu, D.; Wong, H.S.; Yu, S.; et al. Device and circuit optimization of RRAM for neuromorphic computing. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 11.5.1–11.5.4.
41. Gong, N.; Idé, T.; Kim, S.; Boybat, I.; Sebastian, A.; Narayanan, V.; Ando, T. Signal and noise extraction from analog memory elements for neuromorphic computing. *Nat. Commun.* **2018**, *9*, 2102. [CrossRef]
42. Gao, B.; Bi, Y.; Chen, H.-Y.; Liu, R.; Huang, P.; Chen, B.; Liu, L.; Liu, X.; Yu, S.; Wong, H.-S.P.; et al. Ultra-low-energy three-dimensional oxide-based electronic synapses for implementation of robust high-accuracy neuromorphic computation systems. *ACS Nano* **2014**, *8*, 6998–7004. [CrossRef]

43. Park, S.-M.; Hwang, H.-G.; Woo, J.-U.; Lee, W.-H.; Chae, S.-J.; Nahm, S. Improvement of conductance modulation linearity in a Cu^{2+}-doped $KNbO_3$ memristor through the increase of the number of oxygen vacancies. *ACS Appl. Mater. Interfaces* **2020**, *12*, 1069–1077. [CrossRef]

44. Chanthbouala, A.; Garcia, V.; Cherifi, R.O.; Bouzehouane, K.; Fusil, S.; Moya, X.; Xavier, S.; Yamada, H.; Deranlot, C.; Mathur, N.D.; et al. A ferroelectric memristor. *Nat. Mater.* **2012**, *11*, 860–864. [CrossRef]

45. Boyn, S.; Grollier, J.; Lecerf, G.; Xu, B.; Locatelli, N.; Fusil, S.; Girod, S.; Carrétéro, C.; Garcia, K.; Xavier, S.; et al. Learning through ferroelectric domain dynamics in solid-state synapses. *Nat. Commun.* **2017**, *8*, 14736. [CrossRef]

46. Li, J.; Ge, C.; Du, J.; Wang, C.; Yang, G.; Jin, K. Reproducible ultrathin ferroelectric domain switching for high-performance neuromorphic computing. *Adv. Mater.* **2020**, *32*, 1905764. [CrossRef] [PubMed]

47. Ma, C.; Zuo, Z.; Huang, W.; Zhao, L.; Chen, Q.; Lin, Y.; Liu, X.; Chen, Z.; Liu, C.; Sun, H.; et al. Sub-nanosecond memristor based on ferroelectric tunnel junction. *Nat. Commun.* **2020**, *11*, 1439. [CrossRef] [PubMed]

48. Xi, Z.; Ruan, J.; Li, C.; Zheng, C.; Wen, Z.; Dai, J.; Li, A.; Wu, D. Giant tunneling electroresistance in metal/ferroelectric/semiconductor tunnel junctions by engineering the schottky barrier. *Nat. Commun.* **2017**, *8*, 15217. [CrossRef] [PubMed]

49. Tian, B.B.; Wang, J.L.; Fusil, S.; Liu, Y.; Zhao, X.L.; Sun, S.; Shen, H.; Lin, T.; Sun, J.L.; Duan, C.G.; et al. Tunnel electroresistance through organic ferroelectrics. *Nat. Commun.* **2016**, *7*, 11502. [CrossRef]

50. Burgt, Y.; Lubberman, E.; Fuller, E.J.; Keene, S.T.; Faria, G.C.; Agarwal, S.; Marinella, M.J.; Talin, A.A.; Salleo, A. A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat. Mater.* **2017**, *16*, 414. [CrossRef]

51. Yang, C.S.; Shang, D.S.; Liu, N.; Fuller, E.J.; Agrawal, S.; Talin, A.A.; Li, Y.Q.; Shen, B.G.; Sun, Y. All-solid-state synaptic transistor with ultralow conductance for neuromorphic computing. *Adv. Funct. Mater.* **2018**, *28*, 1804170. [CrossRef]

52. Melianas, A.; Quill, T.J.; LeCroy, G.; Tuchman, Y.; Loo, H.V.; Keene, S.T.; Giovannitti, A.; Lee, H.R.; Maria, I.P.; McCulloch, I.; et al. Temperature-resilient solid-state organic artificial synapses for neuromorphic computing. *Sci. Adv.* **2020**, *6*, eabb2958. [CrossRef]

53. Kim, S.; Todorov, T.; Onen, M.; Gokmen, T.; Bishop, D.; Solomon, P.; Lee, K.T.; Copel, M.; Farmer, D.B.; Ott, J.A.; et al. Metal-oxide based CMOS-compatible ECRAM for Deep Learning Accelerator. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 35.7.1–35.7.4.

54. Ji, X.; Paulsen, B.D.; Chik, G.K.K.; Wu, R.; Yin, Y.; Chan, P.K.L.; Rivnay, J. Mimicking associative learning using an ion-trapping non-volatile synaptic organic electrochemical transistor. *Nat. Commun.* **2021**, *12*, 2480. [CrossRef]

55. Li, Y.; Fuller, E.J.; Asapu, S.; Agarwal, S.; Kurita, T.; Yang, J.J.; Talin, A.A. Low-voltage, CMOS-free synaptic memory based on LixTiO2 redox transistors. *ACS Appl. Mater. Interfaces* **2019**, *11*, 38982–38992. [CrossRef]

56. Onen, M.; Emond, N.; Li, J.; Yildiz, B.; Alamo, J.A. CMOS-compatible protonic programmable resistor based on phosphosilicate glass electrolyte for analog deep learning. *Nano Lett.* **2021**, *21*, 6111–6116. [CrossRef]

57. Yao, X.; Klyukin, K.; Lu, W.; Onen, M.; Ryu, S.; Kim, D.; Emond, N.; Waluyo, I.; Hunt, A.; Alamo, J.A.; et al. Protonic solid-state electrochemical synapse for physical neural networks. *Nat. Commun.* **2020**, *11*, 3134. [CrossRef] [PubMed]

58. Zhang, X.; Zhuo, Y.; Luo, Q.; Wu, Z.; Midya, R.; Wang, Z.; Song, W.; Wang, R.; Upadhyay, N.K.; Fang, Y.; et al. An artificial spiking afferent nerve based on Mott memristors for neurorobotics. *Nat. Commun.* **2020**, *11*, 51. [CrossRef] [PubMed]

59. Pickett, M.D.; Medeiros-Ribeiro, G.; Williams, R.S. A scalable neuristor built with Mott memristors. *Nat. Mater.* **2013**, *12*, 114–117. [CrossRef]

60. Stoliar, P.; Tranchant, J.; Corraze, B.; Janod, E.; Besland, M.P.; Tesler, F.; Rozenberg, M.; Cario, L. A leaky-integrate-and-fire neuron analog realized with a Mott insulator. *Adv. Funct. Mater.* **2017**, *27*, 1604740. [CrossRef]

61. Wan, Q.; Sharbati, M.T.; Erickson, J.R.; Du, Y.; Xiong, F. Emerging Artificial Synaptic Devices for Neuromorphic Computing. *Adv. Mater. Technol.* **2019**, *4*, 1900037. [CrossRef]

62. Zhu, J.; Zhang, T.; Yang, Y.; Huaing, R. A comprehensive review on emerging artificial neuromorphic devices. *Appl. Phys. Rev.* **2020**, *7*, 011312. [CrossRef]

63. Zucker, R.S.; Regehr, W.G. Short-Term synaptic plasticity. *Annu. Rev. Physiol.* **2002**, *64*, 355–405. [CrossRef] [PubMed]

64. Bi, G.Q.; Poo, M.M. Synaptic Modifications in Cultured Hippocampal Neurons: Dependence on Spike Timing, Synaptic Strength, and postsynaptic cell type. *J. Neurosci.* **1998**, *18*, 10464–10472. [CrossRef]

65. Zhang, L.I.; Tao, H.W.; Holt, C.E.; Harris, W.A.; Poo, M.M. A critical window for cooperation and competition among developing retinotectal synapses. *Nature* **1998**, *395*, 37–44. [CrossRef]

66. Markram, H.; Lübke, J.; Frotscher, M.; Sakmann, B. Regulation of Synaptic Efficacy by Coincidence of Postsynaptic APs and EPSPs. *Science* **1997**, *275*, 213. [CrossRef]

67. Chen, P.Y.; Lin, B.; Wang, I.T.; Hou, T.H.; Ye, J.; Vrudhula, S.; Seo, J.; Cao, Y.; Yu, S. Mitigating effects of non-ideal synaptic device characteristics for on-chip learning. In Proceedings of the 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, USA, 2–6 November 2015; pp. 194–199.

68. Zhao, M.; Gao, B.; Tang, J.; Qian, H.; Wu, H. Reliability of analog resistive switching memory for neuromorphic computing. *Appl. Phys. Rev.* **2020**, *7*, 011301. [CrossRef]

69. Ambrogio, S.; Narayanan, P.; Tsai, H.; Shelby, R.M.; Boybat, I.; Nolfo, C.; Sidler, S.; Giordano, M.; Bodini, M.; Farinha, N.C.P.; et al. Equivalent-accuracy accelerated neural-network training using analogue memory. *Nature* **2018**, *558*, 60–67. [CrossRef] [PubMed]

70. Chen, P.Y.; Yu, S. Reliability perspective of resistive synaptic devices on the neuromorphic system performance. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; pp. 5C.4-1–5C.4-4.

71. Chen, P.Y.; Peng, X.; Yu, S. NeuroSim$^+$: An integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures. In Proceedings of the2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 6.1.1–6.1.4.

72. Yu, S. Neuro-inspired computing with emerging nonvolatile memory. *Proc. IEEE* **2018**, *106*, 260–285. [CrossRef]

73. Yu, S.; Chen, P.Y.; Cao, Y.; Xia, L.; Wang, Y.; Wu, H. Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect. In Proceedings of the2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 17.3.1–17.3.4.

74. Liu, R.; Lee, H.Y.; Yu, S. Analyzing inference robustness of rram synaptic array in low-precision neural network. In Proceedings of the 47th European Solid-State Device Research Conference (ESSDERC), Leuven, Belgium, 11–14 September 2017; pp. 18–21.

75. Burr, G.W.; Shelby, R.M.; Nolfo, C.; Jang, J.; Boybat, I.; Shenoy, R.S.; Narayanan, P.; Virwani, K.; Giacometti, E.U.; Kurdi, B.N.; et al. Experimental demonstration and tolerancing of a large-scale neural network (165000 synapses) using phase-change memory as the synaptic weight element. *IEEE Trans. Electron. Dev.* **2015**, *62*, 3498–3507. [CrossRef]

76. Kim, S.; Choi, B.; Lim, M.; Yoon, J.; Lee, J.; Kim, H.D.; Choi, S.J. Pattern recognition using carbon nanotube synaptic transistors with an adjustable weight update protocol. *ACS Nano* **2017**, *11*, 2814–2822. [CrossRef]

77. Lee, J.; Lu, W.D. On-Demand Reconfiguration of Nanomaterials: When Electronics Meets Ionics. *Adv. Mater.* **2018**, *30*, 1702770. [CrossRef]

78. Cha, J.H.; Yang, S.Y.; Oh, J.; Choi, S.; Park, S.; Jang, B.C.; Ahn, W.; Choi, S.Y. Conductive-bridging random-access memories for emerging neuromorphic computing. *Nanoscale* **2020**, *12*, 14339–14368. [CrossRef]

79. Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories—Nanoionic Mechanisms, Prospects, and Challenges. *Adv. Mater.* **2009**, *21*, 2632–2663. [CrossRef]

80. Waser, R.; Aono, M. Nanoionics-based resistive switching memories. *Nat. Mater.* **2007**, *6*, 833–840. [CrossRef]

81. Valov, I.; Waser, R.; Jameson, J.R.; Kozicki, M.N. Electrochemical metallization memories-fundamentals, applications, prospects. *Nanotechnology* **2011**, *22*, 254003. [CrossRef]

82. Burr, G.W.; Shelby, R.M.; Sebastian, A.; Kim, S.; Kim, S.; Sidler, S.; Virwani, K.; Ishii, M.; Narayanan, P.; Fumarola, A.; et al. Neuromorphic computing using non-volatile memory. *Adv. Physics X* **2017**, *2*, 89–124. [CrossRef]

83. Hasegawa, T.; Terabe, K.; Tsuruoka, T.; Aono, M. Atomic Switch Atom Ion Movement Controlled Devices for Beyond Von-Neumann Computers. *Adv. Mater.* **2012**, *24*, 252–267. [CrossRef] [PubMed]

84. Valov, I.; Lu, W.D. Nanoscale electrochemistry using dielectric thin film as solid electrolytes. *Nanoscale* **2016**, *8*, 13828. [CrossRef] [PubMed]

85. Jameson, J.R.; Gilbert, N.; Koushan, F.; Saenz, J.; Wang, J.; Hollmer, S.; Kozicki, M.; Derhacobian, N. Quantized Conductance in Ag/GeS$_2$/W Conductive-Bridge Memory Cells. *IEEE Electron. Dev. Lett.* **2012**, *33*, 257–259. [CrossRef]

86. Yuan, F.; Zhang, Z.; Liu, C.; Zhou, F.; Yau, H.M.; Lu, W.; Qiu, X.; Wong, H.S.; Dai, J.; Chai, Y. Real-time observation of the electrode-size-dependent evolution dynamics of the conducting filaments in a SiO$_2$ layer. *ACS Nano* **2017**, *11*, 4097–4104. [CrossRef]

87. Kozicki, M.N.; Park, M.; Mitkova, M. Nanoscale Memory Elements Based on solid-state electrolytes. *IEEE Trans. Nanotechnol.* **2005**, *4*, 331–338. [CrossRef]

88. Butler, J. A kinetic theory of reversible oxidation potentials at inert electrodes. *Trans. Faraday Soc.* **1924**, *19*, 734–739. [CrossRef]

89. Valov, I.; Staikov, G. Nucleation and growth phenomena in nanosized electrochemical systems for resistive switching memories. *J. Solid State Electrochem.* **2013**, *17*, 356–371. [CrossRef]

90. Jo, S.H.; Kim, K.H.; Lu, W. Programmalbe resistance switching in nanoscale two-terminal devices. *Nano Lett.* **2009**, *9*, 496–500. [CrossRef]

91. Celano, U.; Goux, L.; Belmonte, A.; Opsomer, K.; Franquet, A.; Schulze, A.; Detavernier, C.; Richard, O.; Bender, H.; Jurczak, M.; et al. Three-Dimensional Observation of the Conductive Filament in Nanoscaled resistve memory devices. *Nano Lett.* **2014**, *14*, 2401–2406. [CrossRef]

92. Izyumskaya, N.; Alivov, Y.I.; Cho, S.J.; Morkoç, H.; Lee, H.; Kang, Y.S. Processing, Structure, Properties, and Application of PZT thin films. *Crit. Rev. Solid State Mat. Sci.* **2007**, *32*, 111–202. [CrossRef]

93. Seelecke, S.; Kim, S.J.; Ball, B.L.; Smith, R.C. A rate-dependent two-dimensional free energy model for ferroelectric single crystals. *Int. J. Solids Struct.* **2007**, *44*, 1196–1209. [CrossRef]

94. Wei, Y.; Nukala, P.; Salverda, M.; Matzen, S.; Zhao, H.J.; Momand, J.; Everhardt, A.S.; Agnus, G.; Blake, G.R.; Lecoeur, P.; et al. A rhombohedral ferroelectric phase in epitaxially strained Hf$_{0.5}$Zr$_{0.5}$O$_2$ thin films. *Nat. Mater.* **2018**, *17*, 1095–1100. [CrossRef] [PubMed]

95. Wen, Z.; Li, C.; Wu, D.; Li, A.; Ming, N. Ferroelectric-filed-effect-enhanced electroresistance in meta/ferroelectric/semiconductor tunnel junctions. *Nat. Mater.* **2013**, *12*, 617–621. [CrossRef] [PubMed]

96. Burgt, Y.; Melianas, A.; Keene, S.T.; Malliaras, G.; Salleo, A. Organic electronics for neuromorphic computing. *Nat. Electron.* **2018**, *1*, 386. [CrossRef]

97. Sharbati, M.T.; Du, Y.; Torres, J.; Ardolino, N.D.; Yun, M.; Xiong, F. Low-power, electrochemically tunable graphene synapses for neuromorphic computing. *Adv. Mater.* **2018**, *30*, 1802353. [CrossRef] [PubMed]

98. Yang, C.S.; Shang, D.S.; Liu, N.; Shi, G.; Shen, X.; Yu, R.C.; Li, Y.Q.; Sun, Y. A synaptic transistor based on quasi-2d molybdenum oxide. *Adv. Mater.* **2017**, *29*, 1700906. [CrossRef]

99.   Shi, J.; Ha, S.D.; Zhou, Y.; Schoofs, F.; Ramanathan, S. A correlated nickelate synaptic transistor. *Nat. Commun.* **2013**, *4*, 2376.
        [CrossRef]

100.   Wang, S.; Chen, C.; Yu, Z.; He, Y.; Chen, X.; Wan, Q.; Shi, Y.; Zhang, D.W.; Zhou, H.; Wang, X.; et al. A MoS_2/PTCDA hybrid
        heterojunction synapse with efficient photoelectric dual modulation and versatility. *Adv. Mater.* **2019**, *31*, 1806227. [CrossRef]

101.   Fuller, E.J.; Keene, S.T.; Melianas, A.; Wang, Z.; Agarwal, S.; Li, Y.; Tuchman, Y.; James, C.D.; Marinella, M.J.; Yang, J.J.; et al.
        Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing. *Science* **2019**, *364*, 570–574.
        [CrossRef]

102.   Lee, M.J.; Lee, S.; Lee, S.; Balamurugan, K.; Yoon, C.; Jang, J.T.; Kim, S.H.; Kwon, D.H.; Kim, M.; Ahn, J.P.; et al. Synaptic devices
        based on two-dimensional layered single-crystal chromium thiophosphate. *NPG Asia Mater.* **2018**, *10*, 23–30. [CrossRef]

103.   Yang, J.J.; Strukov, D.B.; Stewart, D.R. Memristive devices for computing. *Nat. Nanotechnol.* **2013**, *8*, 13–24. [CrossRef] [PubMed]

104.   Chen, P.Y.; Peng, X.; Yu, S. NeuroSim: A circuit-level macro model for benchmarking neuro-inspired architectures in online
        learning. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2018**, *37*, 3067–3080. [CrossRef]

105.   Agarwal, S.; Plimpton, S.J.; Hughart, D.R.; Hsia, A.H.; Richter, I.; Cox, J.A.; James, C.D.; Marinella, M.J. Resistive memory device
        requirements for a neural algorithm accelerator. In Proceedings of the 2016 International Joint Conference on Neural Networks
        (IJCNN), Vancouver, BC, Canada, 24–29 July 2016; pp. 929–938.

106.   Ge, J.; Li, D.; Huang, C.; Zhao, X.; Qin, J.; Liu, H.; Ye, W.; Xu, W.; Liu, Z.; Pan, S. Memristive synapses with high reproducibility
        for flexible neuromorphic networks based on biological nanocomposites. *Nanoscale* **2020**, *12*, 720. [CrossRef] [PubMed]

107.   Cheema, S.S.; Kwon, D.; Shanker, N.; Reis, R.; Hsu, S.-L.; Xiao, J.; Zhang, H.; Wagner, R.; Datar, A.; McCater, M.R.; et al. Enhanced
        ferroelectricity in ultrathin films grown directly on silicon. *Nature* **2020**, *580*, 478. [CrossRef]

108.   Luo, Q.; Cheng, Y.; Yang, J.; Cao, R.; Ma, H.; Yang, Y.; Huang, R.; Wei, W.; Zheng, Y.; Gong, T.; et al. A highly CMOS compatible
        hafnia-based ferroelectric diode. *Nat. Commun.* **2020**, *11*, 1391. [CrossRef]

109.   Zhou, Y.; Ramanathan, S. Mott memory and neuromorphic devices. *Proc. IEEE* **2015**, *103*, 1289–1310. [CrossRef]

110.   Giovannitti, A.; Sbircea, D.T.; Inal, S.; Nielsen, C.B.; Bandiello, E.; Hanifi, D.A.; Sessolo, M.; Malliaras, G.G.; McCulloch, I.; Rivnay,
        J. Controlling the mode of operation of organic transistors through side-chain engineering. *Proc. Natl. Acad. Sci. USA* **2016**,
        113, 12017–12022. [CrossRef]