Article

High-Quality Few-Layer Graphene on Single-Crystalline SiC thin Film Grown on Affordable Wafer for Device Applications

Norifumi Endoh [1], Shoji Akiyama [2], Keiichiro Tashima [1], Kento Suwa [1], Takamasa Kamogawa [1], Roki Kohama [1], Kazutoshi Funakubo [1], Shigeru Konishi [2], Hiroshi Mogi [2], Minoru Kawahara [2], Makoto Kawai [2], Yoshihiro Kubota [2], Takuo Ohkochi [3], Masato Kotsugi [3], Koji Horiba [4], Hiroshi Kumigashira [4,5], Maki Suemitsu [1], Issei Watanabe [6] and Hirokazu Fukidome [1,*]

1   Research Institute of Electrical Communication, Tohoku University, Sendai, Miyagi 980-8577, Japan; noriendo912@gmail.com (N.E.); tashey@riec.tohoku.ac.jp (K.T.); kensuwa@riec.tohoku.ac.jp (K.S.); b8tm2513@riec.tohoku.ac.jp (T.K.); r-kohama@riec.tohoku.ac.jp (R.K.); kazutoshi.funakubo@shi-g.com (K.F.); suemitsu@riec.tohoku.ac.jp (M.S.)
2   Shin-Etsu Chemical Co., Ltd., Chiyoda-ku, Tokyo 100-0004, Japan; s.akiyama@shinetsu.jp (S.A.); s_konishi@shinetsu.jp (S.K.); hiro_mogi@shinetsu.jp (H.M.); minoru.kawahara@shinetsu.jp (M.K.); mak_kawai@shinetsu.jp (M.K.); kubota-yoshihiro@shinetsu.jp (Y.K.)
3   Japan Synchrotron Radiation Research Institute, Sayo, Hyogo 679-5198, Japan; o-taku@spring8.or.jp (T.O.); kotsugi@spring8.or.jp (M.K.)
4   Photon Factory, Institute of Materials Structure Science, High Energy Accelerator Research Organization, Tsukuba, Ibaraki 305-0801, Japan; horiba@post.kek.jp (K.H.); kumigashira@tohoku.ac.jp (H.K.)
5   Institute of Multidisciplinary Research for Advanced Materials (IMRAM), Tohoku University, Sendai, Miyagi 980-8577, Japan
6   National Institute of Information and Communication Technology, Koganei, Tokyo 184-8795, Japan; issei@nict.go.jp
*   Correspondence: fukidome@riec.tohoku.ac.jp

Abstract: Graphene is promising for next-generation devices. However, one of the primary challenges in realizing these devices is the scalable growth of high-quality few-layer graphene (FLG) on device-type wafers; it is difficult to do so while balancing both quality and affordability. High-quality graphene is grown on expensive SiC bulk crystals, while graphene on SiC thin films grown on Si substrates (GOS) exhibits low quality but affordable cost. We propose a new method for the growth of high-quality FLG on a new template named "hybrid SiC". The hybrid SiC is produced by bonding a SiC bulk crystal with an affordable device-type wafer and subsequently peeling off the SiC bulk crystal to obtain a single-crystalline SiC thin film on the wafer. The quality of FLG on this hybrid SiC is comparable to that of FLG on SiC bulk crystals and much higher than of GOS. FLG on the hybrid SiC exhibited high carrier mobilities, comparable to those on SiC bulk crystals, as anticipated from the linear band dispersions. Transistors using FLG on the hybrid SiC showed the potential to operate in terahertz frequencies. The proposed method is suited for growing high-quality FLG on desired substrates with the aim of realizing graphene-based high-speed devices.

Keywords: epitaxial graphene; SiC; affordable; transistor; terahertz

1. Introduction

Graphene, which is a two-dimensional honeycomb lattice of carbon atoms, exhibits a linear band dispersion of π-electrons near the Fermi level [1–5]. This linear band dispersion results in excellent electronic properties, such as an extremely high carrier mobility [2–4], because of the vanishing of electron backscattering [6]. Furthermore, short-channel effects, which inhibit device integration, are suppressed in graphene, owing to its ultimate thinness [7]. These properties make graphene attractive for use in next-generation devices, such as field-effect transistors (FETs) [2,3,8,9] and lasers with frequencies in the terahertz range [10,11], which can provide the missing link between electronic information processing and optical communications [12].

For the realization of graphene-based devices, it is essential to develop methods for the scalable growth of high-quality graphene on semi-insulating device-type wafers [13]. One promising method involves growing high-quality few-layer graphene (FLG) on SiC bulk single crystals by annealing the crystals to sublimate the surface Si atoms [14,15]. SiC bulk crystals are used in power electronics and are now scaled up to 6 inches in diameter. In addition, this graphitization method eliminates the risk of metal contamination, which has an adverse effect on the functioning of devices such as p-n junctions. Although microscopic variations might exist in the thickness of the thus-grown FLG samples, the use of mesa on SiC substrates fabricated by conventional lithography techniques compatible with existing electronics (e.g., Si integrated circuits) has allowed for the realization of step-free SiC surfaces [16]. This has resulted in the growth of single-layer graphene without microscopic variations in thickness at the desired places for use in cases where high reliability is essential for device functioning, such as FET channels several microns in size [16]. Furthermore, in addition to single-layer graphene, homogeneous high-quality bilayer graphene can also be grown on SiC bulk crystals at temperatures higher than that for single-layer graphene growth [17]. Bilayer graphene on SiC bulk crystals exhibits a considerable bandgap under a vertical electric field [18]; this is predicted to ensure a high on/off ratio ($>10^4$) in graphene-based tunnel FETs [19].

FLG grown on single-crystal SiC is hence promising owing to the above reasons and because of its compatibility with existing electronics (e.g., SiC-based power electronics). Unfortunately, the price of semi-insulating SiC bulk crystals is high. It has thus been difficult to balance affordability and quality when it comes to graphene. To achieve a balance between affordability and quality, we have developed a method for growing FLG on SiC thin films grown directly on Si by sublimating Si atoms on the SiC surface (GOS). The SiC thin films were grown directly on Si substrates using gas-source molecular beam epitaxy, with the source gas being monomethylsilane ($H_3C–SiH_3$) [20–24]. Moreover, combining this growth method and the three-dimensional micropatterning of the Si substrates opens a new way of controlling the formation of metallic and semiconductive FLG at desired locations on Si substrates on the nanoscale [25]. This method shows promise as a pathway towards the integration of electronic and photonic devices that employ graphene for the active layer.

Unfortunately, the quality of GOS remains low compared to that of FLG grown on SiC bulk crystals. This is because of the surface roughness of the 3C-SiC thin film, owing to the large mismatch in the lattice constants of SiC and Si [20–24].

Here we present a new method for the growth of high-quality FLG using a new template, which is termed "hybrid SiC" which consists of a high-quality SiC thin film by the peeling from a SiC bulk crystal, and an affordable device-type wafer. This method allows for the growth of high-quality FLG at affordable costs without any risk of contamination. FLG on the hybrid SiC showed excellent electronic properties. Field-effect transistors (FETs) using FLG on the hybrid SiC exhibited a simultaneous achievement of a large transconductance and drain current saturation. The FET demonstrates the potential to operate terahertz frequencies, and is promising for next-generation wireless communication.

2. Materials and Methods

The proposed method for growing high-quality FLG on the hybrid SiC is shown schematically in Figure 1a. The growth process is classified into two parts. The first part is the fabrication of the hybrid SiC [26]. First, H^+ ions are implanted in the Si face of an on-axis 3-inch SiC bulk crystal to form a cut line (dashed line in Figure 1a), at which the SiC crystal can be separated easily. Then, the SiC bulk crystal is bonded to a device-type wafer (a 3-inch poly-SiC wafer was used in this study) with the intermediate layer, such as a SiO_2 thin layer, which inhibits the channeling during the H^+ implantation. During the bonding, the pressure was given by wafer's own weight and the heating at ~600 K was performed. This is followed by the peeling of the SiC bulk crystal from the device-type wafer. The device-type wafer can be, for example, poly-SiC, Si, and sapphire. Finally, the

surface is flattened by chemomechanical polishing (CMP). This SiC fabrication process is repeatable. Namely, multiple hybrid SiC can be produced by using a SiC bulk crystal. The thickness of the resulting SiC thin film on a device-type wafer was 300 nm. The second part is the graphitization of the hybrid SiC surface by annealing at 1850 K to sublimate the Si atoms on the surface in an argon atmosphere (1 bar), in a manner similar to epitaxial growth on SiC bulk crystals [14,16]. The graphitization was done by using radio frequency induction heating furnace installed in a super clean room (class < 10) of Research Institute of Electrical Communication (RIEC), Tohoku University.
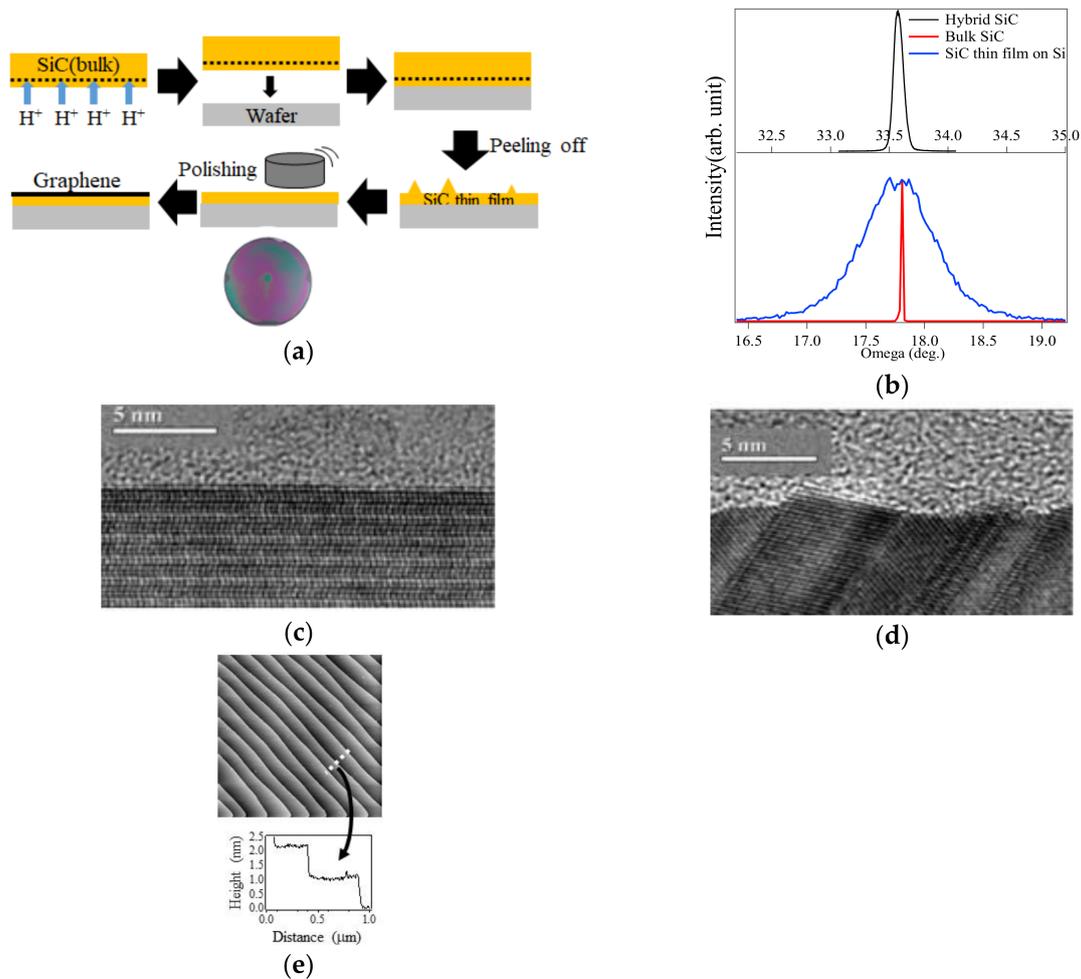

Figure 1. (**a**) Schematics of the fabrication of the hybrid SiC. (**b**) The x-ray diffraction of the hybrid SiC, a 3C-SiC thin film on a Si substrate. (**c**,**d**) are cross-sectional transmission electron micrographs of the hybrid SiC surface and the 3C-SiC thin film on the Si substrate, respectively. (**e**) The atomic force microscopy image of the hybrid surface. Inset shows the line profile across the dotted line.

X-ray diffraction (XRD) was used to characterize the crystallinity of the hybrid SiC, SiC bulk crystal, a 3C- thin film on a Si substrate. X-ray rocking curves were performed by using x-ray diffractometer (SuperLab, Rigaku, Tokyo, Japan) at RIEC. The curves were used to acquire XRD spectra of the hybrid SiC, and the 3C-SiC thin film on the Si substrate and the SiC bulk crystal. Atomic force microscopy was used to probe nanoscale surface roughness of the hybrid SiC. The AFM imaging was performed in air by using atomic force microscopy (Nanocute, Seiko Instruments, Chiba, Japan).

Raman spectroscopy was performed to evidence the high-quality of FLG on the hybrid SiC. Raman spectra were obtained by Raman microscopy (InVia™ confocal Raman microscope, Renishaw, Tokyo, Japan) at an excitation energy of 2.41 eV and lateral resolution of 1 μm.

Low-energy electron spectroscopy (LEEM) was performed to probe microscopic distribution of graphene layer number on the hybrid SiC. The LEEM imaging was done by using a low-energy electron microscope installed at BL 17 SU at SPring-8 (LEEM III, Elmitec, Clausthal-Zellerfeld, Germany) [27,28]. Before the LEEM imaging, the sample was degassed at 873 K under an ultrahigh vacuum (UHV) environment ($<10^{-7}$ Pa). The layer number is digitally determined from the number of the dip in the electron reflectivity spectra which were obtained from the LEEM images [29]. The LEEM imaging was performed at room temperature under the UHV environment. By using the LEEM, microscopic LEED (μ-LEED) was carried out by collecting diffracted electrons from the region imaged by LEEM. The image was distorted a little because of the electron optics of the LEEM instrument [25].

Angle-resolved photoelectron spectroscopy (ARPES) using vacuum ultraviolet (VUV) radiation and core level spectroscopy using soft X-rays (SX) were performed at beamline BL-2 MUSASHI of Photon Factory, High Energy Accelerator Research Organization, Japan. Two undulators for the VUV and SX radiation arranged in a tandem alignment allowed for irradiation of the same position on the sample surface. The ARPES and C 1s core level photoelectron spectroscopy measurements were performed at photon energies of 80 and 800 eV, respectively, with the total resolutions being 20 and 200 meV, respectively. The sample was cooled to 20 K by using liquid He. The Fermi level of the sample was calibrated by measurements of a gold film that was electrically connected to the sample.

Hall-effect mobility measurement was performed to acquire carrier mobility and carrier density of FLG on the hybrid SiC and the SiC bulk crystal by using Van der Pauw method [30]. The carrier density (n_s) is inversely proportional to the Hall voltage:

$$n_s = \frac{BI}{eV_H} \tag{1}$$

where V_H, B, I, e are the Hall voltage, magnetic field, current, and elemental charge, respectively. We calculated n_s using Equation (1). The typical size of the pattern was 50×50 μm. The measurement was performed at room temperatures and under atmospheric environment at RIEC.

Transistors using FLG on the hybrid SiC was fabricated by using the cleanroom of RIEC. The gate insulator was formed by depositing on yttrium thin film, followed by oxidation in air at room temperatures. The gate length and width were 3.8 μm and 10 μm, respectively. The distance between the source and drain electrodes were 8 μm. The thickness of the yttrium oxide was 13.6 nm. Ti/Au thin film (5 nm/150 nm) was deposited on the sample for the formation of source, drain, and gate electrodes. The electrical characterization was performed by using semiconductor parameter analyzer (Agilent B1500A, Keysight).

3. Results

3.1. High Film Quality of the SiC Thin Film in the Hybrid SiC

The quality of SiC is a determining factor in the film quality of graphene layers grown on SiC. We examined the quality of the hybrid SiC by using XRD and X-TEM, and AFM. The crystallinity of the hybrid SiC was investigated by the x-ray rocking curves, as shown in Figure 1b. The full width at half maximum (FWHM) of the hybrid SiC (0.048) was order of magnitude smaller than that of 3C-SiC(111) (0.71), and comparable to that of the SiC bulk crystal (0.015). The obtained FWHM value clearly demonstrated that the crystallinity of the SiC thin film in the hybrid SiC was greatly improved, compared to that of the 3C-SiC thin film on Si(111), and comparable to that of SiC bulk crystal.

The atomistic surface morphology was examined by cross-sectional transmission electron microscopy (X-TEM) (Figure 1c), and compared with that of the 3C-SiC thin film grown directly on a Si substrate (Figure 1d). The X-TEM image of the 3C-SiC thin film (Figure 1d) shows that the grains were separated by grain boundaries, and the size of grains was on the order of 10 nm, as observed in the previous report [31]. On the other hand, the

X-TEM image of the hybrid SiC (Figure 1c) confirms its single-crystalline nature; the grain boundaries are barely visible. Furthermore, the hybrid SiC had wide terraces with regularly spaced steps (Figure 1d). Thus, the hybrid SiC has a higher bulk and surface qualities, compared to that of the 3C-SiC thin film grown on the Si substrate, and comparable to that of the SiC bulk crystal.

3.2. High Film-Quality FLG Growth on the Hybrid SiC

The high quality of growth substrates promises high quality of materials on it. In fact, we demonstrated the high quality growth of FLG on the hybrid SiC by using C 1*s* core level photoelectron spectroscopy, X-TEM, and Raman spectroscopy, as shown below.

The chemical compositions of FLGs on the Si-face and C-face hybrid SiC were revealed by the C 1s core level spectroscopy, as shown in Figure 2a. In the spectrum of FLG on the C-face hybrid SiC, the spectrum consists of two peaks due to FLG (∼284.5 eV) and SiC (∼282.3 eV) [22,23,25,32]. On the other hand, in the spectrum of FLG on the Si-face hybrid SiC, the spectrum contains the peaks labelled as peaks S1 and S2 due to the presence of the buffer layer [25,31], in addition to the peaks due to FLG and SiC. These results are consistent with the previous study on the graphene growth on the Si-face and C-face SiC bulk crystals [32,33]. This indicates that FLG on the hybrid SiC grows in a similar manner to that on the SiC bulk crystals.
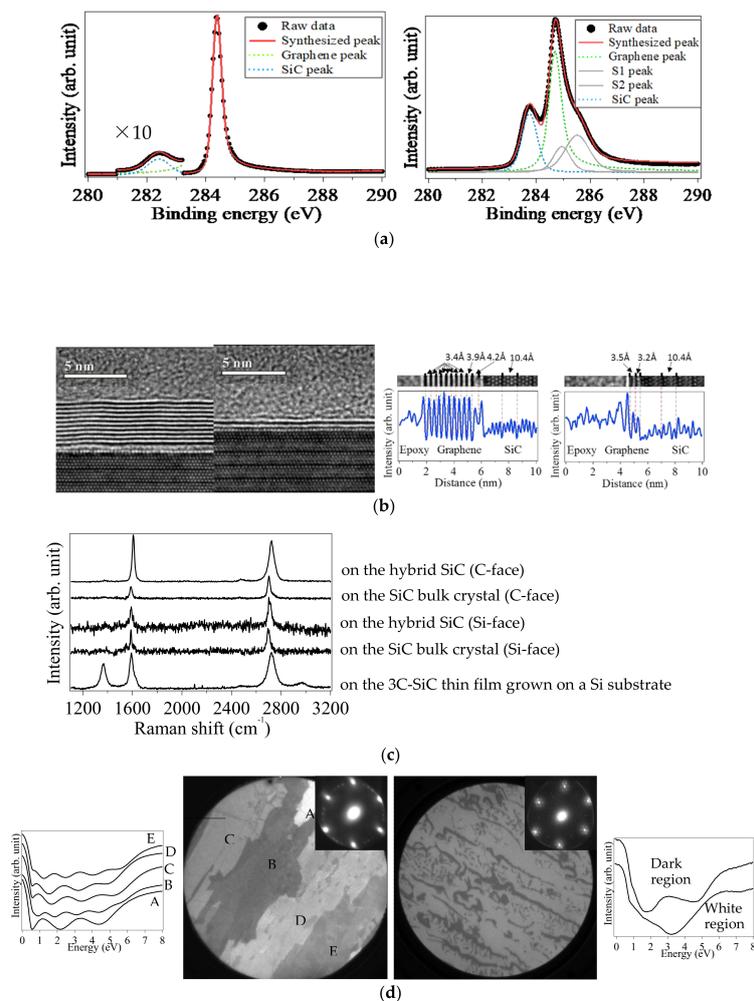

(a)

(b)

(c)

(d)

Figure 2. (**a**) C 1s core level spectra of graphene on the C-face (left) and the Si-face (right) hybrid SiC, respectively. (**b**) Transmission electron micrographs and line profiles of the interfaces between the C-face (left) and Si-face (right) hybrid SiC. (**c**) Raman spectra of graphene grown on the C-face of hybrid SiC and of the SiC bulk crystal, Si-face of hybrid SiC and the SiC bulk crystal, and the 3C-SiC thin film grown on the Si substrate from the top to the bottom, respectively. (**d**) LEEM images and electron spectra of graphene on the C-face (left) and Si-face (right) hybrid SiC, respectively. The field of view is 30 μm, and the energy of the incident electron for the LEEM imaging is 2 eV. The insets are μ-LEED taken from the observed regions.

Interfaces between FLGs and the Si-face and C-face hybrid SiC was investigated by X-TEM, as shown in Figure 2b. The X-TEM images clearly visualized the formation of the abrupt interfaces consisting of non-defective FLG and atomically flat Si-face and C-face hybrid SiC. The distance between the Si-face hybrid SiC surface and the nearest layer, the buffer layer on the Si-face SiC (3.2 Å) which was detected by the C 1*s* core level spectroscopy was shorter, compared to that between the buffer layer and the outmost layer, graphene layer (3.5 Å) [34,35]. The shortened distance arises from the covalent bonding between the SiC surface and the buffer layer, while there is no covalent bonding between graphene and the buffer layer, and between graphene layers [32,35]. On the other hand, the shortening of the distance between the nearest layer and the C-face hybrid SiC surface was not observed. This is explained by the absence of the buffer layer, which was elucidated by the C 1*s* core level spectroscopy (Figure 2a).

The film-quality of FLG was semiquantitatively investigated by using resonant Raman spectroscopy through real states of the valence and the conduction bands of FLG [36], as shown in Figure 2c. Only in the spectrum of graphene grown on the 3C-SiC thin film grown on the Si substrate, there appeared the D band that indicates the presence of defects in graphene. On the other hand, graphene grown on both the hybrid SiC and the SiC bulk crystal did not exhibit the D band. This result is indicative of the high quality of the FLG grown on the hybrid SiC. Semiquantitatively, the film-quality of the FLG was estimated in terms of the average grain size (L_a) using the following empirical equation, which is based on the ratio of the intensities of the G (I_G) and D bands (I_D) [37]:

$$L_a = \frac{560}{E_i^4}\left(\frac{I_G}{I_D}\right) \tag{2}$$

where E_i is the energy of the incident photons (2.41 eV). Then, L_a was assumed to be ~1 μm for the FLG grown on the hybrid SiC. This value is two orders of magnitude larger than that for the FLG grown on 3C-SiC thin films grown on Si substrates (20 nm) and comparable to that of the FLG grown on SiC [38]. The LEEM observation of FLG (Figure 2d) definitely agreed with the evaluation by using Raman spectroscopy. The layer number was digitally determined from the number of the dip in the electron reflectivity spectra which were obtained from the LEEM observation [16,29]. Then, it was found that the domain size of FLG on the hybrid SiC was several hundreds of nanometers to several micrometers. The observed grain size is comparable to that of FLG on SiC bulk crystals [14,16,29,39]. Thus, we successfully grew high film-quality FLG on the hybrid SiC.

The growth mechanism is discussed here. The different growth mechanisms of FLG on the Si-face and C-face hybrid SiC reflects the layer number and stacking manner of FLG. The layer number of FLG on the C-face SiC was larger than that on the Si-face hybrid SiC, as shown by the X-TEM images, the photoelectron spectra, and the LEEM images. The stacking manner was probed by acquiring μ-LEED, as shown in the insets of Figure 2d. The μ-LEED of FLG on the Si-face hybrid SiC exhibited a set of hexagonal spots, while that on the C-face SiC exhibited satellite spots in addition to the intense twinned hexagonal spots. The results indicated that FLG was Bernal-stacked on the Si-face hybrid SiC, while that on the C-face hybrid SiC contained rotational stacking faults [25,40]. This difference is explained by the presence/absence of the buffer layer between FLG and the hybrid SiC. The structure of the buffer layer is similar to that of graphene, but is partially bonded to the surface of the Si-face SiC. The buffer layer works as a precursor of graphene on the Si-face hybrid SiC, as in the similar manner of FLG on the Si-face SiC bulk crystal [14,32,40]. Hence, more energy is needed to grow FLG on the Si-face hybrid SiC owing to the buffer layer, compared to that on the C-face SiC. Therefore, the layer number of FLG on the Si-face hybrid SiC was decreased, compared to that on the C-face hybrid SiC. Simultaneously, the buffer layer works as a good template for Bernal stacking of FLG on the hybrid SiC because of the covalent bonding between buffer layer and the Si-face hybrid SiC. Thus, the rotational stacking faults are suppressed for FLG on the Si-face hybrid SiC. The buffer layer is the key factor in the FLG growth on the hybrid SiC.

3.3. Electronic Structure of FLG on the Hybrid SiC

The high-quality FLG grown on the hybrid SiC promises the linear band dispersion [41]. To confirm whether this was indeed the case, we recorded the ARPES spectra of the FLG sample on the Si-face and C-face hybrid SiC, as shown in Figure 3. On the Si-face hybrid SiC, the bands were energetically split (Figure 3a). As shown in LEEM image, monolayer and bilayer graphene domains exist on the Si-face hybrid SiC, and bilayer graphene is Bernal-stacked. Bernal stacking produces an interlayer interaction between graphene layers [42]. The interlayer interaction between graphene layers in bilayer graphene splits bands energetically, as observed in previous reports of the Bernal-stacked bilayer graphene on the Si-face SiC bulk crystal [18]. Thus, the band structure of graphene on the Si-face hybrid SiC reflects the presence of monolayer and Bernal-stacked bilayer graphene.
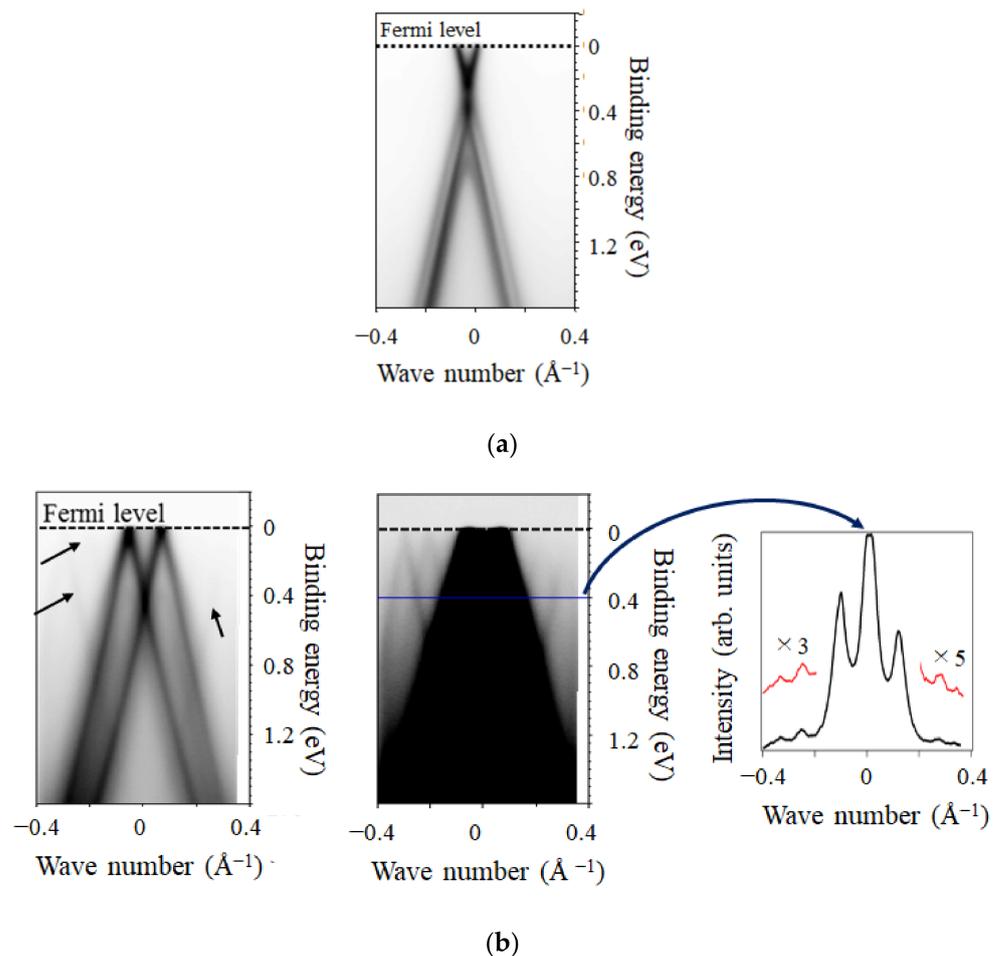

(**a**)

(**b**)

Figure 3. Angle-resolved photoelectron spectra images of few-layer graphene (FLG) on (**a**) the Si-face hybrid SiC and (**b**) the C-face hybrid SiC, respectively. In (**b**), the images with different contrasts and the line profile of the intensity at the binding energy of 0.4 eV for the sake of clarity of the faint bands.

On the other hand, the band structure of graphene on the C-face SiC (Figure 3b) differs from that on the Si-face. In contrast to those on the hybrid Si-face, bands were not energetically split, but multiple bands appeared at different wave vectors. In addition to intense bands, faint bands existed, as indicated by the arrows in the ARPES image (left, in Figure 3b). Although these bands are faint, the presence of the faint bands is confirmed by looking at the image with the different contrast (middle, in Figure 3b) and the intensity line profile (right, in Figure 3b). The observations are explained by the fact that FLG was not Bernal stacked with rotational stacking faults on the C-face hybrid SiC [15,39], as shown in the μ-LEED (Figure 2d). The non-splitting of the bands is explained by the absence of

Bernal stacking, which causes a negligible interlayer interaction.

3.4. Transport Properties of FLG on the Hybrid SiC

The high film-quality and electronic structures promise excellent transport properties. This is corroborated by Hall effect measurements for the FLG films on the hybrid SiC and SiC bulk crystal at room temperatures, as shown in Figure 4. The mobilities of FLG on the SiC bulk crystal were also measured at room temperatures. It was found that the mobility of FLG on the hybrid SiC was comparable to that on a SiC bulk crystal. Furthermore, the carrier mobility increased, as the carrier density decreased. The similar trend is found in a previous report on the carrier mobility of FLG on the SiC bulk crystal [43]. Therefore, it is suggested that the electron transport can be limited mainly by surface polar phonons at room temperatures [43]. Furthermore, the carrier mobility of FLG on the Si-face hybrid SiC was found to be lower, compared to that on the C-face hybrid SiC. The similar trend was found for the carrier mobilities of FLG on the Si-face and C-face SiC bulk crystals [43]. The detailed mechanism for the lowering of the mobility of FLG on the Si-face hybrid SiC remains unclear. However, we guess that the buffer layer is responsible for the lowering of the mobility, as in the case of FLG on the Si-face SiC bulk crystal. One of the possible causes for this degradation is low-energy optical phonons related with the buffer layer [44]. In fact, we discovered the existence of an optical phonon mode associated with the interfacial Si atom possessing Si dangling bond [45], by using scanning inelastic tunneling microscopy, which probes vibrations at an atomic scale. This phonon induces the remote-interfacial phonon scattering and lowers the carrier mobility [46]. Thus, the high film quality of FLG on the hybrid SiC results in high carrier mobilities, comparable to those on the SiC bulk crystal.
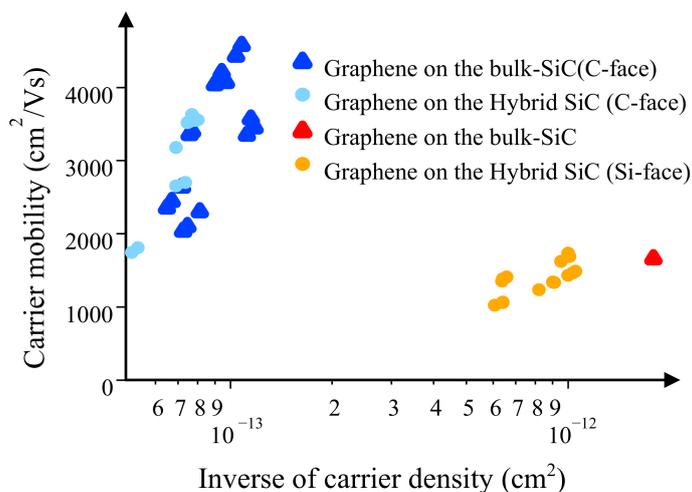

Figure 4. Hall-effect mobility measurements of FLG on the C-face and Si-face hybrid SiC and SiC bulk crystal at room temperatures.

3.5. Device Performances of FET Using FLG on the Hybrid SiC

The observed transport properties comparable to that of graphene on SiC bulk crystal promises excellent device performances. Actually, we succeeded in fabricating a high-performance FET using FLG on the hybrid SiC as a channel. This FET was electrically characterized, as shown in Figure 5. The FET exhibits the excellent DC characteristics of the drain current (I_d)–drain voltage (V_d) (Figure 5a), i.e., the simultaneous realization of a large transconductance (g_m) of 307 mS/mm (maximum value) and quite a small drain conductance of 9.58 μS (minimum value), i.e., drain current saturation, as shown in Figure 5a. Besides, the FET showed an ambipolar behavior arising from the zero bandgap of graphene, as depicted in I_d–gate voltage (V_g) characteristics (Figure 5b). The carrier mobility of this FET was estimated to be 2.2×10^3 cm²/Vs by using the direct transconductance

method (DTM) [47]. The Dirac point where graphene was electrically neutral was around −4.2 V, meaning that graphene was n-doped.
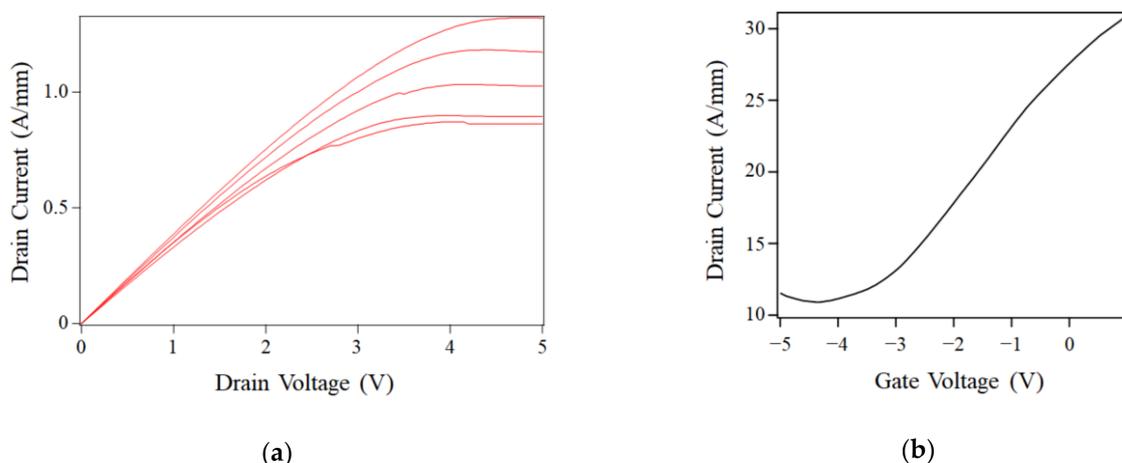

Figure 5. Electrical characteristics of a field-effect transistor using graphene grown on the hybrid SiC, (**a**) drain current–drain voltage with the gate voltages of 0 to 2 V (0.5 V step) and (**b**) drain current-gate voltage with the drain voltage of 10 mV.

The simultaneous realization of the large transconductance and the small drain conductance is significant in applications of FETs using graphene as channels (GFETs) [48]. A lot of previous studies reported that GFETs did not exhibit the drain current saturation because of the zero bandgap of graphene. Nanoribbonization was done to open the bandgap [49], but resulted in the degradations of the carrier mobility and the transconductance [49]. The drain current saturation of GFET without nanoribbonization was reported by few reports [50–52]. According to the previous reports [50,53], the drain current saturation of GFET can be obtained by the interplay of velocity saturation and density-of-states modulation. The interplay works well in case trap densities in the oxide and at the interface between graphene and oxide are mitigated [50]. This indicates the mitigating density of the trapped charges in our work. The high-k dielectrics including yttrium oxide can decrease the influence of the trapped charge [50]. Thus, we achieved the drain current saturation without nanoribbonization by adopting the high-k dielectric yttrium oxide ultrathin film as the gate dielectrics for our GFET, as well as the high quality of graphene on the hybrid SiC.

The simultaneous achievement of the large g_m and the drain current saturation promises excellent high-frequency characteristics of our GFET. We estimated the upper limit of two typical figures of merit of high-frequency performances of our GFET, cutoff frequency for current gain (f_T) and maximum oscillation frequency for power gain (f_{max}) by using equations [48]:

$$f_T = \frac{g_m}{2\pi} \frac{1}{\left(C_{gs} + C_{gd}\right)(1 + g_{ds}(R_S + R_D)) + C_{gd}g_m(R_S + R_D)} \tag{3}$$

$$f_{max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}(R_i + R_S + R_D) + g_m R_G \frac{C_{gd}}{C_{gs}}}} \tag{4}$$

The value of relative dielectric constant of the yttrium oxide on graphene used in this work is 15 [54]. R_S and R_D are the sum of the contact and access-region resistances in the source and drain side. The sum of R_S and R_D is 81.7 Ω, which was obtained by analyzing the $I_d - V_g$ characteristics [55]. C_{gs} and C_{gd} are capacitances between gate and source or drain, respectively. The values of C_{gs} and C_{gd} are 44.3×10^{-15} F and 11.8×10^{-15} F, respectively. The sum of C_{gs} and C_{gd} is the gate capacitance in total (C_G). R_G is the gate resistance, and is 0.65 Ω. R_i is the resistance of the ohmic channel between the source and

the gate. The values of R_G, R_i, C_{gs}, and C_{gd} in this estimation were obtained by analyzing the S-parameter measurement of the transistor using graphene grown on a SiC(0001) substrate with almost the same device structure, with the equivalent circuit where the function of GFET is expressed by the combination of resistors and capacitors [48]. In the equivalent circuit for FETs, the gate capacitance in total is decomposed into C_{gs} and C_{gd} because FET is in general the three-terminal device where the gate is connected to both the source and the drain through the channel. Then, we could estimate the values of f_T and f_{max} to be 23 GHz·μm and 3.2×10^2 GHz·μm, respectively. These estimated values are comparable to or larger than those previously reported experimental values [56]. Especially, the estimated values of f_{max} is promising because the degradation of f_{max} has been the obstacle toward the high-frequency device application of GFET. Our estimation demonstrates that FETs using graphene grown on the hybrid SiC as the channel can be the high-frequency transistor that operate terahertz frequencies at a conventional gate length of 100 nm with proper device fabrication processes including, such as a minimization of the access resistances [57].

4. Discussion

We established the high-quality growth of FLG on a substrate termed hybrid SiC, which consists of a high-quality SiC thin film uniformly transferred from a SiC single crystal onto a device-type wafer with an affordable cost, compared to the graphene growth method using SiC bulk crystals. The fabrication process of the hybrid SiC is repeatable. It is difficult to precisely estimate the number of the repetition times because it depends on the process conditions. However, assuming that the decreased thickness of the SiC bulk crystal is 1 μm during one fabrication process of the hybrid SiC, the repetition times of the fabrication process of the hybrid SiC is roughly to be more than 100 times, considering that the thickness of as-received SiC bulk crystal is several hundreds of micrometers. Therefore, roughly speaking, the material cost of FLG on the hybrid SiC can be two orders of magnitude smaller than that of the conventional growth of FLG using the SiC bulk crystal.

FLG on the hybrid SiC exhibited high carrier mobility, comparable to that of graphene grown on the SiC bulk crystal. Owing to the simultaneous achievement of the complete drain current saturation and the large transconductance, the GFET demonstrated the potential to operate in terahertz frequencies. Our work is promising for the next-generation wireless communication systems that are the basic infrastructure of the forthcoming smart societies. Furthermore, our work may allow for the monolithic integration of graphene-based devices and existing electronics, such as GaN-based high electron mobility transistors (GaN-HEMTs) which use SiC as substrates, owing to the degree of freedom afforded regarding the choice of wafer.

Author Contributions: Conceptualization, H.F.; hybrid SiC fabrication, S.A., S.K., H.M., M.K. (Makoto Kawai), M.K. (Minoru Kawahara), and Y.K.; graphitization, N.E., K.T., K.S., T.K., R.K., K.F., M.S., and H.F.; XRD measurements, N.E.; LEEM measurement, N.E., K.T., T.O., M.K. (Masato Kotsugi), and H.F.; angle-resolved photoelectron spectroscopy, K.H., H.K., N.E., K.T., and H.F.; FET fabrication and measurement, N.E., K.S., T.K., I.W., and H.F.; writing—original draft preparation, H.F.; writing—review and editing, M.S.; project administration, H.F.; funding acquisition, H.F. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

References

1.　Wallace, P.R. The band theory of graphite. *Phys. Rev.* **1947**, *71*, 622–634. [CrossRef]
2.　Novoselov, K.S.; Geim, A.K.; Morozov, S.V.; Jiang, D.; Zhang, Y.; Dubonos, S.V.; Grigorieva, I.V.; Firsov, A.A. Electric field effect in atomically thin carbon films. *Science* **2004**, *306*, 666–669. [CrossRef]
3.　Berger, C.; Song, Z.; Li, T.; Li, X.; Ogbazghi, A.Y.; Feng, R.; Dai, Z.; Marchenkov, A.N.; Conrad, E.H.; First, P.N.; et al. Ultrathin epitaxial graphene: 2D electron gas properties and a route toward graphite-based nanoelectronics. *J. Phys. Chem. B* **2004**, *108*, 19912–19916. [CrossRef]
4.　Castro Neto, A.H.; Guinea, F.; Peres, N.M.R.; Novoselov, K.S.; Geim, A.K. The electronic properties of graphene. *Rev. Mod. Phys.* **2009**, *81*, 109–162. [CrossRef]
5.　Someya, T.; Fukidome, H.; Ishida, Y.; Yoshida, R.; Iimori, T.; Yukawa, R.; Akikuno, K.; Yamamoto, S.; Yamamoto, S.; Yamamoto, T.; et al. Observing hot carrier distribution in an *n*-type epitaxial graphene on a SiC substrate. *Appl. Phys. Lett.* **2014**, *104*, 161103. [CrossRef]
6.　Ando, T.; Nakanishi, T.; Saito, R. Berry's Phase and Absence of Back Scattering in Carbon Nanotubes. *J. Phys. Soc. Jpn.* **1998**, *67*, 2857–2862. [CrossRef]
7.　Avouris, P. Graphene: Electronic and Photonic Properties and Devices. *Nano Lett.* **2010**, *10*, 4285–4294. [CrossRef]
8.　Schwierz, F. Graphene transistors. *Nat. Nanotechnol.* **2010**, *5*, 487–496. [CrossRef]
9.　Novoselov, K.S.; Fal'ko, V.I.; Colombo, L.; Gellert, P.R.; Schwab, M.G.; Kim, K. A roadmap for graphene. *Nature* **2012**, *490*, 192–200. [CrossRef]
10.　Bonaccorso, F.; Sun, Z.; Hasan, T.; Ferrari, A.C. Graphene photonics and optoelectronics. *Nat. Photon.* **2010**, *4*, 611–622. [CrossRef]
11.　Boubanga-Tombet, S.; Chan, S.; Watanabe, T.; Satou, A.; Ryzhii, V.; Otsuji, T. Ultrafast carrier dynamics and terahertz emission in optically pumped graphene at room temperature. *Phys. Rev. B* **2012**, *85*, 035443. [CrossRef]
12.　Tonouchi, M. Cutting-edge terahertz technology. *Nat. Photon.* **2010**, *1*, 97–105. [CrossRef]
13.　Sutter, P.; Sutter, E. Microscopy of Graphene Growth, Processing, and Properties. *Adv. Funct. Mater.* **2013**, *23*, 2617–2634. [CrossRef]
14.　Emtsev, K.V.; Bostwick, A.; Horn, K.; Jobst, J.; Kellogg, G.L.; Ley, L.; McChesney, J.L.; Ohta, T.; Reshanov, S.A.; Röhrl, J.; et al. Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide. *Nat. Mater.* **2009**, *8*, 203–207. [CrossRef]
15.　Sprinkle, M.; Siegel, D.; Hu, Y.; Hicks, J.; Tejeda, A.; Taleb-Ibrahimi, A.; Le Fèvre, P.; Bertran, F.; Vizzini, S.; Enriquez, H.; et al. First direct observation of a nearly ideal graphene band structure. *Phys. Rev. Lett.* **2009**, *103*, 226803. [CrossRef]
16.　Fukidome, H.; Kawai, Y.; Fromm, F.; Kotsugi, M.; Handa, H.; Ide, T.; Ohkouchi, T.; Miyashita, H.; Enta, Y.; Kinoshita, T.; et al. Precise control of epitaxy of graphene by microfabricating SiC substrate. *Appl. Phys. Lett.* **2012**, *101*, 041605. [CrossRef]
17.　Lauffer, P.; Emtsev, K.V.; Graupner, R.; Seyller, T.; Ley, L.; Reshanov, S.A.; Weber, H.B. Atomic and electronic structure of few-layer graphene on SiC(0001) studied with scanning tunnelling microscopy and spectroscopy. *Phys. Rev. B* **2008**, *77*, 155426. [CrossRef]
18.　Ohta, T.; Bostwick, A.; Seyller, T.; Horn, K.; Rotenberg, E. Controlling the electronic structure of bilayer graphene. *Science* **2006**, *313*, 951–954. [CrossRef]
19.　Michetti, P.; Cheli, M.; Iannaccone, G. Model of tunneling transistors based on graphene on SiC. *Appl. Phys. Lett.* **2012**, *96*, 133508. [CrossRef]
20.　Miyamoto, Y.; Handa, H.; Saito, E.; Konno, A.; Narita, Y.; Suemitsu, M.; Fukidome, H.; Ito, T.; Yasui, K.; Nakazawa, H.; et al. Raman-scattering spectroscopy of epitaxial graphene formed on Si substrate. *e-J. Surf. Sci. Nanotechnol.* **2009**, *7*, 107–109. [CrossRef]
21.　Fukidome, H.; Miyamoto, Y.; Handa, H.; Suemitsu, M. Epitaxial growth processes of graphene on silicon substrates. *Jpn. J. Appl. Phys.* **2010**, *49*, 01AH03. [CrossRef]
22.　Fukidome, H.; Abe, S.; Takahashi, R.; Imaizumi, K.; Inomata, S.; Handa, H.; Saito, E.; Enta, Y.; Yoshigoe, A.; Teraoka, Y. Controls over structural and electronic properties of epitaxial graphene on silicon using surface termination of 3C-SiC(111)/Si. *Appl. Phys. Exp.* **2011**, *4*, 115104. [CrossRef]
23.　Fukidome, H.; Takahashi, R.; Abe, S.; Imaizumi, K.; Handa, H.; Kang, H.-C.; Karasawa, H.; Suemitsu, T.; Otsuji, T.; Enta, Y.; et al. Control of epitaxy of graphene by crystallographic orientation of a Si substrate toward device applications. *J. Mater. Chem.* **2011**, *21*, 17242–17248. [CrossRef]
24.　Fukidome, H.; Kawai, Y.; Handa, H.; Hibino, H.; Miyashita, H.; Kotsugi, M.; Ohkochi, T.; Jung, M.-H.; Suemitsu, T.; Kinoshita, T.; et al. Site-selective epitaxy of graphene on Si wafers. *Proc. IEEE* **2013**, *101*, 1557–1566. [CrossRef]
25.　Fukidome, H.; Ide, T.; Kawai, T.; Shinohara, T.; Nagamura, N.; Horiba, K.; Kotsugi, M.; Ohkochi, T.; Kinoshita, T.; Kumighashira, H.; et al. Microscopically-Tuned Band Structure of Epitaxial Graphene through Interface and Stacking Variations Using Si Substrate Microfabrication. *Sci. Rep.* **2014**, *4*, 5173. [CrossRef]
26.　Kawai, M.; Kubota, Y. *The Method for Producing Nanocarbon Film and Nanocarbon Film*; International patent publication number: WO 2014/061337 A1; International Patent Publication Date: 24.04.2014; ShinEtsu Chemical Co., Ltd.: Tokyo, Japan, 2014.
27.　Fukidome, H.; Kotsugi, M.; Nagashio, K.; Sato, R.; Ohkouchi, T.; Itoh, T.; Toriumi, A.; Suemitsu, M.; Kinoshita, T. Orbital-Specific Tunability of Man-Body Effects in Bilayer Graphene by Gate Bias and Metal Contact. *Sci. Rep.* **2014**, *4*, 3713. [CrossRef]

28. Hasegawa, M.; Tashima, K.; Kotsugi, M.; Ohkochi, T.; Suemitsu, M.; Fukidome, H. Inhomogeneous Longitudinal Distribution of Ni Atoms on Graphene Induced by Layer-Dependent Internal Diffusion. *Appl. Phys. Lett.* **2016**, *109*, 111604. [CrossRef]
29. Hibino, H.; Kageshima, H.; Maeda, F.; Nagase, M.; Kobayashi, Y.; Yamaguchi, H. Microscopic thickness determination of thin graphite films formed on SiC from quantized oscillation in reflectivity of low-energy electrons. *Phys. Rev. B* **2008**, *77*, 075413. [CrossRef]
30. Kim, K.-S.; Park, G.-H.; Fukidome, H.; Someya, T.; Iimori, T.; Fumio, K.; Matsuda, I.; Suemitsu, M. A table-top formation of bilayer quasi-free-standing epitaxialgraphene on SiC(0001) by microwave annealing in air. *Carbon* **2018**, *130*, 792–798. [CrossRef]
31. Handa, H.; Takahashi, R.; Abe, S.; Imaizumi, K.; Saito, E.; Jung, M.-H.; Ito, S.; Fukidome, H.; Suemitsu, M. Transmission Electron Microscopy and Raman-Scattering Spectroscopy Observation on the Interface Structure of Graphene Formed on Si Substrates with Various Orientations. *Jpn. J. Appl. Phys.* **2011**, *50*, 04DH02. [CrossRef]
32. Emstev, K.V.; Speck, F.; Seyller, T.; Ley, L. Interaction, growth, and ordering of epitaxial graphene on SiC{0001} surfaces: A comparative photoelectron spectroscopy study. *Phys. Rev. B* **2008**, *77*, 155303. [CrossRef]
33. Riedl, C.; Coletti, C.; Starke, U. Structural and electronic properties of epitaxial graphene on SiC(0001): A review of growth, characterization, transfer doping and hydrogen intercalation. *J. Phys. D Appl. Phys.* **2010**, *43*, 374009. [CrossRef]
34. Norimatsu, W.; Kusunoki, M. Transitional structures of the interface between graphene and 6H–SiC (0001). *Chem. Phys. Lett.* **2009**, *468*, 52–56. [CrossRef]
35. Norimatsu, W.; Kusunoki, M. Epitaxial graphene on SiC{0001}: Advances and perspectives. *Phys. Chem. Chem. Phys.* **2014**, *16*, 3501–3511. [CrossRef] [PubMed]
36. Cançado, L.G.; Takai, K.; Enoki, T.; Takai, K.; Enoki, T. General equation for the determination of the crystallite size L_a of nanographite by Raman spectroscopy. *Appl. Phys. Lett.* **2006**, *88*, 163106. [CrossRef]
37. Tuinstra, F.; Koenig, J.L. Raman spectrum of graphite. *J. Chem. Phys.* **1970**, *53*, 1126–1130. [CrossRef]
38. Caldwell, J.D.; Anderson, T.J.; Culbertson, J.C.; Jernigan, G.G.; Hobart, K.D.; Kub, F.J.; Tadjer, M.J.; Teesco, J.L.; Hite, J.K.; Mastro, M.A.; et al. Technique for the Dry Transfer of Epitaxial Graphene onto Arbitrary Substrates. *ACS Nano* **2010**, *4*, 1108–1114. [CrossRef]
39. Hibino, H.; Kageshima, H.; Maeda, F.; Nagase, M.; Kobayashi, Y.; Kobayashi, Y.; Yamaguchi, H. Thickness Determination of Graphene Layers Formed on SiC Using Low-Energy Electron Microscopy. *e-J. Surf. Sci. Nanotech.* **2008**, *6*, 107–110. [CrossRef]
40. Hass, J.; de Heer, W.A.; Conrad, E.H. The growth and morphology of epitaxial multilayer graphene. *J. Phys. Condens. Matter.* **2008**, *20*, 323202. [CrossRef]
41. Rotenberg, E.; Bostwick, A.; Ohta, T.; McChesney, J.L.; Seyller, T.; Horn, K. Origin of the energy gap in epitaxial graphene. *Nat. Mater.* **2008**, *7*, 258–259. [CrossRef]
42. McCann, E.; Fal'ko, V.I. Landau-Level Degeneracy and Quantum Hall Effect in a Graphite Bilayer. *Phys. Rev. Lett.* **2006**, *96*, 086805. [CrossRef] [PubMed]
43. Tedesco, J.L.; VanMil, B.L.; Myers-Ward, R.L.; McCrate, J.M.; Kitt, S.A.; Campbell, P.M.; Jernigan, G.G.; Culbertson, J.C.; Eddy, C.R., Jr.; Gaskill, D.K. Hall effect mobility of epitaxial graphene grown on silicon carbide. *Appl. Phys. Lett.* **2009**, *95*, 122102. [CrossRef]
44. Ray, N.; Shallcoress, S.; Hensel, S.; Pankratov, O. Buffer layer limited conductivity in epitaxial graphene on the Si face of SiC. *Phys. Rev. B* **2012**, *86*, 125426. [CrossRef]
45. Minamitani, E.; Arafune, R.; Frederiksen, T.; Suzuki, T.; Shahed, S.M.F.; Kobayashi, T.; Endo, N.; Fukidome, H.; Watanabe, S.; Komeda, T. Atomic-scale characterization, of the interfacial phonon in graphene/SiC. *Phys. Rev. B* **2017**, *96*, 155431. [CrossRef]
46. Fratini, S.; Guinea, F. Substrate-limited electron dynamics in graphene. *Phys. Rev. B* **2008**, *77*, 195415. [CrossRef]
47. Brown, M.A.; Crosser, M.S.; Leyden, M.R.; Qi, Y.; Minot, E.D. Measurement of high carrier mobility in graphene in an aqueous electrolyte environment. *Appl. Phys. Lett.* **2016**, *109*, 093104. [CrossRef]
48. Schwierz, F. Graphene Transistors: Status, Prospects, and Problems. *Proc. IEEE* **2013**, *101*, 1567–1584. [CrossRef]
49. Wang, X.; Ouyang, Y.; Li, X.; Wang, H.; Guo, J.; Dai, H. Room-Temperature All-Semiconducting Sub-10-nm Graphene Nanoribbon Field-Effect Transistors. *Phys. Rev. Lett.* **2008**, *100*, 206803. [CrossRef]
50. Han, S.J.; Reddy, D.; Carpenter, G.D.; Franklin, A.D.; Jenkins, K.A. Current Saturation in Submicrometer Graphene Transistors with Thin Gate Dielectric; Experiment, Simulation, and Theory. *ACS Nano* **2012**, *6*, 5220–5226. [CrossRef]
51. Moon, J.S.; Curtis, D.; Bui, S.; Hu, M.; Gaskill, D.K.; Tedesco, J.L.; Asbeck, P.; Jernigan, G.G.; VanMil, B.L.; Myers-Ward, R.L.; et al. Top-gated Epitaxial Graphene FETs on Si-Face SiC Wafers with a Peak Transconductance of 600 mS/mm. *IEEE Electron Device Lett.* **2010**, *31*, 260–262. [CrossRef]
52. Bai, J.W.; Liao, L.; Zhou, H.; Cheng, R.; Liu, L.; Huang, Y.; Duan, X.F. Top-Gated Chemical Vapor Deposition Grown Graphene Transistors with Current Saturation. *Nano Lett.* **2011**, *11*, 2555–2559. [CrossRef] [PubMed]
53. Meric, I.; Dean, C.R.; Young, A.F.; Balitskaya, N.; Trembly, N.J.; Nuckolls, C.; Kim, P.; Shepard, K.L. Channel Length Scaling in Graphene Field-Effect Transistors Studied with Pulsed Current-Voltage Measurements. *Nano Lett.* **2011**, *11*, 1093–1097. [CrossRef] [PubMed]
54. Wang, Z.; Xu, H.; Zhang, Z.; Wang, S.; Ding, L.; Zeng, Q.; Yang, L.; Pei, T.; Liang, X.; Gao, M.; et al. Growth and Performance of Yttrium Oxide as an Ideal High-κ Gate Dielectric for Carbon-Based Electronics. *Nano Lett.* **2010**, *10*, 2024–2030. [CrossRef] [PubMed]

55. Kim, S.; Nah, J.; Jo, I.; Shahrjerdi, D.; Colombo, L.; Yao, Z.; Tutuc, E.; Banerjee, S.K. Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric. *Appl. Phys. Lett.* **2009**, *94*, 062107. [CrossRef]

56. Yu, C.; He, Z.; Song, B.; Liu, Q.B.; Han, T.T.; Dun, S.B.; Wang, J.J.; Zhou, C.J.; Guo, J.C.; Lv, Y.J.; et al. Improvement of the Frequency Characteristics of Graphene Field-Effect Transistors on SiC substrate. *IEEE. Electron Dev. Lett.* **2017**, *38*, 1339–1342. [CrossRef]

57. Jung, M.-H.; Park, G.-H.; Yoshida, T.; Fukidome, H.; Suemitsu, T.; Otsuji, T.; Suemitsu, M. High-Performance Graphene Field-Effect Transistors with Extremely Small Access Length Using Self-Aligned Source and Drain Technique. *Proc. IEEE* **2013**, *101*, 1603–1608. [CrossRef]