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Reconfigurable neuromorphic functions in antiferroelectric transistors through coupled polarization switching and charge trapping dynamics

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The growing demand for energy- and area-efficient emulation of biological nervous systems has fueled significant interest in neuromorphic computing. A promising strategy to achieve compact and efficient neuromorphic functionalities lies in the integration of volatile and non-volatile memory functions. However, implementing these functions is challenging due to the fundamentally distinct physical mechanisms. Traditional ferroelectric materials, with their stable polarization, are ideal for emulating biological synaptic functions but their non-volatile nature conflicts with the short-term memory necessary for neuron-like behavior. Here, we report the design for antiferroelectric gating in two-dimensional channel transistors, incorporating antiferroelectricity with charge trapping dynamics. By tuning the area ratio of the Metal-(Anti-)Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) gate stacks, we enable selective reconfiguration of intrinsic volatile antiferroelectric switching and non-volatile switching-assisted charge trapping/de-trapping, thereby achieving both short- and long-term plasticity. This allows the integration of complementary functionalities of artificial neurons and synapses within a single device platform. Additionally, we further demonstrate synaptic and neuronal functions for implementing unsupervised learning rules and spiking behavior in spiking neural networks. This approach holds great potential for advancing both foundational materials design and technology for neuromorphic hardware applications.

Inspired by biological neural computing, neuromorphic computing based on non-von Neumann architecture is emerging as a promising solution for the next generation of artificial intelligence. By mimicking the functions and operational principles of the human brain through networks of artificial neurons and synapses, neuromorphic computing holds great potential to overcome the memory wall bottleneck inherent in traditional von Neumann systems[1]. Various memory-based devices have been proposed for the hardware implementation of neuromorphic computing, including resistive random access memory (RRAM)[2,3], spin-torque-based memories,[4] ferroelectric tunnel junctions[5], and ferroelectric field-effect transistors (FeFETs)[6,7]. Among these, FeFETs with their intrinsic non-volatile ferroelectric polarization and nondestructive readout operations, have gained considerable attention for their potential to emulate

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biological functions, offering promising application prospects in neuromorphic computing.

Artificial neural networks (ANNs) and spiking neural networks (SNNs) are two primary categories in neuromorphic computing, with artificial neurons and synapses serving as the fundamental building blocks[8–11]. For artificial synapses, achieving multiple analog states with long-term retention is essential, typically realized through non-volatile memory devices. Unlike the continuous signal processing in ANN neurons, SNNs utilize spike trains for communication between neurons, offering a low-power, event-driven, and biologically realistic paradigm[12]. The leaky-integrate-and-fire (LIF) model is among the most widely used frameworks for artificial neurons[13]. In this model, a neuron's membrane potential accumulates over time, emitting a spike once a threshold is reached, followed by a reset to its initial state. Thus, the implementation of neuron functions depends heavily on the short-term dynamic properties. Given these distinct operating principles, artificial neurons and synapses require memory retention across multiple timescales, making it challenging to integrate both functions into a single device. Developing multifunctional devices with reconfigurable plasticity is undoubtedly advantageous, as it would increase device density, reduce chip costs, and simplify the fabrication process.

Various ferroelectric (FE) devices have been implemented as artificial synapses due to their ability to provide distinct, multiple memory states with long retention times. In contrast, antiferroelectric (AFE) materials, which undergo a characteristic AFE-to-FE phase transition (AFE switching) under an electric field, are emerging as promising candidates for volatile neuron-like devices. This is largely due to their intrinsic back-switching (depolarization) upon removal of the electric field, closely mimicking neuronal functions such as the spontaneous return to the initial state after a stimulus is removed. For instance, antiferroelectric transistors based on fluorite hafnium zirconium oxide ($Hf_xZr_{1-x}O_2$, HZO) have demonstrated potential for analog implementation of electronic neurons[14]. Notably, the HZO system, with its energetic and structural similarity between the orthorhombic polar and the tetragonal nonpolar phases, exhibits phase stability influenced by both intrinsic and extrinsic factors[15]. In addition to the composition, which affects the relative free energy (phase stability) of FE and AFE phases[16], factors like surface energy and local charge screening also contribute to the polymorphism of HZO[17]. However, the impact of these factors on the volatile and non-volatile behavior of devices remains insufficiently explored in previous research. For example, a Zr-rich composition is commonly used for AFE HZO in volatile neuronal applications; however, the influence of compositional-dependent phase stability on device performance has not been thoroughly investigated.

Our study addresses this gap by examining the significance of AFE material stability in enabling diverse functionalities and exploring how these functionalities can be manipulated based on the intrinsic properties of AFE materials. Furthermore, the differing memory retention requirements for synaptic and neural functions present a significant challenge. Specifically, the programmable short-term memory (STM) and long-term memory (LTM) requirements are difficult to simulate using a single material property. The incompatibility between material performance and memory timescales increases the hardware costs, limits the versatility of novel materials and device designs, and restricts their potential for neuromorphic computing applications.

In this work, we demonstrate reconfigurable antiferroelectric transistors (AFeFETs) that offer complementary volatile and non-volatile memory functionalities through the synergic effect of stable polarization switching and charge trapping/de-trapping dynamics. This integration is achieved via a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) architecture with a floating gate, allowing for an adaptive gate stack design. The charge trapping dynamics are strongly coupled with AFE switching, which is tuned by adjusting the area ratio of the MFMIS gate stack. The intrinsic back-switching of AFEs exhibits volatile behavior, while charge de-trapping extends the memory retention time. By optimizing AFE properties and charge trapping dynamics, the device can be selectively programmed for reconfigurable operation as either a volatile neuron or a non-volatile synapse. As a non-volatile synapse, it demonstrates long-term potentiation and depression with a stable retention for over 10^4 s, and robust endurance exceeds 10^8 cycles. As a spiking neuron, it exhibits spatiotemporal integration of input signals and eliminates the need for a reset circuit due to inherent AFE back-switching, offering significant hardware acceleration compared to its FE counterpart. An SNN utilizing these synapses and spiking neurons was implemented for MNIST dataset recognition, achieving an accuracy exceeding 97.8%. Notably, the reconfigurable design enables the seamless integration of both volatile and non-volatile devices on a single platform using the same CMOS-compatible fabrication process, which can be adapted for other device systems. This work not only advances the fundamental understanding of AFE materials but also highlights their potential functionalities to simplify design complexity and device-level integration.

Results and discussion

Antiferroelectric HZO gate stack

The HZO system is known for its compositional-dependent ferroelectricity with excellent scalability and complementary metal-oxide-semiconductor (CMOS) compatibility[18,19]. It is practical to study HZO-based antiferroelectrics (AFEs) by drawing comparisons with their ferroelectric counterparts (FEs). Therefore, alongside AFE compounds with Zr-rich content, a reference FE sample with a representative composition of $Hf_{0.5}Zr_{0.5}O_2$ was selected for comparison in this study. The crystal structures of the FE and AFE samples, along with deposition details, can be found in Supplementary Figs. 1, 2. Figure 1a shows the transient current corresponding to the dynamic switching of typical FEs and AFEs in response to two consecutive pulses. For FEs, after the initial write pulse of 3 MV/cm, a current peak corresponds to polarization switching is observed as the voltage is reversed. In the subsequent pulse in the same direction, only a minor plateau, mainly due to the nonlinear dielectric effect (non-FE switching), is observed. Integration of the current difference over time gives a remnant polarization (P_r) of approximately 20 μC/cm^2. However, in AFEs, the polarization induced by the external voltage switches back as the pulse amplitude decreases to zero, resulting in zero net polarization in the absence of an external pulse. In the following pulse, the forward and back-switching are repeated, corresponding to the intrinsic switching properties of AFEs[20].

The origin of the AFE switching and back-switching is the reversible phase transition from an initial tetragonal phase to a polar orthorhombic phase[21,22]. To capture the characteristic switching dynamics of FEs and AFEs, the evolution of switched polarization as a function of applied pulse width was measured, and the pulse scheme is shown in the inset of Fig. 1b. Based on the switching characteristics of FEs and AFEs, the switched polarization is normalized to (−1,1) and (0,1), respectively[23,24]. The switching characteristics are further modeled by the nucleation-limited-switching (NLS) model, which is detailed in Supplementary Information Note 1. In the NLS model, the distribution of the characteristic switching time of polycrystalline materials is described by a Lorentzian function with τ as the characteristic switching time[25,26]. The distribution function for FE and AFE switching is presented in Fig. 1c, where the extracted time constants for AFE and FE under 3 MV/cm are 170 and 398 ns, respectively, suggesting that AFEs switch faster than their FE counterparts. The difference in time constants is consistent with previous studies[24,27] and can be attributed to the different ground states of the materials. For FEs, switched polarization is determined by dipoles being switched into the opposite direction (with a corresponding charge density $\pm 2P_r$), while for AFEs, dipoles are oriented from an initially random state ($\pm P_r$). The smaller time constant for AFE switching suggests that AFEs are more

promising for high-speed applications[28]. Additionally, Supplementary Fig. 3 presents an analysis of the switching dynamics of AFE HZO across various compositions and thicknesses, showing a slight reduction in characteristic switching time with increasing thickness, which is consistent with previous studies.

In the $Hf_xZr_{1-x}O_2$ system, antiferroelectricity becomes increasingly pronounced with higher Zr content[19]. Although an AFE-like double hysteresis loop can be observed across a broad compositional range, the stability of the AFE phase, specifically its resilience to external electric fields, has seldom been thoroughly investigated, and its impact on device performance remains elusive. For example, in the composition $Hf_{0.25}Zr_{0.75}O_2$, the *P-E* loop in Fig. 1d compares the pristine state with that after 5000 cycles of stress at 3 MV/cm. It is obvious that the *P-E* loop is not completely pinched in the pristine state and further opens up with field cycling. The non-zero P_r in the pristine state suggests a polar component due to the presence of a pre-existing FE phase, likely due to the small energy difference between the FE and AFE phase[22]. Further characterization of AFE/FE phase stability was conducted using the first-order reversal curve (FORC) method. FORC assesses the distribution of the switching field within the framework of the Preisach model, which is an effective method to describe the switching characteristics of FEs and AFEs[29]. In other words, the FORC method describes the distribution of the switching field rather than a single coercive field E_c value, which is typically obtained from *P-E* measurements. Supplementary Fig. 4a shows the pulse train used to obtain the switching density $\rho^-(E_r, E)$ during the measurement, in which the field sweeps between a positive saturated field and a reversal field in descending order. The switching density $\rho^-(E_r, E)$ is a function of the applied field E and of the reversal field E_r, defined as the mixed second derivative of polarization in response to the ascending branches of the field sweeps.

$$\rho^-(E_r, E) = \frac{1}{2}\cdot\frac{\partial^2 P^-_{FORC}(E_r, E)}{\partial E_r \partial E} = \frac{1}{2}\frac{\partial E}{\partial t}\frac{\partial j^-_{FORC}(E_r, E)}{\partial E_r}$$

$$\approx \frac{1}{2\dot{E}}\frac{\partial j^-_{FORC}(E_{r,i}, E) - \partial j^-_{FORC}(E_{r,i-1}, E)}{E_{r,i} - E_{r,i-1}} \quad (1)$$

The FORC plot of the reference FE sample is provided in Supplementary Fig. 4b, where a distinct maximum indicates that defects-induced built-in bias has minimal impact. In contrast, Fig. 1e presents

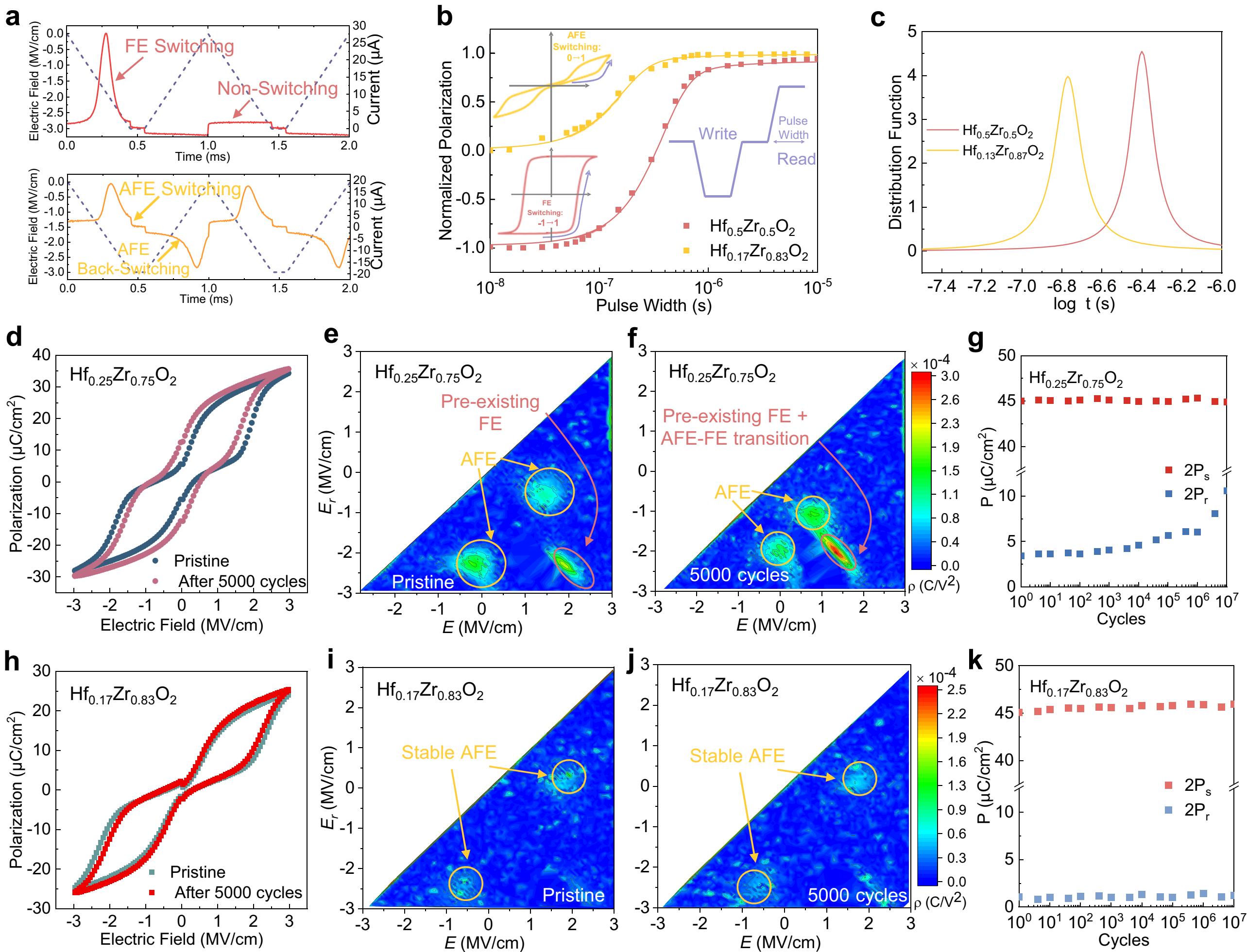

Fig. 1 | Antiferroelectric switching and phase stability. **a** Switching current response of FEs and AFEs to two consecutive pulses. **b** Normalized switched polarization of FE $Hf_{0.5}Zr_{0.5}O_2$ and AFE $Hf_{0.17}Zr_{0.83}O_2$ as a function of pulse width, fitted using the NLS model. Insets show the pulse scheme used for measurement and representative hysteresis loops of FEs and AFEs. **c** Lorentzian fitting of the distribution function showing the characteristic switching time. **d** P-E hysteresis loop of AFE $Hf_{0.25}Zr_{0.75}O_2$, exhibiting a mixed FE/AFE behavior with non-zero remnant polarization. **e** Switching density of pristine $Hf_{0.25}Zr_{0.75}O_2$ extracted from FORC measurement showing three peaks corresponding to AFE switching and the pre-existing FE component. **f** Enhanced switching density of the FE component after 5000 cycles. **g** Evolution of P_r and P_s in $Hf_{0.25}Zr_{0.75}O_2$ under electric field cycling of 2.5 MV/cm, where the increased P_r indicates the degradation of AFE property. **h** P-E hysteresis loop of AFE $Hf_{0.17}Zr_{0.83}O_2$ demonstrating stable AFE back-switching characteristics after 5000 cycles. **i, j** Switching density of $Hf_{0.17}Zr_{0.83}O_2$ before and after cycling, showing stable AFE features. **k** The evolution of Pr and Ps in $Hf_{0.17}Zr_{0.83}O_2$ during endurance measurements indicates stable AFE properties.

the contour plot of the FORC distribution for the pristine AFE $Hf_{0.25}Zr_{0.75}O_2$ film, revealing the presence of three distinct peaks. Two peaks marked by yellow circles correspond to AFE switching behavior, while the additional peak corresponds to the pre-existing FE phase. Additionally, a notable enhancement in ferroelectricity is observed after field cycling, consistent with the opening-up of the hysteresis loop, suggesting an irreversible AFE-FE phase transition. The coexistence of FE and AFE phases is a common phenomenon in both fluorite and perovskite AFEs[30,31]. From a lattice structure perspective, the FE and AFE phases are distorted from the same nonpolar parent phase with high symmetry[32]. Therefore, the AFE phase is close in energy to the competing FE phase, which serves as the basis for the AFE-FE phase transition[33]. This structural and energetic similarity allows for the coexistence of FE and AFE phases at ambient conditions, leading to the noticeable FE characteristics in $Hf_{0.25}Zr_{0.75}O_2$. Furthermore, the bias field for AFE switching and back-switching shows a tendency to converge (Fig. 1f), indicating an evolution towards the FE phase. The presence of this unexpected FE component and the instability of the coercive electric field imply that the back-switching feature of AFE phase degrades with field cycling, leading to reliability issues that are unfavorable for maintaining volatility.

The relative stability of the FE and AFE phases can be altered through compositional manipulation, which allows further stabilization of the AFE phase. As shown in Fig. 1h, for $Hf_{0.17}Zr_{0.83}O_2$, a double hysteresis loop is observed in the pristine state, with no significant opening-up after 5000 cycles, indicating a stabilized AFE phase. This stability is further confirmed by the FORC measurements in Fig. 1i, j, where the peak indicative of AFE switching remains unchanged after cycling. The stabilization of the AFE phase, with its characteristic back-switching, is crucial for achieving reliable volatile behavior in devices.

To further examine the importance of AFE phase stability, endurance measurements were performed on AFE capacitors with different compositions ($Hf_{0.25}Zr_{0.75}O_2$ and $Hf_{0.17}Zr_{0.83}O_2$). The evolution of P_r and saturation polarization P_s is presented in Fig. 1g, k, with corresponding *P-E* hysteresis loops shown in Supplementary Fig. 5. While the $Hf_{0.25}Zr_{0.75}O_2$ film maintained structural integrity without breakdown up to 10^7 cycles, P_r gradually increased during cycling, leading to an opening of the double loops. In contrast, P_r remained stable in $Hf_{0.17}Zr_{0.83}O_2$ throughout cycling, confirming the stability of the AFE phase. Extended endurance measurements for the 15 nm $Hf_{0.17}Zr_{0.83}O_2$ film, as shown in Supplementary Fig. 6, demonstrate sustained performance over 2×10^{12} cycles without breakdown, exceeding the endurance of most reported FE HZO systems. These results emphasize the critical role of AFE phase stability in ensuring reliable volatile functionality, as reliability issues may arise even before device breakdown. The importance of maintaining AFE properties over cycling has been largely overlooked in previous studies. Additional endurance data for $Hf_{0.17}Zr_{0.83}O_2$ film with varying thicknesses is also provided in Supplementary Fig. 6.

Device characteristics and mechanisms of the reconfigurable AFeFET

The AFE composition $Hf_{0.17}Zr_{0.83}O_2$ with stabilized AFE phase is adopted in the fabrication of transistors, with MoS_2 serving as the channel material. The device configuration featuring the MFMIS gate stack is schematically shown in Fig. 2a. An additional floating gate is incorporated into the MFMIS structure, acting as a voltage divider to enable the effective voltage distribution between the Al_2O_3 insulator and the AFE layer. The MFMIS configuration decouples the bottom MFM capacitors from the top MIS layers, allowing independent design by tuning the area ratio A_{MIS}/A_{AFE}. In the devices used in this work, the effective area of the semiconductor channel is modulated while keeping the MFM stack area constant to achieve capacitance matching between the AFE layer and the gate insulator. By scaling down the MFM capacitor area relative to the MIS area, charge compensation between the MFM and MIS can be optimized, thereby providing sufficient electric field for AFE switching while lowering the overall operation voltage[34]. An additional benefit of the MFMIS structure is that the optimized voltage distribution reduces the voltage applied across the insulator layer. This reduction suppresses electron injection from the channel and mitigates interface degradation caused by polarization switching, a common issue in MFIS FeFETs. Detailed discussions of the operating principles of the MFMIS gate stack are provided in the following discussions.

Figure 2b shows the cross-sectional TEM image of the device, highlighting a sharp interface that confirms its high quality. The EDS elemental mapping, presented in Supplementary Fig. 7, demonstrates the homogenous distribution of elements within the device. Figure 2c displays a high-resolution transmission electron microscopy (HRTEM) image of the HZO lattice. The corresponding fast Fourier transformation (FFT) patterns, shown in Fig. 2d, are clearly indexed to the tetragonal phase. Figure 2e presents an atomically stacked image, rebuilt by the inverse FFT of the (101) spot depicted in Fig. 2d. The measured d-spacing of 2.95 Å is consistent with the tetragonal lattice plane. The stable tetragonal antiferroelectric phase is significant for achieving the volatile behavior of the device.

Gate bias with varying sweep rates is used to investigate the device dynamics across a wide timescale. As shown in the pulse I_d-V_g characteristics in Fig. 2f, anticlockwise loops are observed for all sweep rates, indicating AFE switching. Notably, as the sweep pulse width increases or the stress time lengthens, an enlarged memory window (MW) is observed. Statistical analysis of ten devices, shown in Fig. 2g, reveals that when the pulse width is within 1 ms, the MW remains around 0.5 V. With the increasing pulse width, a pronounced enlargement of the MW is evident. The stable MW under short pulse widths is attributed to the intrinsic AFE switching with a characteristic time constant around 170 ns (Fig. 1c). In contrast, the dependence of MW on stress time for pulse width larger than 1 ms suggests a charge trapping-dominated mechanism, which typically exhibits nonlinear dynamics relative to pulse width and amplitude[35–38]. Pulse *I-V* measurements are employed to distinguish the characteristic timescales associated with polarization switching and charge trapping/de-trapping mechanisms. A detailed discussion on the discrepancies between pulse *I-V* and DC *I-V* characteristics is provided in Supplementary Information Note 2. The coexistence of AFE switching and charge trapping enriches the dynamics of devices, enabling adaptive modulation of short-term and long-term memory (STM/LTM). Additionally, DC I_d-V_g curves of the device, provided in Supplementary Fig. 9, show a stable ON/OFF ratio over 10^7 and subthreshold voltage over more than 100 consecutive cycles.

Figure 2h illustrates the current evolution, namely, excitatory postsynaptic currents (EPSC) triggered by different pulse schemes. With a pulse width of 2 ms, the drain current returns to the initial level in the absence of gate voltage. In contrast, with a larger pulse width of 50 ms, the current drops and stabilizes at certain level without significant decay, indicating selectively programmable memory states.

Figure 3a presents the EPSCs triggered by gate voltage with pulse widths ranging from 100 µs to 60 ms, illustrating the transition from STM to LTM. A similar transition can be induced by varying the pulse amplitudes, as depicted in Fig. 3b. The dynamic transition from STM to LTM is driven by the synergistic interplay between AFE switching and electron trapping/de-trapping, which underpin the STM and LTM states, respectively. Charge trapping is commonly observed in ferroelectric transistors where polarization switching is involved in operation[39,40], and its dynamics are strongly coupled with FE/AFE switching[41,42]. This correlation is clearly shown in Fig. 3c, where the critical voltage for the STM-to-LTM transition evolves as a function of the device area ratio. The critical voltage is defined by the change in current in response to the applied electric pulse, as shown in the inset of Fig. 3c. A notable correlation is observed: as the area ratio increases,

the critical voltage decreases, indicating that the device with a larger area ratio requires lower pulse amplitudes to induce LTM. Moreover, as the area ratio continues to increase, the extrapolated critical voltage gradually converges with the coercive voltage for AFE switching, as illustrated in the bottom-left inset of Fig. 3c. According to the principle of capacitors in series, a larger area ratio results in a greater voltage distribution across the AFE layer. Therefore, the trend observed in Fig. 3c further confirms the interplay between AFE switching with charge trapping dynamics.

HZO-based materials are characterized by high intrinsic defect densities, typically in the range of 10^{12}–10^{14} cm^{-2}, due to inherent oxygen vacancies in the bulk[35,43]. Large polarization involved in FE/AFE switching necessitates a substantial number of trapped charges for charge compensation. These trapped charges mitigate the large polarization, acting as negative feedback during polarization switching, which is a phenomenon commonly referred to as trap-assisted or leakage-assisted polarization switching[44]. In the MFMIS configuration, an increased area ratio A_{MIS}/A_{AFE} alleviates the capacitance mismatch between the FE/AFE layer and the insulator layer, resulting in a higher voltage falling on the FE/AFE layer. Supplementary Information Note 3 and Supplementary Fig. 10 provide a detailed analysis of the voltage distribution, and a simple numerical simulation confirms a similar trend for the V_{AFE}/V_G as a function of the area ratio. This quantitative analysis highlights a strong interplay between AFE switching and charge de-trapping behavior, which serves as the foundation for the reconfigurable STM/LTM functionality.

The working mechanism of the reconfigurable device during electrical operation is further illustrated in Fig. 3d–f. Figure 3e details the fundamental switching and back-switching mechanism of AFEs under external voltages below and above the coercive voltage, which serve as the basis for short-term memory and long-term memory, respectively. At a low gate voltage ($V < V_c$), partial AFE switching occurs, where only a fraction of the antiparallel dipoles are flipped, resulting in a small amount of polarization charges. Therefore, a volatile memory behavior will be observed due to the back-switching (Fig. 3d), corresponding to the STM. When the voltage exceeds the coercive voltage ($V > V_c$), complete AFE switching happens, with all antiparallel dipoles oriented towards the electric field. This results in a large polarization that facilitates charge trapping and de-trapping dynamics. As a result, additional electron de-trapping is triggered to compensate for polarization charges, and long stress time contributes to energy accumulation for progressive trapping/de-trapping.[39] Charge de-trapping contributes to further band bending, exhibiting non-volatile behavior even after the gate voltage is removed, thereby achieving the LTM, as shown in Fig. 3f. Through such a selective modulation of the AFE switching, we can achieve reconfigurable STM and LTM in one single AFeFET.

In addition to the charge trapping commonly observed in MFIS transistors, dynamic charge injection can be observed in the switching of HZO ferroelectrics even without an intentional interfacial layer[39]. Figure 3h schematically illustrates electron de-trapping in conjunction with dipole alignment in AFEs. Grain boundaries of polycrystalline HZO are known to be the preferred positions for defect accumulations such as oxygen vacancies[43]. Therefore, electron de-trapping is believed to occur through the electron transfer via the defects. From a thermodynamic viewpoint, both AFE and FE phases are distorted from the

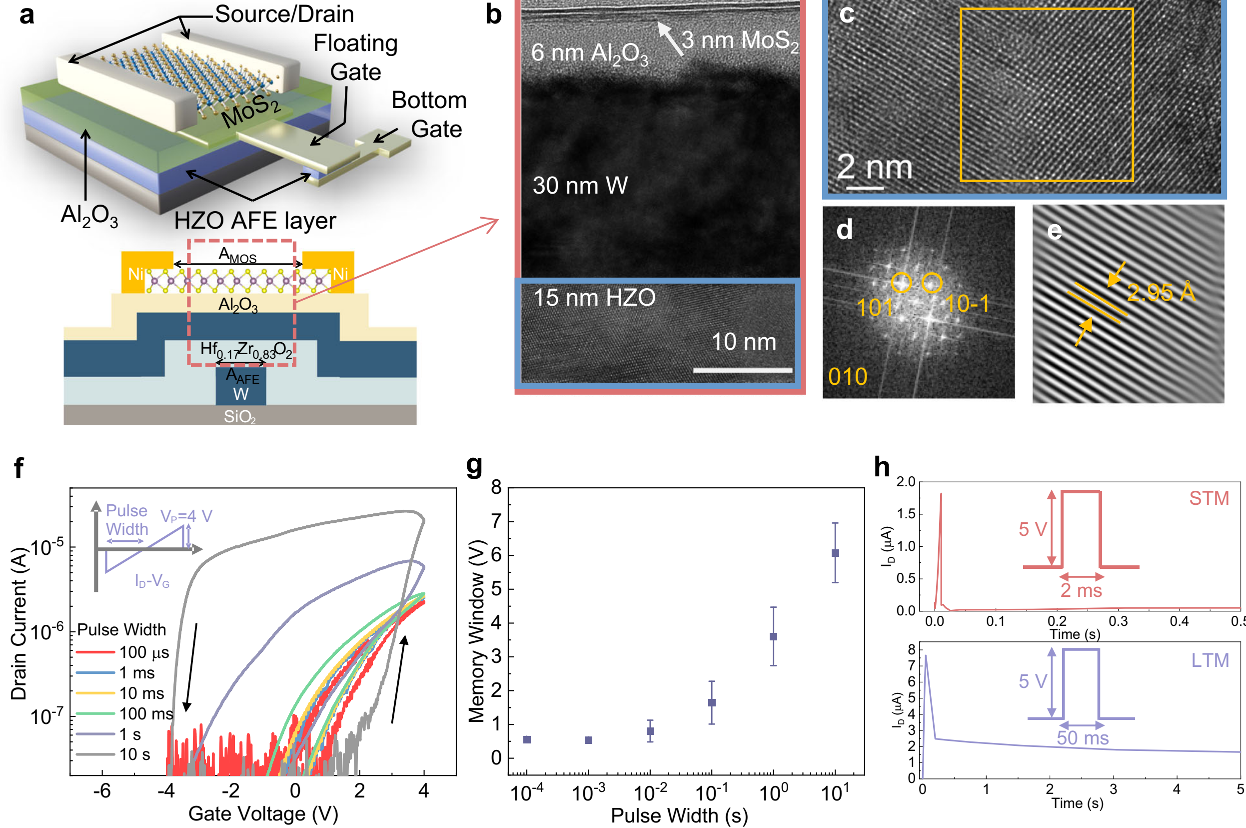

Fig. 2 | Device structure and electrical characterization of the AFeFET. **a** Schematic illustration of the MFMIS-AFeFET showing the tunable area ratio. **b** HRTEM cross-section image of the device. **c** Magnified HRTEM image of the crystalline grain in HZO. **d** The corresponding FFT pattern confirms the tetragonal phase. **e** Inverse Fast Fourier Transformation image with selected spots from (**d**), showing the d-spacing of the tetragonal (101) plane is around 2.95 Å. **f** Pulse I_d-V_g curves measured at different sweep rates. **g** Enlarged MW with increasing sweep pulse width. **h** Short-term and long-term memory are triggered by different pulse schemes.

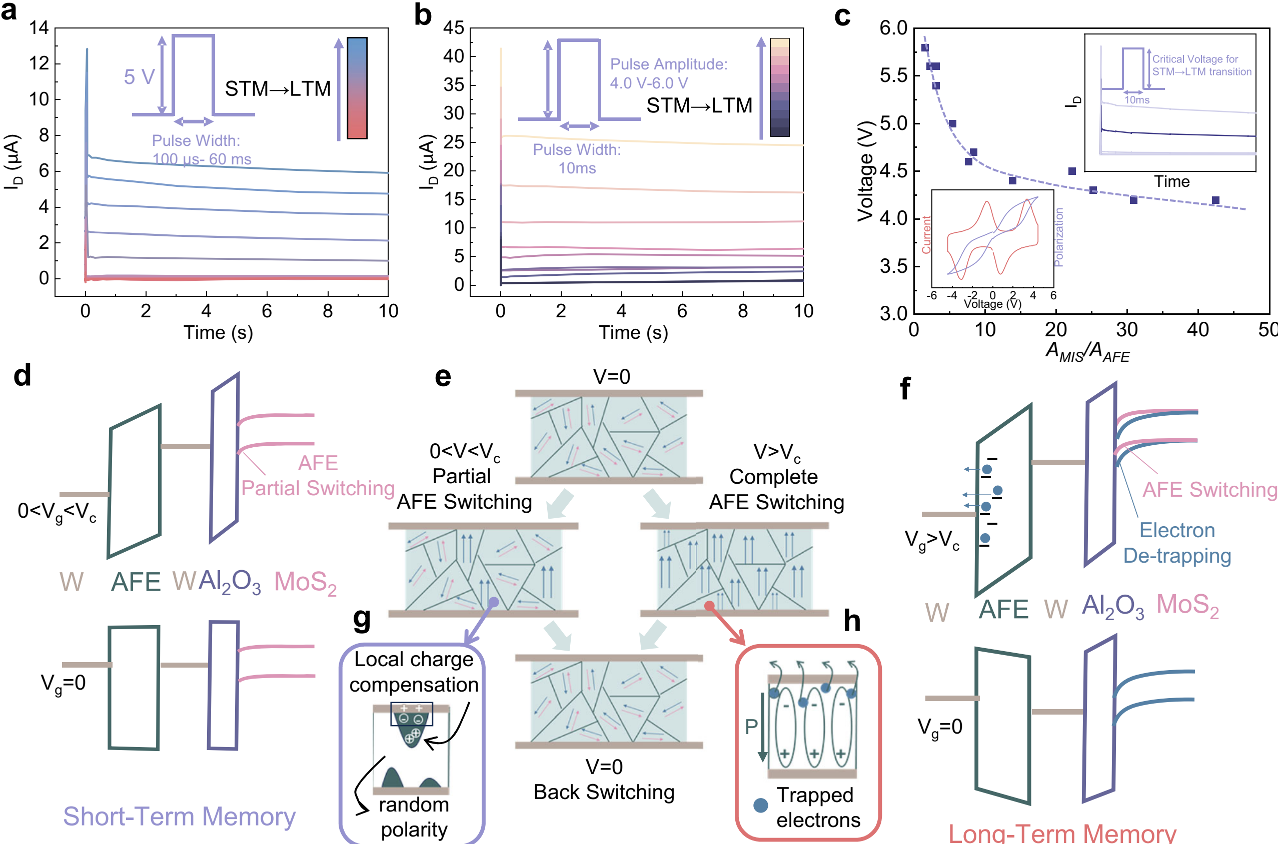

Fig. 3 | Electrical modulation and switching mechanisms in AFeFETs. **a** Channel current modulated by a series of V_g pulses with an amplitude of 5 V and varying pulse widths from 100 µs to 60 ms. **b** Channel current in response to Vg pulses with a fixed pulse width of 10 ms and varying amplitudes from 4.0 to 6.0 V. Both **a**, **b** illustrate the transition of postsynaptic currents from STM to LTM. **c** Critical voltage for STM-to-LTM transition as a function of area ratio A_{MIS}/A_{AFE}. Insets display the determination of the critical voltage and the coercive voltage for AFE switching. **d** Energy band diagram depicting the AFE partial switching mechanism responsible for STM behavior. **e** Schematic illustration of dynamic dipole flipping during AFE switching. **f** Band diagram showing the LTM mechanism attributed to the synergistic effect of AFE switching and switching-assisted charge de-trapping. **g** The transient switching moment during partial AFE switching. **h** Electron de-trapping during complete AFE switching.

same nonpolar phase,[32] suggesting that the interplay between AFE switching and charge trapping/de-trapping should exhibit behavior similar to that in FEs. However, a notable difference is that for partial AFE switching, the charge density at the polar/nonpolar phase boundary is lower compared to the head-to-head or tail-to-tail domain walls in FEs[45], as depicted in Fig. 3g. This leads to more effective compensation of charge trapping during partial AFE switching compared to sub-coercive FEs. Consequently, a stable, volatile behavior is observed with partial AFE switching. The detailed discussion of the charge compensation mechanisms in AFE and FE switching is provided in Supplementary Note 4 and Supplementary Fig. 11.

The reconfigurable STM/LTM functionalities demonstrated in AFeFETs expand the design possibilities for neuromorphic devices beyond a single device or 2D material system. While reconfigurability has been demonstrated in two-terminal devices, their integration typically requires additional circuitry and often involves high electroforming voltages and unreliable set/reset operations, which impose constraints on neuromorphic functionality. In contrast, AFeFETs achieve reconfigurability through the interplay between AFE switching and charge trapping dynamics, which can be quantitatively modeled, indicating the potential for adaption to other device platforms. In addition, using the identical material compositions for both volatile and non-volatile devices eliminates the need for multiple deposition processes, facilitating seamless large-scale integration.

Demonstration of synaptic and neuronal functions

Changes in synaptic weight, or synaptic plasticity, exhibit both potentiation and depression behaviors. In particular, long-term potentiation/depression (LTP/LTD) form the basis of lasting memory. In the AFeFETs, the applied pulse sequence continuously excites charge de-trapping, leading to fine modulation of the LTP and LTD. Figure 4a presents the modulation of conductance states in response to 256 identical pulses of 5 V/1 ms. The device demonstrates a low cycle-to-cycle variation of 2.1% (defined as σ/µ, where σ and µ represent the standard deviation and mean, respectively) over 100 cycles. Further modulation using non-identical pulses (pulse width of 10 µs with pulse amplitudes ranging from 2.0 to 6.8 V for LTP and from −1.0 to −6.5 V for LTD) results in more linear weight update characteristics with a maximum device-to-device variation of 6.1%, as shown in Fig. 4b. Supplementary Fig. 12 confirms that LTP and LTD behaviors can be stably extended to 200 cycles (totaling 5×10^4 pulses), demonstrating the endurance property of the device.

For effective implementation of LTP and LTD in synaptic devices, the modulation of synaptic weights should be non-volatile. Figure 4c illustrates the retention characteristics of the AFeFET, showing that reliable electron de-trapping allows the separate programmed states to be maintained with negligible decay over 10^4 s. The cycling endurance is depicted in Fig. 4d, where the device exhibits reproducible switching without significant degradation over 10^5 cycles under pulse trains. Extended endurance measurements (Supplementary Fig. 13)

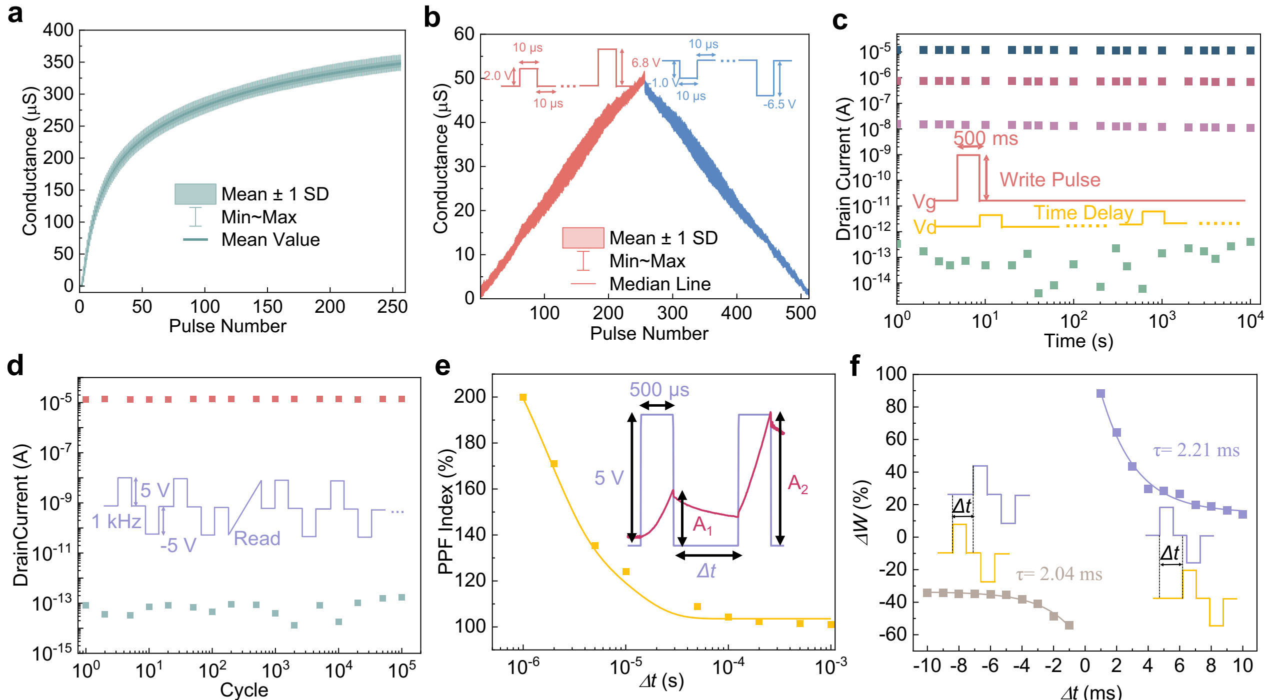

Fig. 4 | Synaptic behavior of AFeFETs. a Modulation of conductance states under identical pulse trains of 5 V showing cycle-to-cycle variations. **b** LTP and LTD responses to non-identical pulse trains, with device-to-device variations across ten devices. **c** Retention stability of the device with separate programmed states switched by different electrical pulses. **d** Cycling endurance of the device measured under program/erase voltages are ±5 V/1 kHz. **e** The PPF ratio as a function of pulse interval. The inset shows the pulse waveforms used for measurement. **f** The STDP learning rule implemented with the device using program/erase voltages are ±5 V/1 ms.

further confirm that the non-volatile characteristics are sustained beyond 10^8 cycles. Paired pulse facilitation (PPF) is another key aspect of synaptic plasticity essential for decoding temporal information in biological systems. It involves the enhancement of the synaptic response to a second stimulus following an initial stimulus. The PPF index, defined as the ratio of the current under two consecutive pulses, is depicted in Fig. 4e. This index can be fitted by a double-exponential function:

$$\text{PPF index} = A_2/A_1 \times 100\% = 1 + C_1 \exp(-\Delta t/\tau_1) + C_2(-\Delta t/\tau_2) \quad (2)$$

where Δt is the time interval, τ_1 and τ_2 denote the two-stage decay time constants, and C_1 and C_2 denote the facilitation magnitudes of the two phases. The fitted time constants are 1.58 and 10 μs, respectively.

Spike-time-dependent-plasticity (STDP) is a fundamental rule for learning and memory in the biological brain, providing dynamic control over synaptic plasticity[46]. For STDP, the update of synaptic weights between a presynaptic and a postsynaptic neuron depends on the delay time between their respective spikes, facilitating the realization of unsupervised learning via synaptic weight modulation[47]. Taking the interval between the presynaptic pulse and the postsynaptic pulse as Δt, the change in synaptic weight (Δw) is determined by the variation in conductance, which can be described using the exponential decay function[48,49]. The variation of the synaptic weight with respect to the time interval Δt is shown in Fig. 4f, where the fitted time constants are 2.21 and 2.04 ms, respectively. Leveraging the STDP characteristics, we demonstrate the pattern recognition capabilities of the AFeFET using a simplified Hopfield neural network[50]. The network is trained using the STDP learning rule to recognize noisy versions of the binary representations of letters “N”, “U”, and “S”. The training algorithm and pattern recognition results are shown in Supplementary Fig. 14, which confirms the effectiveness of the STDP properties of the device in pattern recognition tasks.

Although charge trapping dynamics generally exhibit a larger time constant compared to AFE switching, the energy consumption associated with the non-volatile characteristics of AFeFETs can be significantly reduced by optimizing the applied pulse scheme and device area ratio. As shown in Supplementary Fig. 15, non-volatile behavior can be induced with pulse widths as short as 1 μs in devices with a large area ratio. The resulting energy consumption of ~0.15 pJ per spike demonstrates competitive energy efficiency for a charge trapping-based mechanism (Supplementary Table 3). Notably, the energy consumption for LTM in AFeFETs is substantially lower than that of other reported reconfigurable devices, which typically require prolonged pulse stress to induce non-volatile characteristics.

Neurons in a biological nervous system integrate the action potential from presynaptic neurons, weighted by synapses, and generate a spike when the membrane potential reaches a critical threshold. Unlike synapse-like devices, the development of neuron-like devices has been relatively limited, partly due to the scarcity of materials capable of replicating the characteristic behavior of biological neurons. The dynamic response of AFeFETs is well-suited for emulating spiking neuron behavior in the leaky-integrate-and-fire (LIF) model, as shown in Fig. 5a. The LIF model provides a practical and intuitive framework for simulating biological neurons, where the membrane potential gradually increases in response to presynaptic inputs. Once the integrated input reaches a threshold, the neuron generates a spike followed by a reset of the membrane potential. AFeFETs with their intrinsic back-switching dynamics, show promise in mimicking neuronal functions. As shown in the upper panel of Fig. 5b, the conductance of the AFeFET accumulates in response to consecutive input voltage pulses and exhibits a self-resetting behavior when the applied pulse is removed, closely resembling the reset-to-zero LIF spiking neuron model[51–53]. The ability of the device to return to its initial state without requiring an additional reset operation allows for compact and low-power device designs. The modulation can be re-

initiated after the first self-reset, suggesting reliable LIF functionality. Comparing the dynamics of FeFETs with AFeFETs for neuronal applications reveals intriguing differences. In FeFETs, non-volatility is present even with sub-coercive voltage pulses due to accumulative switching characteristics. The lack of relaxation dynamics in FE polarization requires additional resetting voltage[54], complicating peripheral circuits and making it less ideal for densely packed chips. In contrast, the self-reset feature of AFeFETs is able to achieve integrated functions in a single unit with less area and energy consumption. Additionally, no firing activity occurs at low input strengths, demonstrating the neuron's ability to filter weaker signals, as shown in the lower panel of Fig. 5b. Owing to the excellent endurance and stable AFE properties, the firing behavior of AFeFETs remains robust up to 10^8 cycles with minimal variation, as shown in Fig. 5c, confirming their reliability as neuronal devices.

In biological systems, neurons integrate input signals from pre-neurons both temporally and spatially and transmit these signals by emitting spikes. The spatial integration of inputs can be represented by stimuli with varying strengths. To emulate the strength-modulated characteristics, AFeFETs are subjected to input pulses with varying amplitudes, pulse widths, and pulse intervals, as shown in Fig. 5d, e, and f, respectively. The corresponding statistical analysis based on measurements from 10 devices shows the number of spikes required for firing in the lower panels. In general, increasing input strength enhances the integration, thereby reducing the number of spikes needed for firing, confirming the device's ability to distinguish variations based on spike rate.[55] The spatiotemporal integration of input signals in AFeFETs demonstrates their potential for mimicking biological functionality[56].

Energy consumption is a critical parameter in assessing the performance of artificial neuronal devices. The energy efficiency of these devices can be improved by adjusting the input pulse scheme. As shown in Supplementary Fig. 16, spiking neuronal functions can be triggered with an input pulse width of 400 ns, corresponding to an energy consumption of 0.1 pJ per spike, highlighting the potential of AFeFETs for energy-efficient neuromorphic applications. In practical scenarios, a trade-off between energy consumption and response speed must be considered for specific application requirements[57]. The operating principle of AFeFETs, governed by the interplay between AFE switching and charge trapping/de-trapping dynamics, enables a

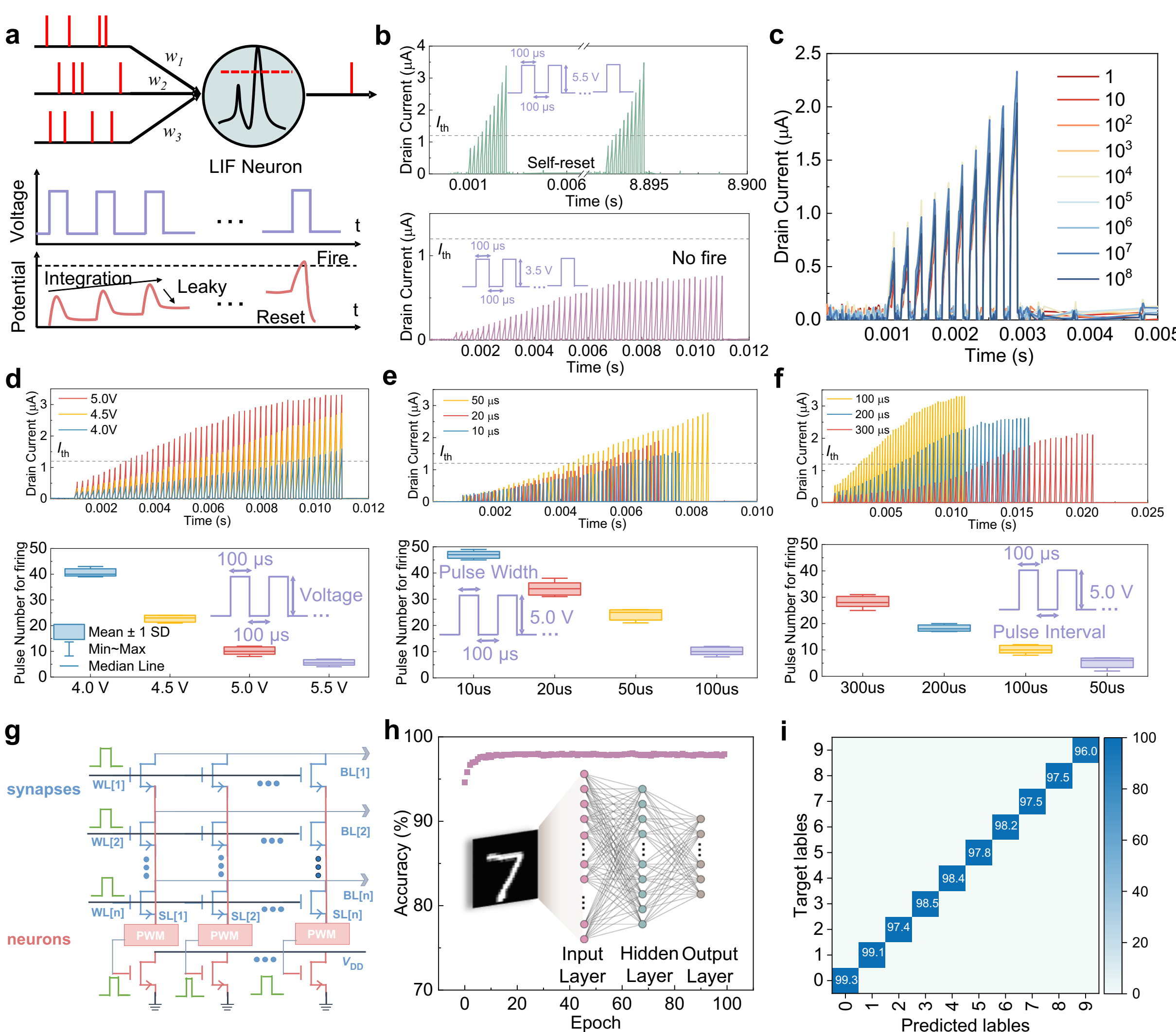

Fig. 5 | Performance of AFeFET-based spiking neurons. a Illustration of the LIF spiking neuron model and the LIF dynamics. **b** Repeated firing events of the AFeFET neuron showing self-reset behavior with no firing triggered by low input strength. **c** Reliable firing performance up to 10^8 cycles, showing minimal cycle-to-cycle variations. **d**–**f** Device responses to pulses with varying amplitudes, pulses widths, and intervals. Corresponding statistical data showing input spike numbers required for firing, with results from ten devices in each box. **g** Schematic of the simulated hardware implementation. **h** Test accuracy of the output results, with the inset showing the configuration of the SNN, including input, hidden, and output layers. **i** Corresponding confusion matrix of the test results.

broad timescale window that supports both volatile and non-volatile characteristics. These intrinsic properties can be further integrated with additional hardware enhancements to accommodate varying firing frequencies for specific applications.

Over the past two decades, neural networks have become prominent in artificial intelligence research, with SNNs offering the potential to enhance the energy efficiency of computing platforms by emulating brain-like features such as spike-based data processing. A schematic representation of the simulated hardware implementation of a network based on AFeFET synapses and neurons is shown in Fig. 5g. The input signal is applied to the drains of FeFETs through bit lines (BLs), while source lines (SLs) collect the resulting current. Pulse width modulators (PWMs) convert the current from the SLs into pulse signals, which are then applied to the gates of neurons for integration and spike generation. Based on the operating principles of AFeFETs, network implementation can be further optimized by utilizing devices with larger area ratios for synaptic functions and smaller area ratios for neuronal functions. This integration allows the network to effectively replicate biological synapses and neurons, enhancing the realism and efficiency of neuromorphic computing.

A three-layer SNN was implemented for the recognition of handwritten digits from the Modified National Institute of Standards and Technology (MNIST) dataset. The linear LTP/LTD characteristics are utilized to modulate synaptic weight updates. LIF spiking neurons populate the layers of the SNN, processing spike trains based on rate coding. As shown in Fig. 5h, the recognition accuracy improves with training iterations, eventually reaching a high accuracy exceeding 97.8%. The corresponding confusion matrix for the final classification results is presented in Fig. 5i. This result indicates that synaptic and neuronal functions can be effectively implemented using our AFeFET, delivering satisfactory performance. Compared to previous studies, our AFeFET offers several advantages, including high endurance, adaptive modulation, diverse functionality, and improved energy efficiency, as summarized in Supplementary Table 4. Furthermore, the multifunctional capabilities of the AFE-based device highlight their significant potential for advancing future neuromorphic computing systems.

In summary, we have demonstrated an antiferroelectric floating-gate transistor capable of reconfigurable short-term and long-term memory functions. This programmability is achieved through the MFMIS configuration with a tunable area ratio, which effectively manipulates the interplay between the intrinsic polarization switching and charge trapping dynamics. The device's non-volatile behavior enables artificial synaptic functions, including long-term potentiation and depression, proving effective for learning and classifying simple binary images. Additionally, the inherent antiferroelectric switching facilitates LIF and self-reset functions under electric field control, offering reduced circuit complexity compared to traditional ferroelectric devices. The neuronal functionality of the AFeFET was demonstrated in spiking neural networks (SNNs) designed to recognize the MNIST dataset, achieving an accuracy exceeding 97.8%. This study underscores the potential of reconfigurable device architectures for multifunctional applications and hardware acceleration in neuromorphic computing.

Methods

Antiferroelectric gate stack preparation

A 30 nm tungsten (W) layer was sputtered and defined on a Si/SiO_2 substrate to form the bottom electrode. Subsequently, a 15 nm hafnium zirconium oxide (HZO) film was deposited using thermal atomic layer deposition (ALD) at 250 °C, employing $Hf[N\text{-}(C_2H_5)CH_3]_4$, $Zr[N\text{-}(C_2H_5)CH_3]_4$, and ozone as precursors. The deposition ratios for $Hf_{0.5}Zr_{0.5}O_2$, $Hf_{0.25}Zr_{0.75}O_2$, and $Hf_{0.17}Zr_{0.83}O_2$ were 1:1, 1:3, and 1:5, respectively. A sacrificial W layer was then sputtered, patterned by lithography, and wet-etched after rapid thermal annealing at 500 °C for 60 s. For the MFMIS gate stack, a 6.5 nm Al_2O_3 layer was deposited by ALD at 150 °C as the insulator. Few-layer MoS_2, used as the channel material, was mechanically exfoliated and transferred onto the substrate. Next, source and drain contacts were defined by electron-beam lithography, followed by the deposition of a 25 nm nickel (Ni) layer and a lift-off process.

Materials characterization

The crystalline phase of the antiferroelectric thin films was characterized by grazing incidence X-ray diffraction (D8 Advance, Bruker). Cross-sectional transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS) mapping were conducted using a Talos F200X TEM.

Device characterization

DC and pulse measurements of capacitors and transistors were conducted using a Keysight B1500A semiconductor analyzer. The measurements of transistors were performed at room temperature in a dark ambient environment.

SNN simulations

The MNIST dataset, consisting of 60,000 training images and 10,000 testing images, was used. Each MNIST sample is a 28 × 28 image containing one of the digits 0–9. A fully connected SNN was implemented with 784 input neurons, 300 hidden layer neurons, and ten output neurons for classification. The LIF model was used to emulate the membrane potential of a time series:[51–53] $U[t+1] = WX[t] + \beta U[t]\text{-}S[t]U_{th}$, where β is the decay rate of membrane potential, W is the weight matrix, $X[t]$ is the input voltage, spike or current, and $S[t]$ is the generated spike train when $U[t] > U_{th}$. The SNN simulations were conducted using the SpikingJelly framework[58].

Data availability

The data supporting the findings of this study are provided in the paper and/or the Supplementary Information. Source data are provided with this paper.

Code availability

The SNN simulations in this work were based on the SpikingJelly framework[58]. All codes are available from the corresponding authors upon request.

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Author contributions

J.G., Y.-C.C. and K.-W.A. conceived the research. K.-W.A. supervised the project. J.G. and Y.-C.C. designed the experiment. J.G. performed the device fabrication, electrical measurements, data analysis, and manuscript writing. Y.-C.C., J.H., L.L., H.Z. and H.X. contributed to the discussion and data analysis. All authors discussed the results and approved the final version of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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