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Lithium ion trapping mechanism of SiO_2 in $LiCoO_2$ based memristors

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Pt/$LiCoO_2$/SiO_2/Si stacks with different SiO_2 thicknesses are fabricated and the influence of SiO_2 on memristive behavior is investigated. It is demonstrated that SiO_2 can serve as Li ion trapping layer benefiting device retention, and the thickness of SiO_2 must be controlled to avoid large SET voltage and state instability. Simulation model based on Nernst potential and diffusion potential is postulated for electromotive force in $LiCoO_2$ based memristors. The simulation results show that SiO_2 trapping layer decreases the total electromotive field of device and thereby prevents Li ions from migrating back to $LiCoO_2$. This model shows a good agreement with experimental data and reveals the Li ion trapping mechanism of SiO_2 in $LiCoO_2$ based memristors.

Boasting high memory density and energy efficiency, memristors are promising alternatives to complementary metal oxide semiconductors (CMOS) for high-density storage and high-performance computing[1–3]. Neural networks based on crossbar arrays of filamentary memristors or phase change memories have been reported and successfully implemented in image recognition and word classification[4–9]. Despite significant progresses, these devices still suffer from several limitations such as excessive "write" noise as well as high switching voltages and currents[10–12]. $LiCoO_2$ based memristors are expected to overcome several limitations. A major advantage of $LiCoO_2$ based memristors is that the intercalation and extraction of Li ions in $LiCoO_2$ are highly reversible leading to high device stability[13,14]. Moreover, Li ions migration in $LiCoO_2$ based memristors is similar to information exchange processes between synapses and neurons in the brain[15]. With a low energy barrier for Li ions transporting, $LiCoO_2$ based memristors have a smaller threshold voltage and are expected to satisfy low-power consumption requirement in high performance computing[16,17].

Generally, $LiCoO_2$ based memristors operate by a common electrochemical reaction between $LiCoO_2$ and Si[18,19]. The conductivity of $LiCoO_2$ changes as a function of Li ions concentration[20,21]. Under a positive electrical field, Li ions migrate from $LiCoO_2$ to Si and the variation of Li ions concentration in $LiCoO_2$ produces a resistive switching (RS) behavior. The RS processes corresponding to Li ions migration out of Li-based oxide have been experimentally verified[22,23]. Furthermore, the electrochemical reaction between $LiCoO_2$ and Si produces an electromotive force (EMF) which in $LiCoO_2$ based memristors can cause electrical short circuit between Li_xCoO_2 and Li_xSi decreasing device retention[24]. It has been reported that SiO_2 between $LiCoO_2$ and Si can work as solid state electrolyte allowing transport of Li ions and trap Li ions when external voltage is removed thus increasing device retention[23,24]. SiO_2 has been also reported to be a promising candidate for the electrolyte or controllable barrier layer in CMOS and Li-ion batteries, which can be used to modulate the Li ions transporting[23–27]. However, the influence of SiO_2 on memristive behavior in $LiCoO_2$ based memristors has not been investigated and the Li ion trapping mechanism of SiO_2 in $LiCoO_2$ based memristors remains to be revealed.

In this work, Pt/$LiCoO_2$/SiO_2/Si stacks with different SiO_2 thicknesses are produced and the corresponding memristive properties such as electrical properties, stabilities and retentions are investigated. SiO_2 serves as a trapping layer for Li ions and is favorable for device retention. It is also necessary to control the SiO_2 thickness to an appropriate range for higher durability and state stability. A simulation model for EMF in $LiCoO_2$ based memristors is proposed to explain the influence of SiO_2 on Pt/$LiCoO_2$/SiO_2/Si stacks. The origins of EMF include Nernst potential and diffusion potential. Thus, this model is based on Nernst potential and diffusion potential and the total electromotive fields of device are calculated. It can be seen that SiO_2 trapping layer can decrease electromotive field of Pt/$LiCoO_2$/SiO_2/Si stacks. This model is consistent with the experimental results and reveals the Li ion trapping mechanism of SiO_2 in $LiCoO_2$ based memristors.

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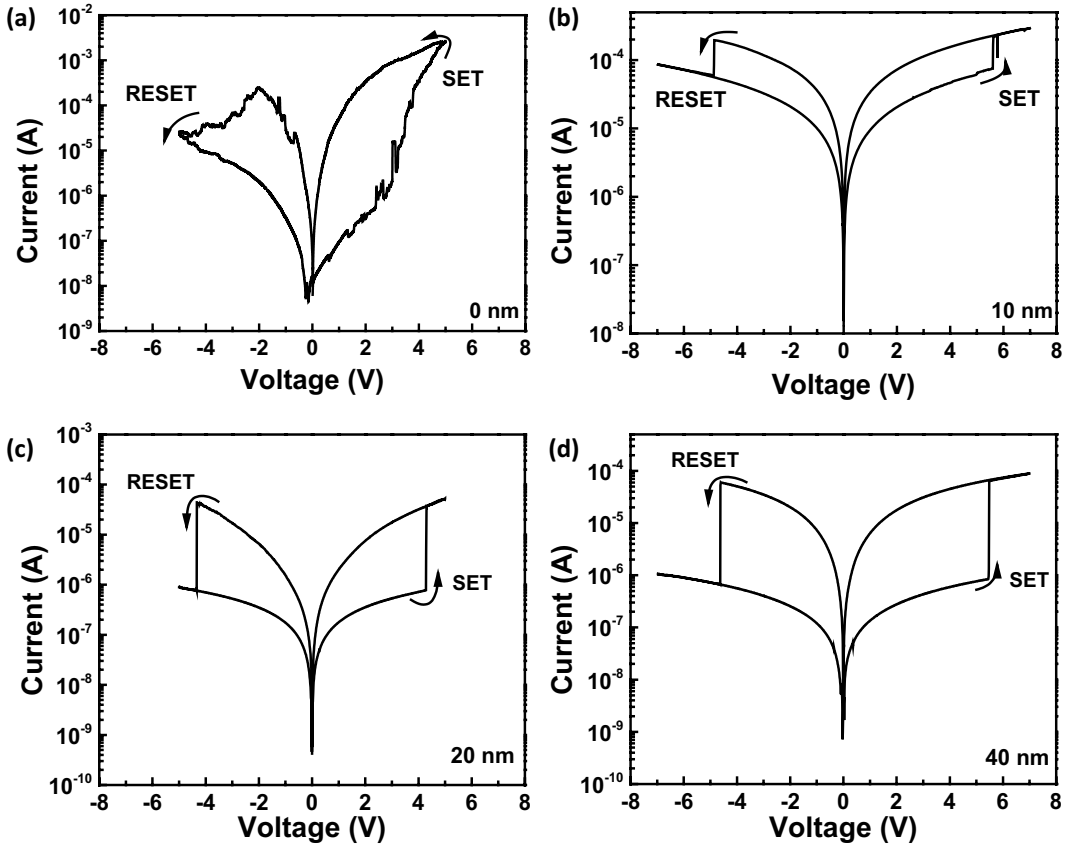

Figure 1. I-V curves of samples with different SiO_2 thicknesses.

Methods

The 40 nm $LiCoO_2$ films were deposited on highly doped p-type Si (111) or SiO_2/Si substrates by pulse laser disposition (PLD) using a stoichiometric $LiCoO_2$ target. $LiCoO_2$ layer was fabricated in O_2 (10 Pa) atmosphere at 550 °C to obtain R-3m $LiCoO_2$ phase through a KrF laser (LightMachinery IPEX-800, $\lambda = 248$ nm and $\tau = 25$ ns) operated at 3 Hz with a fluence of ≈ 1.3 J cm^{-2}. SiO_2 layers were formed by thermal oxidization in an oxygen environment at 900 °C. The thickness of SiO_2 layer was determined by profilometry. The SiO_2 layers had thicknesses of 10 nm, 20 nm and 40 nm (d_{SiO_2}:d_{LiCoO_2} = 1:4, 1:2, 1:1) in order to investigate the influence of the SiO_2 thickness on the memristive behavior of Pt/$LiCoO_2$/SiO_2/Si stacks. The $LiCoO_2$ deposition was carried out under same conditions to obtain same Li ions concentration and layer thickness. To avoid introducing other metal ion such as Ag^+ or Cu^{2+}, noble Pt was used as the top electrodes. The 80 nm thick Pt top electrodes were prepared by magnetron sputtering in pure Ar with a metal mask covering the $LiCoO_2$ layer. The diameter of the top electrode was 1 mm.

The electrical and memristive properties were measured by the voltage sweeping mode on Keithley 4200-SCS semiconductor parameter analyzer at room temperature. The voltages were applied to the Pt top electrode with Si substrate grounded. The cycle tests were collected continually by the direct-current (DC) voltage sweeping mode. The retention tests were conducted after the devices switching to LRS, and the read voltage is 0.1 V. The $LiCoO_2$ layers were analyzed with a LabX XRD-6000 using Cu Kα radiation and operating at 40 kV and 30 mA. The scanning rate was 5°/min.

Results

The Pt/$LiCoO_2$/SiO_2/Si stacks with different SiO_2 thicknesses of 10 nm, 20 nm and 40 nm are fabricated and samples without SiO_2 are also prepared for comparison. The corresponding I-V curves of different samples are shown in Fig. 1. The I-V curve of sample (a) displays gradual RS processes without definite V_{set} and V_{reset}, corresponding to homogeneous RS in $LiCoO_2$[24]. On the contrary, samples (b), (c) and (d) exhibit abrupt current increases similar to RS behavior of electrochemical metallization (ECM)[10], as shown in Fig. 1(b–d) (More I-V curves during cycle tests are shown in supporting information, Fig. S3). Hence, samples with and without SiO_2 characterize different memristive properties which may be attributed to different transport processes of Li ions in SiO_2 and $LiCoO_2$.

In order to investigate the device stabilities, durability tests are conducted on the different samples. As shown in Fig. 2, the V_{SET} and V_{RESET} of samples with 20 nm are more stable. To evaluate the dispersion degree, corresponding coefficients of variation (C_V) are calculated. C_V is defined by[28]

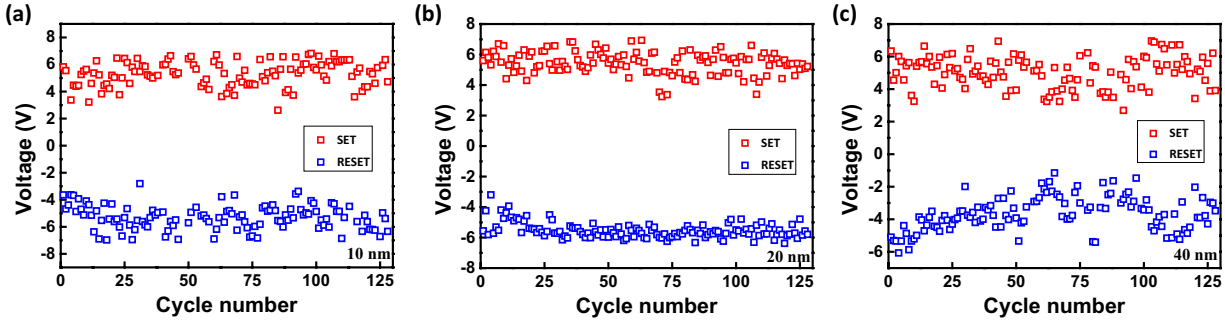

Figure 2. V_{SET} and V_{RESET} of samples with different SiO_2 thicknesses (128 cycles).

Thickness (nm)	V_{SET} (V)	V_{SET} C_V	V_{RESET} (V)	V_{RESET} C_V
0	—	—	—	—
10	2.62~6.82	0.17	−2.81~−6.97	−0.07
20	3.24~6.93	0.14	−3.2~−6.38	−0.08
40	3.42~6.21	0.18	−2.03~−4.28	−0.23

Table 1. The SET voltage, RESET voltage and corresponding coefficients of variation (C_V) of in samples with different SiO_2 thickness.

$$C_V = \frac{\sigma}{\mu} \tag{1}$$

where σ is the standard deviation and μ is the average of several data. The ranges of SET voltage and C_V of different samples are summarized in Table 1 (For each SiO_2 thickness, 15 points of the sample are measured). Samples with 20 nm show smaller C_V than other samples consistent with Fig. 2. To study state stability, the resistances of different samples at HRS and LRS for 128 cycles are also measured. Figure 3 plots the R_{HRS} and R_{LRS} of different samples during 128 cycles. The R_{HRS} of samples (a) and (b) show two orders of magnitude fluctuations while those of samples (c) and (d) are within one order of magnitude. The R_{LRS} of sample (c) shows the smallest fluctuation. The C_V of R_{HRS} and R_{LRS} are also calculated in Table 2 (For each SiO_2 thickness, 15 points of the sample are measured). As the SiO_2 thickness is increased, C_V of R_{HRS} decreases and sample (c) has the smallest C_V of R_{LRS}. However, sample (d) shows several RS failures during the durability test. Hence, samples with 20 nm SiO_2 characterize the best stability. SiO_2 with appropriate thickness is favorable for state stability but SiO_2 that is too thick decreases the state stability.

Retention of $Pt/LiCoO_2/SiO_2/Si$ stacks with different SiO_2 thicknesses is also assessed at a read voltage of 0.1 V to evaluate ability of data storage. Figure 4 shows that $Pt/LiCoO_2/SiO_2/Si$ stacks without SiO_2 maintain retention characteristic of ~10^3 s whereas samples with SiO_2 show good retention characteristics up to 10^5 s. As SiO_2 thickness is increased, device retention increases from 10^4 to 10^5 s. In terms of $Pt/LiCoO_2/SiO_2/Si$ stacks, EMF mainly drives Li ions from Si to $LiCoO_2$ without an external voltage and therefore, SiO_2 can decrease the influence of EMF on $Pt/LiCoO_2/SiO_2/Si$ stacks leading to high retention.

Discussion

To understand the mechanism of trapping of Li ions in SiO_2, it is necessary to investigate the Li ions transporting processes in the $Pt/LiCoO_2/SiO_2/Si$ stacks. The schematic of $Pt/LiCoO_2/SiO_2/Si$ stacks and Li ions transporting processes are shown in Fig. 5(a). The Li ions transporting processes in $LiCoO_2$, SiO_2 and Si have been experimentally verified and reported for Li-ion battery[22,24–26]. The electrochemical reactions involving Li ions in $Pt/LiCoO_2/SiO_2/Si$ stacks are as follows:

$$LiCoO_2 - (1 - x_1)e^- \leftrightarrow Li_{x_1}CoO_2 + (1 - x_1)Li^+ \tag{2}$$

$$SiO_2 + x_2Li^+ + x_2e^- \leftrightarrow Li_{x_2}SiO_2 \tag{3}$$

$$Si + x_3Li^+ + x_3e^- \leftrightarrow Li_{x_3}Si \tag{4}$$

At a positive voltage, Li ions are extracted from $LiCoO_2$ and migrate in the interval positions of SiO_2 finally forming Li_xSi in Si substrate. The $LiCoO_2$ acts as Li ions source and RS layer, SiO_2 allows Li ions transportation, and Si is used to store Li ions. The $LiCoO_2$ layers are annealed at 550 °C to obtain R-3m phase (seen in Fig. S1) which is hexagonal layered structure with a uniform Li ions distribution[19,20]. Owing to the uniform Li ions distribution in crystalline R-3m $LiCoO_2$, the RS processes occur in the entire $LiCoO_2$ layer displaying gradual current changes.

Thickness (nm)	HRS (Ω)	HRS C_V	LRS (Ω)	LRS C_V
0	10^7~10^8	0.59	10^3~10^4	0.97
10	10^6~10^7	0.46	10^3~10^5	1.01
20	10^8	0.44	10^3~10^4	0.80
40	10^7	0.13	10^3~10^6	0.95

Table 2. The HRS, LRS and corresponding coefficients of variation (C_V) of in samples with different SiO_2 thicknesses.

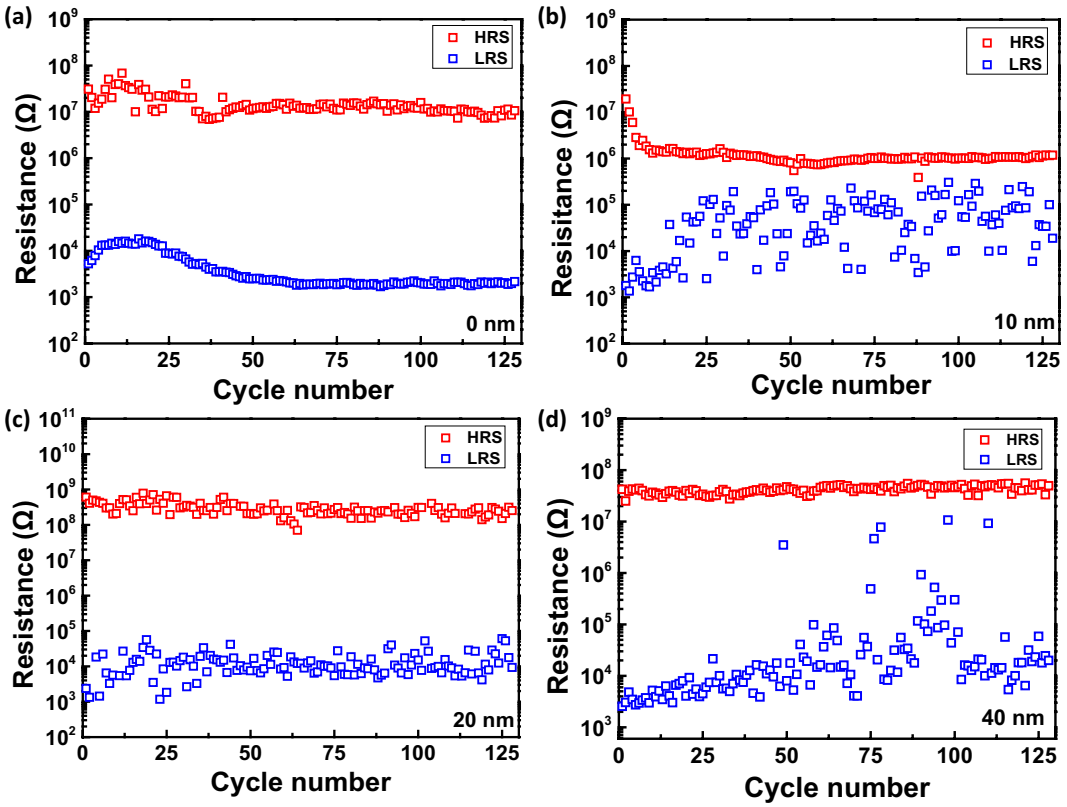

Figure 3. R_{HRS} and R_{LRS} of samples with different SiO_2 thicknesses (128 cycles).

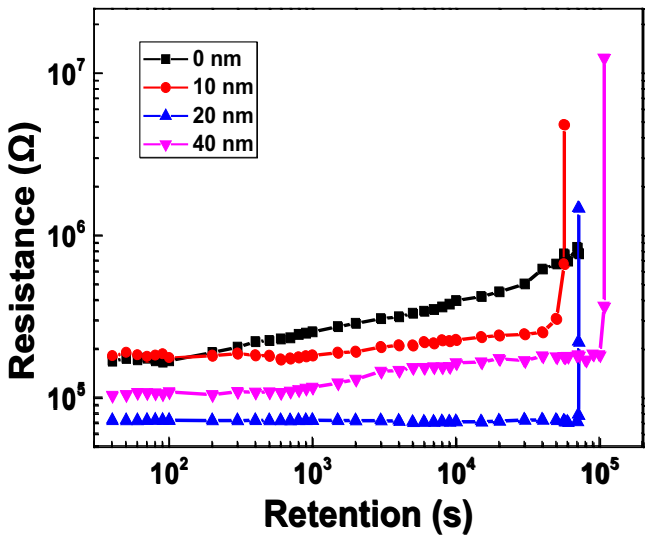

Figure 4. Retention tests of samples with different SiO_2 thicknesses at a read voltage of 0.1 V.

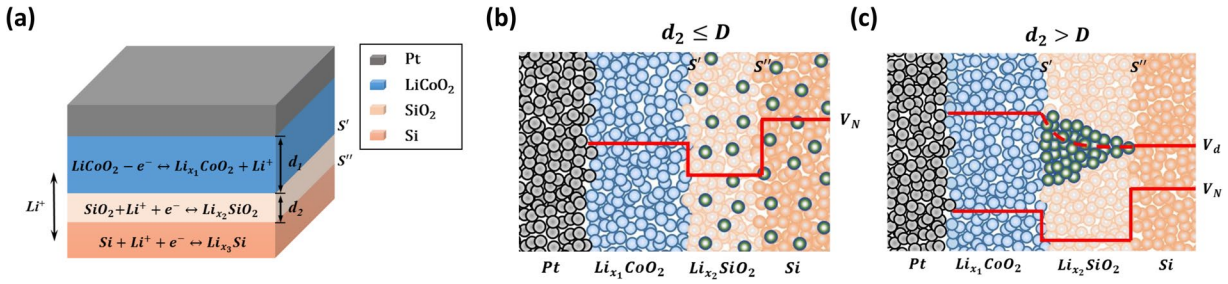

Figure 5. (**a**) Schematic of Pt/$LiCoO_2$/SiO_2/Si stacks and Li ions transportation processes; (**b**) Origins of electromotive force (EMF) in Pt/$LiCoO_2$/SiO_2/Si stacks ($d_2 \leq D$); (**c**) Origins of EMF in Pt/$LiCoO_2$/SiO_2/Si stacks ($D < d_2$)

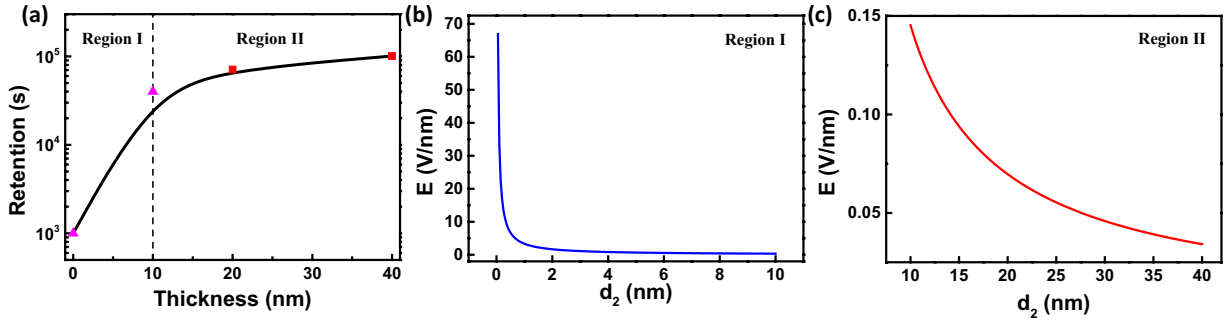

Figure 6. (**a**) Experimental device retention as a function of SiO_2 thickness (2 different regions are observed); (**b**) Simulated E-d_2 characteristics in Pt/$LiCoO_2$/SiO_2/Si stacks without an external voltage ($d_2 \leq 10$ nm); (**c**) Simulated E-d_2 characteristic in Pt/$LiCoO_2$/SiO_2/Si stacks without an external voltage (10 nm $< d_2 \leq$ 40 nm)

In contrast to layered structure $LiCoO_2$, SiO_2 is amorphous with non-uniformity, and the Li ions intercalation processes are inhomogeneous and occur in some partial regions of SiO_2. Therefore, the memristive behavior of samples without SiO_2 shows gradual current changes while samples with SiO_2 exhibit abrupt resistance jumps. Furthermore, it has been reported in Li-ion batteries that insertion of Li ions in Si strongly strains the crystalline lattice thus harming the device stability, the SiO_2 can work as a buffer layer to decrease the crystalline lattice stress[22,29] and trap Li ions decreasing resistance degradation without an external voltage[23,24]. However, thin SiO_2 layer ($\leq$10 nm) is generally rough exhibiting non-uniformity[27], which may be adverse to device stability as shown in Fig. 3(b). And too thick SiO_2, such as 40 nm, exhibit stronger Li ion trap effect which can cause several set failures and reduced performances, as shown in Fig. 3(d). Hence, SiO_2 with the appropriate thickness improves the device stability.

After applying a positive voltage, Li ions transport from $LiCoO_2$ to Si resulting in EMF between $LiCoO_2$/SiO_2 interface (s') and SiO_2/Si interface (s''). Two factors mainly contribute to the EMF: (a) Nernst potential V_N and (b) diffusion potential V_d[30]. SiO_2 works as a Li ion trapping layer allowing Li ions to transport at a positive voltage while trapping Li ions and avoiding resistance degradation without an external voltage. According to the different SiO_2 thickness (d_2), two origins of EMF in Pt/$LiCoO_2$/SiO_2/Si stacks are shown in Fig. 5(b) and (c). When $d_2 \leq$ *Critical poin (D)*, SiO_2 undergoes fully lithiation and exhibits homogeneous Li ions distribution, as shown in Fig. 5(b), and $V_{EMF} = V_N$. When $d_2 > D$, the SiO_2 acts as a RS layer and has an inhomogeneous Li ions distribution as shown in Fig. 5(c), $V_{EMF} = V_N + V_d$. Therefore, the influence of SiO_2 trapping layer on EMF can be divided into two regions. According to the range of x_1 in $Li_{x_1}CoO_2$ and x_2 in $Li_{x_2}SiO_2$, the range of D between region I and region II can be calculated to be 6.96 nm $<$ D $<$ 13.91 nm (Calculation processes are shown in Supplementary Information). Figure 6(a) shows different tendencies in 0~10 nm region and 10~40 nm region. When 0 nm $< d_2 \leq$ 10 nm, the device retention rises rapidly with increasing SiO_2 thickness and when 10 nm $< d_2 \leq$ 40 nm, device retention rises slightly with increasing SiO_2 thickness, indicating that D is near to 10 nm which is consistent with the calculation. This can also explain the abnormal tendency of HRS in Figs. 1 and 3. The HRS of devices mainly consist of $R_{Li_xCoO_2}$ and $R_{Li_ySiO_2}$. For samples without SiO_2, Li ions transport back to $LiCoO_2$ after reset process and $R_{HRS} \approx R_{LiCoO_2}$. For samples with SiO_2, the SiO_2 would trap large amount of Li ions during reset process resulting in decrease of Li ion concentration in $LiCoO_2$ and the retained Li ions in SiO_2 enhance the conductivity. Therefore, the HRS of Pt/$LiCoO_2$/SiO_2 (10 nm)/Si is lower than Pt/$LiCoO_2$/Si. Moreover, 10 nm SiO_2 undergoes full lithiation while 20 nm and 40 nm SiO_2 undergo partly lithiation. Full lithiated SiO_2 would retain higher Li ion concentration and cause lower Li ion concentration in $LiCoO_2$ and higher conductivity. Furthermore, thicker SiO_2 means larger Li ion storage and stronger Li ion trap effect leading to lower Li ion concentration in $LiCoO_2$, which may cause that the HRS of samples with 40 nm SiO_2 is lower than that of samples with 20 nm SiO_2.

The device retention is mainly relative to the electromotive field ($E = V_{EMF}/d_2$), thus the E-d_2 characteristics are discussed. In region I, SiO_2 behaves as solid-state electrolyte exhibiting a homogeneous Li ions distribution and $V_{EMF} = V_N$. EMF drives Li ions migration from Li_xSi to Li_xCoO_2 and the main electrochemical reactions are as follows:

$$Co^{4+} + e^- \leftrightarrow Co^{3+}(Interface\ s') \tag{5}$$

$$Li^+ + e^- \leftrightarrow Li(Interface\ s'') \tag{6}$$

The Nernst potential is given by[30]:

$$V_N = V_{s'} - V_{s''} = V^0 + \frac{kT}{e} ln \frac{a_{Co^{4+}} \cdot a_{Li}}{a_{Co^{3+}} \cdot a_{Li^+}} \tag{7}$$

V^0 is the difference in the standard potentials of these reactions, k is Boltzmann constant, T is temperature, e is electron charge, $a_{M^{z+}}$ denote the activity of the cations ($a = \gamma c$, γ is activity coefficient). The amount of Li ions in $Pt/LiCoO_2/SiO_2/Si$ stacks is constant:

$$c_0 d_1 S = c_1 d_1 S + c_2 d_2 S + c_3 d_3 S \tag{8}$$

where c_0 denotes the initial concentration of Li ions in $LiCoO_2$, c_1, c_2 and c_3 are the concentration of Li ions in Li_xCoO_2, SiO_2 and Si, S is the cell size. d_1, d_2 and d_3 are the thicknesses of $LiCoO_2$, SiO_2 and Si, respectively. The concentration of Li ions can be defined as $c = \frac{\frac{\rho V}{M}}{V} = \frac{\rho}{M}$ (ρ is mass density, V is volume and M is the molar mass). Equation (8) can be written by:

$$\frac{\rho_1}{M_1} d_1 = \frac{\rho_1}{M_1} d_1 x_1 + \frac{\rho_2}{M_2} d_2 x_2 + \frac{\rho_3}{M_3} x_3 d_3 \tag{9}$$

where ρ_1, ρ_2 *and* ρ_3 are mass densities of $LiCoO_2$, SiO_2 and Si, respective. M_1, M_2 *and* M_3 are molar mass of $LiCoO_2$, SiO_2 and Si, respectively. x_1, x_2 and x_3 are the atomic percent in $Li_{x_1}CoO_2$, $Li_{x_2}SiO_2$ and $Li_{x_3}Si$. Due to low concentration of Li ions in $LiCoO_2$ and SiO_2 and small molar mass of lithium, the influences of Li ions on ρ *and* M are neglected. Thus, $c_{Co^{4+}} = \frac{\rho_1}{M_1}(1 - x_1)$, $c_{Co^{3+}} = \frac{\rho_1}{M_1} x_1$, $c_{Li^+} = \frac{\rho_2}{M_2} x_2$, $c_{Li} = \frac{\rho_3}{M_3} x_3$. Based on Equation (9) and γ assumed to be one, the electromotive field in region I ($E_1 = V_{EMF}/d_2$) can be calculated by:

$$E_1 = \frac{V^0}{d_2} + \frac{kT}{ed_2} ln \frac{(1 - x_1)\left[\frac{\rho_1}{M_1} d_1 (1 - x_1) - \frac{\rho_2}{M_2} d_2 x_2\right]}{x_1 d_3 \cdot \frac{\rho_2}{M_2} x_2} \tag{10}$$

To facilitate the discussion of EMF, reference values are chosen according to previous reports, $x_1 = 0.7, \rho_1 = 2.5\ g/cm^3$, $\rho_2 = 2.648\ g/cm^3$, $\rho_3 = 2.329\ g/cm^3$, $M_1 = 97.87\ g/mol$, $M_2 = 60.086\ g/mol$, $M_3 = 28.085\ g/mol$, $V^0 = 3.6\ V$, $x_2 = 2/3$[13,21,31,32]. The thickness of different layers are measured, $d_1 = 40\ nm$, $d_3 = 550\ \mu m$. D is simulated to be 10.43 nm, and the simulated E-d_2 characteristics are shown in Fig. 6(b). E_1 decreases rapidly with d_2, and thereby device retention rises rapidly with increasing SiO_2 thickness.

In region II, SiO_2 acts as a RS layer and $V_{EMF} = V_N + V_d$. The main electrochemical reactions are as follows:

$$Co^{4+} + e^- \leftrightarrow Co^{3+}(Interface\ s') \tag{11}$$

$$Si^{4+} + e^- \rightarrow Si^{3+}\ (Interface\ s'') \tag{12}$$

Nernst potential is given by[30]

$$V_N = V_{s'} - V_{s''} = V^0 + \frac{kT}{e} ln \frac{a_{Co^{4+}} \cdot a_{Si^{3+}}}{a_{Co^{3+}} \cdot a_{Si^{4+}}} \tag{13}$$

Similarly, the amount of Li ions in $Pt/LiCoO_2/SiO_2/Si$ stacks is constant:

$$c_0 d_1 S = c_1 d_1 S + c_2 d_2 S \tag{14}$$

It can be also written as:

$$\frac{\rho_1}{M_1} d_1 (1 - x_1) = \frac{\rho_2}{M_2} d_2 x_2 \tag{15}$$

The Li ions distribution in SiO_2 is inhomogeneous, to simply the Li ions distribution in SiO_2, it is assumed that Li ions in SiO_2 follows constant-total-dopant diffusion and the Li ions distribution in SiO_2 can be defined by[33]:

$$c(y, t) = \frac{Q}{\sqrt{\pi D' t}} \exp\left(-\frac{y^2}{4D' t}\right) \tag{16}$$

where Q is dopant number of average area, D' is the diffusion coefficient, t is the diffusion time and y is the depth. Assuming diffusion length is equal to SiO_2 thickness ($L = \sqrt{D't_1} = d_2$), the total dopant is the amount of Li ions extracted from $LiCoO_2$, thus $Q = (1 - x_1)\frac{\rho_1}{M_1}d_1$. Herein, $c_{Co^{3+}} = \frac{\rho_1}{M_1}x_1$, $c_{Co^{4+}} = \frac{\rho_1}{M_1}(1 - x_1)$, $c_{Si^{3+}} = c_{Li^+} = c(d_2, t_1) = \frac{(1-x_1)\frac{\rho_1}{M_1}d_1}{\sqrt{\pi}d_2}\exp\left(-\frac{1}{4}\right)$, $c_{Si^{4+}} = \frac{\rho_2}{M_2} - c_{Si^{3+}}$. Based on Equations (15, 16) and assuming $\gamma = 1$, the electromotive field (E_N) originating from Nernst potential can be calculated by:

$$E_N = \frac{V^0}{d_2} + \frac{kT}{ed_2}ln\frac{\rho_1 M_2 d_1(1 - x_1)^2\exp(-\frac{1}{4})}{x_1\left[\sqrt{\pi}\rho_2 M_1 d_2 - \exp(-\frac{1}{4})\rho_1 M_2 d_1(1 - x_1)\right]} \quad (17)$$

In region II, V_d should be also taken in account. The diffusion potential formula is given by[30]:

$$V_d = -\frac{kT}{e}\bar{t}ln\frac{a_{s'}}{a_{s''}} \quad (18)$$

where $\bar{t}$ is ion transference number averaged throughout layer thickness, $a_{s'}$ is the activity of Li ions at $LiCoO_2$/SiO_2 interface and $a_{s''}$ is the activity of Li ions at SiO_2/Si interface. According to Equation (16), $c_{s'} = c(0, t_1)$ and $c_{s''} = c(d_2, t_1)$. The remaining reference values are $\bar{t} = 0.4, T = 298\ K$[30]. Assuming $\gamma = 1$, the diffusion potential (V_d) is calculated to be $-2.5 \times 10^{-3}\ V$, which is much less than V_N, meaning that V_d can be neglected. Thus $V_{EMF} \approx V_N$, reference values are $x_1 = 0.7$, $\rho_1 = 2.5\ g/cm^3$, $\rho_2 = 2.648\ g/cm^3$, $M_1 = 97.87\ g/mol$, $M_2 = 60.086\ g/mol$, $V^0 = 1.4\ V$[13,21,31]. The simulated E_2-d_2 characteristics are presented in Fig. 6(c), E_2 decreases with increasing of the SiO_2 thickness. Thus, SiO_2 works as a Li ion trapping layer. When external voltage is removed, the SiO_2 trapping layer decreases the total electromotive field of device and maintains the states resistances.

With external voltage, Li ions transport from $LiCoO_2$ to SiO_2 and Si layers, which can produce a V_{EMF} and exhibit a nanobattery-like behavior. The phenomenon is similar to the observation reported in other redox-based memristors[23,24,34,35]. It has also been demonstrated that V_{EMF} is dependent on the chemistry and the transport properties of the materials system[30,36,37]. Thus, Li ion trapping mechanism, especially the relationship between electromotive field and SiO_2 thickness in different regions, may be also adapted to other devices based on $LiCoO_2$ and SiO_2 material system such as Li-ion batteries and Li-ion based transistors. The critical point is actually relative to thickness and Li ion concentration of $LiCoO_2$ layer, may change with fabrication parameters of devices.

Conclusion

The influence of SiO_2 trapping layer on memristive behavior of Pt/$LiCoO_2$/SiO_2/Si stacks is investigated in terms of electrical properties, device stability and retention. For the $LiCoO_2$ based memristors, the trapping layer benefits device retention. It is necessary to control the thickness of trapping layer to improve device properties. A model based on Nernst potential and diffusion potential is proposed to elucidate the Li ion trapping mechanism in SiO_2 and two different relationships between the electromotive field and SiO_2 thickness are found. According to this model, SiO_2 trapping layer decreases the total electromotive field of device and hence prevents Li ions from migrating back to $LiCoO_2$. These findings reveal the Li ion trapping mechanism of SiO_2 in $LiCoO_2$ based memristors and provide insights into the performance improvement of memristors and other devices based on $LiCoO_2$ and SiO_2.

Data Availability

The datasets generated and analysed during the current study are available from the corresponding author.

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Author Contributions

Q.H. and R.M.L. contributed equally to this work. Q.H. and R.M.L. fabricated the devices, performed electrical measurement and film characterizations; R.M.L., Q.H., X.J.Z. and A.P.H. proposed the simulation model; All authors (including Q.G., M.W., H.L.S., Z.S.X.) discussed the results; Q.H. and R.M.L. wrote the main manuscript text and prepared figures and tables with the help of P.K.C. and A.P.H.; All authors reviewed the manuscript.

Additional Information

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