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A 0.026 mm² Time Domain CMOS Temperature Sensor with Simple Current Source

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Abstract: This paper presents a time domain CMOS temperature sensor with a simple current source. This sensor chip only occupies a small active die area of 0.026 mm² because it adopts a simple current source consisting of an *n*-type poly resistor and a PMOS transistor and a simple current controlled oscillator consisting of three current starved inverter delay cells. Although this current source is based on a simple architecture, it has better temperature linearity than the conventional approach that generates a temperature-dependent current through a poly resistor using a feedback loop. This temperature sensor is designed in a 0.18 μm 1P6M CMOS process. In the post-layout simulations, the temperature error was measured within a range from −1.0 to +0.7 °C over the temperature range of 0 to 100 °C after two point calibration was carried out at 20 and 80 °C, respectively. The temperature resolution was set as 0.32 °C and the temperature to digital conversion rate was 50 kHz. The energy efficiency is 1.4 nJ/sample and the supply voltage sensitivity is 0.077 °C/mV at 27 °C while the supply voltage varies from 1.65 to 1.95 V.

Keywords: temperature sensor; time domain; threshold voltage; poly resistor; temperature error; CMOS integrated circuits

1. Introduction

Due to their small form factor, low power consumption, low cost and convenient digital interface capability, integrated temperature sensor chips have been widely used for thermal monitoring in various smart applications such as the smart farm, smart factory, smart health, and so on. Integrated temperature sensor chips can be implemented in various ways depending on the sensing element which is generally chosen from the threshold voltage, mobility, resistance or thermal voltage; the measured signal type, which is generally chosen from the voltage, current, frequency, or delay time; and the overall architecture which is basically determined by the chosen sensing element and the measured signal type [1–30].

Among the possible architectures, a time domain architecture based on frequency or delay time is promising because it can benefit from the recent trend that time resolution is being increased while voltage resolution is being decreased as the CMOS channel length and the supply voltage are scaled down. By measuring time domain signals such as the clock frequency, clock period or delay time, an efficient estimate of the current temperature can be obtained [1–20]. The sensing element can be chosen from the mobility, threshold voltage or resistance. Depending on the choice, the temperature linearity of a time domain CMOS temperature sensor is fundamentally limited by the temperature linearity of the chosen sensing element. In this paper, we present a time domain CMOS temperature sensor with the sensing element dependent on both the resistance of an *n*-type poly resistor and the threshold voltage of a PMOS transistor at the same time. By adopting this simple current source as a sensing element, we gain the ability to multiply two different types of temperature characteristics of

the resistance of an *n*-type poly resistor and the threshold voltage of a PMOS transistor by each other and improve the temperature linearity of the temperature sensor.

This paper is organized as follows. In Section 2, we explain how this simple current source can have better temperature linearity than the conventional approach. Section 3 describes the architecture and schematics of the implemented time domain CMOS temperature sensor adopting the simple current source. Section 4 shows the simulation results and the performance comparison with the previous works found in literature. Finally, the conclusion is given in Section 5.

2. Temperature Linearity of the Sensing Element

Figure 1 shows the conventional current source based on a single *n*-type poly resistor [1,8,9,13]. It consists of multiple diode-connected PMOS transistors between V_{DD} and the ground, a differential input to a single-ended output amplifier, an *n*-type poly resistor and a PMOS transistor. Since multiple diode-connected PMOS transistors generate a reference voltage, V_{REF} , it is applied across the *n*-type poly resistor, $R_N(T)$, through the feedback loop consisting of the differential amplifier and the PMOS transistor as shown in the below figure. The reference current, $I(T)$, becomes exactly proportional to V_{REF} and inversely proportional to $R_N(T)$ as follows. This current source has been used because its temperature linearity can be made dependent on only that of the resistor; then the analysis and design become simpler than for the other types of current sources.

$$I(T) = \frac{V_{REF}}{R_N(T)} \tag{1}$$

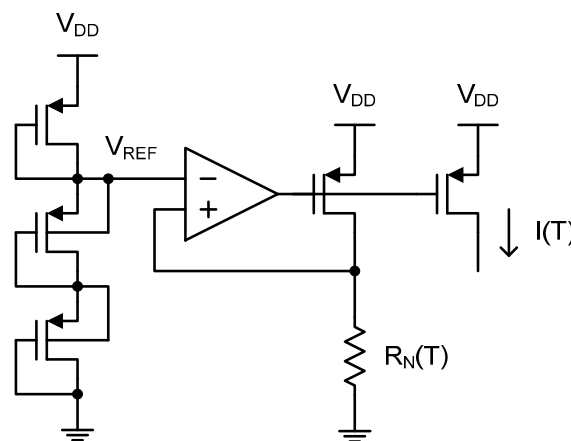


Figure 1. The conventional approach for generating a temperature-dependent current through a poly resistor using a feedback loop.

Figure 2 shows the temperature-dependent variation and temperature linearity error of $R_N(T)$ and $1/R_N(T)$, respectively, where $R_N(T)$ is the resistance of the *n*-type poly resistor. In these figures, the values of $R_N(T)$ and $1/R_N(T)$ were normalized with respect to the values measured at 25 °C and the temperature linearity error is defined as the temperature deviation, which is measured in °C, from the linear fit of $R_N(T)$ or $1/R_N(T)$. Since $R_N(T)$ is convex downward whereas $1/R_N(T)$ is convex upward, they can be modeled as

$$R_N(T) = R_N(25) \times [1 - a(T - 25) + b(T - 25)^2] \tag{2}$$

and

$$\frac{1}{R_N(T)} = \frac{1}{R_N(25)} \times [1 + \alpha(T - 25) - \beta(T - 25)^2] \tag{3}$$

where a , b , α and β are positive first and second order temperature coefficients of $R_N(T)$ and $1/R_N(T)$, respectively. Here, $R_N(25)$ is the resistance of the n -type poly resistor measured at 25 °C. As shown in Figure 2, the temperature linearity error varies from -2.60 to $+2.87$ °C and from -0.79 to $+0.83$ °C for $R_N(T)$ and $1/R_N(T)$, respectively, over the temperature range of 0 to 100 °C. This shows that $1/R_N(T)$ is more linear against temperature variation than $R_N(T)$ if they are implemented by using this CMOS technology. Thus, in this work, we have chosen $1/R_N(T)$ as the sensing element and consequently $I(T)$ of (1) is now expressed as

$$I(T) = \frac{V_{REF}}{R_N(25)} \times [1 + \alpha(T - 25) - \beta(T - 25)^2] \tag{4}$$

when the conventional current source of Figure 1 is used. Since the temperature linearity error of $I(T)$ is limited by that of $1/R_N(T)$ as implied in (4), we can expect that the temperature linearity of the temperature sensor will vary from -0.79 to $+0.83$ °C if there is not any other kind of additional nonlinearity source.

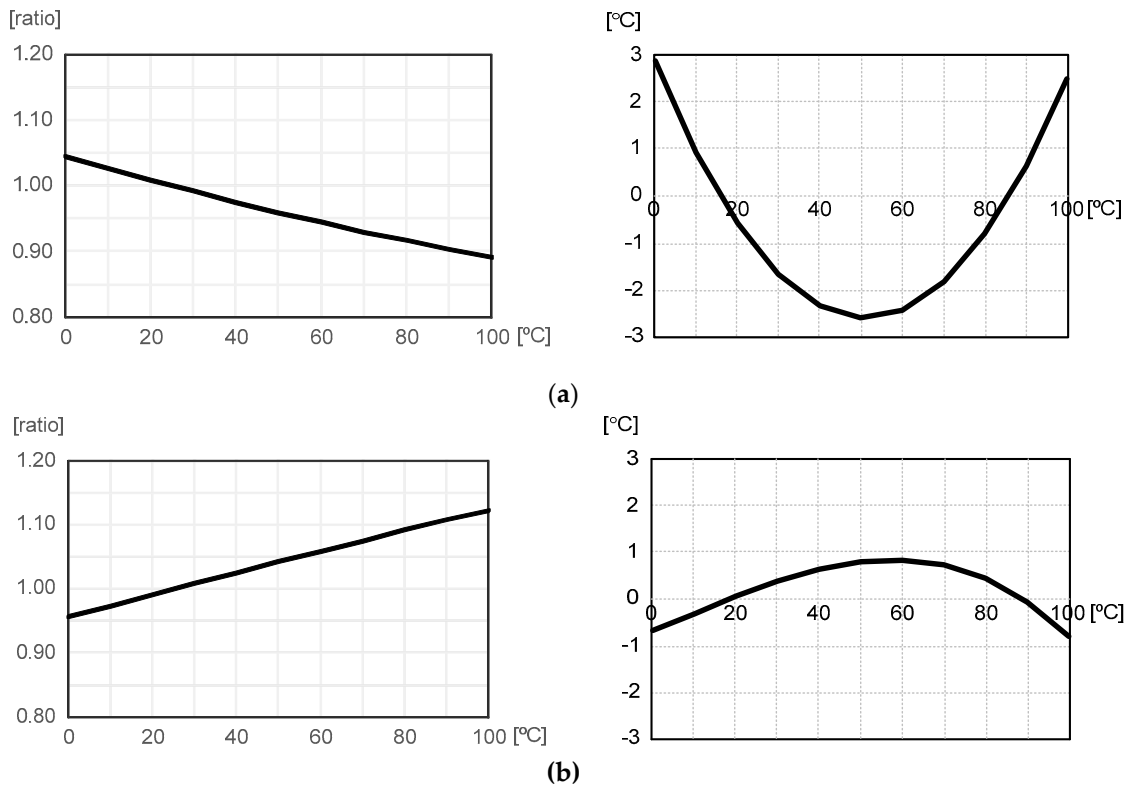


Figure 2. The temperature-dependent variation and temperature linearity error of (a) $R_N(T)$ and (b) $1/R_N(T)$.

Figure 3 shows the simple current source adopted alternatively in this time domain CMOS temperature sensor. As shown in the figure, it just consists of an n -type poly resistor, of which the resistance value is $R_N(T)$, and a single diode-connected PMOS transistor. Since $I(T)$ flows through the n -type poly resistor and PMOS transistor, we can obtain the equation of $I(T)$ by equating two current equations of the n -type poly resistor and the PMOS transistor as follows.

$$I(T) = \frac{1}{2} \mu(T) C_{OX} \frac{W}{L} (V_{SG}(T) - V_{TH}(T))^2 = \frac{V_{DD} - V_{SG}(T)}{R_N(T)} \tag{5}$$

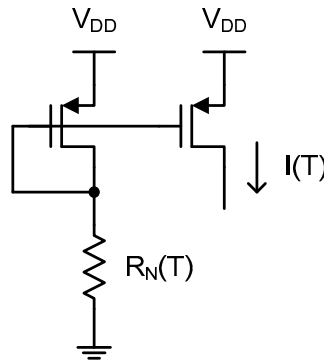


Figure 3. The simple current source for generating a temperature-dependent current through a poly resistor, with better temperature linearity.

Then, $V_{SG}(T)$ is solved as

$$V_{SG}(T) = V_{TH}(T) + \sqrt{\left(V_{DD} - V_{TH}(T) + \frac{1}{\mu(T)C_{OX}\frac{W}{L}R_N(T)} \right)^2 - (V_{DD} - V_{TH}(T))^2} \quad (6)$$

Since the PMOS transistor operates in the vicinity of the threshold voltage for low power consumption in this work, $V_{SG}(T)$ can be simplified to $V_{TH}(T)$ and thus we obtain

$$I(T) \approx \frac{V_{DD} - V_{TH}(T)}{R_N(T)} \quad (7)$$

where

$$V_{TH}(T) = V_{TH}(25) - \gamma(T - 25). \quad (8)$$

Here, γ is the positive temperature coefficient of the threshold voltage of the PMOS transistor and $V_{TH}(25)$ is the threshold voltage measured at 25 °C. $I(T)$ can be finally obtained in quadratic equation form by substituting $1/R_N(T)$ of (3) and $V_{TH}(T)$ of (8) into (7), as follows:

$$I(T) \frac{V_{DD} - V_{TH}(T)}{R_N(T)} = \frac{V_{DD} - V_{TH}(25) + \gamma(T - 25)}{R_N(25)} \times \left[1 + \alpha(T - 25) - \beta(T - 25)^2 \right] \approx \frac{V_{DD} - V_{TH}(25)}{R_N(25)} \times \left[1 + A(T - 25) - B(T - 25)^2 \right] \quad (9)$$

where

$$A = \alpha + \frac{\gamma}{V_{DD} - V_{TH}(25)} \quad (10)$$

and

$$B = \beta - \frac{\alpha\gamma}{V_{DD} - V_{TH}(25)}. \quad (11)$$

Now let us compare (9) with (4) and observe the relative increase and decrease of A and B in (10) and (11), respectively. We can see that $A > \alpha$ and $B < \beta$ and that the temperature linearity of this simple current source has been fairly improved and the amount of the improved temperature linearity error is determined by α , β , γ and $V_{DD} - V_{TH}(25)$ as indicated in (10) and (11). Contrary to the conventional approach shown in Figure 1, the reference current, $I(T)$, of (9) depends on both the resistance of an n -type poly resistor and the threshold voltage of a PMOS transistor at the same time and the temperature linearity error has been successfully reduced as shown in Figure 4. The temperature linearity error of $I(T)$ now varies from -0.40 to $+0.38$ °C over the temperature range of 0 to 100 °C.

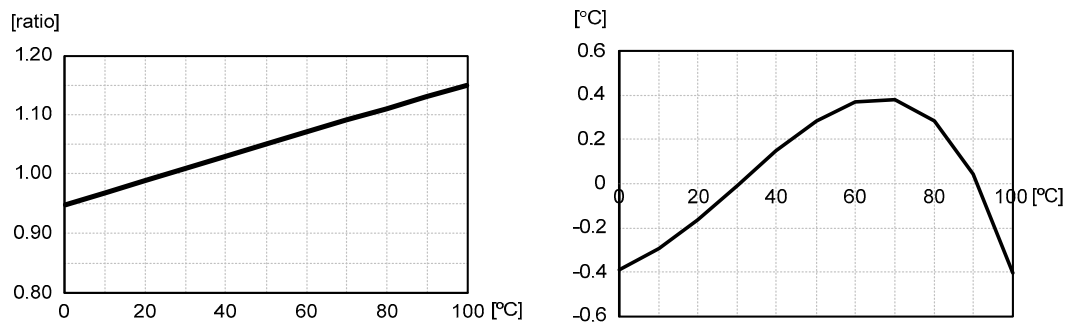


Figure 4. The temperature-dependent variation and temperature linearity error of I(T).

3. Implementation

3.1. Architecture

Figure 5 shows the architecture of the implemented time domain CMOS temperature sensor. It consists of the simple current source, a three stage current controlled oscillator (CCO), an 11b binary counter and an additional digital logic.

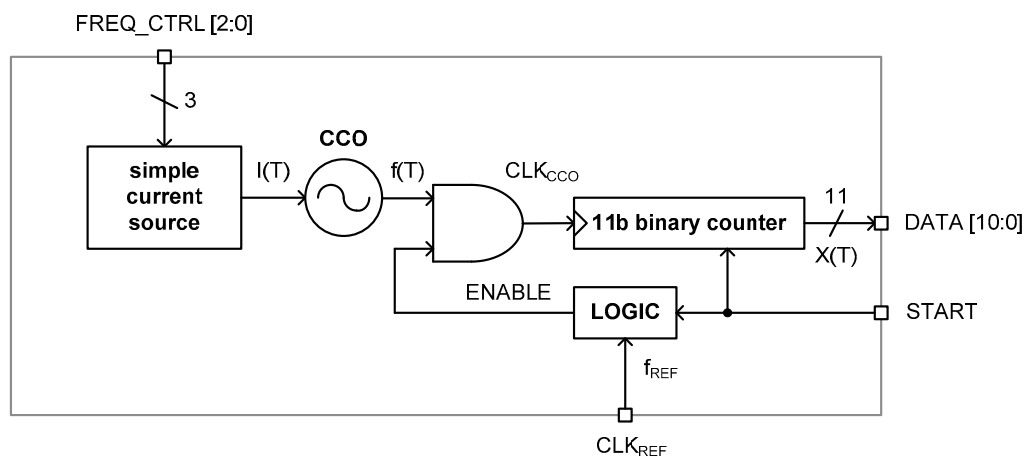


Figure 5. The architecture.

The current source generates the temperature-dependent reference current, I(T), with improved temperature linearity which is fed to the CCO. The CCO generates the clock signal oscillating at the frequency of f(T) which is linear with I(T). The logic circuit generates the ENABLE pulse whose pulse width equals one clock period, 1/f_{REF}, of the external reference clock, CLK_{REF}. As shown in the timing diagram of Figure 6, the rising edges of the clock signal, CLK_{CCO}, generated from the CCO is counted by the 11b binary counter for the time duration of 1/f_{REF} to generate the 11b digital output code, DATA[10:0]. The DATA[10:0] is the quantized digital value of the temperature estimation function, X(T), which is defined as

$$X(T) = \frac{1}{\frac{f_{REF}}{1}} \tag{12}$$

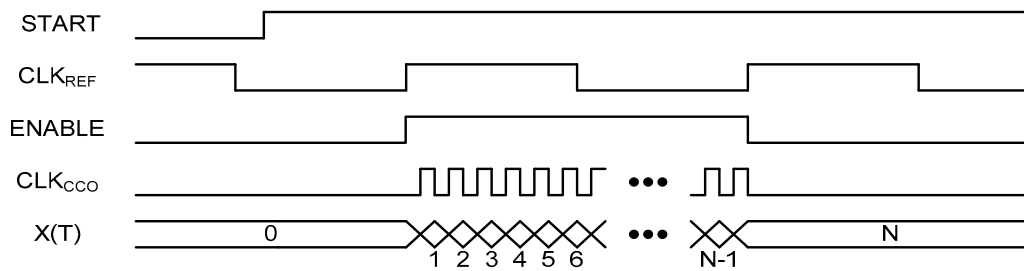


Figure 6. The timing diagram.

In this paper, in regard to the detailed definition of the temperature estimation function, we introduced and explained the 12 types of operational principles and the corresponding temperature estimation functions of the time domain CMOS temperature sensors from our previous work [1]. Finally, the START signal enables the 11b binary counter and the additional logic circuit to start the operation of this time domain CMOS temperature sensor.

3.2. Circuits

Figure 7 shows the schematic of the simple current source and the CCO. In the current source, the resistance of the *n*-type poly resistor, $R_N(T)$, has been designed to be externally tuned by the external 3b digital control word, $FREQ_CTRL[2:0]$. We added these extra 3b digital codes for rough compensation of the probable severe process variation of $R_N(T)$, which rarely happens. If the resistance of the *n*-type poly resistor, $R_N(T)$, is shifted too much from its typical value at the worst case corner, the total power consumption of the total temperature sensor will be affected too much. Thus, this 3b rough digital tuning by $FREQ_CTRL[2:0]$ is only necessary for robust operation and consistent power consumption and should be carried out before we execute the two point calibration. Of course, if the resistance of the *n*-type poly resistor can be accurately controlled during fabrication within the capability of normal two point calibration, $FREQ_CTRL[2:0]$ needs not be additionally implemented.

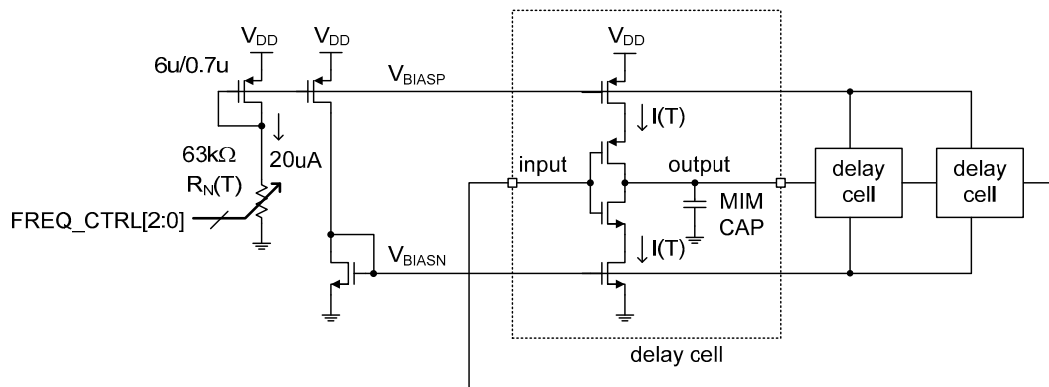


Figure 7. The schematic of the current source (left side) and the CCO (right side).

The temperature-dependent reference current, $I(T)$, is delivered to each current starved inverter type delay cell inside the CCO through two DC bias voltages, V_{BIASP} and V_{BIASN} , respectively. By supplying the almost equivalent currents to the PMOS and the NMOS paths of the current starved inverters, the low to high and high to low propagation delay times of each delay cell can be made almost equal to each other. Because the propagation delay time, $\tau(T)$, of each delay cell is represented as

$$\tau(T) = \frac{V_{DD}}{2} \times \frac{C}{I(T)} \tag{13}$$

the clock frequency, $f(T)$, of the CCO can also be expressed as

$$f(T) = \frac{1}{\tau(T)} \times \frac{1}{2N} = \frac{I(T)}{N \times V_{DD} \times C} \quad (14)$$

where N is the number of total delay cells of the CCO, and $f(T)$ is linear with $I(T)$. Finally, the temperature estimation function, $X(T)$, of the temperature sensor can be represented as

$$X(T) = \frac{V_{DD} - V_{TH}(25)}{f_{REF} \times N \times V_{DD} \times C \times R_N(25)} \times [1 + A(T - 25) - B(T - 25)^2] \quad (15)$$

from (9), (12) and (14).

4. Performance

The time domain CMOS temperature sensor was implemented in a 0.18 μm 1P6M CMOS process with a general V_{TH} . Figure 8 shows the die photo and the active die area is 0.026 mm^2 . To the best of our knowledge, the die area of 0.026 mm^2 is the smallest among the previously published time domain CMOS temperature sensors implemented in 0.18 μm CMOS technology. Figure 9 shows the simulated temperature error over the temperature range of 0 to 100 $^{\circ}\text{C}$ after one point and two point calibrations are carried out, respectively. For the process corners, TT, FF, SS, FS, and SF, the temperature error varies from -2.33 to $+1.99$ $^{\circ}\text{C}$ after one point calibration at 50 $^{\circ}\text{C}$ and from -0.96 to $+0.66$ $^{\circ}\text{C}$ after two point calibration at 20 and 80 $^{\circ}\text{C}$, respectively. The temperature error of the time domain CMOS temperature sensor is measured as being somewhat larger than the temperature linearity error of $I(T)$ only, because the temperature linearity error of the load capacitance, C , may also affect the temperature estimation function, $X(T)$, as can be seen from (15). Additionally, the quantization error at the 11b digital output code, DATA[10:0], the residue process variation error after two point calibration, the approximation error of $I(T)$ made for the derivation of (7), the charge sharing effect within the delay cell and the transistor mismatch effect between current mirrors may also be the sources of additional contributions to the increase of the total temperature error. The temperature error of Figure 9b has been measured greater than the temperature error of Figure 4. The temperature resolution was set as 0.32 $^{\circ}\text{C}$ and the temperature to digital conversion rate, which is exactly equal to f_{REF} in this design, is about 50 kHz. The energy efficiency is 1.4 nJ/sample and most of the power consumption is dissipated by the current source. As shown in Figure 10, the supply voltage sensitivity is measured as low as 0.077 $^{\circ}\text{C}/\text{mV}$ at 27 $^{\circ}\text{C}$ while V_{DD} varies from 1.65 to 1.95 V. Table 1 compares the performances of this temperature sensor with those of the previous works in literature. The previous works are all time domain CMOS temperature sensors which were implemented in CMOS processes with the same minimum channel length of 0.18 μm , for fair performance comparison with this work. Compared to the previous works, we can see that this temperature sensor occupies a relatively small die area and has relatively small temperature error as shown in Table 1.

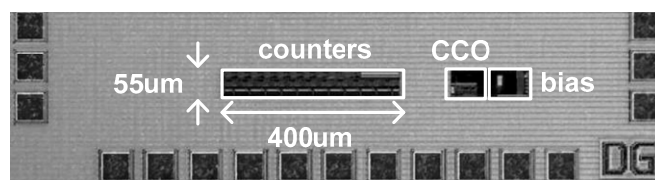
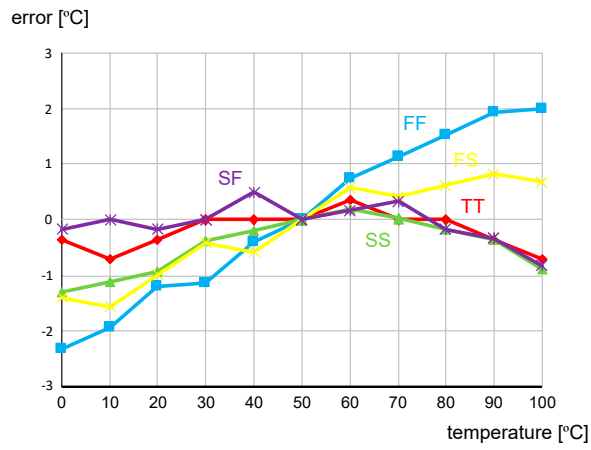
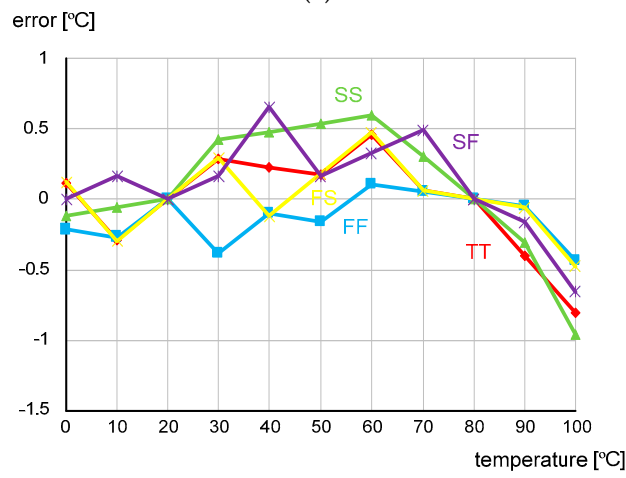


Figure 8. The die photo.



(a)



(b)

Figure 9. The temperature error after (a) one point calibration at 50 °C and (b) two point calibration at 20 and 80 °C, carried out against the different process corners, TT, FF, SS, FS and SF.

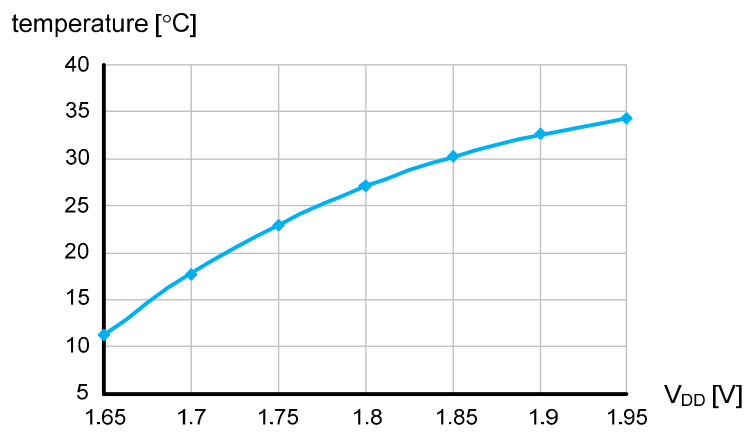


Figure 10. The V_{DD} sensitivity when V_{DD} is swept from 1.65 to 1.95 V.

Table 1. The performance summary.

Reference	[1]	[7]	[8]	[9]	[14]	This Work
CMOS technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Die area	0.432 mm^2	0.074 mm^2	0.05 mm^2	0.09 mm^2	0.19 mm^2	0.026 mm^2
Supply voltage	1.8 V	0.8 V	1.0 V	1.2 V	1.2 V	1.8 V
Temperature range	0–100 $^{\circ}\text{C}$	–20–80 $^{\circ}\text{C}$	0–100 $^{\circ}\text{C}$	0–100 $^{\circ}\text{C}$	–40–85 $^{\circ}\text{C}$	0–100 $^{\circ}\text{C}$
Resolution	0.49 $^{\circ}\text{C}$	0.145 $^{\circ}\text{C}$	0.3 $^{\circ}\text{C}$	0.3 $^{\circ}\text{C}$	0.18 $^{\circ}\text{C}$	0.32 $^{\circ}\text{C}$
Accuracy	–1.6–0.6 $^{\circ}\text{C}$	–0.9–1.2 $^{\circ}\text{C}$	–1.6–3.0 $^{\circ}\text{C}$	–1.4–1.5 $^{\circ}\text{C}$	–1.0–1.0 $^{\circ}\text{C}$	–1.0–0.7 $^{\circ}\text{C}$
Conversion rate	25 kHz	1.2 Hz	100 Hz	33.3 Hz	1kHz	50 kHz
Energy efficiency	7.2 nJ/sample	8.9 nJ/sample	2.2 nJ/sample	2.2 nJ/sample	66.5 nJ/sample	1.4 nJ/sample
V_{DD} sensitivity	0.085 $^{\circ}\text{C}/\text{mV}$	0.0038 $^{\circ}\text{C}/\text{mV}$	-	0.014 $^{\circ}\text{C}/\text{mV}$	-	0.077 $^{\circ}\text{C}/\text{mV}$

5. Conclusions

We implemented a time domain CMOS temperature sensor alternatively adopting a simple current source consisting of an n -type poly resistor, a PMOS transistor and a simple three stage CCO. Although the current source is based on a simple architecture, it can generate a temperature-dependent reference current, $I(T)$, which has better temperature linearity than the conventional approach because it can multiply two different temperature characteristics of the resistance of an n -type poly resistor and the threshold voltage of a PMOS transistor by each other. Consequently, we have successfully implemented a temperature sensor with a small die area and a small temperature error.

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Conflicts of Interest: The authors declare no conflict of interest.

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