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Ferroelectric Content-Addressable Memory Cells with IGZO Channel: Impact of Retention Degradation on the Multibit Operation

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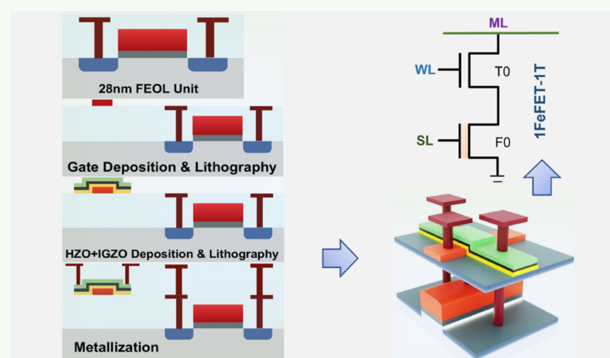
ABSTRACT: Indium gallium zinc oxide (IGZO)-based ferroelectric thin-film transistors (FeTFTs) are being vigorously investigated for being deployed in computing-in-memory (CIM) applications. Content-addressable memories (CAMs) are the quintessential example of CIM, which conduct a parallel search over a queue or stack to obtain the matched entries for a given input data. CAM cells offer the ability for massively parallel searches in a single clock cycle throughout an entire CAM array for the input query, thereby enabling pattern matching and searching functionality. Therefore, CAM cells are used extensively for pattern matching or search operations in data-centric computing. This paper investigates the impact of retention degradation on IGZO-based FeTFT on the multibit operation in content CAM cell applications. We propose a scalable multibit 1FeTFT-1T-based CAM cell composed of only one FeTFT and one transistor, thus significantly improving the density and energy efficiency compared with conventional complementary metal−oxide−semiconductor (CMOS)-based CAM. We successfully demonstrate the operations of our proposed CAM with storage and search by exploiting the multilevel states of the experimentally calibrated IGZO-based FeTFT devices. We also investigate the impact of retention degradation on the search operation. Our proposed IGZO-based 3-bit and 2-bit CAM cell shows 10^4 s and 10^6 s retention, respectively. The single-bit CAM cell shows lifelong (10 years) retention.



KEYWORDS: *computing-in-memory (CIM), content-addressable memory (CAM), ferroelectric memory, HZO, IGZO, FeTFT*

■ INTRODUCTION

The plethora of real-time data generated by social media, Internet search engines, and user-edge devices has mandated the change in the computing paradigm. Therefore, artificial intelligence has become a *de facto* choice of many computer scientists to solve many computationally complex problems. In today's era of big data, the volume of information that requires processing and storage at data centers has been increasing rapidly. As the scaling of logic and memory technologies slows down, the gap between performance and demand increases, thereby calling for an alternative computational paradigm with higher performance and better energy efficiency.[1−3] The paradigm of in-memory computation offers an energy-efficient alternative that can avoid the so-called von Neumann bottleneck in terms of latency and energy consumption.[4−12] There are various computing-in-memory (CIM) hardware systems; among them, content-addressable memory (CAM) is a promising candidate for its wide applications in data-intensive high-performance search operations. CAMs offer massively parallel search in a single clock cycle throughout the entire memory. This is highly desirable in applications, such as network routing, CPU caching, and deep learning.[13−17]

CAM cells are at the heart of a *de facto* configuration of a CIM operation and are extensively used in fast search operations, especially in network routing and CPU caching.[18,19] CAM cells can be used to find the location of the stored data in any 2D array, linked list, stack, or queue. Quintessentially, CAM cells return the location of the stored data by initiating a parallel search operation of the input data in a data structure. Traditionally, a CAM cell is realized by two SRAM cells, which consist of 16 transistors and cause significant energy consumption and low density.[20] As the emerging nonvolatile memories (NVMs) mature technologically, different approaches in designing CAM cells employing

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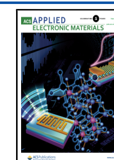

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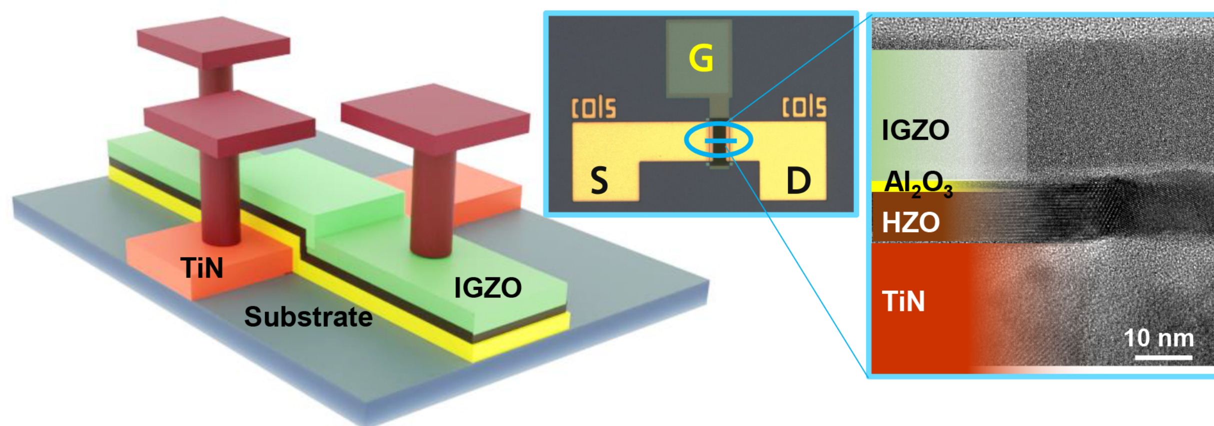

Figure 1. Schematic illustration and transmission electron microscopic (TEM) cross-section image of the fabricated IGZO-based Fe-TFT. The TEM image demonstrates the thickness of each layer.

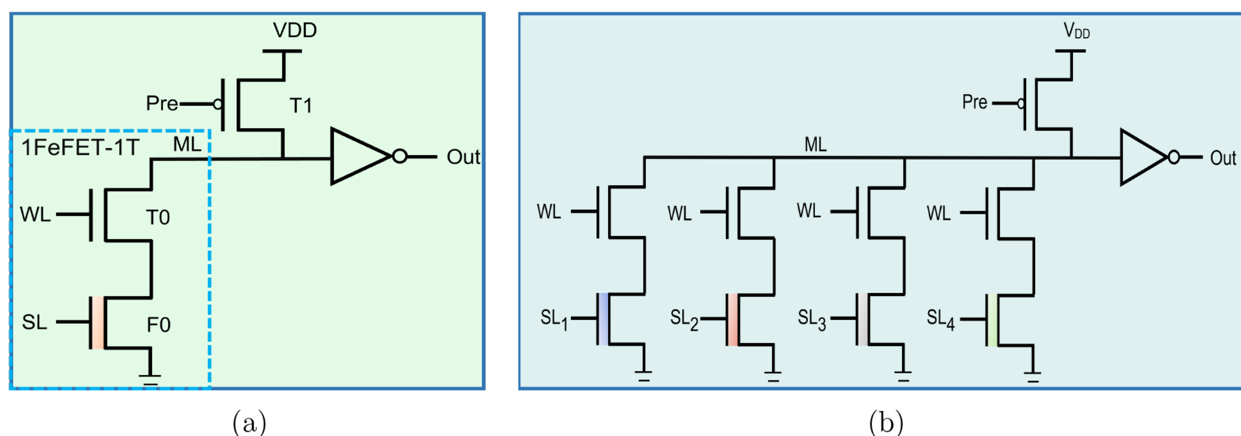

Figure 2. (a) Proposed CAM cell and its peripheral circuits. (b) A 1 × 4 CAM array with 4 cells connected on the same match line.

magnetic tunnel junctions (MTJ),[21] resistive random-access memories (RRAMs),[22−24] phase-change memory (PCM),[25] ferroelectric RAM (FeRAM),[26,27] and ferroelectric field-effect transistors (FeFET)[28−33] are being investigated. Among the emerging memories, the FeFET technology is preferable for CAM design because of its high retention, large on/off ratio, energy-efficient field-driven write mechanism, and ease of integration with complementary metal−oxide−semiconductor (CMOS) processes.[34−37] However, very few analog or multibit FeFET-based CAM (FeCAM) designs have been proposed until now.[30,38,39] Multibit information can be stored in a CAM within a single memory element, and the data can be searched using a multibit query. A bit can be detected when an exact match between the input query and the stored bit is found. Recently, IGZO-based thin-film transistors (TFTs) have been the center of attraction among the research community.[38,40,41] It has been envisaged that IGZO-based TFTs have the potential to replace low-temperature polycrystalline silicon-based TFTs for logic and memory applications. In this work, we have proposed a 1FeTFT-1T multibit CAM cell based on IGZO-FeTFT. The polarization state of the ferroelectric layer is controlled by the programming pulses applied at the gate terminal, which controls the accumulation and depletion of the carriers in the semiconductor. Typically, FeTFTs reported so far for CIM applications have focused on improving the device endurance.[38,42,43] However, for CAM cell operation, retention characteristics are more important than endurance because the search operation in the CAM cell requires reading the data multiple times. In this work, we evaluate the impact of retention degradation on the feasibility of the multibit operation in IGZO-based FeCAM cells. We observed that the 1FeTFT-1T (1 transistor) CAM cell shows 10^4 s and 10^6 s retention for 3 bits/cell and 2 bits/cell operations, respectively. However, the single-bit CAM cell shows lifelong (10 years) retention capability.

EXPERIMENTS

The experiment began with the fabrication of metal−ferroelectric insulator−semiconductor metal (MFISM) capacitors. The ferroelectric, insulator, and semiconductor layers were 10 nm of HZO, 2 nm of Al_2O_3, and 30 nm of IGZO layers, respectively. The MFISM capacitors were fabricated on 300 mm, heavily boron-doped silicon wafers in the industry-standard semiconductor process tools. A titanium nitride (TiN)-based bottom electrode was deposited by atomic layer deposition (ALD) using $TiCl_4$ and NH_3 precursors. The thermal budget for depositing the HZO layer was 300 °C during the ALD process. The atomic layer deposition of HZO was conducted with $HfCl_4$ and ZrCl4 as the precursors and H_2O as the oxidizing agent. The interfacial insulating layer of Al_2O_3 of thickness 2 nm was deposited via the ALD process with trimethyl aluminum and H_2O. The IGZO layer, which acts as a semiconductor, was deposited by RF magnetron sputtering. The RF sputtering was conducted from a ceramic target (In/Ga/Zn = 1:1:1) with a ratio of 33.3:1 for argon to oxygen. The working pressure of the sputtering was μbar. Finally, the titanium nitride (TiN) gate electrode was deposited by sputtering.

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The thermal budget of sputtering was kept below 100 °C. The crystallization of the HZO layer was carried out by thermal annealing inside a furnace at 350 °C for 1 h in a nitrogen atmosphere.

We have fabricated FeTFTs with a gate-first approach with similar gate stacks with a 30 nm IGZO channel, 10 nm HZO channel, and 2 nm of Al_2O_3. The fabrication began with insulation of a 300 mm bulk Si wafer with a silicon dioxide thickness of 100 nm (SiO_2). For FeTFTs, 50 nm of TiN was deposited, and e-beam lithography along with reactive ion etching (RIE) was used for forming the bottom gate. Electron-beam evaporation was used to deposit source−drain contacts, and the lift-off technique patterned the contacts. The annealing for crystallization was performed last. Figure 1 shows the schematic of the fabricated FeTFT and the transmission electron microscopic (TEM) image of the fabricated devices. Further details of these devices, including the band diagram of the gate stack and the impact of Al_2O_3 interfacial layer, are described elsewhere.[44,45]

The electrical characterization for measuring the polarization response concerning the externally applied voltage was performed (Aixacct TF 3000 FE Analyzer) using a triangular waveform at a frequency of 1 kHz. The FeTFTs were characterized using the Keysight B1500A semiconductor analyzer and Keysight B1350A arbitrary waveform generator. The structural information on the crystalline phases of the HZO film was obtained by grazing incidence X-ray powder diffraction experiment (GIXRD). Before mounting of the samples for GIXRD, the samples were rotated 45° between the direction of the silicon wafer (100) and the diffraction plane (001).

Multibit FeCAM Operation. This section discusses the proposed multibit CAM cell, which consists of one FeFET and one logic transistor, as shown in Figure 2a. As a three-terminal device, a FeFET can be used both as the memory and the selector element. This has the potential advantage in terms of area-scaling over 1 transistor−1 resistor (1T-1R) architecture often required for technologies such as phase-change memory (PCM) or resistive memory (RRAM). In addition, heterogeneous integration with a separate selector technology can be avoided. In this work, we utilize the multilevel storage capacity of our FeFET device to design a multibit CAM cell. A FeFET device can be programmed to multiple V_{th} levels by applying voltage pulses of different amplitudes to the gate terminal.[35] Figure 2a shows the design of a 1FeFET-1T CAM cell. The logic transistor (T0) is used in the CAM cell to limit the ON current of the FeFET and acts as an access device to access a particular CAM cell for writing and searching bit-levels from a CAM array without affecting other CAM cell information. This cascoded transistor connected on top of the FeTFT reduces the impact of device variation, especially in the ON-state current. The details of this 1F-1T structure and their applications in memory arrays have been described before.[40,46,47] In this work, we primarily focus on the impact of retention degradation. Figure 2b shows a 1 × 4 CAM array, which is constructed by connecting 4 CAM cells on the same match line. For sensing the bits stored (V_{th} levels) in the CAM, a peripheral circuit is connected to the match line, which consists of a PMOS and an inverter. The PMOS is used to precharge the match line (ML) at the precharge phase (Pre = low) before the search operation and at the evolution phase (Pre = high) when the search operation is conducted. For simplicity, an inverter is used for voltage level sensing to get the binary output for searching the different (V_{th}) levels stored in the CAM. First, the word line (WL) is activated, and a search line voltage (V_{SL}) is applied to the gate terminal of FeFET. When (V_{SL}) matches with the particular (V_{th}) stored in a CAM cell, the FeFET (F0) turns on, and the match line (ML) discharges. As a result, the inverter output reaches a high level ("1"), which indicates a match between the stored bit and the search. Otherwise, the ML remains close to V_{DD}, and correspondingly, the output is low ("0"), which indicates a mismatch. Figure 3 shows an example of a multibit digital FeCAM operation. Four data levels can be stored in each cell. The stored data is shown in a green-colored box. Now, the word line (WL) is activated for searching the stored data, and an appropriate voltage is applied through the search line (SL). The matched and the mismatched cells are indicated in green and red, respectively.

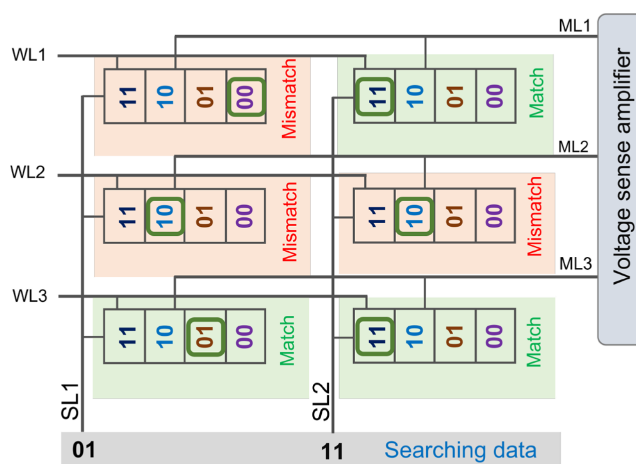

Figure 3. An example of a 2 bits/cell digital FeCAM operation.

RESULTS AND DISCUSSION

In the following section, we discuss the experimental results obtained through GIXRD, electrical characterization, and design of the CAM cells.

GI-XRD. Figure 4 shows the grazing incidence X-ray diffraction (GIXRD) pattern of HZO thin films with different

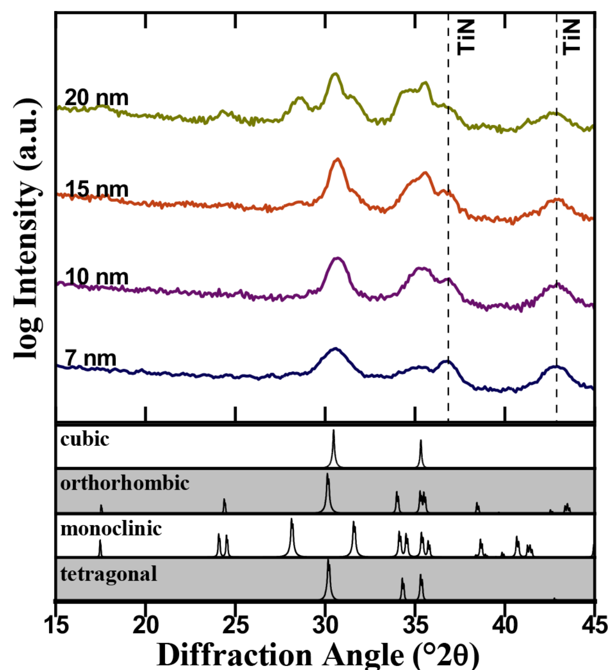

Figure 4. Grazing incidence X-ray diffraction pattern of metal−ferroelectric−metal (MFM) stacks annealed in a furnace oven at 350 °C for 1 h. The thicknesses of the HZO films are 7, 10, 15, and 20 nm.

film thicknesses. It is observed through the XRD analysis that the thermal budget of 350 °C for 1 h is sufficient to form the ferroelectric orthorhombic phase in HZO with a thickness of 10 nm and above. The requirement of a higher annealing temperature with declining film thickness is well known. This phenomenon can be attributed to the increased surface-to-volume ratio of ferroelectric layers, which have a thickness of only a few nanometers.

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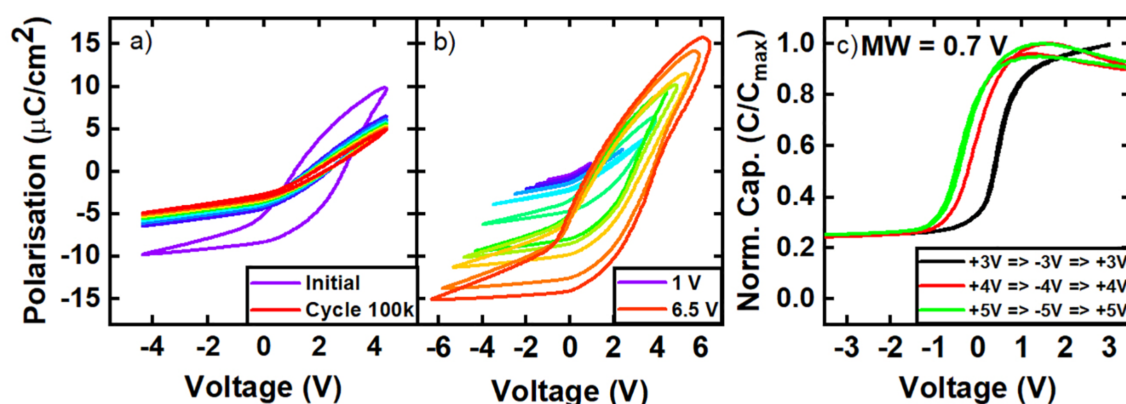

Figure 5. (a) The polarization response with respect to the externally applied voltage (P−V) shows wake-up behavior for up to 10^5 electric field cycles. (b) P−V measurements' major and minor loop characterizations show the polarization paths for bias voltages below the saturation. (c) The capacitance versus voltage characteristics show a memory window around 1 V. The measurement results have been reproduced from the same set of devices reported in our previous publication.[48]

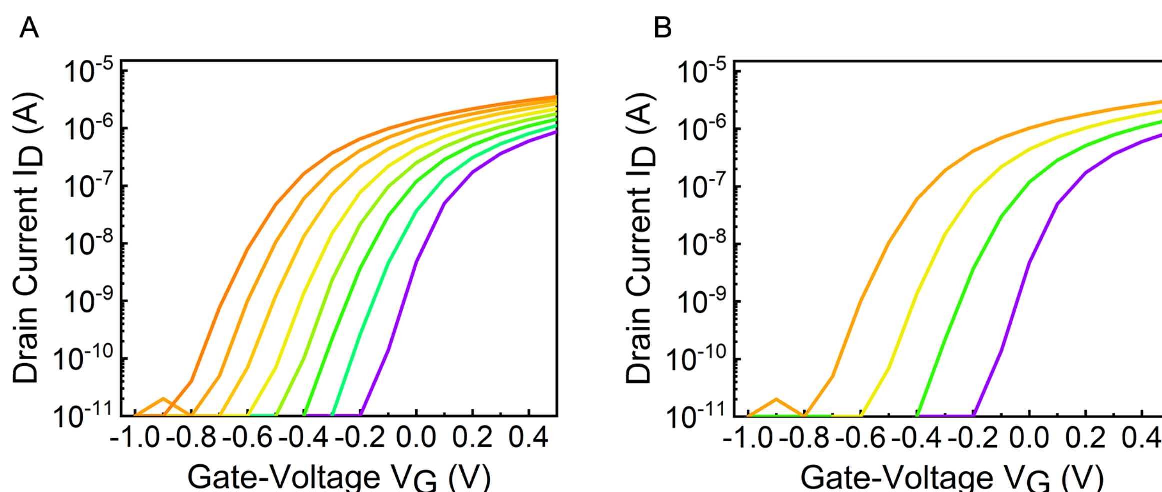

Figure 6. Measured transfer characteristics (I_d−V_g) of the fabricated FeTFTs with 30 nm of IGZO and 10 nm of HZO films. The amplitude of the write pulse varied between 3 and 7 V, whereas the pulse width was fixed at 200 ns. Programming for (a) 8 V_{th} levels and (b) 4 V_{th} levels.

Electrical Characterization. The comprehensive analysis of P−V and C−V characteristics of the MFISM stack with 30 nm of IGZO and 10 nm of HZO is shown in Figure 5. We can observe in Figure 5a monotonic decrease in the memory window with increasing field cycling, and the memory window disappears above 10^5 cycles. Figure 5b shows the evolution of the asymmetric polarization curve with increasing bias voltage. We observe that the negative remnant polarization and the positive coercive voltage increase with increasing bias, which leads to the asymmetric P−V curve. The CV curve shown in Figure 5c demonstrates a capacitance response similar to the metal−insulator−semiconductor structure up to ±3 V, but for voltage above ±4 V, the flat-band voltage is shifted to the left, and a memory window of 0.7 V is observed.

The experimentally measured transfer characteristics (I_d−V_g) of fabricated IGZO-based FeTFTs for 8 V_{th} and 4 V_{th} levels are shown in Figure 6. The V_{th} levels are written with pulses of increasing positive amplitudes (3 V to 7 V) for a fixed pulse width of 200 ns. The FE material can be partially switched to different domains by applying different voltage pulses or various amplitudes or widths at the gate of the FeFET, which results in different V_{th} levels for the device. In this article, we have focused on pulse amplitude-based programming instead of pulse width-based programming, as the former pulsing scheme engenders a wider memory window compared with the later one.[48] The gate voltage was swept only between ±1 V to prevent programming during the readout. Moreover, it is observed that there are no overlaps between the neighboring V_{th} levels. So, it is feasible to store multiple states in the device. The experimentally measured transfer characteristics are calibrated with the multidomain comprehensive model of a FeFET.[49] The calibrated FeFET model is then used for SPICE simulations to demonstrate multibit CAM operation.

Verification of Multibit FeCAM Operation. A 2 bits/cell operation using a single-cell CAM (Figure 2a) is demonstrated with four different V_{th} levels (−0.025, −0.097, −0.168, and −0.253 V). In each configuration, the output voltage is sensed with different V_{SL} values applied for a search time of 10 ns, as shown in Figure 7a−d. The three-dimensional plots in Figure 7a−d are converted to two-dimensional plots (Figure 7e,f) by considering a fixed search time of 10 ns. This is done to realize a sharp nonoverlapping decision range in each state for the match and mismatch cases, as shown in Figure 7e,f. Take the "10" state as an example (written with V_{th3} level). When V_{SL} is greater than V_{th3}, the match line (ML) discharges at a fast rate, and the output gets high (match). However, when V_{SL} is less than V_{th3}, the output is low (mismatch), and the ML remains

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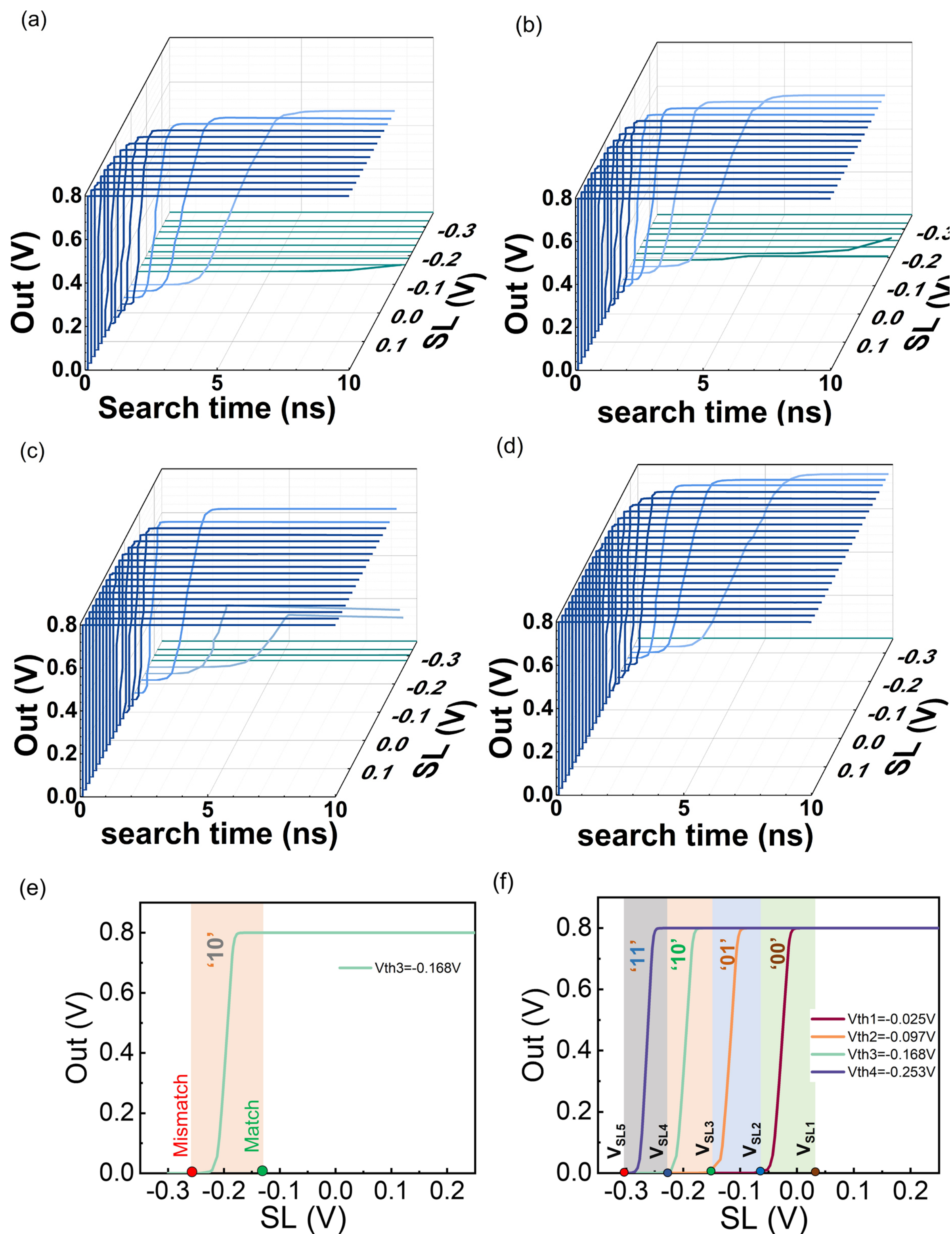

Figure 7. Transient waveform of the sensed output for a single CAM cell. (a−d) Output waveform as a function of V_{SL} and search time for four V_{th} levels of −0.025, −0.097, −0.168, and −0.253 V, respectively. (e) Output waveform for searching for the "10" state, along with match and mismatch case. (f) Output waveform concerning V_{SL} with shaded decision boundary for different bit levels.

close to V_{DD}, as shown in Figure 7e. So, the state "10" can be detected by applying a voltage within a narrow range of voltages close to V_{th3}. If $V_{SL} = V_{SL3}$, we get a match with the state "10". Otherwise, there is a mismatch. We can use a similar strategy to detect the other stored levels in the CAM cell. Note that the sense margin of V_{SL} for the stored levels should be optimized to maintain clear decision boundaries between different levels. For example, the output for the "10" state is high for both V_{SL3} and V_{SL2}, but the output is also high for the

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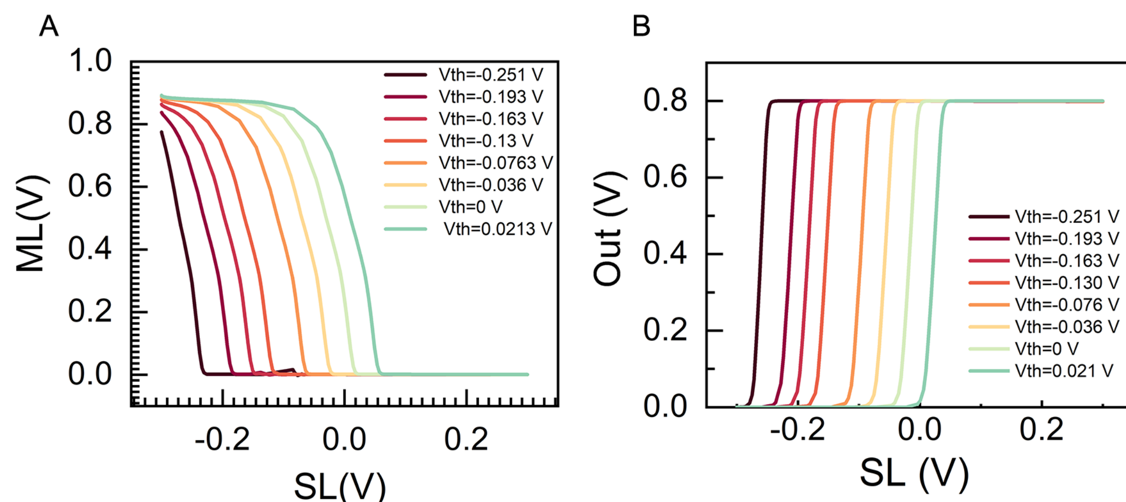

Figure 8. Retention degradation effect on (a) ML and (b) output voltage waveform by configuring different V_{th} state.

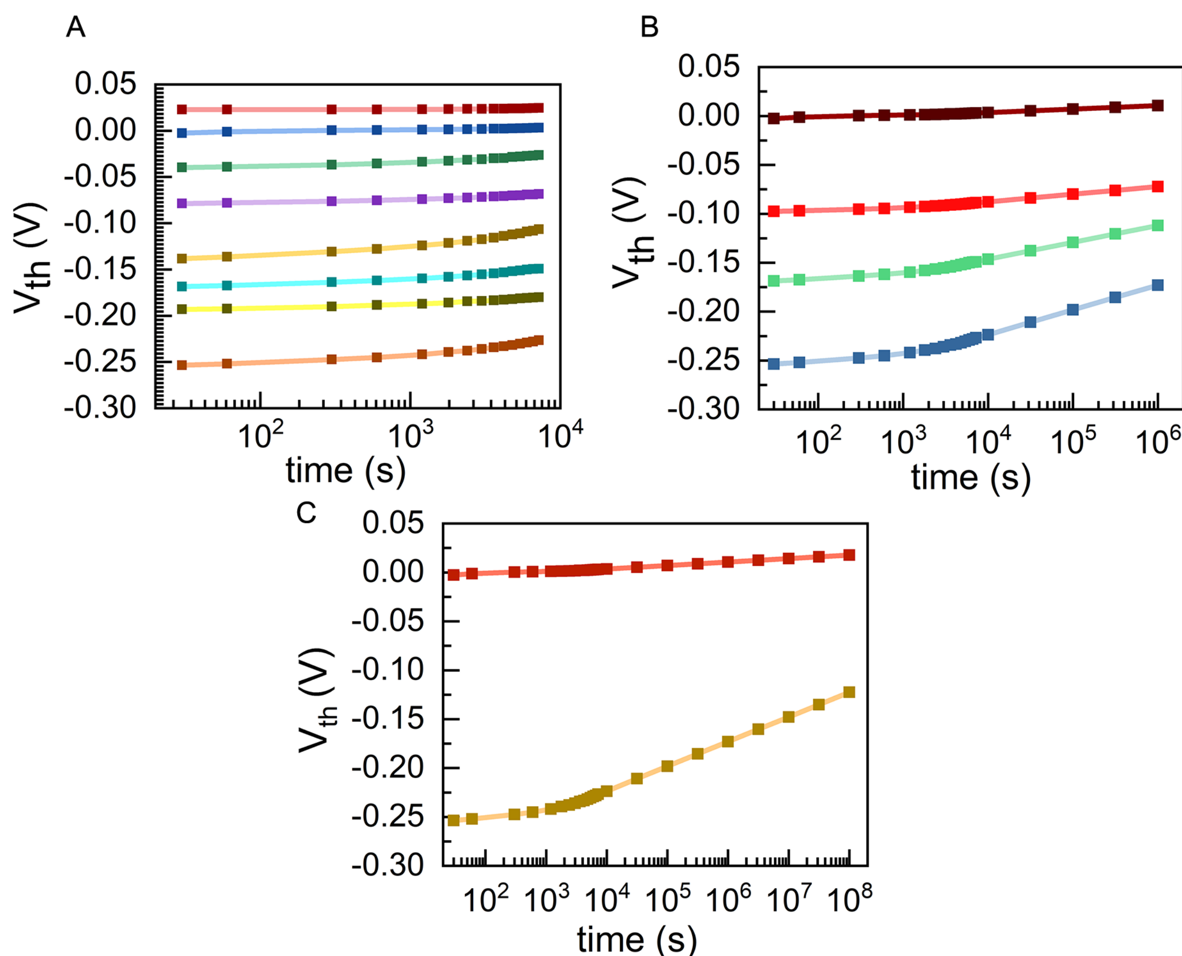

Figure 9. Retention measurements after programming to different intermediate states by using different pulse amplitudes: (a) 3 bits, (b) 2 bits, and (c) single bit.

"01" state at V_{SL2}. However, a value of V_{SL} close to V_{SL3} should be chosen to uniquely detect the state "10".

Impact of Retention Degradation. Retention degradation has been a significant challenge for FeFETs over several decades. The loss of retention over time is attributed to two main reasons: the presence of a depolarization field due to a finite capacitance in series with the ferroelectric layer and the gate leakage followed by trapping and detrapping effect in the interface layers in the gate stack.[50−52] Clearly, operation of a CAM cell can be affected because of this issue. If V_{th} of the FeFET in our CAM cell increases with time, the match line (ML) and the sensed output voltage with respect to V_{SL} will shift, as shown in Figure 8. If the output voltage shifts, the decision boundaries for searching different V_{th} levels will also

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change. Erroneous detection of the stored bits will occur when the V_{th} levels overlap. Figure 9 shows the experimental retention data of the IGZO-based FeFETs for 8 V_{th} levels (3 bits), 4 V_{th} levels (2 bits), and 2 V_{th} levels (1 bit), respectively. Retention for the 3 bit and 2 bit operations are reasonable up to 10^4 s and 10^6 s, respectively. The neighboring V_{th} levels overlap beyond the said time periods, and the multibit operation fails. We also observed that the single-bit operation shows excellent retention over 10 years, as shown in Figure 9c.

■ CONCLUSION

In this work, we have reported a 1FeFET-1T multibit CAM design to perform in-memory search and pattern matching for big-data applications. The operations are evaluated by exploiting the programmable multilevel states of IGZO-based FeTFT devices. Simulation shows that the proposed CAM has sufficient decision range to perform the search operations. We have also demonstrated the impact of retention degradation on the feasibility of the multibit operation in IGZO-based CAM cells. Our proposed CAM is highly promising for energy-efficient in-memory computing platforms compared with other solutions because of its simple one FeFET−one transistor architecture and multibit operation.

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Notes

The authors declare no competing financial interest.

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