micromachines

MDPI

Article

A CMOS-Thyristor Based Temperature Sensor with +0.37 °C/−0.32 °C Inaccuracy

Jing Li *, Yuyu Lin, Siyuan Ye, Kejun Wu, Ning Ning and Qi Yu

University of Electronic Science and Technology of China, Chengdu 610054, China; linyuyuchn@163.com (Y.L.); 18215521294@163.com (S.Y.); kjwu@uestc.edu.cn (K.W.); ning_ning@uestc.edu.cn (N.N.); qiyu@uestc.edu.cn (Q.Y.)

* Correspondence: lijing686@uestc.edu.cn

Received: 12 December 2019; Accepted: 21 January 2020; Published: 22 January 2020

Abstract: This paper describes a voltage controlled oscillator (VCO) based temperature sensor. The VCOs are composed of complementary metal–oxide–semiconductor (CMOS) thyristor with the advantage of low power consumption. The period of the VCO is temperature dependent and is function of the transistors' threshold voltage and bias current. To obtain linear temperature characteristics, this paper constructed the period ratio between two different-type VCOs. The period ratio is independent of the temperature characteristics from current source, which makes the bias current generator simplified. The temperature sensor was designed in 130 nm CMOS process and it occupies an active area of 0.06 mm^2. Based on the post-layout simulation results, after a first-order fit, the sensor achieves an inaccuracy of +0.37/−0.32 °C from 0 °C to 80 °C, while the average power consumption of the sensor at room temperature is 156 nW.

Keywords: temperature sensor; CMOS thyristor; VCO

1. Introduction

Temperature sensors are desirable for temperature sensing and compensation in modern applications, such as medical, environmental monitoring, thermal monitoring and wireless Internet-of-Things (IoT) platforms [1–3]. Most of such applications are battery powered for portability, durability or deployment flexibility [4,5], and put a strict power budget on temperature sensor which drives the power consumption to sub-μW and even to near-zero.

Prior works have demonstrated low-power-consumption temperature sensors based on bipolar junction transistors (BJT) [6–8], resistors [9,10], and complementary metal–oxide–semiconductor (CMOS) [11–16]. BJT-based temperature sensors converse the temperature by comparing a temperature-dependent voltage to a temperature-insensitive voltage or inversely temperature-dependent voltage. The voltage difference between these two voltages is quantized by a ΣΔ-ADC (Analog-to-Digital Converter), which achieves high resolution up to 0.002 °C and inaccuracy less than ±0.2 °C [6–8]. Resistor-based temperature sensors can achieve higher resolution and energy efficiency than BJT-based sensors. As discussed in Ref. [9], the authors use a temperature-dependent RC (Resistor and Capacitor) filter to extract the temperature information. In Ref. [10], the authors build a resistor based Wheatstone bridge whose voltage difference is proportional to the temperature. Both the temperature-dependent phase shift and voltage difference are sequentially digitized by ΣΔ-ADCs. ΣΔ-ADCs achieve high resolution at the cost of high power consumption and hardware cost from the decimation filter which normally are not mentioned in papers. Thus, the sacrifice of power consumption and hardware make BJT and resistor based temperature sensors not an optimal choice for battery powered applications. CMOS based temperature sensors are normally composed of digital delay cells. They are much more area efficient and easier to scale down with process. The authors in Ref. [13] demonstrate a VCO based temperature

sensor. The temperature information is extracted by two VCOs with different temperature-dependent frequency. The temperature sensor is fully composed of digital circuit and thus achieves an attractive area. On the other hand, the authors in Ref. [12] firstly create a temperature-dependent current and then transfer the current to frequency by VCOs. It provides better linearity and accuracy.

This paper proposes a VCO based temperature sensor and the VCO is composed of two-stage CMOS thyristor to simplify the circuit and achieve low power consumption.

2. Proposed CMOS Thyristor Based VCO

The proposed VCO is composed of multi-stage delay cells circled together. The desired oscillation frequency is inversely proportional to the number of stages and delay time of delay cell. Increasing the stages or delay time is necessary to reduce the oscillation frequency for low power consumption. Commonly, CMOS invertor is adopted as delay cell for its simplicity and scalability [12–16]. Its delay time is process dependent and ranges from ps to ns in sub-μm CMOS process. It may achieve μs delay by using the current-starved architecture but at the cost of large capacitors [14–16].

2.1. Basics of CMOS Thyristor Based Delay Cell

CMOS thyristor was proposed to increase the delay [17,18]. As shown in Figure 1, M_2 and M_4 work as a thyristor. M_3 and M_5 receive the input signal V_{IP} and V_{IN}, respectively, while V_{IN} is the complementary signal of V_{IP}. Current source I_{BN} is used to sink current from V_{ON} via switch M_1 according to the status of V_{IP}. C_0 is the total capacitance on node V_{ON}. When V_{IP} is low, M_5/M_3 are conducted and M_1 is non-conducted, V_{ON} and V_{OP} are reset to *VDD* and *GND*, respectively. When V_{IP} is changing to high, M_5/M_3 switch off and M_1 switches on. Current source I_{BN} starts sinking current from V_{ON} which results in node voltage decreasing from *VDD*. Approximately, M_4 conducts when V_{IP} reaches *VDD*-V_{thp}, where V_{thp} is the threshold voltage of M_4. After that, V_{OP} is charged from power supply *VDD* via M_4 and increased rapidly. Sequentially, M_2 conducts when V_{OP} reaches V_{thn} and discharges current from V_{ON} together with I_{BN}, where V_{thn} is the threshold voltage of M_2. It accelerates the node voltage decrease on V_{ON} and constitutes a positive feedback loop between M_2 and M_4. Once the positive feedback is built, V_{ON} and V_{OP} toggle to the opposite state in a short time. The corresponding delay value is calculated as [17]

$$td = \frac{C_0 V_{thp}}{I_{BN}} + \sqrt{\frac{6C_1{C_0}^2}{\kappa {I_{BN}}^2} V_{thn}} + \delta t \quad (1)$$

where the first term on the right is the delay contributed by discharging C_0, the second term is the delay contributed by charging C_1, and δt is the regeneration time of the CMOS thyristor. C_1 is the parasitic capacitance of V_{OP}. In reality, because of the subthreshold effect, M_4 charges the C_1 simultaneously with M_2 discharging C_0. The second term can be neglected. Comparing to the first term, the regeneration time δt is small and can be omitted. The delay value can be approximated as

$$td \approx \frac{C_0 V_{thp}}{I_{BN}} \quad (2)$$

Both adopting a larger capacitor C_0 and reducing sink current I_{BN} are effective to increase the delay value. Since C_0 generally adopts metal capacitor which is mostly temperature independent, the temperature coefficients are decided by the ratio of V_{thp}/I_{BN}.

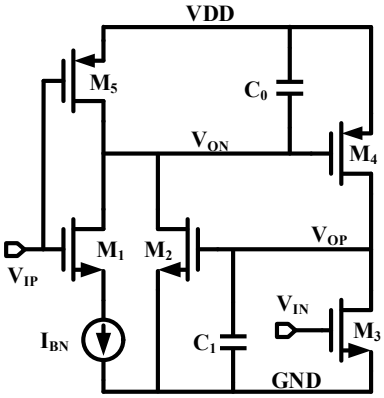


Figure 1. Complementary metal–oxide–semiconductor (CMOS) thyrsitor based delay cell.

2.2. Proposed CMOS Thyristor Based VCO

VCO is generally constituted by multiple stages (beyond three stages) to satisfy the desired frequency. The more stages it has, the more devices are required, which would consume more power and also deteriorate the wave performance. To simplify the circuit and reduce device counts, a two-stage ring VCO is proposed and shown in Figure 2. The delay cell is composed of the CMOS thyristor based delay cell aforementioned. In the proposed architecture, the negative output V_{ON1} of the first stage is connected to the negative input V_{IN} of the second stage and V_{OP1} is connected to V_{IP}. In this way, four-stage inversion is produced in the closed loop and thus makes it easy to satisfy the oscillation requirement of 360° phase shift.

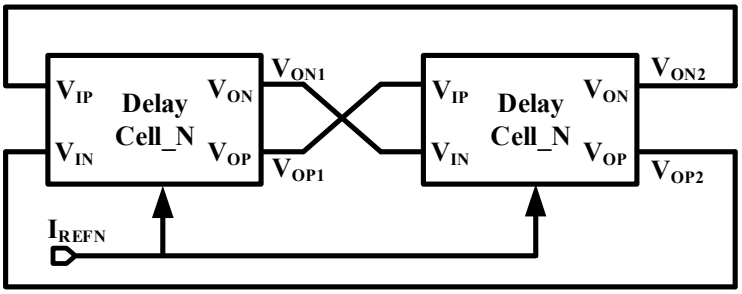


Figure 2. Proposed CMOS thyristor based voltage controlled oscillator (VCO).

Referred to the delay value of CMOS thyristor based delay cell in Equation (1), the oscillation period of the proposed VCO is given by

$$T_{VCO\_P} = \frac{2C_0V_{thp}}{I_{BN}} \tag{3}$$

3. Temperature Sensor Architecture

As shown in Figure 3, two types of VCO are adopted to constitute the proposed temperature sensor. At the top, P-type VCO is composed of Delay_Cell_Ps. The delay value of Delay_Cell_P is approximately the discharging time on V_{ON} via I_{REFN} according to aforementioned analysis. Referring to Equation (3), the period of P-type VCO is given as

$$T_{VCO\_P} = \frac{2C_0V_{thp}}{I_{REFN}} \tag{4}$$

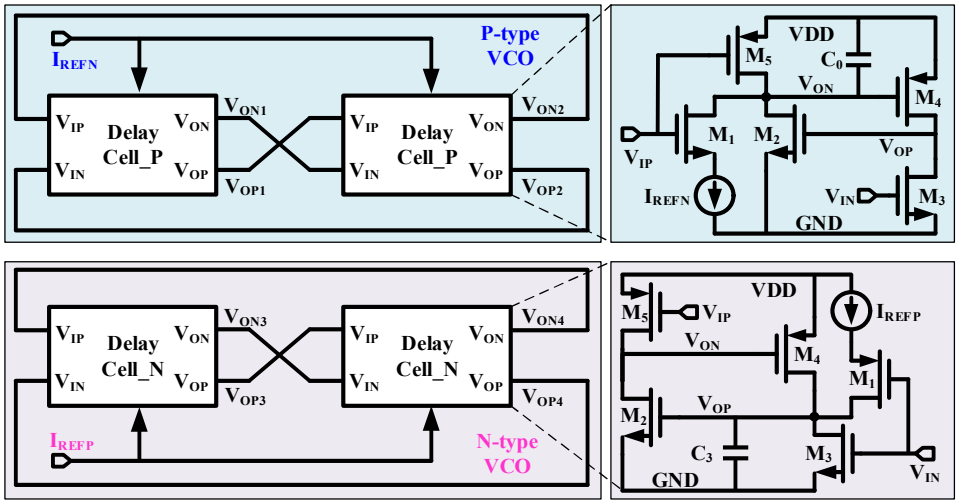


Figure 3. Proposed temperature sensor architecture.

Similarly, N-type VCO is composed of Delay_Cell_Ns. The delay value of Delay_Cell_N is approximately the charging time on V_{OP} via I_{REFP} according to aforementioned analysis. Referring to Equation (3), the period of N-type VCO is given as

$$T_{VCO\_N} = \frac{2C_3 V_{thn}}{I_{REFP}} \tag{5}$$

Based on Equations (4) and (5), the ratio between T_{VCO_P} and T_{VCO_N} is calculated

$$ratio\_T = \frac{T_{VCO\_P}}{T_{VCO\_N}} = \frac{C_0 I_{REFP}}{C_3 I_{REFN}} \frac{V_{thp}}{V_{thn}} \tag{6}$$

C_0 and C_3 are composed of metal capacitors, which are temperature independent. I_{REFP} and I_{REFN} come from the same current source and they will have the same temperature characteristics and value. Thus, the ratio can be updated as

$$ratio\_T \propto \frac{V_{thp}}{V_{thn}} \tag{7}$$

Because V_{thp} is temperature dependent to the first order [19], $ratio\_T$ is proportional to the temperature [13]. Thus, the ratio of the two-type VCO is used to detect temperature.

The complete block diagram of the proposed temperature sensor is shown in Figure 4. The left block is temperature sensor core which is composed of a P-type and a N-type VCO aforementioned. Bias current generator is used to provide the charging/discharging current I_{REFN}/I_{REFP}.

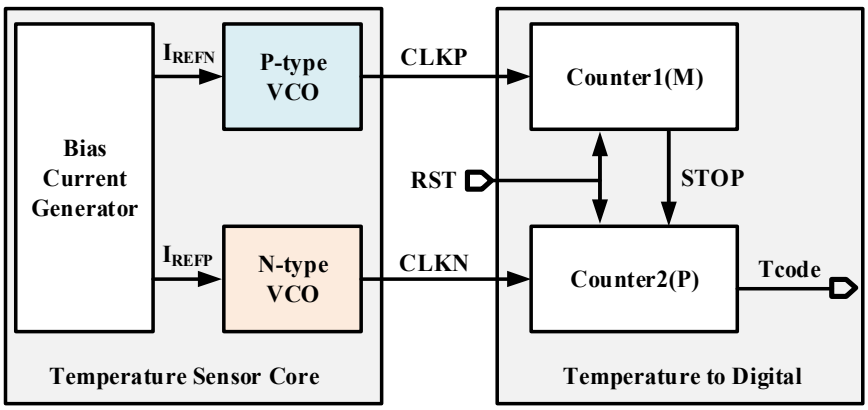


Figure 4. Block diagram of the temperature sensor.

The right block calculates the ratio between periods and transfers temperature to digital codes via two counters. The working principle of the *Temperature to Digital* is as follows. After *RST* switches to low, both counters start counting simultaneously. Counter1 counts *CLKP* to a constant value *M* and generates a flag signal *STOP*. When receiving *STOP* signal, Counter2 ends counting *CLKN* with a value of *P*. The counting time of both counters are equal and it can be expressed as

$$M \cdot T_{VCO\_P} = P \cdot T_{VCO\_N} \tag{8}$$

The ratio between periods can be obtained

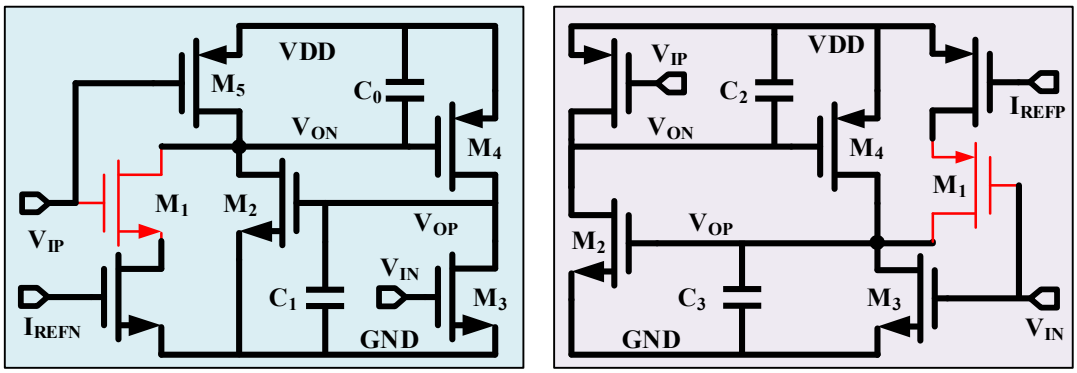
$$ratio\_T = \frac{T_{VCO\_P}}{T_{VCO\_N}} = \frac{P}{M} \tag{9}$$

Since *M* is a constant value, *P* represents the *ratio_T* and thus is proportional to the temperature. Eventually, *P* is converted to digital code of *Tcode* and output for measurement.

4. Circuit Implementation

4.1. Delay Cell

The detail of delay cell is shown in Figure 5. The bias current I_{REFP} and I_{REFN} are composed of NMOS and PMOS working in saturation region separately. The switches M_1 in both delay cells adopt thin-gate MOSFET to achieve fast switching and low conductive resistance. Considering the charging/discharging current of I_{REFP}/I_{REFN} on the magnitude of nA, all the others are thick-gate MOSFET to reduce influence of leakage current. Instead of just using C_0 and C_3 as what is shown in Figure 3, C_1 and C_2 are added to keep the load balance between Delay_Cell_P and Delay_Cell_N. MIM (Metal-Insulator-Meatal) capacitors are adopted for C_0-C_3 to maintain process and temperature independence.



(**a**) (**b**)

Figure 5. Detail of delay cell (**a**) Delay_Cell_P (**b**) Delay_Cell_N.

4.2. Bias Current Generator

Bias current could be designed with any kind of temperature characteristics, such as proportional, exponential, or independent [12,20]. It is hard to obtain a temperature dependent or independent current with outstanding linearity even at the cost of power or hardware. Instead of designing a high-linearity and temperature-dependent current generator, this paper adopted a simple current generator since the proposed temperature sensor is independent of I_{BN}. Figure 6 shows the architecture of the bias current generator.

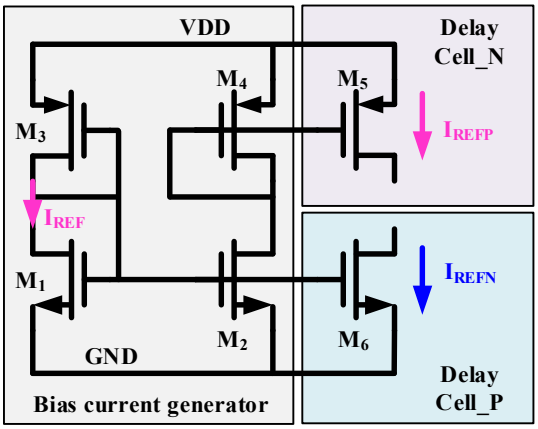


Figure 6. Bias current generator.

As described in Equation (6), I_{REFP} and I_{REFN} can be removed as long as they have the same temperature characteristics and magnitude. Thus, the bias current generator is simply composed of M_1-M_4. M_1 and M_3 work in sub-threshold region and provide the source current I_{ref}.

$$I_{ref} = \sqrt{\mu_p \mu_n C_{oxp} C_{oxn} \frac{W_p}{L_p} \frac{W_n}{L_n}} (m-1) {V_T}^2 \exp\left(\frac{V_{DD} - V_{thn} - V_{thp}}{2mV_T}\right) \quad (10)$$

where μ is mobility, C_{ox} is oxide capacitance, W is transistor width, L is transistor length, m is subthreshold slop factor, V_T is thermal voltage (kT/q), Vth is transistor threshold voltage and V_{DD} is the power supply voltage. The source current is mirrored to Delay_Cell_P and Delay_Cell_N for I_{REFN} and I_{REFP} respectively. According to Equation (6) and Equation (7), I_{REFP} and I_{REFN} should be of equal magnitude. Current mismatch between I_{REFP} and I_{REFN} will deteriorate the temperature linearity. To maintain the same magnitude of I_{REFP} and I_{REFN}, the optimal matching among current mirrors (M_1/M_2/M_6 and M_4/M_5) is required. Thus, the maximum length of 20 μm is adopted for the current-mirror MOSFETs. The current generator is of simple structure but suffers from the influence of the power supply. Thus, a stable and clean power supply is required.

4.3. Quasi-Static D-Flip Flop

The counters consist of two cascaded dividers (divide by two) which are composed of quasi-static D-Flip Flop for low power consumption (shown in Figure 7). Note that no risk presents in the glitches. The D-Flip Flop adopts dual-feedback loop to remove the impact from leakage. When the counting value of Counter1 reaches *M*, the input clock is blocked, and all dividers in Counter1 and Counter2 stop working and hold the states. Counting value *P* in Counter2 is output as *Tcode* for measurement.

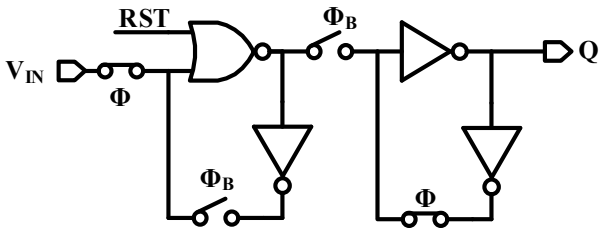


Figure 7. Quasi-static D-Flip Flop.

5. Simulation Results

The proposed temperature sensor was designed in 130 nm CMOS process. It does not need external voltage, current and frequency reference. The layout is shown in Figure 8 and the active area

is 0.065 mm^2. The power supply voltage is 1 V to achieve low power consumption while keeping the bias current generator working properly under all corners and temperatures. The bias current was set to 6 nA with oscillation periods about 240 µs under typical corner and room temperature. The average power is 156 nW at 27 °C while VCO consumes 89%, as shown in Figure 9.

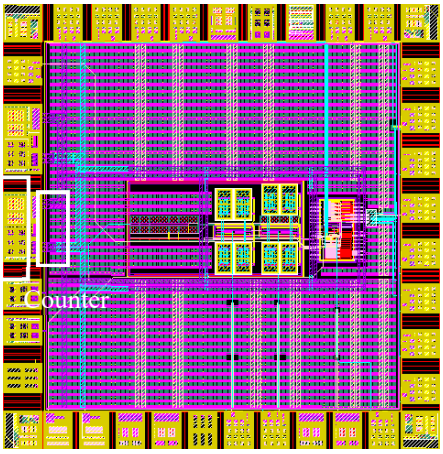


Figure 8. Layout.

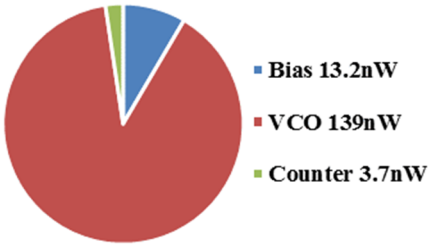


Figure 9. Power breakdown.

5.1. VCO Simulation

The proposed VCOs were designed and simulated. Figure 10 shows the simulated results. Since the bias generator works in sub-threshold region, the bias current has exponential relation to temperature. Accordingly, both VCO periods have exponential relation to temperature as shown in Figure 10a. Because of the threshold voltage difference between PMOS and NMOS, T_{VCO_P} is larger than T_{VCO_N}. *ratio_T* is shown in Figure 10b. It is inversely proportional to the temperature with an outstanding linearity which is in good accordance with the analysis in Equation (7).

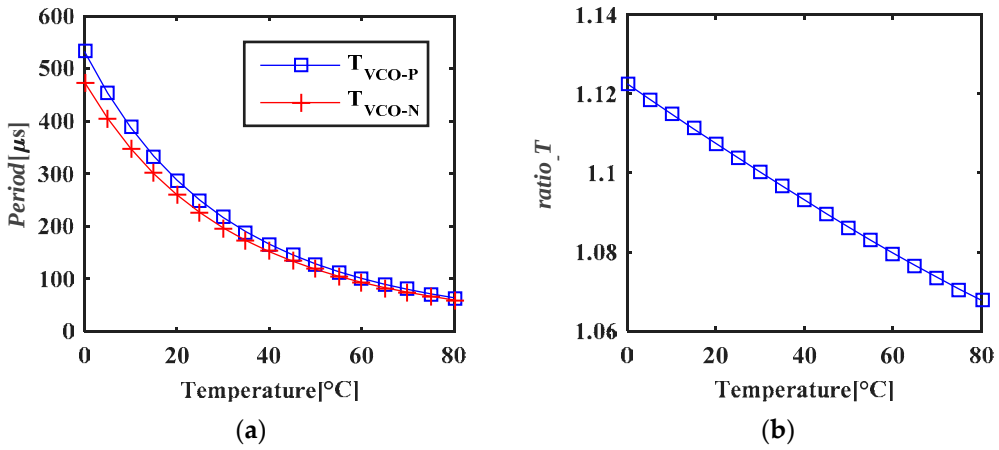


Figure 10. Simulated temperature performance of VCO (**a**) periods vs. temperature (**b**) *ratio_T* vs. temperature.

5.2. Temperature Sensor Simulation

As shown in Figure 10b, *ratio_T* changes slightly over the temperature range of 0 °C to 80 °C. To maintain a 10-bit level resolution, Counter1 is designed to be 14 bits. According to the Monte Carlo simulations, *ratio_T* is always greater than 1 but less than 2, so Counter2 is set to be 15 bits. The proposed temperature sensor is simulated from 0 °C to 80 °C. Both MOSFET mismatches and MIM capacitor mismatch are taken into account and verified with 20 Monte Carlo runs. The standard deviation of the transistors' mismatch and MIM capacitors' mismatch are 0.3% and 0.03%, respectively, which are provided by the foundry. Figure 11a shows a temperature error of +1.65 °C /−1.84 °C after 1st order polyfit. Figure 11b shows a temperature error of +0.57 °C /−0.44 °C after 2nd order polyfit.

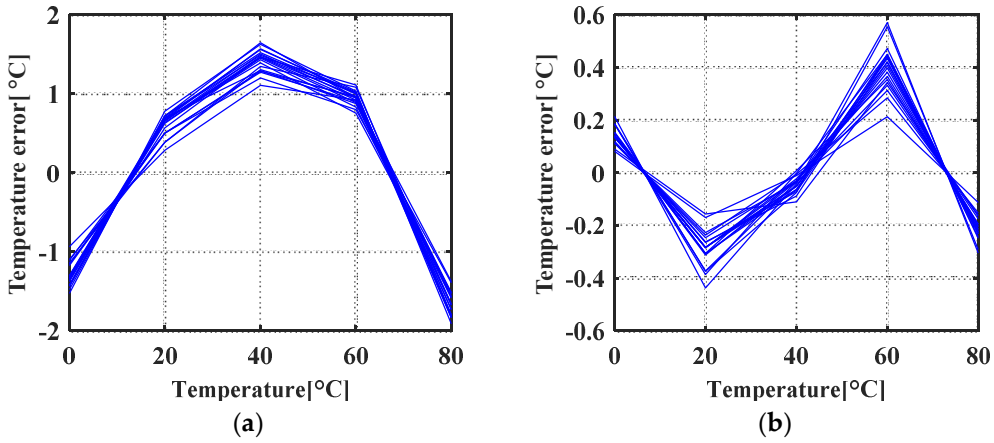


Figure 11. Simulated temperature error (**a**) after 1st order polyfit, (**b**) after 2nd order polyfit.

The proposed temperature sensor exhibits a systematic error profile dominated by the nonlinearity of *ratio_T* across the temperature range which is in good accordance with the analysis in Equation (7). After 1st order polyfit and the nonlinearity removal (Figure 12a), a maximum temperature error of +0.37 °C/−0.32 °C was observed across a 0 °C to 80 °C temperature range. After 2nd order polyfit and the nonlinearity removal (Figure 12b), a maximum temperature error of +0.17 °C/−0.19 °C was observed.

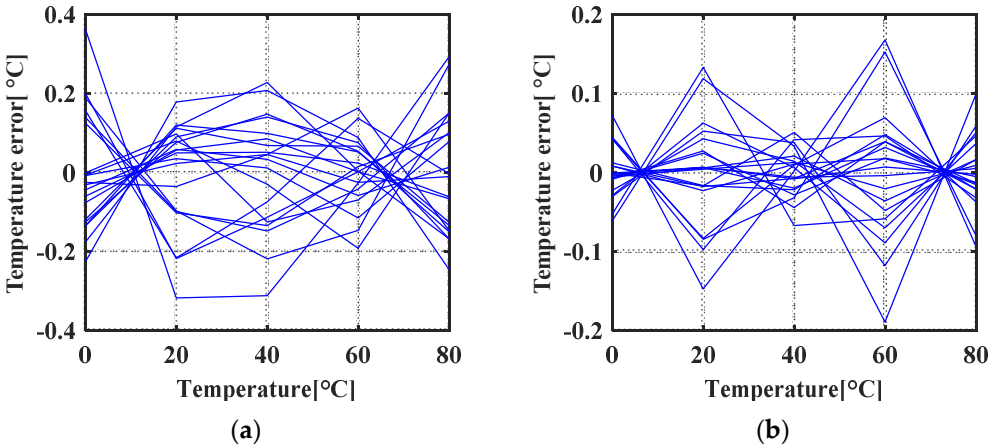


Figure 12. Simulated temperature error (**a**) after 1st order polyfit and systematic nonlinearity removal (**b**) after 2nd order polyfit and systematic nonlinearity removal.

The proposed temperature sensor was verified under corners. The results are shown in Figure 13. The SS corner shows the best performance while the worst performance can be observed in the FF (Fast-Fast) corner. This is because in the FF corner, the MOSFETs have the lowest threshold voltage. When we increase the reference current, the oscillation period reduces. That results in a worse approximation in Equation (2) and poor linearity.

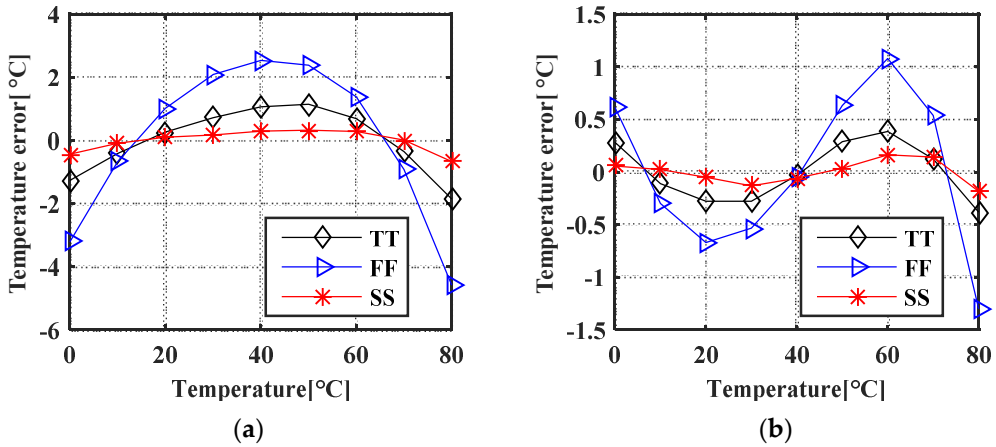


Figure 13. Simulated temperature error vs corners (**a**) after 1st order polyfit; (**b**) after 2nd order polyfit.

Table 1 compares the proposed sensor with the state-of-the-art temperature sensors. The proposed sensor does not need any external clock references or voltage regulators. It is designed with simple current mirrors and CMOS thyristors, and it achieves a competitive inaccuracy of +0.37/−0.32 °C and low power consumption of 156 nW within a compact area of 0.06 mm^2.

Table 1. Summarizes the performance of the proposed sensor.

	[13]	[12]	[11]	[21]	This Work *
Technology [nm]	65	180	180	65	130
Area [mm^2]	0.004	0.09	0.22	0.06	0.06
Supply Voltage [V]	0.85–1.05	1.2	1.2	1	1
External Clock	NO	NO	NO	YES	NO
Temperature Range [°C]	0–100	0–100	−20–80	0–100	0 to 80
Resolution [°C]	0.3	0.3	0.09	0.61	0.09
Conversion Time [s]	22×10^{-6}	30×10^{-3}	8×10^{-3}	10×10^{-6}–1	3.9
Power [nW]	154,000	71	570	488.3–0.17	156
Calibration	2-point	2-point	2-point	1-point	2-point
Inaccuracy [°C]	±0.9	+1.5/−1.4	±0.76	+1.5/−1.1	+0.37/−0.32

* Post layout simulation.

6. Conclusions

A CMOS thyristor based temperature sensor was proposed in this paper. Two VCOs composed of CMOS thyristor with different threshold voltage were exploited. The period ratio between two VCOs extracts the temperature information. The ratio calculation is simply realized by two counters where a constant-value counter stops another free running counter. Therefore, the external clock reference was avoided. A diode-connected bias current generator was exploited for its simplicity and little impact on the temperature extraction. The prototype was designed in 130 nm CMOS process and occupies an active area of 0.06 mm^2. According to the post-layout simulation, it achieves an inaccuracy of +0.37/−0.32 °C from 0 °C to 80 °C after 1st order polyfit and nonlinearity removal with a power consumption of 156 nW.

Author Contributions: Conceptualization, J.L.; Formal analysis, J.L.; Methodology, J.L.; Project administration, K.W.; Supervision, Q.Y.; Validation, J.L., Y.L. and S.Y.; Writing—original draft, J.L.; Writing—review & editing, N.N., Y.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Science and Technology on Analog Integrated Circuit Laboratory under project NO. JCKY2019210C057.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Floyd, M.; Allen-Ware, M.; Rajamani, K.; Brock, B.; Lefurgy, C.; Drake, A.J.; Pesantez, L.; Gloekler, T.; Tierno, J.A.; Bose, P.; et al. Introducing the adaptive energy management features of the Power7 chip. *IEEE Micro* **2011**, *31*, 60–75. [CrossRef]
2. Oshita, T.; Shor, J.; Duarte, D.E.; Kornfeld, A.; Zilberman, D. Compact BJT-based thermal sensor for processor applications in a 14 nm tri-gate CMOS process. *IEEE J. Solid State Circuits* **2015**, *50*, 799–807. [CrossRef]
3. Shim, D.; Jeong, H.; Lee, H.; Rhee, C.; Jeong, D.K.; Kim, S. A process-variation-tolerant on-chip CMOS thermometer for auto temperature compensated self-refresh of low-power mobile DRAM. *IEEE J. Solid State Circuits* **2013**, *48*, 2550–2557. [CrossRef]
4. Ha, S.; Akinin, A.; Park, J.; Kim, C.; Wang, H.; Maier, C.; Cauwenberghs, G.; Mercier, P.P. A 16-channel wireless neural interfacing SoC with RF-powered energy-replenishing adiabatic stimulation. In Proceedings of the 2015 Symposium on VLSI Circuits (VLSI Circuits), Kyoto, Japan, 17–19 June 2015; pp. C106–C107.
5. Wang, H.; Mercier, P.P. A 51 pW reference-free capacitive discharging oscillator architecture operating at 2.8 Hz. In Proceedings of the 2015 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 28–30 September 2015; pp. 1–4.
6. Pertijs, M.A.P.; Makinwa, K.A.A.; Huijsing, J.H. ACMOS smart temperature sensor with a inaccuracy of C from to 125 C. *IEEE J. Solid State Circuits* **2005**, *40*, 2805–2815. [CrossRef]
7. Aita, A.L.; Pertijs, M.A.P.; Makinwa, K.A.A.; Huijsing, J.H. A CMOS smart temperature sensor with a batch-calibrated inaccuracy of C from C to 130 C. In Proceedings of the 2009 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 8–12 February 2009; pp. 342–343.
8. Sebastiano, F.; Breems, L.J.; Makinwa, K.A.A.; Drago, S.; Leenaerts, D.M.W.; Nauta, B. A 1.2-V 10-µW NPN-based temperature sensor in 65-nm CMOS with an inaccuracy of 0.2 °C from 70° C to 125 °C. *IEEE J. Solid State Circuits* **2010**, *45*, 2591–2601. [CrossRef]
9. Pan, S.; Gürleyük, Ç.; Pimenta, M.F.; Makinwa, K.A.A. A 0.12 mm^2 Wien-Bridge Temperature Sensor with 0.1 °C (3σ) Inaccuracy from −40 °C to 180 °C. In Proceedings of the 2019 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2019; pp. 184–186.
10. Pan, S.; Makinwa, K.A.A. A Wheatstone Bridge Temperature Sensor with a Resolution FoM of 20fJ.K^2. In Proceedings of the 2019 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2019; pp. 186–188.
11. Yang, K.; Dong, Q.; Jung, W.; Zhang, Y.; Choi, M.; Blaauw, D.; Sylvester, D. A 0.6 nJ −0.22/+0.19 °C Inaccuracy Temperature Sensor Using Exponential Subthreshold Oscillation Dependence. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 5–9 February 2017; pp. 160–162.
12. Jeong, S.; Foo, Z.; Lee, Y.; Sim, J.Y.; Blaauw, D.; Sylvester, D. A fully-integrated 71 nW CMOS temperature sensor for low power wireless sensor nodes. *IEEE J. Solid State Circuits* **2014**, *49*, 1682–1693. [CrossRef]
13. Anand, T.; Makinwa, K.A.A.; Hanumolu, P.K. A VCO Based Highly Digital Temperature Sensor with 0.034 °C/mV Supply Sensitivity. *IEEE J. Solid-State Circuits* **2016**, *51*, 2651–2663. [CrossRef]
14. Lin, Y.S.; Sylvester, D.; Blaauw, D. An Ultra Low Power 1 V, 220 nW Temperature Sensor for Passive Wireless Applications. In Proceedings of the 2008 IEEE Custom Integrated Circuits Conference(CICC), San Jose, CA, USA, 21–24 September 2008; pp. 507–510.
15. Kim, C.K.; Kong, B.S.; Lee, C.G.; Jun, Y.H. CMOS Temperature Sensor with Ring Oscillator for Mobile DRAM Self-refresh Control. In Proceedings of the 2008 IEEE International Symposium on Circuits and Systems, Seattle, WA, USA, 18–21 May 2008; pp. 3094–3097.
16. Hwang, S.; Koo, J.; Kim, K.; Lee, H.; Kim, C. A 0.008 mm^2 500 µW 469 kS/s Frequency-to-Digital Converter Based CMOS Temperature Sensor with Process Variation Compensation. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2013**, *60*, 2241–2248. [CrossRef]
17. Kim, G.; Kim, M.K.; Chang, B.S.; Kim, W. A low-voltage, low-power CMOS delay element. *IEEE J. Solid State Circuits* **1996**, *31*, 966–971.
18. Saft, B.; Schäfer, E.; Jäger, A.; Rolapp, A.; Hennig, E. An Improved Low-Power CMOS Thyristor-Based Micro-to-Millisecond Delay Element. In Proceedings of the ESSCIRC 2014—40th European Solid State Circuits Conference (ESSCIRC), Venice Lido, Italy, 22–26 September 2014; pp. 123–126.
19. Tsividis, Y.P. *Operation and Modeling of the MOS Transistor*; McGraw-Hill: New York, NY, USA, 1987.

20. Wang, H.; Mercier, P.P. A 3.4-pW 0.4-V 469.3 ppm/°C Five-Transistor Current Reference Generator. *IEEE Solid State Circuits Lett.* **2018**, *1*, 122–125. [CrossRef]
21. Xin, H.; Andraud, M.; Baltus, P.; Cantatore, E.; Harpe, P. A 174 pW–488.3 nW 1 S/s–100 kS/s all-dynamic resistive temperature sensor with speed/resolution/resistance adaptability. *IEEE Solid State Circuits Lett.* **2018**, *1*, 70–73. [CrossRef]