MATERIALS SCIENCE

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Layer-resolved release of epitaxial layers in III-V heterostructure via a buffer-free mechanical separation technique

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Layer-release techniques for producing freestanding III-V epitaxial layers have been actively developed for heterointegration of single-crystalline compound semiconductors with Si platforms. However, for the release of target epitaxial layers from III-V heterostructures, it is required to embed a mechanically or chemically weak sacrificial buffer beneath the target layers. This requirement severely limits the scope of processable materials and their epi-structures and makes the growth and layer-release process complicated. Here, we report that epitaxial layers in commonly used III-V heterostructures can be precisely released with an atomic-scale surface flatness via a buffer-free separation technique. This result shows that heteroepitaxial interfaces of a normal lattice-matched III-V heterostructure can be mechanically separated without a sacrificial buffer and the target interface for separation can be selectively determined by adjusting process conditions. This technique of selective release of epitaxial layers in III-V heterostructures will provide high fabrication flexibility in compound semiconductor technology.

INTRODUCTION

Heterogeneous integration of materials is one of the important processing technologies for emerging electronic and optoelectronic applications such as monolithic three-dimensional (3D)–integrated circuit (IC) chips and high-performance flexible devices based on single-crystalline inorganic semiconductors. The cointegration of heterogeneous materials with dissimilar electrical and optical properties enables advanced device technologies with a broad spectrum of functionalities beyond the limitations of a single-material nature. In particular, the cointegration of compound semiconductor devices and Si-based ICs can offer an effective pathway for overcoming Si's poor light-emitting properties and ultimately realizing the monolithic integration of photonic circuits with complementary metal-oxide semiconductor (CMOS) ICs on a single chip (*1*–*3*). The simplest approach to this cointegration is to directly grow epitaxial layers of compound semiconductors on desired regions of an Si substrate. The compound semiconductors required for the cointegration with Si are typically GaAs- or InP-based III-V alloys such as InGaAs and InGaAsP, which are used for the fabrication of light sources and photodetectors in Si photonics (*4*). However, it is extremely difficult to epitaxially grow high-quality heterostructures composed of these compound semiconductors on an Si substrate because of a large lattice and thermal expansion coefficient (TEC) mismatch with Si(100) (*5*, *6*). For instance, the lattice/TEC mismatch of GaAs and InP with Si is approximately 3.9/128.1 and 8.0/73.1%, respectively, which induces a large density of dislocations and excessive strain upon the heterostructures (*6*, *7*).

As an approach without direct heteroepitaxy, layer release/transfer techniques for separating a thin layer of single-crystalline compound semiconductors and subsequently bonding it to arbitrary substrates have been actively developed at the industrial scale because this approach can enable a versatile combination of various semiconductors for heterointegration without the limitations of lattice and TEC mismatch. One of the commonly used processes is epitaxial lift-off (ELO) and its variant techniques. The most typically used ELO process is a chemical lift-off technique. For this process, a chemically weak layer is first grown as a sacrificial buffer during a heterostructure epitaxy step, and the weak layer is then selectively etched away for the release of the epitaxial layers on top of the buffer (*8*–*10*). Although this process has been widely used to fabricate thin, flexible, and 3D-integrated structures, it can only be applied to epitaxial heterostructures with extremely high etching selectivity between the sacrificial buffer and other layers and has limitations in high-throughput wafer-scale processes because of the slow lateral etching rate of the sacrificial buffer (*11*). Another type of the ELO process is a mechanical lift-off technique. For this process, a mechanically weak defective or porous sacrificial buffer is first formed within a heterostructure, and the sacrificial buffer is then physically broken for the layer release (*12*, *13*). This is a much faster process than the chemical lift-off technique. However, the formation of the mechanically weak buffer in the heterostructure makes the growth process very complicated and limits the crystal quality of single-crystalline epitaxial layers grown on the buffer. In addition, this process is also allowed only for the limited scope of III-V materials and epitaxial structures. Recently, a graphene-assisted layer release/transfer technique has been suggested (*14*–*16*). This technique is based on remote epitaxy allowing the growth of single-crystalline compound semiconductor layers on a graphene buffer, which thereby enables facile layer release from the graphene surface because of

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its weak van der Waals bonding. Although this technique has been widely applied for the cointegration of various heterogeneous materials, for industrial adoption, it is still necessary to improve the processes for the growth and transfer of large-scale defect-free graphene layers because the process yield depends on the quality of transferred one- or few-monolayer graphene (*16*).

As an alternative approach without using a sacrificial buffer, a mechanical separation technique called thickness-controlled spalling has been actively studied because it enables the fast and kerf-less release of wafer-scale semiconductor layers through a relatively simple and low-temperature process (*11*, *17*–*31*). In this process, a thin single-crystalline semiconductor layer is mechanically released by the stress induced from a stressor film (typically, Ni) deposited on the substrate. Because the spalling process of semiconductors relies on the mechanical separation of crystal planes in the single-crystalline substrates, a thin-layer release is possible without a sacrificial buffer. Moreover, the thickness of the released layer can be controlled from hundreds of nanometers to tens of micrometers by adjusting the thickness and stress of the Ni film. On the basis of these advantages, the thickness-controlled spalling technique has been applied to a wide range of materials from elemental semiconductors (*11*, *17*–*24*, *30*, *31*) to compound semiconductors (*21*, *25*–*29*). In particular, this technique has been effectively used in device fabrication with a thin layer of elemental semiconductors (Si and Ge). For instance, flexible logic and memory ICs based on sub–30-nm CMOS technology (*17*–*20*), wearable/stretchable sensors (*30*, *31*), and thin-film photovoltaic cells (*21*–*24*) for flexible applications have been demonstrated using Si or Ge spalling processes. In practice, the greater potential of this buffer-free mechanical separation technique is derived from the layer release of compound semiconductors, which enables the versatile heterointegration of III-Vs and Si. However, it is known that this technique has a critical issue for applying to III-V semiconductors. In contrast to elemental semiconductors, the spalling process for zinc-blende (100) compound semiconductors such as GaAs- or InP-based III-Vs leaves zigzag corrugations on the surface of the released III-V layers and substrates because of the undulating crack propagation along the {110} planes (*21*, *25*–*28*). It has been reported that the height and pitch of the corrugations can be as large as several to tens of micrometers (*21*, *27*). This is a substantial problem that limits practical applications of this buffer-free mechanical separation technique to cointegration of III-V and Si devices because the nonflat surface impedes the subsequent transfer of the released layer and the continuous reuse of the substrate.

In this study, we propose a layer-resolved mechanical separation technique that can precisely release target III-V epitaxial layers from a single-crystalline heterostructure without a sacrificial buffer. This technique is based on mechanical exfoliation at the epitaxial interface of a heterostructure and allows the release of single-crystalline III-V layers with an atomically flat surface. To demonstrate this technique, we epitaxially grow a lattice-matched heterostructure with multiple InP/InGaAs junctions on an InP(100) wafer and show that the epitaxial layers can be released at a specific junction of the heterostructure. Furthermore, we demonstrate that the target junction for separation can be selectively determined by controlling the strain energy induced by the Ni stressor film. Structural characterizations based on energy-dispersive x-ray spectroscopy (EDS), Raman spectroscopy, and atomic force microscopy (AFM) measurements prove that layer release occurs precisely at junctions between the InGaAs and InP epitaxial layers and the surface of the released layers is atomically flat. Last, we confirm the effect of the proposed layer-release process on crystal and material quality by measuring high-resolution x-ray diffraction (XRD) and photoluminescence (PL) characteristics after the transfer of the released InP/InGaAs epitaxial layers onto an Si substrate.

RESULTS

Layer release of III-V compound semiconductors

Thickness-controlled spalling technique and its mechanism for layer release of single-crystalline semiconductors are summarized in the Supplementary Materials (fig. S1 and note S1). As reported in the literature, it can be observed that the spalling process for zinc-blende III-V(100) compound semiconductors such as GaAs(100) and InP(100) leaves zigzag corrugations on the surface of the released layers, unlike the spalling process for elemental semiconductors. The origin of the formation of the corrugations in III-V(100) spalling could be explained by undulating crack propagation along the {110} planes (*25*, *27*, *28*), as shown in Fig. 1A. In the spalling of (100) semiconductors, the (100) plane is oriented parallel with the "local symmetry plane" where the mode-II stress intensity factor (K_{II}, in-plane shear mode) is zero (i.e., $K_{II} = 0$). However, in the case of III-V(100), the crack is inclined to deviate from the local symmetry plane to grow on the (110) plane because the surface energy of the (100) plane is considerably higher than that of the (110) cleavage plane (*32*, *33*). As the crack grows off from the local symmetry plane, the magnitude of K_{II} grows from 0, and K_{II} at the crack tip evolves to act in a way of stabilizing the crack path (i.e., inducing the crack to grow back toward the local symmetry plane with a decrease in its magnitude). When K_{II} decreases back to 0, the crack deviates from the local symmetry plane again to grow on the ($\bar{1}10$) plane. This directional change of the crack is repeated alternatively with respect to the local symmetry (100) plane. Thus, after successive directional changes of the crack, the periodic zigzag corrugation is formed at the released surface. To investigate the surface structure of the released III-V(100) layers, we fabricated thin GaAs and InP layers with various layer thicknesses. First, as expected from the suggested theory, there was correlation between the peak-to-peak height and pitch of the zigzag corrugations on the released layers. Half of the zigzag pitch was directly proportional to the zigzag height over the entire released region, as shown in Fig. 1B; this indicates that the facet of the corrugation is composed of {110} cleavage planes. This result supports the idea that the corrugations originate from the surface-energy contrast between the (100) and (110) crystal planes. Second, we observed that the height of the zigzag corrugations was dependent on the released-layer thickness. In our study, the zigzag height was approximately 1.2 times larger than the released-layer thickness in its range from 2 to 13 μm (Fig. 1C). This result suggests one simple approach to minimizing zigzag corrugations, that is, releasing the III-V(100) layer as thin as possible. However, the practical problem is that the minimum spalling depth (released-layer thickness) guaranteeing the reliability of this process is typically limited to 1 to 2 μm (*11*, *20*). When the Ni film is too thin, it is difficult to initiate a crack. Last, the local nonuniformity of the film stress and undesirable external force can cause nonuniform crack propagation. Thus, it may be difficult to remove the surface corrugation by engineering the process conditions, and this issue limits practical applications of the spalling process because of the

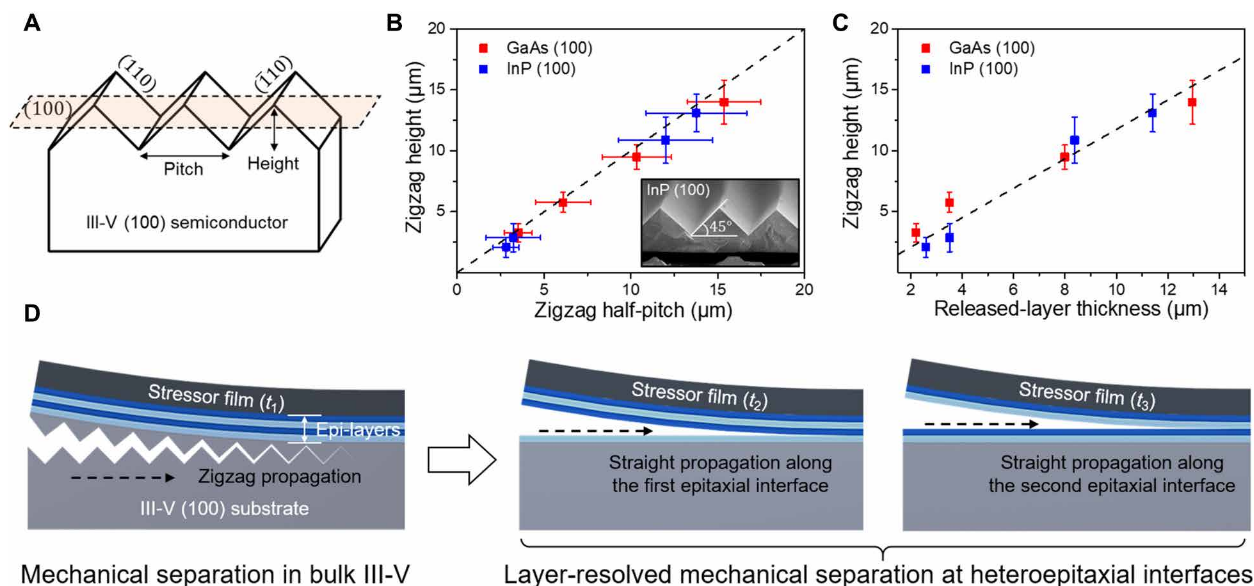

Fig. 1. Formation of zigzag corrugations in a bulk III-V(100) and layer-resolved mechanical separation for III-V heterostructures. (**A**) Crystallographic planes of zigzag corrugation formed in the spalling of a bulk III-V(100) semiconductor. The corrugation originates from undulating crack propagation along the {110} planes because of the surface-energy contrast between the (100) and (110) crystal planes. (**B**) Correlation between the height and half-pitch of the zigzag corrugations on the released GaAs(100) and InP(100) layers, confirming that the facets of the corrugations are composed of {110} cleavage planes. (**C**) Peak-to-peak height of the zigzag corrugations increases along with the thickness for both the released GaAs(100) and InP(100) layers. (**D**) A schematic of the proposed layer-resolved mechanical separation technique. By matching the location of the local symmetry plane (where $K_{II} = 0$) with a specific interface of an epitaxial heterostructure, a crack can propagate straightly along the junction between heteroepitaxial layers because of the relatively weak surface energy at the interface. The target junction for layer release in the heterostructure can be selectively determined by controlling the strain energy induced by the stressor film.

difficulty with the transfer of the released III-V layers and the continuous reuse of substrates (fig. S2 and note S2).

Layer-resolved mechanical separation technique for III-V heterostructures

As an alternative approach, based on the results and mechanism of the III-V(100) spalling, we designed a layer-resolved mechanical separation process for III-V heterostructures. The zigzag corrugations originate from the fact that the surface energy of the local symmetry (100) plane is significantly higher than that of another crystal plane, i.e., the (110) plane. This means that the spalling of III-V compound semiconductor layers with a flat surface and a uniform thickness may become possible if we can find a condition in which the surface energy of the local symmetry plane is less than that of the (110) plane. To achieve this condition, our approach is to match the location of the local symmetry plane (i.e., spalling depth) to a covalent-bonded epitaxial interface in a III-V heterostructure composed of multiple epitaxial layers. The reason is that the surface energy (i.e., crystal binding energy) of an epitaxial interface in III-V heterostructures can be reduced by the misfit-induced strain energy. In cases of lattice-mismatched heterostructures, a strong misfit strain is induced between the heteroepitaxial layers, and furthermore, localized dislocations and defects are often introduced into the crystals near the epitaxial interface (*5*–*7*, *16*). Even in lattice-matched heterostructures, it is known that an abruptly inverted heteroepitaxial interface contains at least one or few monolayers of undesirable lattice-mismatched III-V alloy, which is induced by phase intermixing because of interdiffusion of atoms or memory effects of precursors (*34*–*41*). For instance, compressive-strained InAs and InAsP or tensile-strained InGaP layers are formed at the heteroepitaxial interface of the lattice-matched $InP/In_{0.53}Ga_{0.47}As$ heterostructure (*38*–*41*). Thus, as the localized misfit strain energy is introduced at the epitaxial interface, the surface energy of the (100) plane aligned with the strained interface layers can be reduced to less than that of the (110) plane, and thereby, the (100) interface plane becomes preferable to the (110) plane for the layer release in spalling processes. The reduction in crystal binding energy at a heteroepitaxial interface of lattice-matched heterostructures can also be predicted from a simple binding-energy calculation on the basis of density functional theory (see fig. S3 and note S3 for calculation results of the representative lattice-matched III-V heterostructures, InP/InGaAs, and GaAs/InGaP).

Because III-V semiconductors are typically grown as an epitaxial heterostructure rather than as a bulk for device applications, if this process is viable, then it would enable a versatile III-V spalling technique capable of selectively releasing single-crystalline III-V layers of interest from a heterostructure. The concept of this process is illustrated in Fig. 1D. Crack propagation is not straight when the local symmetry plane is located in the bulk substrate; however, if the location of the local symmetry plane is matched to one of the hetero-interfaces (i.e., junctions between heteroepitaxial layers) that are covalently bonded, then layer release can occur at a specific junction via a straight crack propagation along the relatively weak local symmetry plane. Furthermore, the target interface to be separated in the multiple epitaxial layers can be selectively determined by controlling the strain energy from the stressor film.

To demonstrate the proposed layer-resolved mechanical separation technique, we first grew a III-V heterostructure composed of lattice-matched multiple $InP/In_{0.53}Ga_{0.47}As$ epitaxial layers on an InP(100) wafer using a metalorganic chemical vapor deposition

(MOCVD) system. This structure is one of the commonly used heterostructures for fabricating a near-infrared–sensitive *p*–*i*–*n* photodiode (*42*, *43*). The epitaxial layer structure is shown in Fig. 2A. To verify the layer selection capability of the proposed technique, we designed process conditions to set the local symmetry plane at three different locations in the heterostructure. The first process condition corresponds to that in which layer release occurs in the bulk substrate (process I). The other process conditions are designed to match the location of the local symmetry plane to one of the interfaces between the heteroepitaxial layers (processes II and III). The locations of the local symmetry planes in processes I, II, and III are denoted in Fig. 2A. In process II, the local symmetry plane is set to the junction between the *n*-InGaAs and *n*-InP layers. In process III, the local symmetry plane is set to another junction, the epitaxial interface between the *n*-InP and *i*-InGaAs layers. To establish detailed experimental conditions for the three layer-release processes, it is essential to estimate the correlation between the spalling depth and the strain energy determined by the thickness and stress of the Ni stressor film. Thus, we first measured the internal stress of the Ni film with varying Ni thicknesses using a multibeam optical sensor system (*44*) and calculated the strain energy accumulated in the substrate as a function of the Ni thickness (Fig. 2B). This result shows that the strain energy can be controlled by adjusting the Ni thickness. Then, the estimated spalling depth was calculated as a function of the Ni thickness using an analytical model based on delamination theory (*11*, *45*–*47*). In this model, the spalling depth is determined from the thermodynamic equilibrium condition in which the total strain energy accumulated in the Ni film and the released layer is balanced with the crystal binding energy of a (100) plane (see fig. S4 and note S4 for details of the analytical model and calculation procedure).

The calculated spalling depth is shown by the solid line in the plot of Fig. 2C. From this analytical calculation, we estimated the Ni thickness for processes II and III to be ~3.5 and 3 μm to match the spalling depth to two different junction depths. For process I, we set a thicker Ni thickness (7 μm) to guarantee that the layer release occurs in the InP bulk. On the basis of these estimates, we released the III-V epitaxial layers using the Ni stressor films with various Ni thicknesses and found out that release of the layers with a flat and uniform surface at specific junctions was possible when the Ni

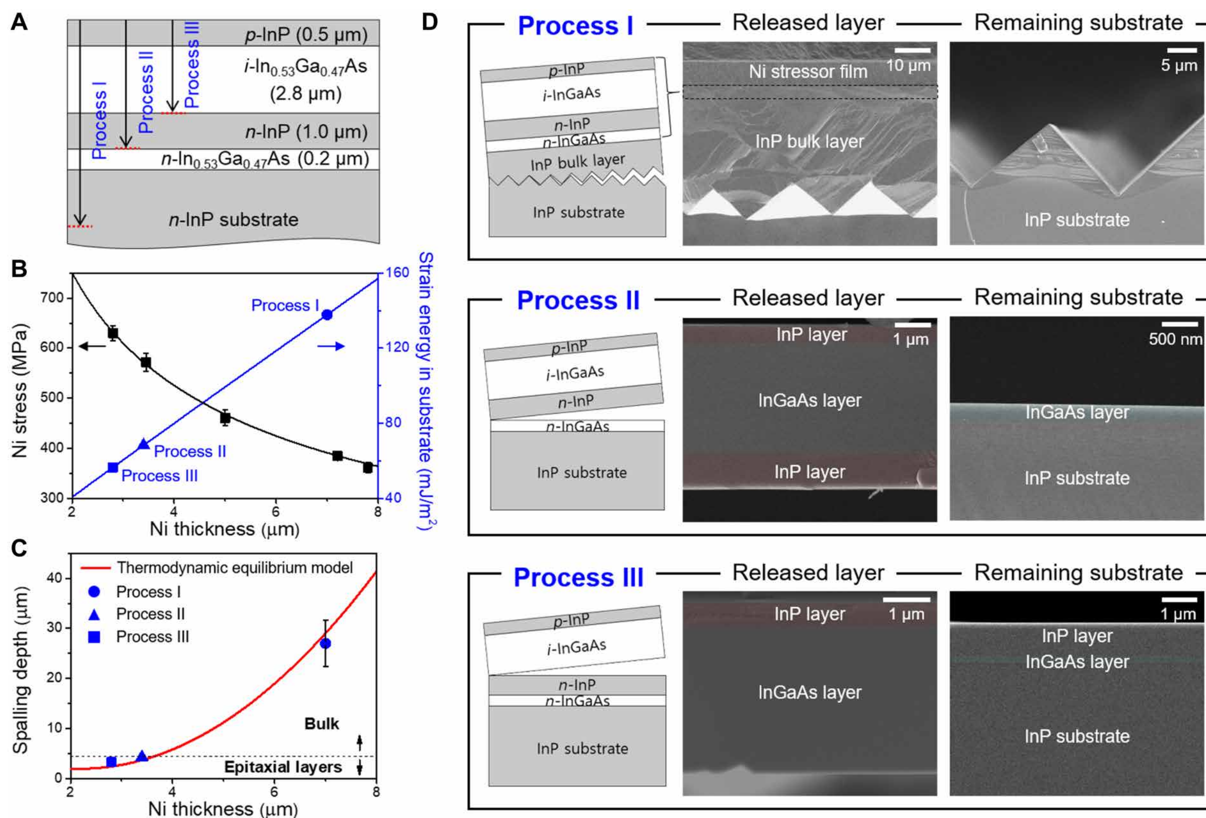

Fig. 2. Selection of target junctions for layer release in an InP/InGaAs heterostructure by controlling the strain energy induced by the Ni stressor film. (**A**) A schematic of the epitaxial heterostructure with multiple InP/InGaAs junctions used in this study. Processes I, II, and III denoted in the schematic indicate layer-release processes with three different locations of local symmetry planes (dashed red lines). Process I corresponds to a process condition for layer release in the bulk substrate. Processes II and III correspond to process conditions that are designed for the release of the epitaxial layers at different InP/InGaAs junctions. (**B**) Internal stress of the Ni film and the strain energy accumulated in the substrate as a function of the Ni thickness, showing that strain energy can be controlled by adjusting the Ni thickness and stress. (**C**) The estimated spalling depths of the layers as a function of the Ni thickness (red solid line) calculated from an analytical model on the basis of the thermodynamic equilibrium condition between the stress-induced strain energy and the crystal binding energy. Dots in the plot indicate the empirical results for processes I, II, and III, showing good agreement with the estimates obtained by the analytic model. (**D**) Cross-sectional scanning electron microscopy (SEM) images of the released layers and the remaining substrates after processes I, II, and III. These show that the epitaxial layers released at the InP/InGaAs junctions are flat and the target junction for layer release can be controlled by the strain energy induced by the Ni stressor film, whereas the surface of the layer released in the InP bulk exhibits the zigzag corrugation.

thickness was 3.2 μm for process II and 2.8 μm for process III. When we deposited 7-μm-thick Ni, the spalling occurred in the bulk with a released-layer thickness of 28 μm, as expected. The released-layer thicknesses (spalling depths) in processes I, II, and III are shown by the dots in Fig. 2C. The empirical results showed good agreement with the estimates by the analytic model. The cross-sectional scanning electron microscopy (SEM) images of the released layers and the remaining substrate after the three processes are shown in Fig. 2D. (The SEM images obtained with different magnifications are shown in fig. S5.) Process I with thick Ni film left zigzag corrugation on the surface of the released layer and the substrate because the layer release occurred in the bulk. On the other hand, the SEM images show that the surfaces of the released layers after processes II and III were flat, and the images indicate that the layer release occurred, respectively, at the target InP/InGaAs junctions because the thicknesses of the epitaxial layers in the released layers and remaining structures were the same as the junction depths of the heterostructure. In the SEM images, the color and brightness of the relatively thin epitaxial layers have been adjusted to make them more visible (see fig. S6 for the original SEM images). From the surface images taken after the spalling, we could also estimate the yield of the layer release at the heteroepitaxial interface. The estimated yield was about 78% (see fig. S7 and note S5 for details of the yield estimation). In addition, we could evaluate the thickness uniformity by measuring the released surface morphology after processes II and III over the entire region of the spalled sample (sample size of 15 × 15 mm^2). The results indicate that both processes II and III enabled uniform layer release at the target heteroepitaxial interfaces (i.e., local symmetry planes we designed) in the large area of the sample (>12 × 12 mm^2) except for the sample edge regions (figs. S8 and S9).

Characterizations of the layer-resolved mechanical separation technique

We investigated the elemental compositions and structural information of the layers to confirm that layer release occurred at the target junctions between the InGaAs and InP epitaxial layers (Fig. 3). Cross-sectional SEM images and EDS elemental-mapping images (P, In, Ga, and As) of the released epitaxial layers and the remaining substrates are shown in Fig. 3 (A and B) for processes II and III, respectively. Because process II was designed to separate the interface between *n*-InP and *n*-InGaAs, the released structure was composed of three epitaxial layers (InP/InGaAs/InP), as could be observed from the SEM image. The elemental-mapping image of the released layer is clearly divided into three different regions. As shown in Fig. 3A, the Ga and As composition signals are depleted in the top

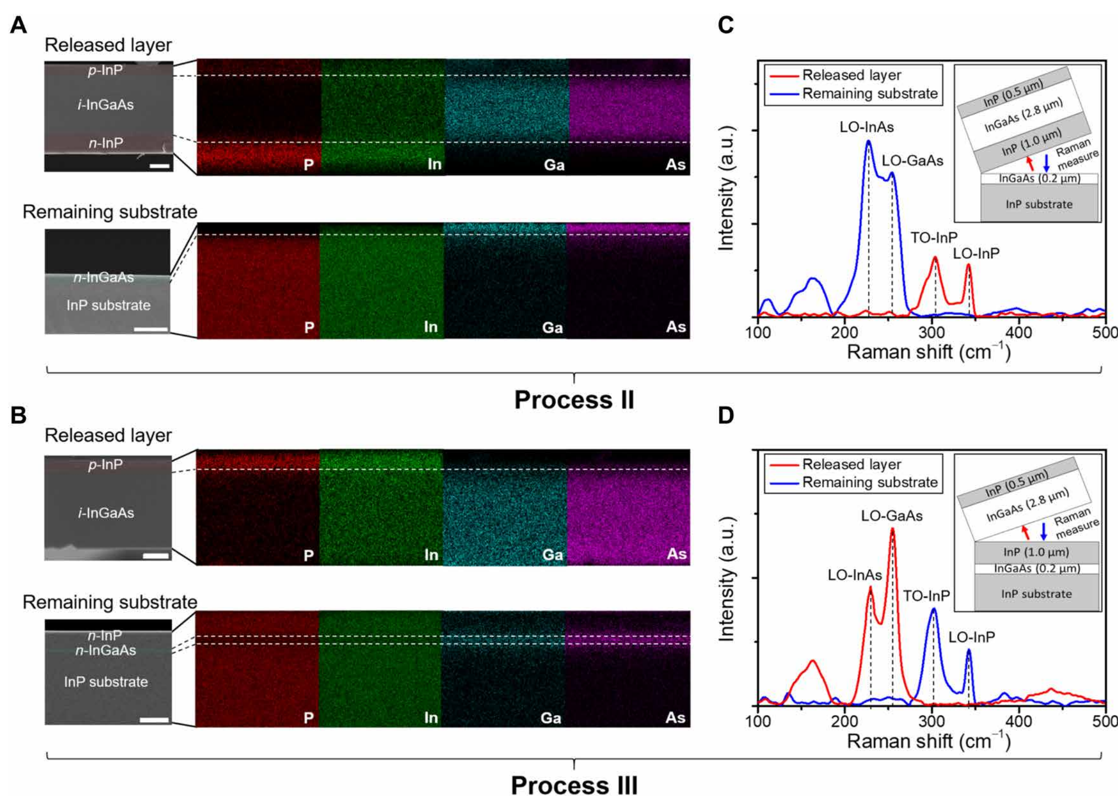

Fig. 3. Confirmation of layer-resolved release of epitaxial layers at different InP/InGaAs junctions. (**A** and **B**) Cross-sectional SEM images and EDS elemental-mapping images of the released layer and the remaining substrate after (A) process II and (B) process III. Scale bars, 1 μm. The spatial distributions of the P, In, Ga, and As signals of EDS agree well with the elements of each epitaxial layer. The dashed lines indicate the interfaces between the heteroepitaxial layers determined from the SEM images. (**C** and **D**) The Raman spectra measured from the surface of the released layer (red arrows in the insets) and the remaining substrate (blue arrows in the insets) after (C) process II and (D) process III. The spectra with the InP-like LO and TO mode peaks indicate InP surfaces, and those with the InAs-like LO mode and GaAs-like LO mode peaks correspond to InGaAs surfaces. This result shows that the epitaxial layers are precisely released at the different target InP/InGaAs junctions of the heterostructure via processes II and III. a.u., arbitrary units.

and bottom regions, and the P signal is depleted in the middle region of the released layer while the P composition signal is depleted in the thin top region of the remaining substrate. In the case of process III, the released layer is composed of two epitaxial layers (InP/InGaAs), and the remaining substrate has two epitaxial layers on the InP bulk. This compositional structure can be also confirmed by elemental-mapping images for process III (Fig. 3B). The P signal is depleted in the bottom region of the released layer, while the Ga and As signals are depleted in the top of the remaining substrate. For more rigorous confirmation, we analyzed the III-V structure of the released layers and the remaining substrates by measuring Raman spectroscopy on their surfaces after layer release by processes II and III. Figure 3C shows the Raman spectra for process II. The two primary peaks of the Raman spectrum measured on the surface of the released layer correspond to the InP-like longitudinal optical (LO) mode and transverse optical (TO) mode (*48*). The main peaks observed on the surface of the remaining substrate correspond to the InAs-like LO mode and the GaAs-like LO mode (*49*, *50*). On the other hand, the Raman spectra for process III indicate that the main peaks on the released layer correspond to the InAs-like LO mode and the GaAs-like LO mode, and those on the substrate correspond to the InP-like LO and TO modes (Fig. 3D). These results clearly confirm that spalling process II released the InP/InGaAs/InP epitaxial layer and process III released the InP/InGaAs epitaxial layer. The important aspect of these results is that the proposed process can enable a III-V spalling technique that can selectively release single-crystalline epitaxial layers of interest from a III-V heterostructure wafer by controlling the strain energy induced by the Ni film. Last, to confirm the presence of an intermixing layer that plays a dominant role in enabling the flat and uniform layer release at the target epitaxial interfaces, we performed transmission electron microscopy (TEM) and additional Raman analysis on the interface between InP and InGaAs layers. High-resolution TEM images and the additional Raman investigation showed the lattice-matched InP/InGaAs heterostructure contains an intermixing layer with a two- or three-monolayer thickness at the epitaxial interface between InP and InGaAs layers (fig. S10).

To confirm whether the proposed layer-release technique can be applied to practical applications, we transferred the released layer onto a Si(100) substrate and investigated the crystal and material qualities of the transferred epitaxial layers (Fig. 4). The transfer process was performed by a spin-on-glass process with a tetraethyl orthosilicate (TEOS)–based SiO_x-bonding layer (*51*, *52*). Because the surface of the layer released by the proposed technique was flat,

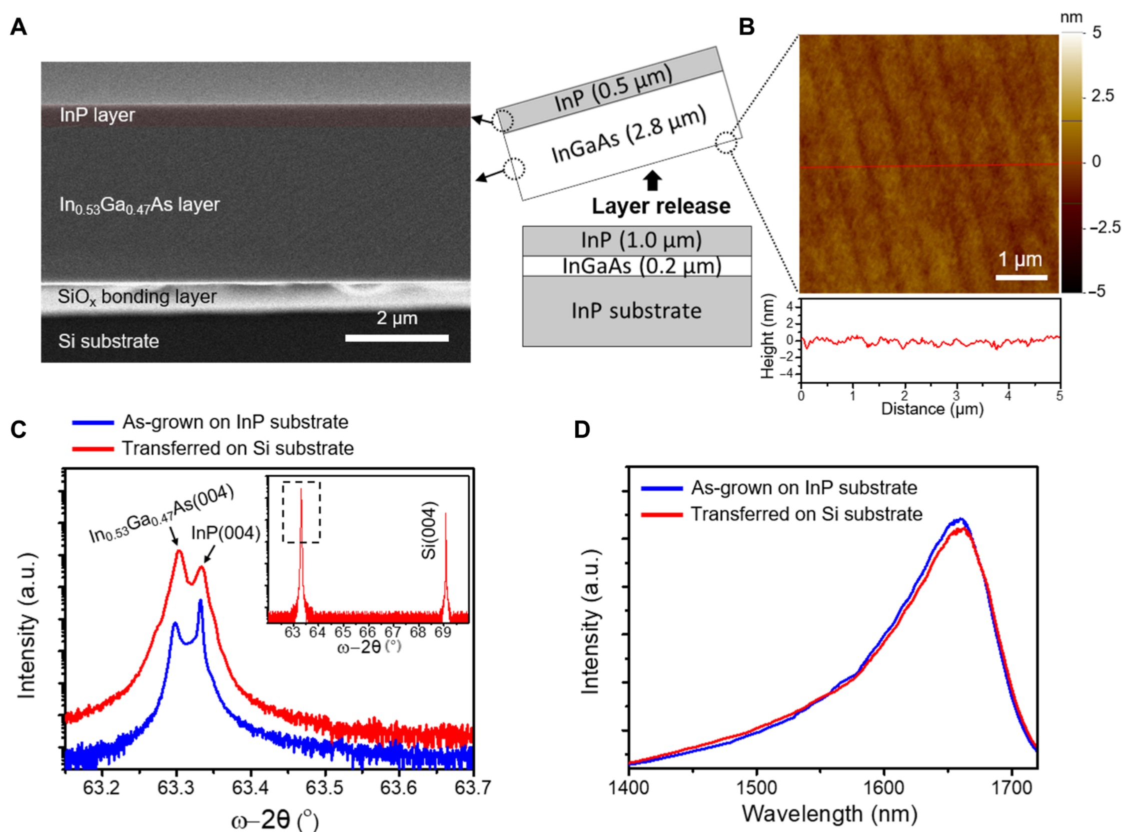

Fig. 4. Characterization of InP/InGaAs epitaxial layer transferred onto an Si substrate. (**A**) Cross-sectional SEM image of the transferred InP/InGaAs epitaxial layer on an Si(100) substrate after process III and (**B**) an AFM image of the surface of the released epitaxial layer (root-mean-squared surface roughness of 3.7 Å), showing that the surface of the released layer is atomically flat and the layer can be transferred without air voids. (**C**) High-resolution XRD ω–2θ scans of the InP/InGaAs epitaxial layer grown on the InP substrate and transferred onto the Si substrate, showing XRD peaks corresponding to the (004) lattice of InGaAs and InP (inset, wide-range XRD ω–2θ scan including the Si lattice). (**D**) Steady-state room temperature PL spectra of the InP/InGaAs epitaxial layer grown on the InP substrate and transferred onto the Si substrate. These results indicate that the layer-resolved mechanical separation process enables atomically flat release and transfer of a III-V epitaxial layer without degradation in both crystal and material quality.

we could reliably transfer the epitaxial layer (InP/InGaAs) onto the Si substrate without any air voids at the interface between the epitaxial layer and bonding layer (Fig. 4A). We characterized the surface morphology of the released layers by using AFM measurement. As shown in Fig. 4B, the surface of the released layer was atomically flat with a root-mean-squared surface roughness of ~3.7 Å. This flatness is comparable with the spalling result of elemental semiconductors (*11*). Figure 4C shows the characterization on the crystallinity of the transferred epitaxial layer based on the high-resolution XRD measurement. The slight shift in XRD peaks toward higher diffraction angles (~0.005°) indicates that there was a weak remaining compressive stress after the transfer, and the full-width at half-maximum values less than 0.01° (<40 arc sec) of the XRD peaks corresponding to the (004) lattice of transferred InGaAs and InP indicate that there was no noticeable degradation in crystal quality of the single-crystalline epitaxial layer after the processes. In addition, we confirmed the material quality of the transferred epitaxial layer by measuring the steady-state PL characteristics at room temperature. There was no noticeable difference between the spectrum of the epitaxial layer as-grown on InP and that of the released/transferred layer (Fig. 4D). No peak shift induced by the optical-bandgap change nor peaks activated by defects were observed after the processes. Consequently, these structural and optical characterization results indicate that the proposed layer-resolved mechanical separation process enables atomically flat release and transfer of a III-V(100) epitaxial layer without noticeable degradation in both crystal and material quality.

DISCUSSION

In summary, we proposed a layer-resolved mechanical separation technique that can selectively release III-V(100) epitaxial layers of interest from a normal lattice-matched heterostructure without an embedded sacrificial buffer. Because the layer release precisely occurs at a heteroepitaxial interface with a relatively weak surface energy, this technique can enable atomically flat and uniform release of single-crystalline III-V epitaxial layers without degradation in crystal and material quality. Furthermore, we demonstrated that the target heteroepitaxial interface for layer release can be selectively determined by controlling the strain energy induced by the Ni stressor film. This technique will offer an effective processing technique required for heterogeneous integration of III-V compound semiconductors with Si or other substrates and provide high fabrication flexibility in compound semiconductor technology.

MATERIALS AND METHODS

Epitaxial growth

The InP/InGaAs heterostructure was epitaxially grown on a 2-inch on-axis *n*-InP(100) wafer by a MOCVD reactor (D180 LDM, Veeco Inc.). After growing a 0.3-μm-thick buffer layer (Si-doped *n*-InP) on the InP substrate, a lattice-matched 0.2-μm-thick n-$In_{0.53}Ga_{0.47}As$ layer (Si doped with a doping concentration of 5×10^{16} cm^{-3}) was grown as an etch-stop layer for n-type contact formation. For a *p–i–n* structure, a 1-μm-thick n-type contact layer (Si-doped InP), 2.8-μm-thick active layer (undoped $In_{0.53}Ga_{0.47}As$), and 0.5-μm-thick p-type contact layer (Zn-doped InP) were sequentially grown. The doping concentrations of the *n*-InP and *p*-InP contact layers were 3×10^{18} and 5×10^{17} cm^{-3}, respectively. In this growth process, the InP/InGaAs epitaxial layers were grown at 650°C under N_2 ambience, and phosphine, trimethylindium, trimethylgallium, and arsine were used as P, In, Ga, and As precursors, respectively.

Mechanical release of thin semiconductor layers

The Si, GaAs, InP, and InP/InGaAs heteroepitaxial layers were mechanically released by the Ni stressor film with a handling layer. Before the deposition of the Ni film, a 20-nm-thick Ti film was deposited by DC magnetron sputtering with a system power of 600 W and a working pressure of 3 mT to promote adhesion between the Ni film and substrate. Subsequently, in the same chamber, an Ni film with a high internal tensile stress was deposited with a system power of 300 W and a working pressure of 3 mT. After unloading the Ni-deposited samples and cooling them to room temperature, the semiconductor layers were released from their substrates by using a thermal-release tape (Revalpha, Nitto Denko Inc.) as a handling layer for the layer release/transfer process. In this step, we attached the thermal-release tape on top of the Ni film and manually applied an external lifting force to the sample using the handling tape to initiate the crack at the sample edge. After the crack initiation, because of the high stress induced by the Ni film, the crack propagated almost spontaneously until the semiconductor layer was completely released from the substrate.

Transfer of released semiconductor layers

The released semiconductor layers were transferred onto an Si substrate by using the spin-on-glass process (*51*, *52*). First, TEOS-based solution-processable SiO_x was spin coated on the Si substrate as a bonding layer; then, a released semiconductor layer was placed onto the SiO_x-coated Si substrate. Subsequently, to cure the SiO_x layer and bond the semiconductor layer with the Si substrate, we baked the sample at 120°C for 2 hours with applying a pressure of 55 g cm^{-2}. In this step, the thermal release tape was detached from the surface of the sample because of the baking temperature being higher than the release temperature of the tape (90° to 120°C). The thickness of the SiO_x layer was about 500 nm after the baking step. Last, the stressor film was completely removed by wet etching. The Ni film was etched in a 0.1 M ferric chloride ($FeCl_3$) solution, and the thin Ti layer was etched in a diluted (1%) hydrogen fluoride solution.

Stress measurement

The internal stress of the Ni film was measured with a multibeam optical sensor system (*44*). In this measurement, the internal stress was estimated on the basis of Stoney's method (*53*), which is a standard method for measuring film stress. The internal stress was deduced from the curvature change in the film/substrate, which was estimated from the change in the measured spacing between multiple beams. The relation between the internal stress of the film and the measured beam spacing is given by

$$\sigma_f = \left(\frac{\Delta d}{d_0}\right)\frac{Y_s t_s^2 \cos\alpha}{12(1-\nu_s)\, t_f L}$$

where σ_f, Δd, d_0, Y_s, v_s, t_s, t_f, α, and L are the internal stress of film, the difference in beam spacing due to stress-induced curvature, the initial beam spacing before film deposition, the Young's modulus of the substrate, the Poisson ratio of the substrate, the thickness of the substrate, the thickness of the film, the detection angle, and the detection length, respectively. To calculate the estimated spalling

depth as a function of Ni thickness, we deposited Ni films with various thicknesses on InP(100) substrates and measured the internal stresses depending on their thicknesses.

Characterizations

The cross-sectional images of the released layers and the remaining substrates and the mapping images of their elemental compositions were obtained by using field-emission SEM (SU8220, Hitachi Inc.) combining with EDS (MX80, Oxford Instruments Inc.). The III-V structures on the surfaces of the released layers and the remaining substrates were evaluated via Raman spectroscopic measurement (inVia reflex, Renishaw Inc.) with a laser wavelength of 532 nm. The AFM image was obtained by the tapping-mode operation of a scanning probe microscope (NX20, Park Systems Inc.). An AC-mode Si probe with a resonance frequency of 300 kHz was used for imaging. The crystal quality of the epitaxial layers was characterized by an XRD measurement system (Empyrean, Malvern PANalytical Inc.) with Cu $K\alpha$ radiation operated at 40 kV and 25 mA. The material quality was characterized by a PL measurement system (LabRAM HR-800, Horiba Jobin Yvon Inc.) with a 514-nm line laser and a Ge photodetector. The cross-sectional images of the heteroepitaxial interface between the InP and InGaAs layers were obtained by using field-emission TEM (Titan G2 ChemiSTEM Cs Probe, FEI Company Inc.).

SUPPLEMENTARY MATERIALS

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REFERENCES AND NOTES

1. J. Justice, C. Bower, M. Meitl, M. B. Mooney, M. A. Gubbins, B. Corbett, Wafer-scale integration of group III-V lasers on silicon using transfer printing of epitaxial layers. *Nat. Photonics* **6**, 610–614 (2012).
2. D. Liang, J. E. Bowers, Recent progress in lasers on silicon. *Nat. Photonics* **4**, 511–517 (2010).
3. A. W. Elshaari, W. Pernice, K. Srinivasan, O. Benson, V. Zwiller, Hybrid integrated quantum photonic circuits. *Nat. Photonics* **14**, 285–298 (2020).
4. B. E. A. Saleh, M. C. Teich, *Fundamentals of Photonics* (Wiley, 2019).
5. O. Moutanabbir, U. Gösele, Heterogeneous integration of compound semiconductors. *Annu. Rev. Mater. Res.* **40**, 469–500 (2010).
6. P. Demeester, A. Ackaert, G. Coudenys, I. Moerman, L. Buydens, I. Pollentier, P. Van Daele, Relaxed lattice-mismatched growth of III-V semiconductors. *Prog. Cryst. Growth Charact. Mater.* **22**, 53–141 (1991).
7. J. Narayan, Recent progress in thin film epitaxy across the misfit scale (2011 Acta Gold Medal Paper). *Acta Mater.* **61**, 2703–2724 (2013).
8. E. Yablonovitch, T. Gmitter, J. P. Harbison, R. Bhat, Extreme selectivity in the lift-off of epitaxial GaAs films. *Appl. Phys. Lett.* **51**, 2222–2224 (1987).
9. J. Yoon, S. Jo, I. S. Chun, I. Jung, H.-S. Kim, M. Meitl, E. Menard, X. Li, J. J. Coleman, U. Paik, J. A. Rogers, GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature* **465**, 329–333 (2010).
10. C.-W. Cheng, K.-T. Shiu, N. Li, S.-J. Han, L. Shi, D. K. Sadana, Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nat. Commun.* **4**, 1577 (2013).
11. H. Park, C. Lim, C.-J. Lee, M. Choi, S. Jung, H. Park, Analytic model of spalling technique for thickness-controlled separation of single-crystalline semiconductor layers. *Solid State Electron.* **163**, 107660 (2020).
12. M. B. Joshi, M. S. Goorsky, Transfer of InP thin films from engineered porous silicon substrates. *J. Appl. Phys.* **107**, 024906 (2010).
13. Y. Zhang, B. Leung, J. Han, A liftoff process of GaN layers and devices through nanoporous transformation. *Appl. Phys. Lett.* **100**, 181908 (2012).
14. J. Kim, C. Bayram, H. Park, C.-W. Cheng, C. Dimitrakopoulos, J. A. Ott, K. B. Reuter, S. W. Bedell, D. K. Sadana, Principle of direct van der Waals epitaxy of single-crystalline films on epitaxial graphene. *Nat. Commun.* **5**, 4836 (2014).
15. Y. Kim, S. S. Cruz, K. Lee, B. O. Alawode, C. Choi, Y. Song, J. M. Johnson, C. Heidelberger, W. Kong, S. Choi, K. Qiao, I. Almansouri, E. A. Fitzgerald, J. Kong, A. M. Kolpak, J. Hwang, J. Kim, Remote epitaxy through graphene enables two-dimensional material-based layer transfer. *Nature* **544**, 340–343 (2017).
16. H. Kum, D. Lee, W. Kong, H. Kim, Y. Park, Y. Kim, Y. Baek, S.-H. Bae, K. Lee, J. Kim, Epitaxial growth and layer-transfer techniques for heterogeneous integration of materials for electronic and photonic devices. *Nat. Electron.* **2**, 439–450 (2019).
17. S. W. Bedell, K. Fogel, P. Lauro, D. Shahrjerdi, J. A. Ott, D. Sadana, Layer transfer by controlled spalling. *J. Phys. D Appl. Phys.* **46**, 152002 (2013).
18. Y. Zhai, L. Mathew, R. Rao, D. Xu, S. K. Banerjee, High-performance flexible thin-film transistors exfoliated from bulk wafer. *Nano Lett.* **12**, 5609–5615 (2012).
19. D. Shahrjerdi, S. W. Bedell, Extremely flexible nanoscale ultrathin body silicon integrated circuits on plastic. *Nano Lett.* **13**, 315–320 (2013).
20. H. Park, C. Lim, Y. Noh, C.-J. Lee, H. Won, J. Jung, M. Choi, J.-J. Kim, H. Yoo, H. Park, Investigation of electrical characteristics of flexible CMOS devices fabricated with thickness-controlled spalling process. *Solid-State Electron.* **173**, 107901 (2020).
21. S. W. Bedell, D. Shahrjerdi, B. Hekmatshoar, K. Fogel, P. A. Lauro, J. A. Ott, N. Sosa, D. Sadana, Kerf-less removal of Si, Ge, and III-V layers by controlled spalling to enable low-cost PV technologies. *IEEE J. Photovolt.* **2**, 141–147 (2012).
22. D. Shahrjerdi, S. W. Bedell, A. Khakifirooz, K. Cheng, Mechanically flexible nanoscale silicon integrated circuits powered by photovoltaic energy harvesters. *Solid State Electron.* **117**, 117–122 (2016).
23. H.-S. Yang, J. Kim, S. Kim, N. S. A. Eom, S. Kang, C.-S. Han, S. H. Kim, D. Lim, J.-H. Lee, S. H. Park, J. W. Choi, C.-L. Lee, B. Yoo, J.-H. Lim, Kerf-less exfoliated thin silicon wafer prepared by nickel electrodeposition for solar cells. *Front. Chem.* **6**, 600 (2019).
24. D. Shahrjerdi, S. W. Bedell, C. Ebert, C. Bayram, B. Hekmatshoar, K. Fogel, P. Lauro, M. Gaynes, T. Gokmen, J. A. Ott, D. K. Sadana, High-efficiency thin-film InGaP/InGaAs/Ge tandem solar cells enabled by controlled spalling technology. *Appl. Phys. Lett.* **100**, 053901 (2012).
25. C. A. Sweet, K. L. Schulte, J. D. Simon, M. A. Steiner, N. Jain, D. L. Young, A. J. Ptak, C. E. Packard, Controlled exfoliation of (100) GaAs-based devices by spalling fracture. *Appl. Phys. Lett.* **108**, 011906 (2016).
26. C. A. Sweet, J. E. McNeely, B. Gorman, D. L. Young, A. J. Ptak, C. E. Packard, Engineering controlled spalling in (100)-oriented GaAs for wafer reuse, *paper presented at the 2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, New Orleans, LA USA, 14 to 19 June 2015.
27. C. A. Sweet, "Spalling fracture behavior in (100) gallium arsenide", thesis, Colorado School of Mines, Golden, CO (2016).
28. Y. H. Lee, J. Kim, J. Oh, Wafer-scale ultrathin, single-crystal Si and GaAs photocathodes for photoelectrochemical hydrogen production. *ACS Appl. Mater. Interfaces* **10**, 33230–33237 (2018).
29. S. W. Bedell, P. Lauro, J. A. Ott, K. Fogel, D. K. Sadana, Layer transfer of bulk gallium nitride by controlled spalling. *J. Appl. Phys.* **122**, 025103 (2017).
30. N. Li, S. Bedell, H. Hu, S.-J. Han, X. H. Liu, K. Saenger, D. Sadana, Single crystal flexible electronics enabled by 3D spalling. *Adv. Mater.* **29**, 1606638 (2017).
31. K. Sakuma, H. Hu, X. H. Liu, J. Ni, S. W. Bedell, B. Webb, S. L. Wright, P. Lauro, K. Latzko, M. Agno, J. Tornello, J. U. Knickerbocker, CMOS-compatible wearable sensors fabricated using controlled spalling. *IEEE Sens. J.* **19**, 7868–7874 (2019).
32. C. Messmer, J. C. Bilello, The surface energy of Si, GaAs, and GaP. *J. Appl. Phys.* **52**, 4623 (1981).
33. S. Adachi, *Physical Properties of III-V Semiconductor Compounds* (Wiley, 1992).
34. S.-W. Ryu, W. G. Jeong, I. Kim, H.-D. Kim, H.-H. Kim, B.-D. Choe, S.-H. Park, Reduction of as carryover by PH_3 overpressure in metalorganic vapor-phase epitaxy. *J. Cryst. Growth* **179**, 26–31 (1997).
35. T. Mozume, H. Kashima, K. Hosomi, K. Ogata, K. Suenaga, A. Nakano, Tailored heterointerface formation in InGaAs/InP superlattices by gas source migration-enhanced epitaxy. *Appl. Surf. Sci.* **75**, 233–241 (1994).
36. B. Lakshmi, B. J. Robinson, D. T. Cassidy, D. A. Thompson, Anisotropic interfacial strain in InP/InGaAs/InP quantum wells studied using degree of polarization of photoluminescence. *J. Appl. Phys.* **81**, 3616–3620 (1997).
37. J. M. Vandenberg, R. A. Hamm, S. N. G. Chu, Interface structure of large-period lattice-matched in GaAs/InP superlattices grown by metalorganic molecular beam epitaxy: A high-resolution x-ray diffraction study. *J. Cryst. Growth* **144**, 9–14 (1994).
38. J. Decobert, G. Patriarche, Transmission electron microscopy study of the InP/InGaAs and InGaAs/InP heterointerfaces grown by metalorganic vapor-phase epitaxy. *J. Appl. Phys.* **92**, 5749–5755 (2002).
39. X. S. Jiang, A. R. Clawson, P. K. L. Yu, Study of interrupted MOVPE growth of InGaAs/InP superlattice. *J. Cryst. Growth* **124**, 547–552 (1992).
40. A. R. Clawson, T. T. Vu, S. A. Pappert, C. M. Hanson, Effects of hydrogen-only interrupts on InGaAs/InP superlattices grown by OMVPE. *J. Cryst. Growth* **124**, 536–540 (1992).
41. T. Anan, S. Sugou, K. Nishi, T. Ichihashi, Improvement of InP/InGaAs heterointerfaces grown by gas source molecular beam epitaxy. *Appl. Phys. Lett.* **63**, 1047–1049 (1993).

42. D.-M. Geum, S. Kim, S. K. Kim, S. Kang, J. Kyhm, J. Song, W. J. Choi, E. Yoon, Monolithic integration of visible GaAs and near-infrared InGaAs for multicolor photodetectors by using high-throughput epitaxial lift-off toward high-resolution imaging systems. *Sci. Rep.* **9**, 18661 (2019).
43. G. Chen, M. Wang, W. Yang, M. Tan, Y. Wu, P. Dai, Y. Huang, S. Lu, Optical properties of Zn-diffused InP layers for the planar-type InGaAs/InP photodetectors. *J. Semicond.* **38**, 124004 (2017).
44. E. Chason, Resolution and sensitivity of stress measurement with the k-Space Multi-beam Optical Sensor (MOS) system (Sandia National Laboratories, USA, 2005); www.k-space.com/wp-content/uploads/MOSbyChason.pdf.
45. W. D. Nix, Mechanical properties of thin films. *Metall. Trans. A.* **20**, 2217–2245 (1989).
46. J. Kim, D. Inns, D. K. Sadana, Investigation on critical failure thickness of hydrogenated/nonhydrogenated amorphous silicon films. *J. Appl. Phys.* **107**, 073507 (2010).
47. R. T. Murray, C. J. Kiely, M. Hopkinson, Crack formation in III-V epilayers grown under tensile strain on InP(001) substrates. *Philos. Mag. A* **74**, 383–393 (1996).
48. J. H. Park, C.-H. Chung, Raman spectroscopic characterizations of self-catalyzed InP/InAs/InP one-dimensional nanostructures on InP(111)B substrate using a simple substrate-tilting method. *Nanoscale Res. Lett.* **14**, 355 (2019).
49. J. Li, G. Miao, Z. Zhang, Y. Zeng, Experiments and analysis of the two-step growth of InGaAs on GaAs substrate. *CrstEngComm* **17**, 5808–5813 (2015).
50. M.-S. Park, M. Razaei, K. Barnhart, C. L. Tan, H. Mohseni, Surface passivation and aging of InGaAs/InP heterojunction phototransistors. *J. Appl. Phys.* **121**, 233105 (2017).
51. D. Goustouridis, K. Minoglou, S. Kolliopoulou, S. Chatzandroulis, P. Morfouli, P. Normand, D. Tsoukalas, Low temperature wafer bonding for thin silicon film transfer. *Sens. Actuator A Phys.* **110**, 401–406 (2004).
52. R. Go'mez, R. Bashir, A. Sarikaya, M. R. Ladisch, J. Sturgis, J. P. Robinson, T. Geng, A. K. Bhunia, H. L. Apple, S. Wereley, Microfluidic biochip for impedance spectroscopy of biological species. *Biomed. Microdevices* **3**, 201–209 (2001).
53. G. G. Stoney, The tension of metallic films deposited by electrolysis. *Proc. R. Soc. Lond. A* **82**, 172–175 (1909).
54. Z. Suo, J. W. Hutchinson, Steady-state cracking in brittle substrates beneath adherent films. *Int. J. Solids Struct.* **25**, 1337–1353 (1989).
55. J. W. Hutchinson, Z. Suo, Mixed mode cracking in layered materials. *Adv. Appl. Mech.* **29**, 63–191 (1991).
56. D. Crouse, J. Simon, K. L. Schulte, D. L. Young, A. J. Ptak, C. E. Packard, Increased fracture depth range in controlled spalling of (100)-oriented germanium via electroplating. *Thin Solid Films* **649**, 154–159 (2018).
57. P. Giannozzi, S. Baroni, N. Bonini, M. Calandra, R. Car, C. Cavazzoni, D. Ceresoli, G. L. Chiarotti, M. Cococcioni, I. Dabo, A. D. Corso, S. de Gironcoli, S. Fabris, G. Fratesi, R. Gebauer, U. Gerstmann, C. Gougoussis, A. Kokalj, M. Lazzeri, L. Martin-Samos, N. Marzari, F. Mauri, R. Mazzarello, S. Paolini, A. Pasquarello, L. Paulatto, C. Sbraccia, S. Scandolo, G. Sclauzero, A. P. Seitsonen, A. Smogunov, P. Umari, R. M. Wentzcovitch, QUANTUM ESPRESSO: A modular and open-source software project for quantum simulations of materials. *J. Phys. Condens. Matter* **21**, 395502 (2009).
58. P. E. Blöchl, Projector augmented-wave method. *Phys. Rev. B* **50**, 17953–17979 (1994).
59. J. P. Perdew, K. Burke, M. Ernzerhof, Generalized gradient approximation made simple. *Phys. Rev. Lett.* **77**, 3865–3868 (1996).
60. G. Cai, C. Wang, W. Wang, E. Liang, Band offsets and electronic structures of interface between $In_{0.5}Ga_{0.5}As$ and InP. *J. Appl. Phys.* **119**, 055705 (2016).
61. O. Schuler, O. Dehaese, X. Wallart, F. Mollot, Interface quality and electron transfer at the GaInP on GaAs heterojunction. *J. Appl. Phys.* **84**, 765–769 (1998).
62. A. Aurand, J. Leymarie, A. Vasson, M. Mesrine, J. Massies, M. Leroux, Investigation of the P–As substitution at GaAs/$Ga_{0.51}In_{0.49}P$ interfaces by photoluminescence under pressure. *J. Appl. Phys.* **89**, 3775–3782 (2001).
63. J. Kim, H. Park, J. B. Hannon, S. W. Bedell, K. Fogel, D. K. Sadana, C. Dimitrakopoulos, Layer-resolved graphene transfer via engineered strain layers. *Science* **342**, 833–836 (2013).
64. L. Peternai, J. Kováč, G. Irmer, S. Hasenöhrl, J. Novák, R. Srnánek, Investigation of graded $In_xGa_{1-x}P$ buffer by Raman scattering method. *Microelectron. J.* **37**, 487–490 (2006).

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