



# Role of Structure and Composition on the Performances of P-Type Tin Oxide Thin-Film **Transistors Processed at Low-Temperatures**

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Abstract: This work reports on the role of structure and composition on the determination of the performances of p-type  $SnO_x$  TFTs with a bottom gate configuration deposited by rf magnetron sputtering at room temperature, followed by a post-annealed step up to 200 °C at different oxygen partial pressures  $(O_{pp})$  between 0% and 20% but where the p-type conduction was only observed between in a narrow window, from 2.8% to 3.8%. The role of structure and composition were evaluated by XRD and Mössbauer spectroscopic studies that allows to identify the best phases/compositions and thicknesses (around 12 nm) to be used to produce p-type TFTs with saturation mobility of 4.6 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and on-off ratio above  $7 \times 10^4$ , operating at the enhancement mode with a saturation voltage of -10 V. Moreover, a brief overview is also presented concerning the present state of the existing developments in processing SnO<sub>x</sub> TFTs with different methods and using different device configurations.

p-type TFT; p-type oxide semiconductors; SnO electrical properties; oxide Keywords: structure analysis

# 1. Introduction

Oxide electronics are a promising alternative to amorphous silicon (a-Si:H) and organic semiconductors to build reliable Thin Film Transistors (TFT) and more complex electronic circuits, addressing the challenges of flexible electronics and of the low cost and disposable electronics. In spite of the earlier work made during the 60s concerning the processing of n-type TFT [1,2], only forty five years later, with the work of Hosono [3], Wager [4], Carcia [5] and Fortunato [6], a significant worldwide interest materialised, especially for the active matrix for organic light emitting diodes (AMOLED) technology, exploiting their electronic properties, such as high saturation mobility, excellent uniformity and homogeneity, together with a high reliability associated with a low or room processing temperature [7].

However, there is no report on p-type oxide TFTs that are processed and cured at low temperatures with a performance similar to n- type, due to the low hole mobilities so far achieved in running stable and reliable devices [8]. The achievement of reliable p-type TFT, with performances similar to n-type



TFT is of great importance for shaping electronics challenges towards the production of complementary metal oxide semiconductors (CMOS), a key device for analogic and digital electronic systems, thanks to their low power consumption. This is a noticeable relevant CMOS property for low cost flexible electronics. To this end, we could use organic semiconductors, aiming to exploit the advantage that they can be processed at low temperatures.

Concerning organic p-type TFTs, most device performances on stability and mobility ( $<2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) are low [9–12], while the n-type organic TFT still exhibits low mobilities ( $\le 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) and requires a high absolute on voltages to switch it on [13,14].

An alternative to this is the inorganic oxide TFT, which is robust but in most cases requires high process temperatures. So far, most of the reported oxide TFTs are n-type, processed either on rigid or flexible substrates in which exists a consolidate set of results for films processed via physical or chemical methods [1–8,15,16]. For p-type, the transport due to holes is associated wirh oxygen *p* asymmetric orbitals, which severely limit the carrier mobility and therefore the TFT performances. In spite of Cu<sub>2</sub>O being a p-type oxide with mobility >100 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> [17,18], the TFT based on these thin films or their compositions as Cu:NiO, exhibit mobilities and On-Off current ratios of <1.5 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and 10<sup>4</sup> respectively [17–21]. Other materials have been also reported, such as NiO<sub>x</sub> processed/annealed at 300 °C, exhibiting mobilities above 25 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> [22].

Tin oxide has been studied as an alternative material to produce p-type oxides, with similar performances as those obtained in n-type oxides. The structure, morphology and ambipolar characteristic of these films are well known for oxides processed by reactive sputtering using metal targets and heat treated at 400 °C [23]. Indeed, it is known that SnO has an indirect band gap structure specifically controlled by the divalent tin (SnII), in a layered crystal structure [24,25] with major contributions from Sn 5*s* and O 2*p* orbitals near the valence band maximum (VBM) and Sn 5*p* orbitals towards the conduction band minimum (CBM). The p-type behaviour is mainly attributed to the Sn vacancy and the O interstitial where tin is in Sn<sup>2+</sup> oxidation state [24,25]. The excess oxygen in the film transforms some cations in Sn<sup>3+</sup> to maintain electrical neutrality. This process is considered to be Sn<sup>2+</sup> capturing a hole and forming weak bonded holes, located inside the bandgap, near the top of the valence band as localized acceptor states [26,27]. This means that the final free carriers' behaviour of the films process is highly dependent on how oxygen is bonded and how it may compensate for defects.

Here, the contributions from Sn 5*s* states to VBM offer appreciable hole mobility in this material, without using a high processes temperature [28,29]. This leads also to the production of TFT with different geometry configurations [30] or using, besides metallic targets, ceramic ones on films grown by rf magnetron sputtering, heat treated at 400 °C [31].

In Table 1 we present the set of developments obtained concerning the performances of p-type SnO TFTs produced by Radio Frequency Magnetron Sputtering (RFMS) in the last 10 years [28,32–49]. There, we also present the architecture selected (SBG: staggered bottom-gate; STG: staggered top-gate; CBG: coplanar bottom-gate; CTG: coplanar top-gate; DG: double-gate), the process temperature, the oxygen partial pressure ( $O_{pp}$ ) and the type of dielectric used.

Method	Device Structure	Process Temp. (°C)	O <sub>pp</sub> (%)	Dielectric	$\mu_{h,FE}$ (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> )	I <sub>on</sub> /I <sub>off</sub>	Year	Ref.
RFMS	SBG	RT *	11.5	ATO	1.2	10 <sup>3</sup>	2010	[28]
RFMS	SBG	300	1	SiN <sub>x</sub>	0.24	10 <sup>2</sup>	2010	[32]
RFMS	SBG	150	n.r.	Paper	1.3	$10^{2}$	2011	[33]
RFMS	SBG	250	n.r.	SiO <sub>2</sub>	1.8	$10^{3}$	2013	[34]
RFMS	SBG	225	4.3	HfO <sub>2</sub>	0.33	$10^{3}$	2014	[35]
RFMS	SBG	230	n.r.	SiO <sub>2</sub>	0.59	$3  imes 10^3$	2014	[36]
RFMS	CTG	200	9	P(VDF-TrFE)	3.3	$3 \times 10^2$	2014	[37]
RFMS	SBG	200	11.8	SiO <sub>2</sub>	1.36	$2  imes 10^3$	2014	[38]
RFMS	STG	200	9	P(VDF-TrFE)	2.7	$2 \times 10^2$	2014	[39]
RFMS	SBG	200	n.r.	SiO <sub>2</sub>	0.61	$6.2  imes 10^5$	2015	[40]
RFMS	SBG	250	n.r.	SiO <sub>2</sub>	1.8	$10^{5}$	2015	[41]
RFMS	SBG	200	7.5	SiO <sub>2</sub>	4.13	$6  imes 10^2$	2015	[42]
RFMS	SBG	250	-	$SiO_2$	1.16	$2.3  imes 10^2$	2015	[43]
RFMS	SBG	300	n.r.	$SiO_2$	3.33	$10^{4}$	2016	[44]
RFMS	SBG	200	n.r.	SiO <sub>2</sub>	0.63	$5.2 \times 10^{6}$	2017	[45]
RFMS	SBG	225	n.r.	$Al_2O_3$	0.7	$2.6  imes 10^4$	2018	[46]
RFMS	SBG	120	9	$HfO_2$	5.53	$2.7  imes 10^3$	2018	[47]
RFMS	SBG	225	3.1	SiO <sub>2</sub>	1.41	$1.5  imes 10^3$	2018	[48]
RFMS	SBG	225	3.1	SiO <sub>2</sub>	0.87	$1.88  imes 10^4$	2019	[49]
RFMS	SBG	RT *	3.0	ATO	4.6	$7  imes 10^4$	2019	This work

**Table 1.** Recent developments concerning the performances of p-type SnO TFTs processed by Radio Frequency Magnetron Sputtering (RFMS), using different type of device configurations, O<sub>pp</sub>, dielectrics and process temperatures.

\* Post deposition annealed at 200 °C; n.r.: not reported; RT = Room Temperature; ATO = Aluminum Titanium Oxide.

Overall, we notice that the only devices processed at room temperature using the RFMS technique are those developed by the present group [28,33]. Here, it is also relevant to mention that the presence of low oxygen partial pressure during the deposition process enables the production of more stable devices [35,48,49]. Apart from that, the configuration most used is the staggered bottom-gate, while the most common dielectric used is the silicon dioxide. Apart from that, most of the substrates used are rigid (glass or silicon wafer), except that referred to as CMOS devices integrating p-type TFT based on SnO<sub>x</sub> made on paper [33].

Besides stability and reproducibility issues, the data presented show that the device with the best mobility (5.53 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, with Perovskite-Mediated Photogating [47]) does not correspond to the device with the highest On/Off ( $I_{on}/I_{off}$ ) ratio (5.2 × 10<sup>6</sup>, using argon-plasma surface treatment [45]). Apart from that, most of the TFT studied does not work on the enhancement mode, as desired for application purposes.

Moreover, we noticed that the thickness of the channel layer, together with the state of the surface (degree of roughness and surface defects), determine the electrical characteristics presented by TFT and its stability.

In Table 2 we present the most significant data achieved in the last ten years concerning the production of  $SnO_x$  p-type TFT using different processing techniques such as: Pulsed Laser Deposition (PLD); Electron-Beam Evaporation (EBE); Thermal Evaporation (TE); direct current magnetron sputtering (DCMS); PVD: Physical Vapor Deposition (PVD); Atomic Layer Deposition (ALD); Spin-Coating (SC). As in Table 1, the different type of device configurations are also shown (SBG: staggered bottom-gate; STG: staggered top-gate; CBG: coplanar bottom-gate; CTG: coplanar top-gate; DG: double-gate); Oxygen partial pressures (O<sub>pp</sub>); dielectrics and process temperatures used.

Method	Device Structure	Process Temp. (°C)	Oxygen Partial Pressure (%)	Dielectric	$\mu_{h,FE} (cm^2 V^{-1} s^{-1})$	I <sub>on</sub> /I <sub>off</sub>	Year	Ref.
PLD	STG	575	$4  imes 10^{-2} \mathrm{Pa}$	$Al_2O_3$	1.3	10 <sup>2</sup>	2008	[50]
PLD	STG	250	$1 imes 10^{-2}~{ m Pa}$	SiO <sub>2</sub>	0.81	$\sim 10^{2}$	2011	[51]
PLD	SBG	300	$1 imes 10^{-2}~{ m Pa}$	SiO <sub>2</sub>	2.18	_	2014	[52]
EBE	SBG	400	n.r.	SiO <sub>2</sub>	0.32	$5 \times 10^2$	2013	[53]
TE	SBG	250	n.r.	$Al_2O_3$	1.4	$5 imes 10^4$	2018	[54]
DCMS	SBG	180	9	HfO <sub>2</sub>	6.75	$\sim 10^{3}$	2013	[29]
DCMS	DG	300	$3.07 \times 10^{-2}$ Pa	SiO <sub>2</sub>	6.54	$10^{5}$	2015	[30]
DCMS	SBG	200	n.r.	HfO <sub>2</sub>	5.56	$4.8  imes 10^4$	2016	[55]
DCMS	SBG	200	n.r.	HfO <sub>2</sub>	7.6	$3 \times 10^4$	2018	[31]
PVD	SBG	200	n.r.	HfO <sub>2</sub>	2.13	$9.6  imes 10^6$	2017	[56]
ALD	SBG	250	n.r.	$Al_2O_3$	1	$2 imes 10^6$	2017	[57]
SC	SBG	450	-	SiO <sub>2</sub>	0.13	85	2012	[58]

**Table 2.** Recent developments concerning the performances of p-type SnO TFTs processed by other physical and chemical process techniques, for different device configurations, O<sub>pp</sub>, dielectrics and process temperatures.

\* Post deposition annealed at 200 °C; n.r.: not reported.

Overall, the best p-type TFTs fabricated so far have been those processed by DCMS, exhibiting a mobility of 6.54 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and an On/Off ratio of 10<sup>5</sup>, working in the depletion mode [30]. Moreover, the p-type TFT processed by PVD and using a STG configuration exhibit the highest recorded On/Off ratio (9.6 × 10<sup>6</sup>) [56].

From the present state of the art, we saw that there are several parameters that impact on the electrical performance presented by p-type TFT  $SnO_x$  based, most of them connected to the process parameters used, the structure of the films obtained, as well as the dielectric and the geometry configuration used.

In this paper, we report the fabrication of p-type  $SnO_x$  TFTs deposited by RFMS technique at RT that are post-annealed up to 200 °C, turning the process compatible with the use of low-cost flexible substrates as paper [7]. In this study, we aim to better understand the role that the structure, surface finishing and oxygen play during the growing process of  $SnO_x$  in order to define a process window that allows the production of reliable and high stable p-type TFT with high electronic performances, such as field effect mobility and On-Off- current ratios.

## 2. Materials, Methods and Results

## 2.1. Experimental Details

## **Films Preparation**

SnO<sub>x</sub> thin films (5–100 nm) were deposited on glass substrates with an r.f. magnetron sputtering system at room temperature, using a metallic tin target (99.999% pure). Depositions were carried out in a controlled atmosphere of oxygen and argon, using an r.f. power of 40 W and 4 substrates of 1 inch ×1 inch placed in the substrate holder were rotated at a speed of 40 rpm, aiming to get high uniform films overall substrate area. Experiments were performed by varying  $O_{pp}$  ( $O_{pp} = P_{O2}/(P_{O2} + P_{Ar})$ , between 0% and 20%, where  $P_{O2}$  and  $P_{Ar}$  are partial pressures of oxygen and argon, respectively, keeping the total deposition pressure constant at 0.2 Pa. Moreover, the argon gas flow was kept constant—around 50sccm—while the oxygen gas flow varied from 0 to 12.5 sccm. At these conditions, the deposition rate was 40 Å/min. After deposition, the films were annealed under standard environment conditions at temperatures around 200 °C, for different times inside a tubular furnace.

## 2.2. Structure Morphology, Composition and Electro-Optical Data and Analysis

Prior to processing the TFT devices, the material in which the channel is based was deposited on glass substrates and their structure, morphology, composition and electro-optical properties were fully analysed, aiming to determine the best conditions in which to grow the channel layers of the TFT. The structure of the films was studied by X-ray diffraction (XRD) using a PANalytical X'Pert PRO (Cambridge, MA, USA) with Cu K $\alpha$  radiation ( $\lambda = 1.540598$  Å) while the morphology was assessed by scanning electron microscopy (SEM) with a ZEISS SEM/FIB AURIGA (Jena, Germany) operated at 2 kV, with an aperture size of 30 µm and a working distance of 5.2 nm. The surface roughness of the films was analysed using atomic force microscopy (AFM) with an Asylum MFP-3D instrument (Oxford Instruments, Oxford, UK) in non-contact mode.

The optical transmittance (T%) was measured between 300 to 2500 nm, using a double-beam UV–vis-NIR spectrometer (Lambda 950, San Dimas, CA, USA).

The electrical resistivity ( $\rho$ ), Hall mobility ( $\mu$ ) and free carrier concentration and their nature (electrons or holes) were determined by Hall effect measurements in Van der Pauw geometry in a Biorad HL 5500 equipment (York, England) using a constant magnetic field of 0.5 T. The electrical properties of the samples were measured at room temperature.

## 2.3. Structure Data and Analysis

Figure 1 shows the XRD and Mössbauer and CEMS spectra of as-deposited and annealed  $SnO_x$  films with  $O_{pp} = 3.0\%$  and  $O_{pp} = 3.6\%$   $O_{pp}$ , respectively, as the limits of the interval where a p-type transport behaviour is observed, as proven by Hall effect measurements (a positive Hall coefficient obtained for all samples evaluated, after annealing).



**Figure 1.** (a) Diffractograms of SnO<sub>x</sub> thin films as-deposited. (b) Transmission <sup>119</sup>Sn Mössbauer and CEMS spectra of as-deposited and annealed SnO<sub>x</sub> films with  $O_{pp} = 3.0\%$  and  $O_{pp} = 3.6\%$   $O_{pp}$ , respectively.

The XRD data show that the films as deposited are amorphous, turning crystalline after annealing at 200  $^{\circ}$ C.

Figure 1a shows that the XRD pattern of films are 120 nm thick as deposited, where we can see that the metallic tin dominates over the SnO phase. It also shows the XRD diffractograms for SnO powder and metallic Sn, to be taken as references.

Room temperature transmission Mössbauer and <sup>119</sup>Sn conversion-electron Mössbauer spectroscopy (CEMS) were performed on the set of samples prepared, before and after annealing, using a proportional backscatter detector RIKON-5 (Wissel) in flowing 5% CH<sub>4</sub>-95% He gas mixture (see Figure 1b). The spectra were collected using a conventional constant acceleration spectrometer and a 5 mCi Ca<sup>119m</sup>SnO<sub>3</sub> source. The velocity scale was calibrated using a <sup>57</sup>Co (Rh) source and an  $\alpha$ -Fe foil. The Sn isomer shifts (IS) are given relative to BaSnO<sub>3</sub> reference material at 295 K (RT) and obtained by adding 0.031 mm/s to the IS relative to the source. The spectra were fitted to Lorentzian lines using a non-linear least-squares method. The set of extrapolated parameters extracted are presented in Table 3.

Sample	IS (mm/s)	QS (mm/s)	Γ (mm/s)	Sn Phase	I (%)
SnO <sub>2</sub> bulk	0.01	0.56	1.34	-	100
	2.67	1.34	0.98	α-SnO	95
$\alpha$ -SnO bulk	-0.03	0.58	0.77	$SnO_2$	5
-Sn metal	2.56	-	1.03	-	100
E:1	2.76	1.87	1.04	SnO	65
	0.11	0.52	0.84	$SnO_2$	15
$O_{pp} = 3.0\%$ , KI	2.56	_	1.3	-Sn	20
Film	2.7	1.38	0.79	SnO	81
	0.08	0.59	0.7	$SnO_2$	8
$O_{\rm pp} = 3.0\%, 200$ C, 30 min	2.56	_	1.35	-Sn	11
Film	2.73	1.82	1.02	SnO	78
$\mathbf{\Gamma}_{\mathbf{IIIII}}$	0.11	0.53	0.81	SnO <sub>2</sub>	15
$O_{pp} = 5.6 \%, RT$	2.56	_	1.3	-Sn	7
Film	2.7	1.34	0.82	SnO	88
$O_{pp} = 3.6\%$ , 200 °C, 30 min	0.06	0.48	0.85	$SnO_2$	12

**Table 3.** Extrapolated parameters from the transmission <sup>119</sup>Sn Mössbauer spectra of bulk samples and CEMS spectra of films taken at RT.

IS (mm/s) isomer shift relative to metallic BaSnO<sub>3</sub> at 295 K; QS (mm/s) quadrupole splitting;  $\Gamma$  (mm/s) line-width; I relative area. Estimated errors  $\leq$ 0.02 mm/s for IS, QS,  $\Gamma$  and <2% for I.

The Mössbauer spectra of Sn, SnO and SnO<sub>2</sub> samples were also taken as reference samples in order to compare with those of the phases detected in the films by CEMS. The spectra of the reference samples reveal the typical spectra corresponding to  $\beta$ -Sn,  $\alpha$ -SnO and SnO<sub>2</sub>, respectively [59,60]. The  $\alpha$ -SnO spectrum reveals the typical air contamination due to the higher recoilless fraction of Sn<sup>4+</sup> in SnO<sub>2</sub> as compared to Sn<sup>2+</sup> in  $\alpha$ -SnO [61,62], besides the presence of the  $\alpha$ -SnO [60–63]. The spectra recorded were fitted by three contributions connected to isomer shifts (IS) of Sn<sup>4+</sup>, Sn<sup>2+</sup> and metallic Sn (see Table 1). The absorption peak due to metallic Sn is similar to that of the  $\beta$ -Sn, confirming its presence, which agreed with the XRD data. Moreover, the IS quadrupole splitting (QS) and the line widths of  $Sn^{2+}$  in the films before annealing are higher than the corresponding parameters for bulk  $\alpha$ -SnO. After annealing, the widths of Sn<sup>2+</sup> decrease, reaching values close to those of crystalline  $\alpha$ -SnO. This suggests that the Sn<sup>2+</sup> oxide present is amorphous before annealing, transforming into the crystalline form after annealing at 200 °C for at least 30 minutes. These data agree with those obtained from XRD for the same samples, showing that the films as-deposited are mainly composed of amorphous SnO and metallic  $\beta$ -Sn, with residual amounts of SnO<sub>2</sub>, which were only detected by CEMS. The SnO<sub>2</sub> IS and quadrupole splitting (QS) deduced differs from those of bulk SnO<sub>2</sub> which we attribute to the low degree of crystallinity of the films. Assuming that the recoilless factors of  $\beta$ -Sn, SnO and SnO<sub>2</sub> in films are not different for the same species in the different samples, the fraction of Sn atoms in each phase should follow the same trend, with annealing or with  $O_{pp}$  used. Indeed, the data recorded reveal that the fraction of Sn present as  $\beta$ -Sn is lower in the film deposited at higher  $O_{pp}$  (3.6%), than in those deposited at 3.0%. After annealing at 200 °C, the films crystallize leading to the formation of a strong  $\alpha$ -SnO phase which also contributes to the oxidation of  $\beta$ -Sn. Under these conditions, the  $SnO_x$  with 1 < x < 2, is the dominant phase of the channel layer with a small contribution from metallic tin, explaining the p-type transport behaviour observed.

#### 2.4. Electrical Data and Analysis

Hall Effect measurements were performed to identify the charge carrier and carrier mobility in the material. As we are in the presence of ambipolar material, as it is the case of  $SnO_x$  [64], electrons and holes will pile up at the same side of the sample and consequently the measured Hall voltage depends on the relative mobilities and concentrations of holes and electrons. Hall mobility for an ambipolar semiconductor is thus given by,

$$\mu_{Hall} = \frac{n \cdot \mu_n^2 - p \cdot \mu_p^2}{n \cdot \mu_n + p \cdot \mu_p} \tag{1}$$

where *n*, *p*,  $\mu_n$  and  $\mu_p$  represent electron density, hole density, electron mobility and hole mobility respectively. This leads to a reduction in the Hall mobility, compared to the mobilities of the charge carriers.

In the present study, the samples as deposited exhibit fluctuations in the sign and magnitude of the Hall coefficient, where the average mobilities of carriers were of about  $10^{-1}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>. After annealing up to 200 °C for 30 minutes, films prepared with 2.8% < O<sub>pp</sub> <3.8 show a positive Hall coefficient. This suggests a considerably large density of holes compared to the density of electrons, resulting in a positive Hall voltage with typical Hall mobility of 2 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> associated to the materials' evaluated.

Figure 2 shows the resistivity variation of  $SnO_x$  films for different  $O_{pp}$ , as deposited and after annealing at 200 °C, for different annealing times.



**Figure 2.** Resistivity of  $SnO_x$  films as a function of annealing time, for films processed at different  $O_{pp}$ , as depicted in the Figure.

The data show that the resistivity of the films processed tends to saturate around 30–40  $\Omega$ ·cm, for annealing times above 30 mn. The lowest annealing time is for samples processed with O<sub>pp</sub> above 3.20%, while the highest time (above 60 mn), for samples prepared with 2.80%< O<sub>pp</sub> <3.20%.

Annealing at temperatures above 200 °C cause again a decreasing tendency in material resistivity (not shown here) that can be associated with the phase transformation of the material from SnO (p-type) to SnO<sub>2</sub> (n-type). These data are consistent with those depicted in Figure 1b.

#### 2.5. Optical Data and Analysis

Figure 3a shows the optical transmittance data of the films processed for 2.80%<  $O_{pp}$  <3.20%, as deposited (RT) and after annealing at 200 °C, during 30 mn. The data depicted show that as  $O_{pp}$  increases the films become more transparent, as expected. As deposited, independent of  $O_{pp}$  used, the data depicted show, on average, transmittances below 20% in the visible region. These low values are attributed to the presence of large concentration of metallic tin in the films. By annealing the films, the optical transmittance in the visible region increases up to 55%, function of the  $O_{pp}$  used.



**Figure 3.** (a) Optical transmission of as prepared and annealed  $SnO_x$  films. (b) Plot for the estimation of the direct band gap estimation; Dependence of the estimated direct (c) and indirect (d) band gap on  $O_{pp}$  used, before and after annealing the films for 30 mn.

The optical band gap  $E_g$  of the films were determined by the relationship:

$$\alpha \cdot h \cdot \nu = const \cdot \left(h \cdot \nu - E_g\right)^r \tag{2}$$

where  $\alpha$  is the absorption coefficient,  $h\nu$  denotes the photon energy and r a constant depending on the type of optical transition expected. The  $E_g$  value is then obtained by linearly extrapolating the plot of  $(\alpha \cdot h \cdot \nu)^{1/r}$  versus  $h \cdot \nu$  and finding the intersection with the abscissa.

The optical data in Figure 3a were analysed with  $r = \frac{1}{2}$  (direct transition, for SnO, expected to be  $E_g \sim 2.5$  eV and for SnO<sub>2</sub>  $E_g \sim 3.6$  eV, see Figure 3b) and r = 2 (Indirect transition, for SnO  $E_g \sim 1$  eV). For the different O<sub>pp</sub> used, as deposited the direct band gap varies between 1.5 eV and 1.8 eV, while the estimated indirect band gap is kept around 0.6 eV. These values reflect the quasi metallic state of the films produced. After annealing, the films are better oxidized and the structure changes, as observed in Figure 1. Overall, we estimate a direct band gap with 2.6 eV  $\langle E_g \rangle$  2.75 eV, while the indirect band gap is 1.6 eV  $\langle E_g \rangle$  2.2 eV (see Figure 3c,d). These values are close to the reported bandgap values for SnO films, showing for the range of O<sub>pp</sub> used the SnO<sub>2</sub> phase does not dominate the optical characteristics

of the films produced. Small variations in these values could be understood on the basis of fractional variations of various phases (metallic tin, SnO and  $SnO_2$ ) in the films.

## 3. Devices Results and Analysis

Taking into a count the set of results obtained during the evaluation of the films processed, we centred our attention in evaluating the devices performances by using tin oxide channel layers processed close to the extremes of the  $O_{pp}$  window in which a clear p-type behaviour was observed after annealing, respectively for  $O_{pp} = 3.0\%$  ( $\approx 1.57$  sccm) and  $O_{pp} = 3.6\%$  ( $\approx 1.78$  sccm). To reduce the channel conductance, thus allowing a better modulation of the same, we reduced the channel layer thickness to values around 12 nm. A batch of more than 40 devices were evaluated and the devices performances varied within a standard deviation of about  $\pm 7\%$  from the average.

### 3.1. Devices Structure, Geometry, Fabrication and Characterization Conditions

Bottom gate TFTs were fabricated on glass substrates coated with 150 nm thick layer of sputtered ITO and a 220 nm thick layer of aluminium-titanium oxide (ATO). SnO<sub>x</sub> channel layer (width/length = 50 nm/50 nm and 12 nm thick) was deposited over this coating by r.f. magnetron sputtering at RT, using the same process conditions as reported before. Drain and source electrodes were based on Ni/Au (9 nm/60 nm) stack layers deposited by electron beam evaporation. After deposition, the devices were annealed in air up to 200 °C for 30 minutes.

Figure 4a–d show the SEM and AFM images of the surface morphology of the TFT channel layer 12 nm thick. The data depicted show that the shape of the microstructure of the grains obtained are similar, slightly increasing as  $O_{pp}$  increases, while the roughness decreases, respectively from 4.6 nm to 4.3 nm.



**Figure 4.** After annealing (60 mn) scanning electron microscope (SEM) images of  $SnO_x$  films processed at  $O_{pp} = 3.0\%$  (**a**)  $O_{pp} = 3.6\%$  (**b**) 3.6%, respectively. (**c**) and (**d**) show the corresponding AFM images. (**e**) Schematic illustration of  $SnO_x$  TFT structures fabricated. (**f**) Cross-sectional SEM image of the fabricated TFT.

Figure 4e is a schematic of the  $SnO_x$  TFT with a bottom gate configuration. Figure 4f shows the cross-section SEM image of the TFT prepared at 3.0%  $O_{pp}$ , revealing a perfect step coverage of the deposited layer (channel and drain/source contacts), highly compact, uniform and homogeneous, without visible defects.

TFT electrical characterization was performed with an Agilent 4155C semiconductor parameter analyzer (Santa Clara, CA, USA) and a Cascade Microtech M150 microprobe station (Livermore, CA,

USA) inside a dark box at ambient atmosphere. By doing so, we avoid problems that may arise from persistent photoconductive effects [65].

#### 3.2. Capacitance Measurements Data and Analysis

In order to better understand the role of the interfaces as well as of the dielectric on the TFT performances, CV measurements were directly performed on the TFTs by performing measurements between the gate electrode and drain and source short-circuited. The data were interpreted using an electrical model consisting of a contact resistance  $R_C$  (the same value for drain and source regions) in series with a combination of two parallel RC resonators as shown in the sketch of Figure 5a. One of the resonators represents the semiconductor channel capacitance ( $C_S$ ) that varies dynamically, depending on the extension of the accumulation/depletion layer. The other component is the interface trap capacitance ( $C_{it}$ ) in series with the corresponding associated interface resistance  $R_{it}$ , both depending on the interface defects given by:

$$C_{it} = \frac{\rho(V)}{\frac{dV}{dx}} = \varepsilon \varepsilon_0 \frac{\rho(V)}{Q} = \frac{q^2 D_{it}}{1 + \omega^2 \tau_{it}^2}$$
(3)

where  $D_{it}$  is the interface trap density,  $\tau_{it} = R_{it} \times C_{it}$  is the trap response time. Finally, we have in series the insulator geometric capacitance ( $C_{ox}$ ). As the frequency tends to a steady state condition, we have almost  $C_{it}$  in parallel with  $C_s$  and the resulting capacitance in series with  $C_{ox}$ . Therefore, for non-perfect semiconductors (basically, the amorphous ones), by using a frequency modulation less than the relaxation frequency of the semiconductor ( $f_r = \frac{1}{2\pi R_B C_s} = \frac{1}{2\pi \rho_B \varepsilon_s \varepsilon_0}$ , where  $R_B$  is the channel bulk resistance), we expect that capacitance will be influenced by the number and nature of the interface defects, their length and depth extension which determines the way in which the structure responds to the electrical stimulus in the low frequency regime. On the other hand, at very high frequencies,  $C_s$  dominates and  $C_{it} \cong 0$ , being now relevant the role of  $R_{it}$  in parallel with  $C_{ox}$ . In this case the capacitance-voltage curves can be distorted due to charging effects, leading to a decrease or even to a not well-defined flat capacitance maximum ( $C_{max}$ ), as observed in the normalized C-V plots of Figure 5b for different frequencies and on the behaviour of  $C_{max}$  with the frequency, depicted in Figure 5c. Figure 5b also shows the transfer characteristics of the TFT under analysis, where the hysteresis behaviour recorded is visible, which we associate with the role of interface defects.

Figure 5c shows the dependence of the maximum capacitance recorded on the frequency. There, we notice that at frequencies below 100 Hz the capacitance tends to reach flat behaviour while the hysteresis voltage shift is enhanced, following a similar trend as that of the I-V TFT transfer characteristics. We associate this behaviour with interface localized states that respond at frequencies below  $f_r$ .

The analysis of the C-V plots shows that the minimum capacitance is not fully flat. This behaviour is attributed to the small thickness of the semiconductor ( $\leq 12$  nm), which limits the extension of the depletion region. As the possible maximum width of depletion region is 12 nm (the semiconductor thickness), this means that the minimum capacitance of the system will not be much lower than the total capacitance. We also estimate the flat band voltage shift and the oxide charge density.



**Figure 5.** (a) Cross section sketch of the TFT, where t is also shown the equivalent electrical circuit based on RC resonators. (b) Normalized C-V plot taken for different frequencies (below) and the IV transfer characteristic of the TFT (above); (c) Dependence of the maximum capacitance ( $C_{max}$ ) achieved on the frequency used.

Figure 6 shows the dependence of these parameters on the frequency, for the upward and downwards sweeps, in order to take into account the hysteresis observed. For the set of calculations performed, it was considered that the level of acceptor concentration ( $N_a$ ) was in the range of  $10^{17}$  cm<sup>-3</sup> with a good work function match between the gate electrode and the semiconductor.



**Figure 6.** (a) Flat band Voltage dependence on the frequency; (b) Oxide charge density as a function of the frequency. The upper curves correspond to the upwards sweep while the lower curves to the downwards sweep (see Figure 5b).

Overall the data depicted show an enhancement on the flat band voltage and on the oxide charge density as the frequency decreases.

Figures 7 and 8 show the TFT electrical characteristics of the two extreme cases evaluated, as processed, and after 50 days as a way to determine their stability (devices ageing effects).



**Figure 7.** (a) Output characteristics of SnO<sub>x</sub> p-channel TFT. The gate voltage is varied from 0 V to -50 V in -10 V steps. (b) Transfer characteristics of SnO<sub>x</sub> p-channel TFT with different channel thickness. (c) Plot of square root of drain current, at V<sub>DS</sub> = -30 V, for evaluating saturation mobility and threshold voltage. (d) Transfer characteristics of SnO<sub>x</sub> p-channel TFT (channel thickness 12 nm) for different annealing time.



**Figure 8.** Transfer characteristics of  $SnO_x$  p-channel TFT measured at different days after device fabrication (**a**) and corresponding variations in saturation mobility and threshold voltage (**b**).

Figure 7a shows the output characteristics ( $I_{DS}$ - $V_{DS}$ ) of such TFT produced at  $O_{pp}$  = 3.0%. The gate voltage was varied from 0 V to -50 V in -10 V steps. Very small  $I_{DS}$  at zero gate voltage indicates

an almost closed channel. On increasing the gate voltage to higher negative values, holes accumulated at the channel-insulator interface forms a conduction path between source and drain. These TFTs exhibit hard saturation at large  $V_{DS}$ , which is similar to pinch off in the usual field-effect transistors, revealing the high quality of the devices fabricated.

Figure 7b shows the transfer characteristics of the same TFT, as above, but now using two different thicknesses for the channel layer, 12 nm and 28 nm respectively. The data depicted reveal that by decreasing the channel thickness the On/Off ratio improves from  $\sim 10^2$  to  $7 \times 10^4$ , while the subthreshold swing voltage (the slop of the transfer curve when the current goes from the Off state to the On state) is reduced by more than a factor of 3. This allows us to select 12 nm as the best device thickness as stated before.

Figure 7c shows the plot of the square root of the absolute value of the drain current, at  $V_{DS} = -30$  V as a function of  $V_{GS}$ , for the same samples depicted in Figure 7b, for evaluating saturation mobility and threshold voltage, respectively. The data depicted show that irrespective of the channel layer thickness, the saturation mobility achieved is around 4.6 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, while the threshold voltage is shifted from 8.1 V to -10 V on reducing the channel thickness from 28 nm to 12 nm, respectively. Negative threshold voltage indicates the enhancement mode operation of the p-channel TFTs, as required to keep the channel closed when no voltage is applied to the gate.

Figure 7d shows the dependence of the absolute value of  $I_{DS}$  [ABS( $I_{DS}$ )] as a function of  $V_{GS}$  for devices fabricated using  $O_{pp}$  equal to 3% and 3.6%, respectively and heat treated at 200 °C during 30 mn and 60 mn, respectively. Table 4 shows the TFT parameters extracted from Figure 7d, where the dominant phase composition of the films processed is also shown, as revealed by the difractograms in Figure 1. The data show that the most stable devices with the best device performances are achieved when using an  $O_{pp}$  of about 3% and an annealing time of around 30 minutes, where the main dominant phase is just attributed to  $\alpha$ -SnO. On the other hand, the films processed at  $O_{pp} \ge 3.6\%$  reveal a growing role of the  $\beta$ -SnO phase and so increase the ambipolar behaviour of the films processed.

Annealing Conditions	Oxygen Partial Pressure (%)	Field Effect Mobility $(cm^2 V^{-1} s^{-1})$	Saturation Mobility (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> )	Threshold Voltage (V)	On-Off Ratio	Dominant Composition Phase
200 °C, 30 min	3.0	3.3	4.6	-10	$7 imes 10^4$	α-SnO
200 °C, 60 min	3.0	2.2	2.6	-7.2	$9  imes 10^4$	α-SnO
200 °C, 30 min	3.6	0.16	0.28	-29	$2\times 10^5$	α-SnO + β-SnO
200 °C, 60 min	3.6	0.02	0.03	-38.6	$3 imes 10^4$	α-SnO + β-SnO

**Table 4.** Electrical properties of  $SnO_x$  p-channel TFTs for different annealing time (channel thickness 12 nm). After annealing all structures are polycrystalline.

Figure 8 shows the transfer curves of TFTs fabricated using  $O_{pp} = 3\%$  and  $O_{pp} = 3.6\%$ , measured along consecutive 50 days after their fabrication. The data show that the TFTs are very stable in operation, without any significant variation on On/Off ratio, threshold voltage and mobility.

## 4. Discussion of the Results

The analysis of the structure, composition and morphology of the films processed, together with the evaluation of their electrical and optical performances, allow us to select the best process conditions to produce high stable and reliable p-type tin oxide films by RFMS at RT, surpassing the existing state of the art knowledge, as shown in Table 1. The data shown in Figure 1 reveal a structure in which the metallic tin dominates over the SnO phase, as also confirmed by Mössbauer spectroscopy data. This suggests that in the  $\alpha$ -SnO phase, the Sn<sup>2+</sup> oxide present is amorphous. After annealing in air, the metallic tin ( $\beta$ -Sn) is oxidized leading to the SnO<sub>x</sub> (1 < x <2) phase formation, where now the Sn<sup>2+</sup> oxide present is crystalline, with a strong  $\alpha$ -SnO phase for which the minimum heat treatment time required is of about 30 min. To reach this goal O<sub>pp</sub> of  $\geq$ 2.8% is needed which corresponds with the use of an oxygen gas flow above 1.46 sccm.

Below an oxygen gas flow of 1.46 sccm, films are metallic in nature and adhesion to the glass substrate was very poor.

On the other hand, if  $O_{pp} > 3.8\%$ , which corresponds with the use of an oxygen gas flow above 1.89 sccm, the films are highly resistive (>10<sup>8</sup>  $\Omega$ ·cm), decreasing substantially after annealing, with SnO<sub>2</sub> being the dominant phase. In these conditions, films exhibit an n-type conduction behaviour. This clearly favours the ambipolar behaviour, as broadly observed [38,42,51,53].

Since we used a metallic tin target for sputtering, very low  $O_{pp}$  was not sufficient to oxidize the film. The experimental data show that a stable SnO phase is only obtained if used during the deposition process of an oxygen gas flow in the range of 1.46–1.89 sccm (2.8% <  $O_{pp}$  <3.8%.), after heat treatment at 200 °C for 30 minutes. This corresponds to producing films with a resistivity in the range of 30–40  $\Omega$ .cm (see Figure 2). On the other hand, the use of high oxygen gas flow (more than 1.89 sccm) favours SnO<sub>2</sub> formation. That is, we can use the same material and, by proper control of the process parameters such as  $O_{pp}$  and gas flow, turn it into an n-type or p-type semiconductor [51,53].

The optical data shows that the transparency in the visible range for films as deposited is below 20%, increasing as O<sub>pp</sub> increases. Moreover, the heat treatment enhances the optical transparency by about 3 times, proving that under these conditions the oxidation phase dominates over the metallic one (see Figure 3). The estimated bandgap value for the films deposited using oxygen flow in the range of 1.46–1.89 sccm was around 2.6 eV (see Figure 3). This agrees with the reported direct bandgap value of 2.7 eV, associated with the SnO dominant phase.

The study described above allowed us to select the best process conditions to grow p-type tin oxide films as being those for which  $O_{pp} = 3\%$ . Moreover, allow us also to observe that the thickness of the films plays a relevant role in determining the electrical modulating behaviour of the channel, as also observed in other works [48]. This led us to select the proper thickness of the channel layer as being 12 nm, as shown in Figure 4.

The analysis of the capacitance measurements realized on the TFT (pad contact area of about 100  $\mu$ m × 100  $\mu$ m) shows that the capacitance reaches a flat maximum for frequencies below 100 Hz, which corresponds to a value of about 23.8 nF/ $\mu$ m<sup>2</sup>. This allowed us to infer the saturation mobility [15]. Here, the reduced channel thickness ( $\leq 12$  nm), limits the extension in which the channel is depleted and also its modulation extension. The hysteresis observed is attributed to the role of interface localized states in responding to electrical stimulus below the relaxation frequency  $f_r$ . Moreover, from these measurements we could estimate the flat band voltage shift and the oxide charge density (see Figure 6) as being in the range from 13–15 V and 5 × 10<sup>12</sup>–6 × 10<sup>12</sup> C/cm<sup>3</sup>, for the low frequency regime, shifting towards 9–10 V and 3.5 × 10<sup>12</sup>–4 × 10<sup>12</sup> C/cm<sup>3</sup>, respectively for the high frequency regime, where shallow states do not respond to the electrical stimulus [15].

The analysis of the electrical characteristics of the TFT depicted in Figures 7 and 8 show that p-channel oxide TFTs manufactured at RT, followed by intentional heat treatment at 200 °C, using a narrow process window associated with the oxygen gas flow used are highly reproducible, reliable and stable. In addition, they all work in the enhancement mode, exhibiting very good electronic performance, translated by high mobility and On/Off ratio, together with a relative low threshold voltage. The annealing temperature used is suitable for fabricating these devices on plastic or even on paper substrates [7], which cannot be the case when using heat treatment much above 200 °C [29–32]. The data depicted clearly show that the films developed throughout this study are among the best ever produced, as can be seen in Tables 1 and 2, irrespective of the process technique used. Moreover, the very high On current of these devices makes them ideal for fabricating active matrix OLED driving circuits, where a TFT must supply sufficient hole current to the anode of the OLED. Use of an n-channel TFT results in a voltage drop over the OLED, which affects the drain current of the TFT. However, it does not affect the drain current of a p-channel TFT in the saturation mode.

# 5. Conclusions

In summary, we have fabricated highly reproducible high-performance p-channel oxide TFTs on glass substrates using an SnO<sub>x</sub> channel layer, for which the proper process conditions were selected. The SnO phase was identified and quantified by two independent techniques, XRD and Mossbauer spectroscopy, corroborating the p-type oxide semiconductor behaviour obtained, for films grown at low O<sub>pp</sub> (around 3%), where the dominant phase is due to  $\alpha$ -SnO. The TFTs fabricated show typical saturation mobility of 4.6 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and On-Off ratio > 7 × 10<sup>4</sup>, with threshold voltages of about -10 V, indicating that the devices work in the enhancement mode. This is one of the best stable electrical performances achieved so far for p-type oxide TFTs processed at RT and heat treated at temperatures around 200 °C, as the survey conducted concerning the present state of the art in producing p-type TFT based on tin oxide shows (see Tables 1 and 2). This will enable the fabrication of fully transparent CMOS either on rigid or flexible substrates, associated with all the advantages offered by transparent/oxide electronics.

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