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Letter

Effects of Charge Trapping at the MoS_2–SiO_2 Interface on the Stability of Subthreshold Swing of MoS_2 Field Effect Transistors

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Abstract: The stability of the subthreshold swing (SS) is quite important for switch and memory applications in logic circuits. The SS in our MoS_2 field effect transistor (FET) is enlarged when the gate voltage sweep range expands towards the negative direction. This is quite different from other reported MoS_2 FETs whose SS is almost constant while varying gate voltage sweep range. This anomalous SS enlargement can be attributed to interface states at the MoS_2–SiO_2 interface. Moreover, a deviation of SS from its linear relationship with temperature is found. We relate this deviation to two main reasons, the energetic distribution of interface states and Fermi level shift originated from the thermal activation. Our study may be helpful for the future modification of the MoS_2 FET that is applied in the low power consumption devices and circuits.

Keywords: transition metal dichalcogenides (TMDCs); MoS_2 FET; hysteresis; subthreshold swing; interface states

1. Introduction

Recently, transition metal dichalcogenides (TMDCs) are leading the trend of studying various two-dimensional (2D) materials. In particular, MoS_2, which is a representative of the TMDCs, presents an indirect bandgap of 1.29 eV for the bulk form and transforms to direct band semiconductor (bandgap of 1.8 eV) as the number of layers decreases to one [1,2] Additionally, for a top gate MoS_2 FET, the on/off ratio is up to 10^9 and the subthreshold swing of is as low as 65 mV/decade, which is comparable to that of its opponent SOI MOSFET, compared to typical values of 10^6 and close to 80 mV/decade of conventional Si CMOS technology, making MoS_2 quite suitable for use in switches, logic circuits, amplifiers, and low power dissipation circumstances [3–7].

However, as a 2D material, because of the extremely high surface-to-volume ratio, the properties of MoS_2 FETs, such as threshold voltage, hysteresis, on/off ratio, and *SS*, can be easily affected by interface states at the interface between the MoS_2 channel and the gate dielectric [5,8]. During the sweep of gate voltage, the interface states are electrically equivalent to an additional capacitance which is first in parallel to the semiconductor capacitance, and their result is then series to the oxide capacitance by exchanging electrons with the MoS_2 channel, thus sabotaging the stability of MoS_2 FETs. Among the device performance stability issues caused by the interface states, the enlargement of *SS* will slow down the switch speed and hugely increase the static power consumption of FETs, which will hinder the use of MoS_2 FETs in low-power applications [9,10].

SS is normally considered to have a linear relationship with temperature. This might be valid for top gate FETs whose gate dielectric capacitance is large enough so that the influence of interface states capacitance (C_{it}) could be ignored. However, for research concerns, a back gate metal-oxide-semiconductor (MOS) structure based on SiO_2 dielectric is usually adopted to study the basic properties of MoS_2 FETs whose *SS* is typically more than 1000 mV/dec [11]. Note that the *SS* can be hugely decreased by replacing SiO_2 with a high-k dielectric [12].

Thus, for the first time, an obvious deviation of *SS* from its linearity with temperature is observed for the backgated MoS_2 FET with 300 nm SiO_2 dielectric. We explain this anomalous phenomenon with the energetic distribution of interface states density and the temperature induced Fermi level shift. According to these results, *SS* stability of the devices critically relies on a rational design of gate dielectric.

2. Experiments

In our study, with the scotch tape method [13,14], the device was prepared by mechanically exfoliating MoS_2 thin films onto 300 nm SiO_2 grown on low resistive Si substrate. Drain and source electrode pads of Ti/Au (10/100 nm) were formed through e-beam lithography, e-beam evaporation and lift-off processes in sequence. Figure 1a,b show the schematic view and colored SEM (Tescan, Brno, Czechoslovakia) image of the fabricated MoS_2 FET. The channel length and width of the device were about 3 µm and 5 µm, respectively. The thickness of the MoS_2 film was about 4 nm measured using a Park Systems' atomic force microscope (AFM, Park Systems, Hyderabad, India) as shown in Figure 1c,d. The MoS_2 FET was placed in a shielded probe station under vacuum condition (less than 10^{-5} mbar) in order to minimize the influence of water and oxide molecules in ambient air. All electrical transport characteristics were measured using an Agilent B1500 semiconductor parameter analyzer (Agilent, Santa Clara, CA, US) under dark conditions. The transfer characteristics were obtained by sweeping V_{BG} from a negative gate voltage $V_{BG, min}$ to a positive gate voltage $V_{BG, max}$ (forward sweep), and then back to $V_{BG, min}$ (backward sweep) again at a constant V_{DS} = 1 V at room temperature. Wherein, $V_{BG, max}$ was fixed at 50 V and $V_{BG, min}$ was varied from −50 V to −80 V in steps of −10 V for each measurement, respectively.

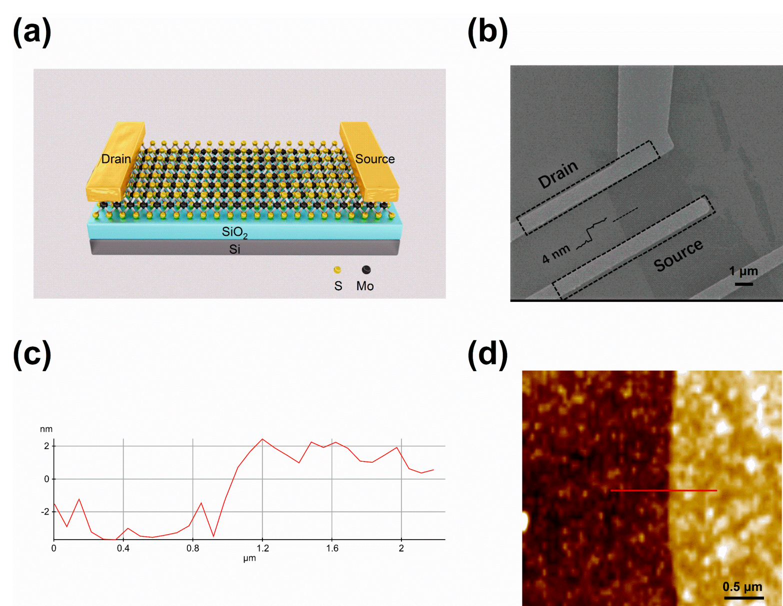

Figure 1. (**a**) Schematic of the fabricated MoS_2 FET. (**b**) SEM image of the MoS_2 FET. The drain and sources are indicated by dashed boxes. (**c**,**d**) AFM profile revealing the MoS_2 thickness along the red line.

3. Results and Discussions

Figure 2a represents the transfer curves of the MoS_2 FET measured at 310 K with varying $V_{BG,\,min}$s. With $V_{BG,\,min}$ varied from −50 V to −80 V, the threshold voltage (V_{TH}) of the device negatively shifted for both forward sweep and backward sweep. For forward sweeps, the threshold voltage of the device shifted from −30 to −43 V. For backward sweeps, the threshold voltage of the device shifted from −23 to −35 V. Meanwhile, the hysteresis of the device increased from 5 to 9 V. For MoS_2 FETs, threshold voltage shift and hysteresis are mainly caused by the interface states acting as charge traps at the MoS_2–SiO_2 interface. These interface states are the result of dangling bonds formed at the surface of SiO_2 during the growth process of SiO_2. By exchanging electrons with the MoS_2 channel, the interface states can be viewed as a "impurity band" in the MoS_2 bandgap [15,16]. At 310 K, as the gate voltage sweeps from $V_{BG,\,min}$ to 50 V, the conduction band bends downward relative to the Fermi level. The positions of the Fermi level corresponding to $V_{BG,\,min}$s of −50 to −80 V are shown, respectively, in the inset of Figure 2a. As the gate voltage increases, a part of energy levels of the interface states will be swept over by the Fermi level. This will cause the charge traps to capture/release electrons. When the energy levels of the interface states are below the Fermi level, it indicates the energy level are occupied by electrons as shown in Figure 2b. When the energy levels of the interface states are above the Fermi level, electrons that used to be trapped in these interface states tend to get de-trapped, as shown in Figure 2c. When a negative gate bias is applied at the beginning of forward sweep, a portion of electrons are released to the MoS_2 channel, the empty traps become positively charged. This will weaken the depletion of the MoS_2 channel, because the positive charges will partially "screen" the negative gate voltage. The threshold voltage will then negatively shift. For a more negative $V_{BG,\,min}$, more positive charges will be present. Then, it will require a more negative gate bias to depletion the MoS_2 channel. Therefore, the threshold voltage will keep on shifting to the negative direction. As for the hysteresis, because we used a constant gate voltage sweeping rate of 2 V/s, the accumulation time interval in one gate voltage sweep cycle is 50 s. The depletion time interval from $V_{BG,\,min}$ to 0 V in the forward sweep is shorter than the accumulation time interval, even for the $V_{BG,\,min}$ of −80 V condition. Together with the fact that the de-trapping process is much lower than electron movements in the MoS_2 channel [8], the refilled traps during the accumulation process will partly screen the negative gate voltage and cause a positive shift of V_{TH}. Thus, the hysteresis occurs.

Like hysteresis and threshold voltage shift, *SS* shift can also be attributed to the interface states. However, the *SS* shift can hardly be observed without gate bias stressing [17], because the density of states (DOS) distribution of interface states is seldom considered. In this study, DOS distribution of the interface states is assumed to coincide with Gaussian distribution and its maximum value is located at a few tens of meV below the conduction band, as shown in Figure 2 [15,18,19]. For both forward sweeps and backward sweeps, as the gate voltage sweeping range expands, the *SS* of the device is enlarged because more traps are depleted or in other words "activated" when larger negative gate bias is used. *SS* increases from 2188 to 2898 mV/dec for forward sweeps. *SS* increases from 648 to 1550 mV/dec for backward sweeps. For forward sweeps, the interface states density (D_{it}) is extracted to be 2.64×10^{12} $eV^{-1}cm^{-2}$ for $V_{BG,\,min}$ of −50 V, and D_{it} is extracted to be 3.49×10^{12} $eV^{-1}cm^{-2}$ for $V_{BG,\,min}$ of −80 V, by using the following equations [20]:

$$SS = \ln 10 \times kT/q \times (1 + C_{it}/C_{OX}) \quad (1)$$

$$D_{it} = C_{it}/q^2 \quad (2)$$

where k is the Boltzmann's constant, T is the measurement temperature, q is the electron charge, and C_{ox} is the gate dielectric capacitance density which is 11.5 nF/cm^2 ($C_{ox} = \varepsilon_0\varepsilon_r/d$; $\varepsilon_r = 3.9$; $d = 300$ nm) for the MoS_2 FET.

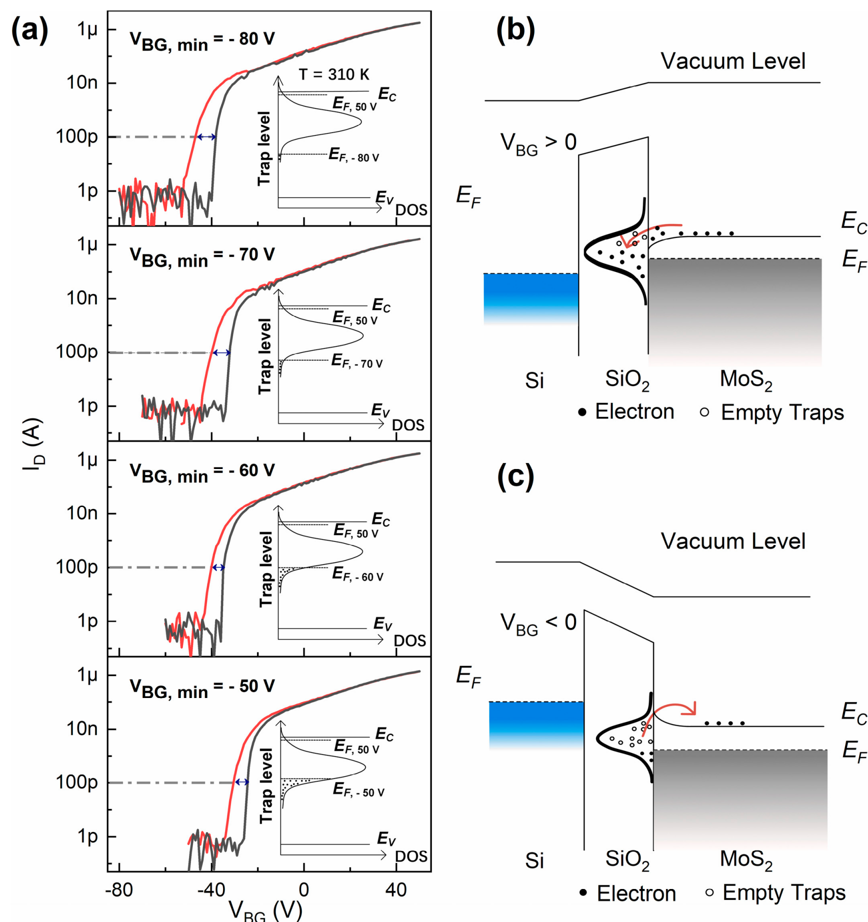

Figure 2. (**a**) The transfer curves for forward sweep (red line) and backward sweep (black line) measured at 310 K. The hysteresis is selected as the voltage shift between the transfer curves of the forward sweep and the backward sweep at I_{DS} = 100 pA, which is indicated by a double-headed arrow. The inset shows the positions of the Fermi level corresponding to $V_{BG,\,min}$s of −50 to −80 V, respectively. (**b**,**c**) The band structure of MoS_2 channel considering the interface states at the MoS_2–SiO_2 interface.

To further study the mechanism of the SS shift, we conducted transfer characteristics measurements at a series of temperatures. Figure 3a,b show the transfer curves for $V_{BG,\,min}$s of −50 V for forward and backward sweeps, respectively, in a temperature range from 10 to 310 K. The V_{TH} shifts negatively as temperature increases. The transfer curves for $V_{BG,\,min}$s from −60 to −80 V in steps of −10 V with constant V_{DS} = 1 V were also measured. The relationship between V_{TH}, temperature, and $V_{BG,\,min}$ is extracted and illustrated in Figure 3c,d for forward and backward sweeps, respectively. For more negative $V_{BG,\,min}$s, the V_{TH} shift enlarges more abruptly compared to less negative $V_{BG,\,min}$s when the temperature is above 100 K, which means the "screening" mentioned above becomes stronger above 100 K. No gate bias stressing is applied in this experiment, therefore the electron exchange between the MoS_2 channel and interface states is incomplete. For more complete delegation by larger gate bias, the "effective" D_{it} is higher. As the unoccupied traps are positively charged, the electrons in the MoS_2 channel will suffer from Coulomb scattering. We have $\sigma_{DS} \propto n^{\alpha}$, wherein σ_{DS} the conductance of the MoS_2, $1 \le \alpha \le 2$ is the coefficient that reflects the screening of Coulomb scattering. If the Coulomb scattering is fully screened, then $\alpha = 1$. For bare Coulomb scattering, $\alpha = 2$. As $I_{DS} \propto \sigma_{DS}$, $V_{BG} - V_{TH} \propto n$, the coefficient α is the slope of $\ln I_{DS}$ versus $\ln(V_{BG} - V_{TH})$ [8]. By calculating the data from Figure 3a,b, we obtain a minimum α of 1.56 for $V_{BG,\,min}$ of −80 V and a maximum α of 1.72 for $V_{BG,\,min}$ of −50 V at 310 K. The fact that more negative $V_{BG,\,min}$ corresponds to weaker Coulomb scattering indicates the extra electrons depleted to the MoS_2 channel by the larger $V_{BG,\,m}$ (more negative)

is more effective on screening the Coulomb scattering caused by the unoccupied traps than causing more severe scattering. This also suggests large amount of interface states intrinsically exist at the MoS_2/SiO_2 interface.

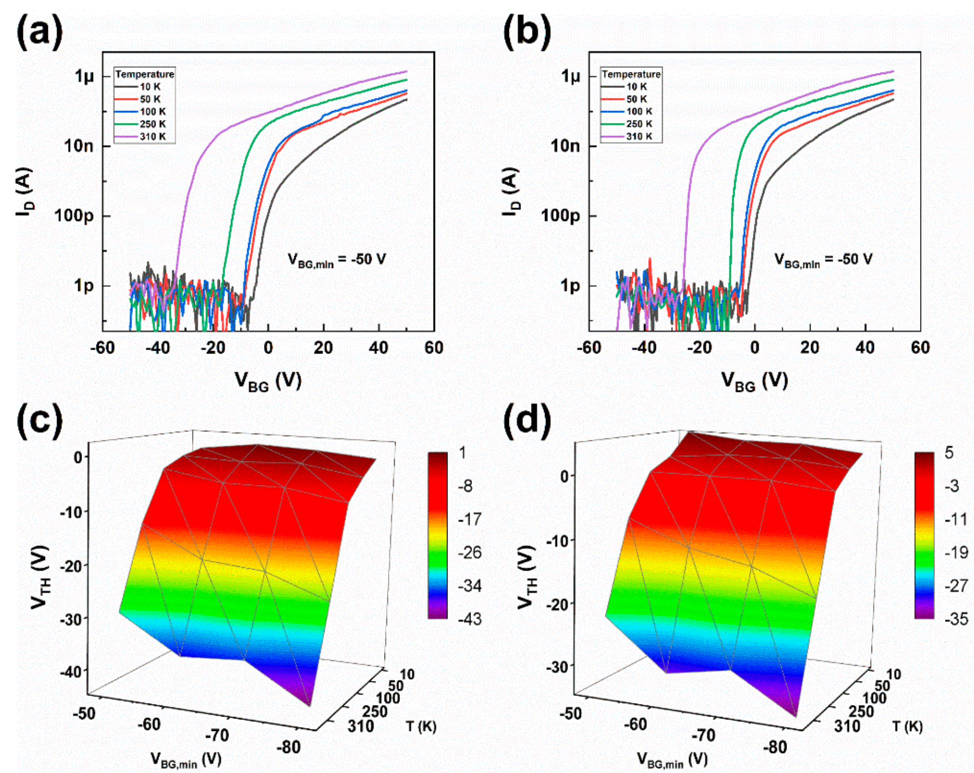

Figure 3. Transfer curves at a series of temperatures (10–310 K) for forward sweep (**a**) and backward sweep (**b**), respectively. Relationship between V_{TH}, $V_{BG,\,min}$, and temperature for forward sweep (**c**) and backward sweep (**d**), respectively.

Figure 4a,b show the relationship between *SS* and temperature extracted from Figure 3a,b for forward sweep and backward sweep, respectively. Normally, *SS* should have a linear relationship with temperature. However, for forward sweeps, for $V_{BG,\,min}$ of −50 V, the *SS* versus *T* curve increased from 10 K and reached a maximum mV/dec at 50 K, then dropped to a minimum at 100 K, and began to increase linearly above 100 K. The *SS* versus temperature curve presents an abnormal bulge in the temperature range of 10 to 100 K. For $V_{BG,\,min}$ of −60 V, the bulge expands to 250 K and *SS* begins to increase linearly from there on. As $V_{\mathrm{BG,\,min}}$ further decreases to −70 V, the bulge expands at least to 310 K. For $V_{BG,\,min}$ of −80 V, the range of the bulge is similar to that for $V_{BG,\,min}$ of −70 V. Although for $V_{BG,\,min}$s of −70 and −80 V, the *SS* does not show a linear increase in the temperature range of this experiment; we believe the *SS* will still begin to increase linearly at a higher temperature. For backward sweeps, the range of the bulge is almost the same for each $V_{BG,\,min}$. The *SS* curves all begin to increase linearly at around 250 K. Moreover, the scale of the bulge is even larger for small $V_{BG,\,min}$s compared to forward sweeps. For this abnormal deviation of *SS* from linearity with temperature, the energetic distribution of interface states density and the temperature induced Fermi level shift mechanisms are adopted to explain it.

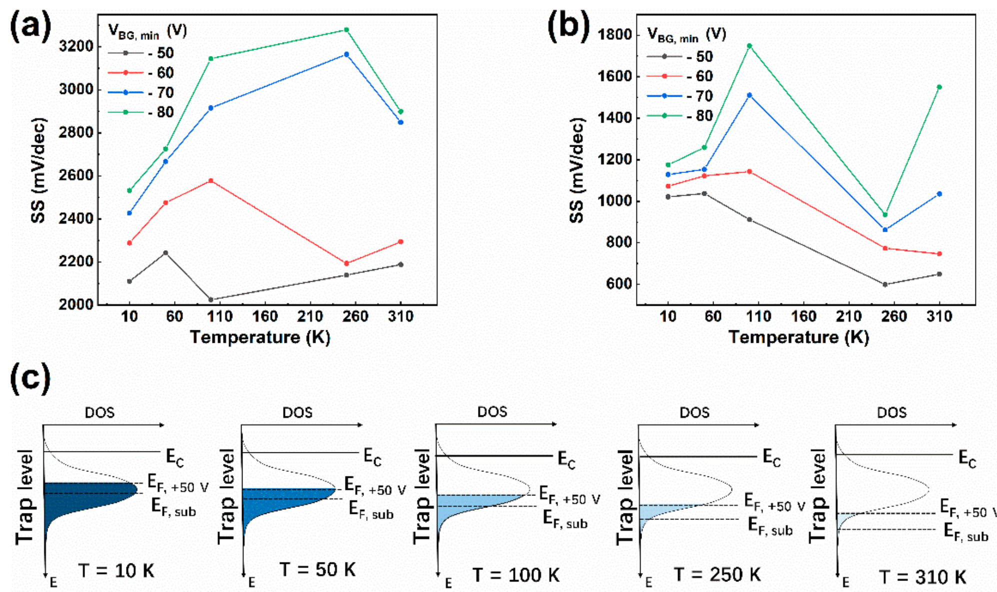

Figure 4. Relationship between *SS* and temperature for forward sweep (**a**) and backward sweep (**b**), respectively. (**c**) Schematic of Fermi level shifting progress of MoS_2 channel relative to the interface states and conduction band caused by the increasing of temperature from 10 to 310 K for $V_{BG, min}$ of −50 V. $E_{F, +50 V}$ and $E_{F, sub}$ correspond to the Fermi level for gate voltage of +50 V and subthreshold voltage, respectively.

Due to the trapping and releasing processes of electrons in the traps, the interface states can be viewed as a capacitor. The capacitance C_{it} is determined by the density of the interface states D_{it}. Thus, D_{it} is the key to study this abnormal relationship between *SS* and temperature. As we assume D_{it} has Gaussian distribution as shown Figure 2, it can be written as

$$D_{it}(E) = D_{it,\ max}(E) \times f(E) \tag{3}$$

and $f(E)$ in Equation (3) can be written as

$$f(E) = \exp\left[-4 \times \log 2 \times \left(\frac{E_F(T) - E_D}{\text{FWHM}}\right)^2\right] \tag{4}$$

where in $D_{it,\ max}(E)$ is the maximum value the D_{it} can reach during the shift of Fermi level as temperature increases, $E_F(T)$ is the location of Fermi level as a function of temperature, and $f(E)$ is the energetic distribution function of the interface states [19,21]. $f(E)$ represents the possibility that a certain energy level is occupied. *FWHM* is the full width at half maximum of D_{it}. On the other hand, because of the activation of bulk charge traps (including bulk MoS_2 trap charges, fixed oxide charges, and oxide trap charges inside a thick SiO_2 insulator) and interface states [22], the location of the Fermi level can be modulated by temperature and can be expressed as

$$E_F = (E_C/E_D)/2 + (kT/2)\ln(N_D/2N_C) \tag{5}$$

$$E_F = E_C + kT\ln(N_D/N_C) \tag{6}$$

corresponding to low temperature weak ionization region (Equation (5)) and high temperature strong ionization region (Equation (6)), wherein E_C, N_C, and N_D are the bottom of the conduction band, effective density of states of conduction band, and donor concentration of the interface states for MoS_2, respectively. As shown in Figure 4c, the position of the Fermi level corresponding to subthreshold

situation ($E_{F,\,sub}$) shifts downward relative to the energy levels of the interface states when temperature increases from 10 to 310 K. Thus, the D_{it} corresponding to $E_{F,\,sub}$ will change with temperature.

Due to the Gaussian distribution, D_{it} has a maximum value $D_{it,\,max}$. For a certain temperature, the more the Fermi level approaches $D_{it,\,max}$, the larger the *SS* is and vice versa. When substituting above Equations (2)–(6) back into Equation (1), the expression of *SS* can be written as

$$SS = q\ln 10 \times kT \times D_{it,\,max}(E) \times \exp\left[-4 \times \log 2 \times \left(\frac{E_F(T) - E_D}{\mathrm{FWHM}}\right)^2\right] / C_{OX} + kT/q \times \ln 10 \quad (7)$$

The deduced expression for *SS* has two terms. The first term is a nonlinear term which corresponds to the depletion of interface states by the gate voltage, and the second term is a linear term which is only affected by temperature. Taking the situation for $V_{BG,\,min}$ of −50 V as an example, for forward sweep, from 10 to 50 K, D_{it} corresponding to $E_{F,\,sub}$ increases rapidly. Thus, the nonlinear term of Equation (7) dominates and the *SS* curve begins to increase and deviate from linearity. After 50 K, as $E_{F,\,sub}$ passed $D_{it,\,max}$, the nonlinear term begins to decrease. If the increasing of the linear term and the decreasing the nonlinear term reach an equilibrium, the *SS* will saturate. When temperature continues to increase, the drop down of D_{it} will experience an acceleration. The nonlinear term will dominate again during this fast drop and *SS* will drop with it. When the decrease of D_{it} slows down at a position that is far from $D_{it,\,max}$, another equilibrium with the linear term will be accomplished. Thus, *SS* will reach a minimum. As the temperature further increases, the linear term will dominate and the nonlinear term will be negligible. The *SS* will increase linearly along with the linear term. When $E_{F,\,sub}$ shifts downward as temperature increases, because the effective D_{it} is actually higher compared to the situation for $V_{BG,\,min}$ of −50 V, the *SS* will be generally larger, as can be seen in Figure 4a,b and the shift of $E_{F,\,sub}$ will be slowed down in the temperature dimension because more traps have to be thermally activated. Then the maximum or minimum of *SS* will be achieved at higher temperatures. The above discussion also explained why the deviation from linearity is hardly observed for small gate voltage sweep ranges (e.g., from −30 V to 30 V) in which case the effect of the nonlinear term is too small and is covered up by the linear term. For backward sweep, because the traps refilled when the gate voltage is positive have not fully de-trapped yet. Then, effective D_{it} becomes smaller compared to forward sweep. The *SS* for backward sweep is thus generally smaller than that for forward sweep. This result coincides with the fact that the V_{TH} shift for backward sweep is generally smaller than that for forward sweep, which also originates from the more incomplete depletion of interface states for backward sweep. From the above discussion, we can infer that the *FWHM* of D_{it} is important for whether the deviation of *SS* from linearity can be observed. If the *FWHM* is small enough, the distribution of D_{it} can be viewed as a step function. The slope of *SS* will change abruptly to another value at a certain temperature as is observed by Park et al. [22,23]. However, if the *FWHM* is large, the situation will become what we observed for our MoS_2 FET.

4. Conclusions

In conclusion, we have investigated the *SS* instability with temperature of back-gated multilayer FET device induced by interface states in the temperature range of 10–310 K. We found that the relationship between *SS* and temperature will deviate from linearity if the energetic distribution of the interface states is abroad enough. Because of the Fermi level shift with temperature induced by the terminal activation of bulk charge traps and interface states, and broad interface states density distribution, the capacitor effect of the interface states can greatly influence the *SS* instability with temperature. Moreover, we can potentially predict the relationship between *SS* and temperature for MoS_2 FETs with other interface states situations. Our study is helpful for understanding interface properties of MoS_2 FETs and has important implications for gate dielectric material modification for low power applications based on MoS_2.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Mak, K.F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T.F. Atomically thin MoS_2: A new direct-gap semiconductor. *Phys. Rev. Lett.* **2010**, *105*, 136805. [CrossRef] [PubMed]
2. Parthé, E.; Gmelin, L. *Gmelin Handbook of Inorganic and Organometallic Chemistry: TYPIX.Standardized Data and Crystal Chemical Characterization of Inorganic Structure Types*; Springer: Berlin/Heidelberg, Germany, 1993; Volume 1.
3. Chang, H.Y.; Yogeesh, M.N.; Ghosh, R.; Rai, A.; Sanne, A.; Yang, S.; Lu, N.; Banerjee, S.K.; Akinwande, D. Large-area monolayer MoS_2 for flexible low-power RF nanoelectronics in the GHz regime. *Adv. Mater.* **2016**, *28*, 1818–1823. [CrossRef] [PubMed]
4. Desai, S.B.; Madhvapathy, S.R.; Sachid, A.B.; Llinas, J.P.; Wang, Q.; Ahn, G.H.; Pitner, G.; Kim, M.J.; Bokor, J.; Hu, C.; et al. MoS_2 transistors with 1-nanometer gate lengths. *Science* **2016**, *354*, 99–102. [CrossRef] [PubMed]
5. Illarionov, Y.Y.; Smithe KK, H.; Waltl, M.; Knobloch, T.; Pop, E.; Grasser, T. Improved hysteresis and reliability of MoS_2 transistors with high-quality CVD growth and Al_2O_3 encapsulation. *IEEE Electron. Device Lett.* **2017**, *38*, 1763–1766. [CrossRef]
6. Xue, F.; Chen, L.; Wang, L.; Pang, Y.; Chen, J.; Zhang, C.; Wang, Z.L. MoS_2 Tribotronic transistor for smart tactile switch. *Adv. Funct. Mater.* **2016**, *26*, 2104–2149. [CrossRef]
7. Yu, L.; El-Damak, D.; Radhakrishna, U.; Ling, X.; Zubair, A.; Lin, Y.; Zhang, Y.; Chuang, M.H.; Lee, Y.H.; Antoniadis, D.; et al. Design, modeling, and fabrication of chemical vapor deposition grown MoS_2 circuits with E-mode FETs for large-area electronics. *Nano Lett.* **2016**, *16*, 6349–6356. [CrossRef]
8. Guo, Y.; Wei, X.; Shu, J.; Liu, B.; Yin, J.; Guan, C.; Han, Y.; Gao, S.; Chen, Q. Charge trapping at the MoS_2-SiO_2 interface and its effects on the characteristics of MoS_2 metal-oxide-semiconductor field effect transistors. *Appl. Phys. Lett.* **2015**, *106*, 103109. [CrossRef]
9. Ionescu, A.M.; Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **2011**, *479*, 329–337. [CrossRef]
10. Sicard, E. *Introducing 7-nm FinFET Technology in Microwind*; HAL: Lyon, France, 2017.
11. Peng, S.; Jin, Z.; Yao, Y.; Li, L.; Zhang, D.; Shi, J.; Huang, X.; Niu, J.; Zhang, Y.; Yu, G. Metal-contact-induced transition of electrical transport in monolayer MoS_2: From thermally activated to variable-range hopping. *Adv. Electron. Mater.* **2019**, *5*, 1900042. [CrossRef]
12. Zou, X.; Xu, J.; Huang, H.; Zhu, Z.; Wang, H.; Li, B.; Liao, L.; Fang, G. A comparative study on top-gated and bottom-gated multilayer MoS_2 transistors with gate stacked dielectric of Al_2O_3/HfO_2. *Nanotechnology* **2018**, *29*, 245201. [CrossRef]
13. Ayari, A.; Cobas, E.; Ogundadegbe, O.; Fuhrer, M.S. Realization and electrical characterization of ultrathin crystals of layered transition-metal dichalcogenides. *J. Appl. Phys.* **2007**, *101*, 014507. [CrossRef]
14. Novoselov, K.S.; Geim, A.K.; Morozov, S.V.; Jiang, D.; Zhang, Y.; Dubonos, S.V.; Grigorieva, I.V.; Firsov, A.A. Electric field effect in atomically thin carbon films. *Science* **2004**, *306*, 666–669. [CrossRef] [PubMed]
15. Gray, P.V.; Brown, D.M. Density of SiO_2–Si interface states. *Appl. Phys. Lett.* **1966**, *8*, 31–33. [CrossRef]
16. Lu, C.P.; Li, G.; Mao, J.; Wang, L.M.; Andrei, E.Y. Bandgap, mid-gap states, and gating effects in MoS_2. *Nano. Lett.* **2014**, *14*, 4628–6433. [CrossRef] [PubMed]

17. Lee, J.-M.; Cho, I.-T.; Lee, J.-H.; Kwon, H.-I. Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors. *Appl. Phys. Lett.* **2008**, *93*, 093504. [CrossRef]
18. Illarionov, Y.Y.; Knobloch, T.; Waltl, M.; Rzepa, G.; Pospischil, A.; Polyushkin, D.K.; Furchi, M.M.; Mueller, T.; Grasser, T. Energetic mapping of oxide traps in MoS_2 field-effect transistors. *2D Mater.* **2017**, *4*, 025108. [CrossRef]
19. Miczek, M.; Mizue, C.; Hashizume, T.; Adamowicz, B. Effects of interface states and temperature on the C-V behavior of metal/insulator/AlGaN/GaN heterostructure capacitors. *J. Appl. Phys.* **2008**, *103*, 104510. [CrossRef]
20. Yang, Z.; Liu, X.; Zou, X.; Wang, J.; Ma, C.; Jiang, C.; Ho, J.C.; Pan, C.; Xiao, X.; Xiong, J. Performance limits of the self-aligned nanowire top-gated MoS_2 transistors. *Adv. Funct. Mater.* **2017**, *27*, 1602250. [CrossRef]
21. Deuling, H.; Klausmann, E.; Goetzberger, A. Interface states in Si-SiO_2 interfaces. *Solid State Electron.* **1972**, *15*, 559–571. [CrossRef]
22. Park, Y.; Baac, H.W.; Heo, J.; Yoo, G. Thermally activated trap charges responsible for hysteresis in multilayer MoS_2 field-effect transistors. *Appl. Phys. Lett.* **2016**, *108*, 083102. [CrossRef]
23. Yang, G.; Chuai, X.; Niu, J.; Wang, J.; Shi, X.; Wu, Q.; Su, Y.; Zhao, Y.; Liu, D.; Xu, G. Anomalous positive bias stress instability in MoS_2 transistors with high-hydrogen-concentration SiO_2 gate dielectrics. *IEEE Electron. Device Lett.* **2018**, *40*, 232–235. [CrossRef]

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