



Article

# Combined Organic Photovoltaic Cells and Ultra Low Power CMOS Circuit for Indoor Light Energy Harvesting

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**Abstract:** This paper describes an energy harvesting system composed of an organic photovoltaic cell (OPV) connected to a DC–DC converter, designed in a 130 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology, with a quasi- maximum power point tracking (MPPT) algorithm to maximize the system efficiency, for indoor applications. OPVs are an emerging technology with potential for low cost indoor light energy harvesting. The OPV current-voltage curves (I-V) under an irradiance of solar simulator Oriel Sol 3A, at room temperature, are obtained and an accurate electrical model is derived. The energy harvesting system is subjected to four different indoor light sources: 35 W halogen, 3.5 W LED, 5 W LED, and 7 W LED, positioned at three different heights (0.45 m, 0.26 m, and 0.11 m), to evaluate the potential of the system for indoor applications. The measurements showed maximum efficiencies of 60% for 35 W halogen and 45% for 7 W LED at the highest distance (0.45 m) and between 60% (5 W LED) and 70% (35 W halogen), at the shorter distance (0.11 m). Under irradiation, the integrated CMOS circuit presented a maximum efficiency of 75.76%, which is, to the best of the authors' knowledge, the best reported power management unit (PMU) energy system using organic photovoltaic cells.

**Keywords:** indoor light harvesting; organic photovoltaic cells; integrated circuit; CMOS technology

## 1. Introduction

The downscaling of integrated circuit technology, especially CMOS, is pushing the limits of miniaturization and portability. The availability of ultra-low power ( $\mu$ W) and complex monolithic circuits in CMOS nanotechnology opens new research on Internet of Things (IoT) solutions for a wide range of applications [1–18], including sensing, data processing, and communication. The power requirement for these systems depends on the application. Although these 'smart' sensors are typically battery powered [19], the use of harvesting techniques to obtain energy from different sources, such as ambient light, vibration/motion of human body parts, temperature differences, and Radio Frequency (RF) electromagnetic radiation, can improve battery lifetime and energy autonomy. Harvesting from

the sun or ambient light is the most effective way to power a sensor node, with power densities in the range of tens of mW/cm<sup>2</sup> [20,21]. Light energy harvesting (Figure 1) depends upon the ambient light to be harvested, which may be a mix between natural light coming from the outside, and artificial light provided by overhead lamps or luminaries.

A previous work [21] that reported on indoor light availability, in which the artificial light was generated by fluorescent light tubes, showed that when placing the harvester very close to overhead lamps, it was possible to achieve an irradiance of 10 W/m². A more in-depth study was carried out in [22], in which the light availability inside an office was assessed for different times of the day, encompassing various ways to place and orient a harvester, either giving more emphasis to natural light, artificial light, or a combination of both. The worst-case irradiance during daytime, for solar radiation inside the room, had the value of 130 mW/m². In addition, when using artificial light only, at night time, the worst-case measurement yielded a value of 730 mW/m². The artificial light was provided by two fluorescent light tubes, each with a power of 36 W [22].

More recent studies have mainly focused on the use of flexible photovoltaic films of various natures, under LED lighting [23], taking into consideration that the typical irradiance amounts of  $66 \text{ mW/m}^2$ , down to  $7 \text{ mW/m}^2$ , are enough for the tested photovoltaic (PV) harvesting modules to operate favorably. The operating spectrum of the LED devices considered in [23] are very similar to those used in the present work.

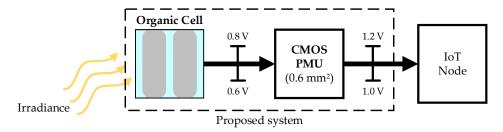


Figure 1. Indoor application of a PV cell.

In this work, an organic photovoltaic cell is used as the harvesting device. OPVs is an emerging technology based on heterojunctions of organic semiconductors (organic compounds, polymers, carbon-nanoparticles) [24–26]. These compounds can have very different chemical structures and properties. The solubility in common solvents is important because it allows the active/organic layer of the devices to be processed from solutions, i.e., as inks, by low cost deposition methods (e.g., spin coating, ink-jet printing, or roll-to-roll printing) over flexible substrates (plastics, e.g., PET, polyethylene terephtalate). The unique characteristics of OPVs, such as being lightweight and flexible, combined with their performance under diffuse light, allows for applications that more conventional technologies, such as crystalline silicon-based cells, cannot be easily adapted to, despite their higher efficiencies. State-of-the-art OPVs have already achieved power density levels of 14 mW/cm² under simulated solar light of 100 mW/cm² in laboratory prototypes, using glass substrates [27].

Typically, harvesting devices are connected to a power management unit based on a separated DC–DC converter. The harvested source is typically a thermoelectric generator (TEG) and the DC–DC conversion is mostly based on switched inductive converters (usually boost type), with battery assisted, mechanical, capacitor pre-charge, RF kick-start, or even step-up transformers power-up schemes [28–32]. Fully electric power-up solutions from a few tens of mV can be a CMOS Integrated Circuit (IC) and external high-value energy storage components (values of external inductances and capacitances can be as high as 1 mH and 100  $\mu$ F, respectively) on a separate Printed Circuit Board (PCB) [33–35]. The DC–DC converters have been designed for relatively small input voltage variations (few tens to few hundreds of mV), due to the TEG harvesting output range. However, in contrast with TEGs, harvesting from PV cells requires a converter for a wider range of input voltages (100 mV < V<sub>OC</sub> < 1 V). There are few reported works on step-up conversion of a PV cell output voltage, [36–40].

Battery powered systems usually include a power management unit (PMU) to achieve a fixed regulated voltage with variable battery charge levels [41–47]. The architecture of the system proposed in this work is new with respect to state-of-the-art systems, as it leads to a small size (<1 cm<sup>2</sup>) and an energy self-sustainable device (Figure 2), suitable for portable applications.

The main goal of this paper is the development of a batteryless ultralow-power energy supply system, combing organic photovoltaic cell and a PMU (an integrated CMOS circuit) for indoor applications.

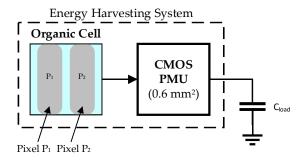


Figure 2. Proposed energy harvesting system.

#### 2. Characterization of a Photovoltaic Cell

#### 2.1. OPV Fabrication and Characteristics

The OPV devices were prepared on indium tin oxide (ITO), (100 nm thick)-coated glass substrates previously cleaned sequentially with distilled water and a non-ionic detergent, distilled water, acetone, and isopropyl alcohol under ultrasounds.

The OPV cell consisted of a multilayer device with the structure: Glass/ITO/PEDOT:PSS/PffBT4T-2OD:PC<sub>60</sub>BM/LiF/Al cells, where:

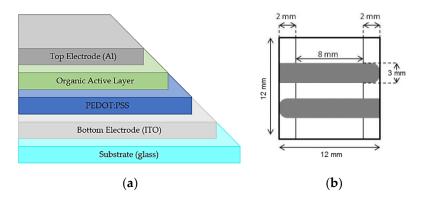
- ITO is a conducting oxide;
- PEDOT:PSS is the conducting polymer Poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) (ca. 40 nm thick) acting as a hole transport layer;
- LiF/Al is the top metallic electrode, which is thermally evaporated on top of the active layer (LiF is 1.5 nm thick and Al is ca. 100 nm thick).

The organic/active layer was a mixture of PffBT4T-2OD and PC<sub>60</sub>BM:

- PffBT4T-2OD is poly[(5,6-difluoro-2,1,3-benzothiadiazol-4,7-diyl)-*alt*-(3,3'''-di(2-octyldodecyl)-2,2';5',2''';5'',2'''-quaterthiophen-5,5'''-diyl)];
- PC<sub>60</sub>BM is [6,6]-Phenyl C61 butyric acid methyl ester [48,49].

The device architecture is shown in Figure 3:

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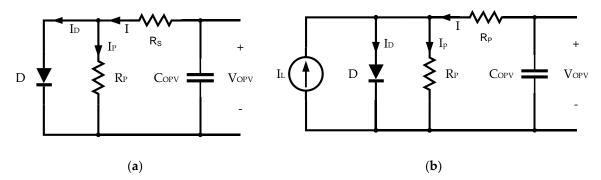


**Figure 3.** (a) Organic photovoltaic cell (OPV) structure of the organic PV cell used in this work: Glass/ITO/PEDOT:PSS/:PC60BM/LiF/Al; (b) active area 0.24 cm<sup>2</sup>.

## 2.2. OPV Electrical Model (I-V Characterization)

A photovoltaic cell can be characterized from its current-voltage curves (I-V), obtained in two different light conditions: Dark and standard solar conditions, i.e., under AM1.5G light with an irradiance of  $100 \text{ mW/cm}^2$ .

The equivalent circuit of the cell, as shown in Figure 4a, can be obtained from the curve in the dark. It is described by a combination of a junction diode D and two resistors ( $R_s$  and  $R_p$ ). The resistors  $R_s$  and  $R_p$  are associated with losses and leakage currents, respectively.



**Figure 4.** Equivalent circuit of a photovoltaic cell: (a) In dark conditions; (b) at standard irradiance conditions  $(1000 \text{ W/m}^2)$ .

The cells were fabricated with an absorbing layer composed of a bulk heterojunction of organic semiconductors, where the p-type semiconductor is a polymer, and the n-type semiconductor is a fullerene. When the light radiation struck the active layer, through the glass transparent electrode, a flow of charges was generated, which can be collected near the electrodes area. In this way, the diode D in the equivalent circuit diagram, allowed to characterize the p-n junction. The equation of  $I_d$  running through the diode is depicted in (1), where  $I_s$  is the saturation current of the diode, n is the diode factor,  $V_D$  is the voltage at the terminals of the diode and  $V_T$  is the thermal voltage. It should be noted that  $V_D = Vout - I \times R_s$ .

$$I_d = I_s \left( e^{\frac{V_D}{nV_T}} - 1 \right) \tag{1}$$

The thermal voltage is defined from Equation (2) where k represents Boltzmann's constant, T the cell temperature and q the electron charge.

$$V_T = \frac{kT}{q} \tag{2}$$

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The resistors represent a decrease in the efficiency of the photovoltaic cell. It is assumed that the current delivered to the load in the dark is (3).

$$I_{out} = I_s \left( e^{\frac{V_{out} - IR_s}{nV_T}} - 1 \right) + \frac{V_{out} - IR_s}{R_v}$$

$$\tag{3}$$

The cell generated an  $I_L$  current as a result of the incident radiation, as shown in Figure 4. The current at the terminals of the photovoltaic cell,  $I_{out}$ , under standard irradiance conditions, is

$$I = I_s \left( e^{\frac{V_{out} - IR_s}{nV_T}} - 1 \right) + \frac{V_{out} - IR_s}{R_v} - I_L$$

$$\tag{4}$$

This equation shows that the efficiency of the cell is dependent on the two resistors and the diode parameters in the equivalent circuit. To enhance the efficiency of the PV cells, the series resistance  $R_s$  should be close to zero and the parallel resistance  $R_v$  should be as large as possible, ideally infinite.

The Fill Factor (FF) is figure-of-merit used to specify the quality of the PV cell. Considering that the voltage provided by the cell varies between zero and the open-circuit voltage  $V_{oc}$ , and that the current supplied varies between zero and the value of the short-circuit current  $I_{sc}$ , there is a point on the characteristic curve of the cell, where the output power is maximum,  $P_{max}$ , i.e., this voltage/current product reaches its maximum value, with the correspondent values of current ( $I_{mp}$ ) and voltage ( $V_{mp}$ ). Thus, the fill factor of the photovoltaic cell, is defined as the ratio between  $P_{max}$  and the product of the open-circuit voltage  $V_{oc}$  and the short-circuit current  $I_{sc}$ ,

$$FF = \frac{P_{max}}{V_{oc}I_{sc}} = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}} \tag{5}$$

It is desirable to have a *FF* close to 1. The capacitance of a photovoltaic cell can be represented by a capacitor in parallel with the output of the cell [50],

$$C_{OPV} = \frac{\varepsilon_0 K_{\rm s} A}{d} \tag{6}$$

where  $\varepsilon_0$  corresponds to the permittivity in vacuum,  $K_s$  is the dielectric constant of the semiconductor, the active area of the cell is given by A and the semiconductor thickness is defined by d. The current–voltage (I-V) characteristics are measured in an inert atmosphere (N<sub>2</sub>) using a Keithley K2400 source-meter unit. The curves under illumination are measured with the solar simulator Oriel Sol 3A, 69920, Newport.

The power conversion efficiency (PCE) of the cells can be calculated from their I-V curves under illumination, using the open-circuit voltage (*Voc*), the short-circuit current (*Isc*), and the *FF*.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_{sc} \cdot V_{oc} \cdot FF}{P_{in}} \tag{7}$$

where  $P_{out}$  is the maximum power generated by the device,  $P_{in}$  represents the power of the incident light (provided by the solar simulator lamp), and FF is defined as in (5).

For each level of irradiance, each PV cell has a specific behaviour, with different values of  $V_{oc}$  and  $V_{mp}$ . These two voltages are related to each other by a factor k, which can be defined as

$$k = \frac{V_{mp}}{V_{oc}}. (8)$$

This characteristic will be exploited in the maximum power point tracking (MPPT) method that is selected for this application, considering the specific characteristics of the OPV cells that serve as harvesters in this work.

## 2.3. Experimental Characterization of the OPV

From the electrical point of view, the two terminals coming from the pixels implement the negative poles of each OPV while the terminal of the ITO corresponds to the positive terminal, which is common to the two pixels of the substrate. It should also be noted that the active area of each pixel was 0.24 cm<sup>2</sup>.

The measurement setup, in which the I-V curves were obtained (by averaging of the two pixels substrate), is shown in Figure 5. A light source was required (solar simulator) and an output variable voltage source, in which the output current was measured for different output voltage values using a data acquisition system.

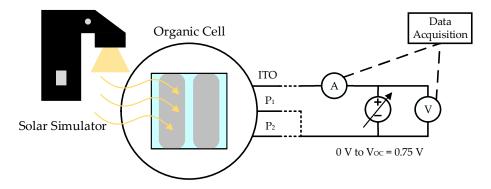


Figure 5. Measure setup for OPV characterization.

Four different incident radiation densities were considered, while keeping the sample-source distance of 19.5 cm, as shown in Figure 6. Figure 7 shows the measured I-V characteristic of an organic photovoltaic cell in dark condition.

Considering that the main function of a photovoltaic cell is to provide power to a load, the OPV power curves were obtained for the different levels of incident radiation (based on the I-V curves of Figure 6), as shown in Figure 8.

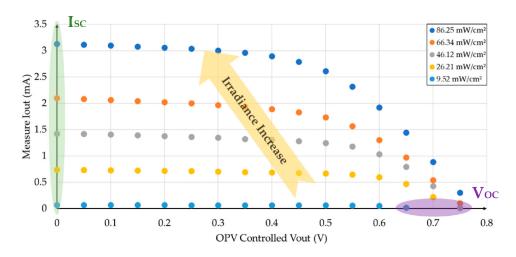


Figure 6. Measured I-V characteristics for different lighting levels in the OPV substrate.

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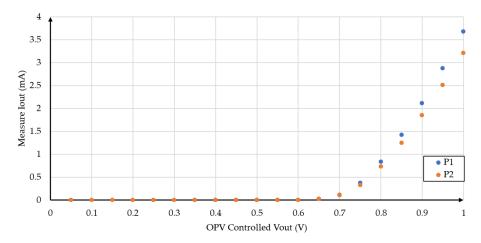


Figure 7. Measured I-V characteristics in dark conditions for the two pixels in the OPV substrate.

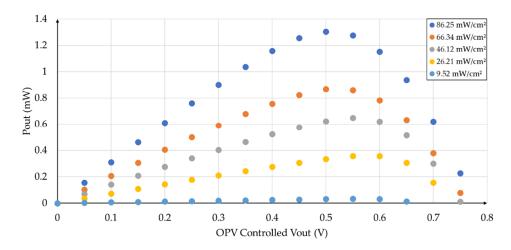


Figure 8. Experimental power curves of an OPV for different measured lighting levels.

The parameters of the OPV cell, are shown in Table 1, and the equivalent circuit (Figure 4a) is shown in Table 2 for the different intensities of incident radiation. The five parameters ( $I_1$ ,  $I_S$ , n,  $R_s$  and  $R_p$ ) were obtained by applying a numerical least squares curve fitting technique to the I-V curves of the cells under various light conditions [51] (Figure 7) and based on the equivalent circuit Equation (4) [52]. Thus, in order to observe the accuracy of the resulting theoretical electrical model, the I-V curves of this circuit model, obtained using an electrical simulation program, were plotted for the different irradiances (as shown in Figure 9), and compared with the original I-V experimental data (presented in Table 1).

Irradiance (mW/cm <sup>2</sup> )	$ I_{sc} $ (mA)	$V_{oc}$ (V)	$ I_{mp} $ (mA)	$V_{mp}$ (V)	$P_{max}$ (mW)	k	FF
86.25	3.13	0.77	2.61	0.50	1.31	0.65	0.54
66.34	2.10	0.76	1.66	0.53	0.87	0.69	0.55
46.12	1.42	0.75	1.18	0.55	0.65	0.73	0.61
26.21	0.74	0.73	0.63	0.58	0.36	0.79	0.67
9.52	0.07	0.66	0.06	0.55	0.03	0.83	0.74

**Table 1.** Experimental electrical characteristics of an OPV cell.

Irradiance (mW/cm <sup>2</sup> )	<i>I</i> <sub>1</sub> (mA)	I <sub>S</sub> (pA)	п	$R_s$ ( $\Omega$ )	$R_p$ (k $\Omega$ )
86.25	3.23	342.71	1.89	63.93	2.18
66.34	2.20	145.68	1.81	80.88	2.02
46.12	1.48	0.35	1.33	87.47	2.90
26.21	0.76	0.01	1.16	98.91	6.83
9.52	0.07	0.01	1.14	106.13	76.43

**Table 2.** Parameters of the equivalent circuit of an OPV for different irradiances.

From Tables 1 and 2 we can conclude that the output current was reduced by reducing the input radiance, which led to a strong reduction in the output power. The *FF* slightly increased and the OPV cells performance was better for low input radiance.

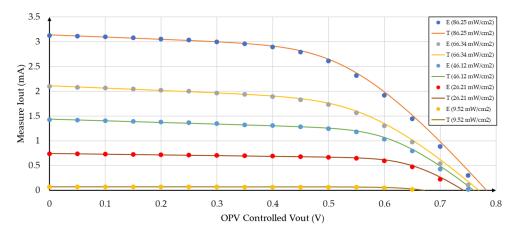


Figure 9. Experimental (E - dots) vs. theoretical (T - line) I-V curves for different irradiances.

Using (6), we have obtained that the capacitance C, in parallel with the equivalent OPV model was 37.5 nF. For this calculation we have considered a dielectric constant ( $K_s$ ) for the semiconductor of 3 nm and a thickness (d) of 170 nm (thickness of the active layer measured with a profilometer).

## 3. Integrated CMOS Test Circuit

The OPV cells studied in this work were connected to an integrated CMOS DC-D SC switch capacitor (SC) converter system with MPPT capability, designed and built using a 0.13  $\mu$ m CMOS technology [53]. The block diagram of this system is shown in Figure 10.

The SC voltage doubler, local supply, start up, and phase controller blocks were integrated into a CMOS silicon die with a layout area of less than  $1 \text{ mm}^2$ .

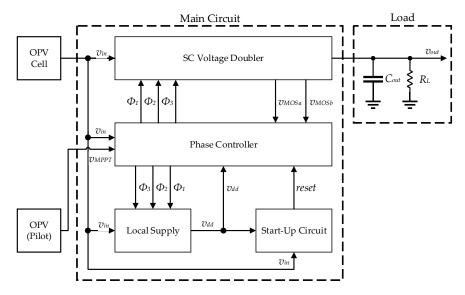


Figure 10. Block diagram of the power management unit (PMU).

# 3.1. Switched-Capacitor Voltage Doubler with Charge Reuse

A switched capacitor-based converter was chosen to reduce the cost and volume of the overall system by avoiding an external inductor, usually required by inductive switch mode DC–DC converters. A simplified schematic of the step-up converter circuit is depicted in Figure 11.

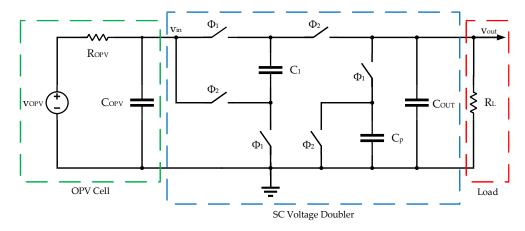
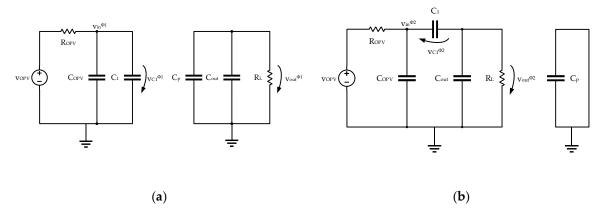


Figure 11. Simplified schematic of the voltage doubler.

This schematic also includes a switched parasitic capacitor ( $C_p$ ), representing the load created by the operation of the phase controller circuit and clock drivers, shown in Figure 11. This controller circuit was responsible for producing the clock phases  $\phi_1$ ,  $\phi_2$ , and  $\phi_3$ . Capacitor  $C_{OPV}$  represents the parasitic capacitance of the PV cell, which has been linearized, and is represented by its Thévenin equivalent circuit ( $v_S$  and  $R_S$ ).

The basic principle of operation of this circuit relies of the fact that, during  $\phi_1$ ,  $C_1$  is connected in parallel with  $v_{in}$  and charged to this voltage value, whereas in  $\phi_2$ ,  $C_1$  is placed in series with  $v_{in}$ , leading to an output voltage ( $v_{out}$ ) ideally two times the input.

From the analysis of the two configurations of the circuit of Figure 11 (shown in Figure 12), in phases  $\phi_1$  and  $\phi_2$  it is possible to write the equations for the conservation of the charge of the circuit capacitors. These equations are obtained considering that  $T_{CLK} >> R_{ON} \times C_1$  (the switch resistance is negligible) and that  $T_{CLK} << R_{OPV} \times C_{OPV}$  and  $T_{CLK} << R_L \times C_{out}$ . A detailed theoretical analysis showing how these equations are derived, can be found in [53].



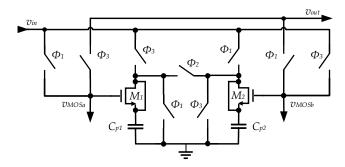
**Figure 12.** (a) Circuit configuration in phase  $\phi_1$ . (b) Circuit configuration in phase  $\phi_2$ .

From the charge conservation equations, it is possible to obtain the expressions for the steady-state input and output voltages of the circuit [53] considering an OPV at input:

$$V_{in} = \frac{T_{CLK}(4(C_{out}C_p + C_1(C_{out} + C_p))R_L + (C_1 + 4C_{out} + C_p)T_{CLK})v_{OPV}}{16C_1C_{out}C_pR_LR_{OPV} + 4(C_{out}C_pR_L + C_1(C_{out} + C_p)R_L + C_1(4C_{out} + C_p)R_{OPV})T_{CLK} + (C_1 + 4C_{out} + C_p)T_{CLK}^2}$$
(9)

$$V_{out} = \frac{2C_1(4C_oR_L - T_{CLK})T_{CLK}v_{OPV}}{16C_1C_{out}C_pR_LR_{OPV} + 4(C_{out}C_pR_L + C_1(C_{out} + C_p)R_L + C_1(4C_{out} + C_p)R_{OPV})T_{CLK} + (C_1 + 4C_{out} + C_p)T_{CLK}^2}$$
(10)

To minimize the area, Metal-Oxide-Semiconductor (MOS) transistor capacitors were used that have the largest available capacitance per unit area in the selected CMOS technology, which resulted in a large bottom plate parasitic capacitance, charged to  $v_{in}$  during phase  $\phi_1$  and discharged during phase  $\phi_2$ . This lowered the efficiency of the circuit and, to improve it, it was necessary to reduce the amount of charge lost through the bottom plate parasitic capacitance. This was done by splitting the capacitance in two and duplicating the circuit. Considering now as  $\phi_3$  the old  $\phi_2$  phase, a third phase ( $\phi_2$ ), was introduced between  $\phi_1$  and  $\phi_3$ . During this new phase  $\phi_2$ , the bottom plate nodes of the two half-circuits were connected resulting in charge redistribution between the two parasitic capacitances [53]. This circuit is depicted in Figure 13. Because one of these capacitances was charged to  $v_{in}$ , while the other was completely discharged, when they were connected, the charge was equally divided between them, and each capacitor had half of the charge of the capacitor that was firstly charged to  $v_{in}$ . Either in phase  $\phi_1$  or in phase  $\phi_3$ , the parasitic capacitor connected to the input will already be pre-charged to half of its final charge value, thus requiring only half of the charge from the input source.



**Figure 13.** Schematic of the step-up doubler switch capacitor (SC) converter, using MOS capacitors with charge reuse.

## 3.2. Other Blocks

The clock phases that control the SC voltage doubler had a frequency that maximized the power transfer from the PV cells. Since this frequency changed with the light intensity and temperature,

the controller circuit producing these clock phases should use an MPPT method in order to continuously adjust the clock frequency value. The fractional open circuit voltage (Fractional  $V_{OC}$ ) method ([22]) was chosen, because of its simplicity. This method explores the intrinsic characteristic of PV cells, in which there is a proportionality factor (k) between their open circuit voltage and the voltage at which the maximum power point (MPP) occurs ( $v_{MPP}$ ). This factor must be determined beforehand, by studying the PV cell behavior under several conditions of illumination and temperature.

Pilot PV cells in open circuit (unloaded) were used to measure the open circuit voltage. The optimum voltage of the unloaded PV cell ( $v_{MPP}$ ) was determined by multiplying the open circuit reference pilot voltage by k, using a resistive divider. The pilot PV cells can be smaller than the main PV cells and they must have the same temperature and illumination as the main cells, for the fractional  $V_{OC}$  method to accurately track the MPP voltage. The state diagram that represents the MPPT algorithm, the generation of the three clock phases, and the conditions that must be met to go from one state to the next, are shown in Figure 14.

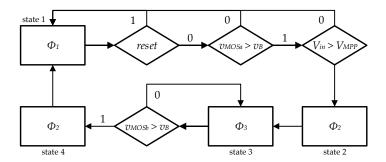


Figure 14. State diagram of the algorithm implemented by the state machine.

Since this is an energy harvesting system, it must have its own power supply for the controller circuit that generates the clock signals. The main output voltage cannot be used to power the clock generation circuit, because during the start-up of the system will remain close to 0 V for a long time, if there is a large capacitance at the output. The solution was to create a supply voltage, independent from the output voltage. This allowed the system to start-up even if the large output capacitor was charged from 0 V.

This local supply block was a smaller SC voltage doubler circuit, controlled by the same phase signals, and was used to create a local supply voltage in an internal decoupling capacitor. This circuit was a replica of the main SC circuit, but, with its capacitors and switches, was scaled down to a fraction of the size of those in the main SC circuit.

Since the local supply voltage was initially 0 V, a start-up circuit was required to convert the input node to the output node of the local power supply. As soon the capacitor was charged to a voltage value enough for the phase generator circuit to start working, this connection was removed, and the circuit started its normal operation. The start-up circuit also provided a reset signal for the phase generator circuit, to guarantee that this circuit started working in state 1 (as shown in Figure 14).

## 4. Test Circuit and Measurement Results

To study the performance of the circuit proposed in [53] considering OPVs as an energy source, it was necessary to readjust the parameters of the PMU to reach maximum efficiency. Since the control system was implemented from the fractional  $V_{OC}$  algorithm, it was required, based on the power curve of the OPV cell, to find the voltage that corresponded to the maximum power value made available by the cell. Based on the characterization of the OPV cells presented in Table 2, and the power curves (Figure 8), the performance of the system for different levels of irradiance with a load of 9.9 k $\Omega$  is shown in Table 3. In Table 1 the value of the k factor for the cell was obtained for different radiation levels and it varied between 0.65 and 0.83. In order to set MPPT algorithm, an average of the k values, for Table 1, was used in the resistive divider of the CMOS DC–DC converter.

Due to the inert atmosphere chamber used in the tests of the OPV cells, it was only possible to test two connection configurations, namely with the pixel  $P_1$  as the main cell and the pixel  $P_2$  as the pilot cell (Config. 1), and with the two pixels in parallel connected to the input of the circuit ( $V_{in}$ ) (Config. 2). In this last configuration, the pilot cell open circuit voltage ( $V_{OC}$ ) required for the MPPT algorithm was replaced by an external voltage of 1.2 V. Considering that the two pixels shared a common substrate, the increase of the output power was achieved by connecting them in parallel. Yet, since the output was limited to 0.6 to 0.7 V, the IC CMOS circuit, besides the MPTT, needed to double the output voltage, in order to reach the required 1.2 V. The output power was 0.14 mW, for a low power IoT node, due to limitations in the available CMOS circuit die area. However, this value can be easily increased by using higher area capacitors. The test setup is shown in Figure 15 and circuit die photo (0.95 × 0.67 mm²) is shown in Figure 16.

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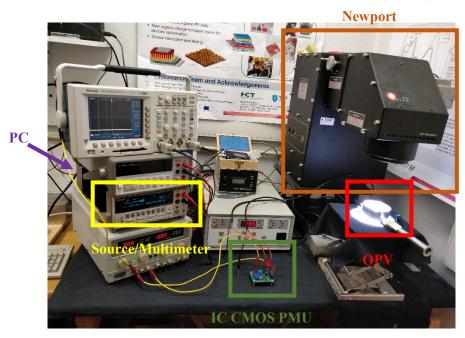


Figure 15. Test setup.

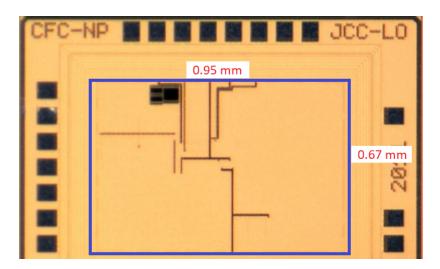


Figure 16. Circuit die micro-photograph.

Config.	Irradiance (mW/cm <sup>2</sup> )	$V_{in}$ (V)	$V_{mppt}$ (V)	k	I <sub>in</sub> (mA)	$P_{in}$ (mW)	$V_{out}$ (V)	Iout (mA)	Pout (mW)	η (%)
	86.25	0.65	0.62	0.81	0.43	0.28	1.20	0.11	0.13	47.23
	66.34	0.66	0.63	0.83	0.35	0.23	1.20	0.12	0.14	62.79
1	46.12	0.65	0.63	0.84	0.32	0.21	1.19	0.12	0.14	68.92
	26.21	0.62	0.60	0.82	0.43	0.27	1.15	0.12	0.14	51.49
	9.52	0.57	0.51	0.77	0.40	0.23	0.92	0.09	0.08	36.08
	86.25	0.68	0.50	0.65	0.66	0.45	1.14	0.11	0.13	27.93
	66.34	0.69	0.52	0.69	0.63	0.43	1.15	0.11	0.13	29.25
2	46.12	0.67	0.55	0.74	0.58	0.39	1.15	0.11	0.13	32.43
	26.21	0.65	0.55	0.76	0.48	0.31	1.17	0.12	0.14	45.05
	9.52	0.63	0.55	0.84	0.29	0.18	1.15	0.12	0.14	75.76

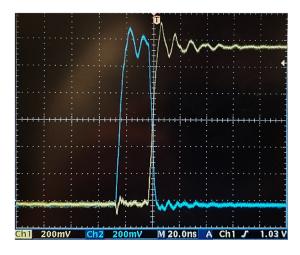
**Table 3.** Measured performance of the system proposed in [19] with OPVs.

In order to validate the correct functioning of the circuit, the waveform of  $\Phi_1$  and  $\Phi_2$ , are shown in Figure 17, channel 1 (Ch1) and channel 2 (Ch2), respectively. The frequency of the clocks can be found in Table 4. Figure 18 shows the start-up of the circuit, for the irradiance level of 26 mW/cm<sup>2</sup>. The above confirms that the control module and the PMU startup worked correctly.

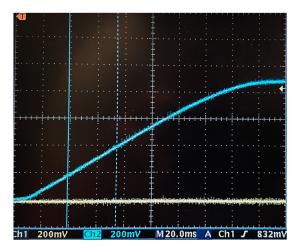
Irradiance (mW/cm <sup>2</sup> )	Φ <sub>1</sub> (MHz)	Φ <sub>2</sub> (MHz)
86.25	1.89	7.66
66.34	1.98	7.82
46.12	1.81	7.45
26.21	2.34	8.48
9.52	4.46	16.33

**Table 4.** Frequency of clock  $\Phi_1$  e  $\Phi_2$ .

Since the current density of the organic photovoltaic cells was approximately 13 mA/cm<sup>2</sup>, for the maximum irradiance value, it was verified that when the irradiance had decreased, i.e., when the current density is low, the frequencies of  $\Phi_1$  and  $\Phi_2$  approximate the values for which the system is scaled. Therefore, it is possible to identify the optimal point of operation of the circuit, minimizing the PMU power dissipated by the control module, while the remaining power was delivered to the load.



**Figure 17.** Waveform of phases  $\Phi_1$  and  $\Phi_2$  for the irradiance of 86.25 mW/cm<sup>2</sup>.



**Figure 18.** Starting the circuit for the irradiance of 26.21 mW/cm<sup>2</sup>.

Table 5 shows the technical characteristics of the lamps used. Considering that these characteristics were different from those of the solar simulator with which the first tests were carried out, the light spectrum is also expected to be different. Thus, the standardized luminous spectra of the four lamps considered in this test are shown in Figure 19 for the irradiance described in Table 5.

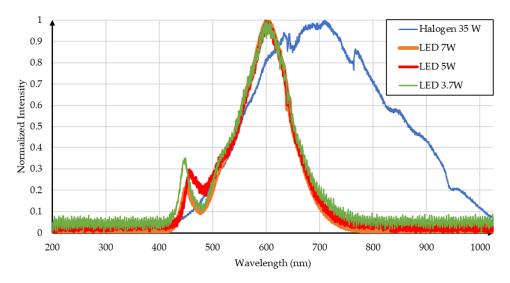


Figure 19. Light spectrum of lamps.

Table 5. Technical characteristics of the lamps used.

Lamp	Color Temperature (K)	Irradiance (mW/cm <sup>2</sup> )
Halogen 35W	3000	23.41
LED 7W	3000	3.34
LED 5W	3000	0.71
LED 3,7W	2800	0.67

The current–voltage and power curves are shown in Figure 20. The short-circuit current of this OPV was 2.27 mA, the open-circuit voltage was 750 mV, and for the maximum power value (660  $\mu$ W). The voltage value, i.e., the voltage value where the maximum power required for the MPPT algorithm was 400 mV.

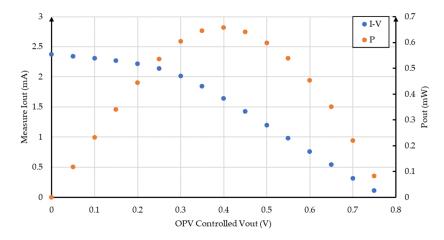


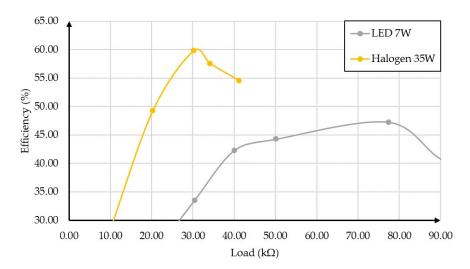
Figure 20. I-V and power curves for the OPV used in the second phase of tests.

The lamps were located at three different (heights) from the OPVs: 0.45 m, 0.26 m, and 0.11 m. Using the Newport 91150V calibration cell, the four lamps were irradiated at different heights, as shown in Table 6.

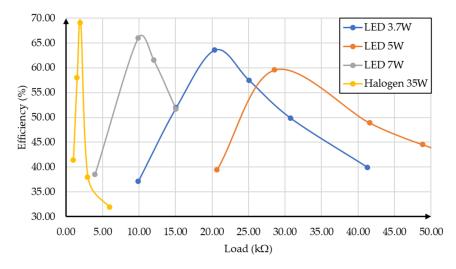
<b>Table 6.</b> Irradiance (mW/cm <sup>2</sup> ) of	of the different lamps for	the three heights.
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Lamp	0.45 m	0.26 m	0.11 m	
Halogen 35W	6.30	32.50	119.30	
LED 7W	1.28	3.73	19.31	
LED 5W	-	0.86	2.76	
LED 3.7W	0.18	0.44	1.56	

The maximum efficiency value of the PMU, for each illumination value, was determined by varying the PMU load. Due to the low irradiation power of the 5 W and 3.7 W lamps, the proposed PMU worked only for the minimum height considered (0.11 m). Figures 21 and 22 represent the efficiency as a function of the load of the architecture for the heights of 0.45 m and 0.11 m, respectively, for each lamp. It was not possible to perform the comparison for the height of 0.26 m.



**Figure 21.** Efficiency as a function of the load for the height of 0.45 m.



**Figure 22.** Efficiency as a function of the load for the height of 0.11 m for different light sources.

Observing the results in Figures 21 and 22, we can see that the circuit presented maximum efficiency with the 35 W halogen lamp. However, it is necessary to consider the supercharging of the cell in the situation whose height to the work plane is 0.11 m. In this case, the variation of the efficiency as a function of the resistance was very narrow (around 2 k $\Omega$ ).

In the first set of OPVs, it was verified that the efficiency of the PMU proposed reached 75.76% with an irradiance of 9.52 mW/m² provided by the radiation simulator and a load of 9.9 k $\Omega$  ( $P_{out}=0.14$  mW). A test setup was used with four indoor lamps, each lamp being placed at three levels of height. A maximum efficiency of 65.98% was achieved for the 7 W LED, with an irradiance of 19.31 mW/cm² and a load of 9.9 k $\Omega$  ( $P_{out}=103.43~\mu W$ ). Although the efficiency obtained by the remaining lamps were lower, it was above 45%.

When comparing the results with the state-of-the-art harvesters (Table 7), it was noted that the presented PMU had unique features in terms of efficiency and in its construction and implementation. Being the control of this architecture based on a MPPT algorithm, it was guaranteed that the energy provided by the OPV was optimized to the PMU load.

The typical power consumption for IoT nodes is in the order of tens mW, as shown in [54] (Table 4). Furthermore, recently, there have been several papers that have used a SC fully integrated circuit with a lower pout than the proposed PMU in this paper [55].

Article	[56]	[57]	[58]	[59]	[60]	[61]	[61]	This Work
Technology	0.35 μm CMOS	0.25 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	SMT	SMT	0.13 μm CMOS
Year	2010	2011	2012	2014	2016	2017	2017	2018
Vin (V)	0.025	0.5-2	0.12	0.6	0.4	0.65	0.65	0.63
Vout (V)	1.8	0–5	1.2	1.2	2.4	1.93	2.7	1.15
Area (mm <sup>2</sup> )	1.7	N/A	0.273	0.31	0.204	228	215	0.6
Freq. (MHz)	N/A	0.1	1–5	0.1 - 0.3	10	1.2	1.2	0.1 - 0.3
Efficiency (%)	58	70	30	70.3	N/A	N/A	N/A	75.76

**Table 7.** Performance comparison with state-of-the-art power management units.

## 5. Conclusions

In this work, we present a proof of concept that highlights the possibility for the integration of organic photovoltaic cells and a CMOS PMU circuit for indoor light harvesting. The OPV cells were connected to an ultra-low power, low area, and low cost, fully integrated CMOS circuit prototype, designed in a 130 nm process, which used a quasi-MPPT algorithm to maximize the efficiency.

It was shown that the organic cells can operate, combined with a CMOS PMU circuit, in the presence of different indoor light lamps: 35 W halogen, 3.5 W LED, 5 W LED, and 7 W LED. They were irradiated by the light of these lamps from three different heights (0.45 m, 0.26 m, and 0.11 m). For 0.45 m, the maximum efficiency was 60% (35 W halogen) and 45% for 7 W LED. For 0.11 m, they showed a maximum efficiency between 60% (5 W LED) and 70% (35 W halogen).

It was verified that the integrated CMOS circuit presented a maximum efficiency above 75% when the OPV cells were illuminated by the solar simulator, which makes this PMU energy system a promising proof of concept for energy harvesting of organic photovoltaic cells. The results presented in this paper can be scaled up by using a larger OPV and a PMU system with large capacitors in order to be able to supply IoT nodes with higher power requirements.

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