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Two-stage isolated AC/DC converter and its compound control strategy

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Abstract

With the continued development of the new energy vehicle industry, two-stage isolated AC/DC converters are widely used because of their simple topology and easy control characteristics. In this study, we investigate the front-stage Buck power factor correction (PFC) converter and rear-stage full-bridge converter. The main circuit design and component selection were completed through a detailed analysis of the circuit characteristics. In terms of the control strategy, the front-stage adopting PI control and parameter adaptive terminal sliding mode control strategy were proposed for the rear-stage full-bridge converter. This new compound control strategy ensures an optimal regulation of the system under different operating conditions. Simulation analysis verified the correctness of the system topology and control strategy. Based on an analysis of the main parameters of the system, a low-power experimental prototype was trial-produced. The experimental results show that under the same load switching conditions, the parameter-adaptive terminal sliding mode control enhanced faster dynamic regulation and stronger robustness than the conventional PI control. The study is also a good reference in terms of engineering work.

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1 Introduction

With the development of power electronics technology, high efficiency, high power density, and wide voltage range of AC/DC converter using two-stage circuit structure have become the industry research hotspot.

The front stage of the AC/DC converter is a power factor correction circuit, which can improve the power factor and reduce grid-side current harmonics. Its performance affects the utilization of grid energy and control effect of the rear-stage DC/DC converter. Current research on PFC circuits mainly focuses on Boost and its improved circuits. However, traditional Boost PFC circuits have a high output voltage, which has great voltage stress on the rear-stage components and is not conducive to rear-stage circuit design. Improved circuits also have limitations such as complex drive design and low overall efficiency [1]. The Buck PFC circuit has a low-voltage stress requirement on the component and strong ability to control the input and output currents. It is particularly suitable for high-voltage input and low-voltage operation of the load; however, owing to its structural limitations, the input current has a

dead-time. Scholars have proposed several solutions to this problem. For example, in [2], the circuit operates in Buck-Boost mode at dead-time by adding auxiliary switches and diodes, and a nonlinear control strategy was used to achieve power-factor correction. In [3], an improved Buck PFC circuit was proposed, which works in Buck-Boost mode when the input voltage is lower than the output voltage. In [4], the Buck converter was combined with Flyback converter in parallel, which eliminated the input current dead-time and reduced the current harmonics. In [5], a Buck circuit with an active buffer was proposed to reduce the input current dead-time. In [6], a series-capacitor based interleaved Buck PFC converter was proposed, which reduces the current dead time through extremely low output voltage and achieves high power factor. The circuit structure and control strategy used in the aforementioned studies are still relatively complex. Combined with the design requirements of a two-stage low-power experimental prototype, this study investigated the Buck PFC circuit.

The rear-stage of an AC/DC converter often uses an isolated DC/DC converter. Full-bridge converters have been widely used in many fields owing to their high power density, high voltage conversion ratio, and low switching loss [7,8]. Compared to other converter topologies, the full-bridge converter can realize zero-voltage switching by the resonance of its own parasitic parameters, which greatly reduces the switching loss of components, and improves the efficiency of the circuit. Therefore, this study considers the full-bridge converter as the research object of the rear-stage main circuit.

From the perspective of the full-bridge converter control strategy, traditional PID control has many advantages, such as simple design, convenient application, and easy hardware implementation [9]. However, there are also problems, such as slow start speed and long adjustment time. Thus, various new control strategies have been proposed. For example, in [10], a fuzzy control was combined with PI control to overcome the unfavorable factors such as variable parameters and nonlinearity of the system to some extent. in [11], a BP neural network was introduced into the generation process of PID parameters, and the PID parameters were adjusted in real time based on the circuit state to optimize the PID parameters. However, neural networks should be driven by big data. This is quite different from the circuit characteristics of the full-bridge converter. Therefore, the training effect is difficult to guarantee.

In recent years, sliding mode control has been widely applied to DC/DC converters due to its easy design and robustness. Currently, the studies on sliding mode control strategy for DC/DC converter topologies are mainly focused on Buck circuit. In [12], a method for designing sliding mode coefficients was proposed, which is based on the circuit parameters and design index of Buck converter. In [13], a fractional-order sliding mode control strategy was proposed, which not only reduces the sensitivity of the system to mismatched interference, but also improves the transient performance of the system. In addition, adaptive hysteresis sliding mode control method [14] and second-order sliding mode control method [15] have also achieved favorable control effects. However, the control strategy designed for the Buck circuit cannot be directly applied to the full-bridge converter, which requires a new mathematical model and an equivalent control law.

Some solutions have been proposed by scholars for the sliding mode control strategy of full-bridge converters. In [16], a PWM full-order sliding mode control strategy for full-bridge converters was proposed, which makes the full-bridge converter operate in the fixed frequency state and shows strong robustness when the external working state changes. In [17], the backstepping method was combined with sliding mode control theory, which overcomes the strong dependence of the traditional backstepping method on the system model and shows strong resistance to input and load disturbances. In [18], a method combining adaptive fuzzy control and sliding mode control was adopted, which significantly improves the system performance. In [19], a double integral indirect sliding mode control strategy was proposed to effectively

eliminate the state error in the output and improve the dynamic performance of the full-bridge circuit. The above strategies based on the sliding mode control theory have the characteristics of strong robustness. However, there are still problems in that parameters depend strongly on the system, and different parameter settings have a significant influence on the system control effect. Therefore, a parameter-adaptive control algorithm with a fast-approaching speed is required to ensure that the system has a better dynamic performance.

Based on the above discussion, a two-stage isolated AC/DC converter was designed in this study, and a compound control strategy with power factor correction, strong dynamic recovery performance and parameter adaption was proposed. The main contributions of this paper are as follows:

1. The front-stage PFC circuit adopts a Buck circuit with an LC filter, and makes it operate in the discontinuous capacitor voltage mode (DCVM). Through detailed analysis of the circuit principle and reasonable parameter selection, the input current dead-time is eliminated and the power factor correction is realized.
2. The equivalent mathematical model of the full-bridge circuit is established based on the state-space averaging method, which lays the foundation for the controller design.
3. A parameter adaptive terminal sliding mode control strategy for full-bridge converter is proposed. The strategy has strong anti-interference capability and the parameters γ can be adjusted in real time according to the system state to ensure the optimal control effect of the system under different operating conditions.

This paper is organized as follows. Section 2 introduces the analysis and design of the front-stage Buck PFC circuit. Section 3 presents the analysis and design of the rear-stage full-bridge DC/DC converter. Section 4 introduces the control strategies of the front and rear stages respectively, and shows the simulation results. Section 5 shows and analyzes the experimental results. Finally, Section 6 summarizes the conclusions.

2 Analysis and design of front-stage Buck PFC circuit

2.1 Analysis of operating characteristics of Buck PFC circuit in DCVM mode

The front stage uses a Buck PFC circuit operating in discontinuous capacitor voltage mode [20], as shown in (Fig 1). An LC filter circuit was added to the input side of the conventional Buck PFC circuit. The value of inductor L_1 is sufficiently large to ensure that the current flowing through L_1 is always continuous during the switching cycle. The value of capacitor C_1 is sufficiently low to ensure that the voltage across MOSFET Q_1 can drop to zero when Q_1 turns on.

(Fig 2) shows a typical waveform of the Buck PFC circuit working in the DCVM mode. A complete switching cycle consists of three operating modes, which can be briefly summarized as capacitor C_1 discharge mode, diode D_5 freewheeling mode, and capacitor C_1 charging mode.

From (Fig 2), when $T = T_s$, the voltage across capacitor C_1 reaches its maximum, and the peak voltage is

$$V_{cm} = \frac{I_{L1}}{C_1}(1\text{-}D)T_s \tag{1}$$

where V_{cm} is the peak voltage across capacitor C_1, I_{L1} is the current of inductor L_1 and D is the duty cycle.

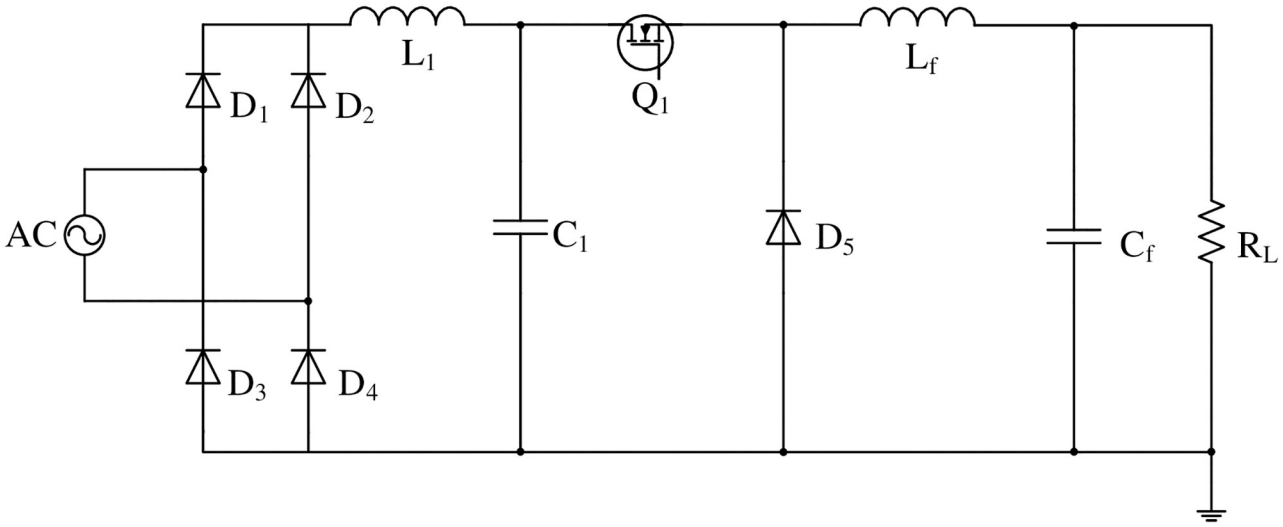

Fig 1. Buck PFC circuit operating in DCVM mode.

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According to the principle of volt-second balance, the average voltage across inductors L_1 and L_f were both 0 V at steady state, thus the expression can be obtained:

$$V_{rec} = \frac{(1\text{-}D+D_1)V_{cm}}{2} \tag{2}$$

$$V_o = \frac{D_1 V_{cm}}{2} \tag{3}$$

where V_{rec} is the rectified voltage on the input side, V_o is the output voltage, and D_1 is the proportionality coefficient.

From Eqs (1)–(3), we obtain:

$$R_1 = \frac{T_s}{2C_1}(1\text{-}D)^2 \frac{V_{rec}}{V_{rec}\text{-}V_o} \tag{4}$$

where R_1 is the equivalent resistance viewed from the input side.

For convenience, the derivation of the subsequent formulas is based on the following assumptions:

1. The input voltage is a sine wave after the rectification. The input voltage is expressed as $V_{in}=V_1 \sin w_L t$, where $w_L=2\pi/T$, V_1 is the input voltage peak, T is the power frequency voltage period, and $T >> T_s$.
2. The filter capacitor C_f is sufficiently large to ensure that the output voltage can be regarded as a constant within half a power-frequency period.
3. The input side inductance L_1 and output side inductance L_f are sufficiently large to ensure that the current flowing through them in one switching cycle can be regarded as a constant.

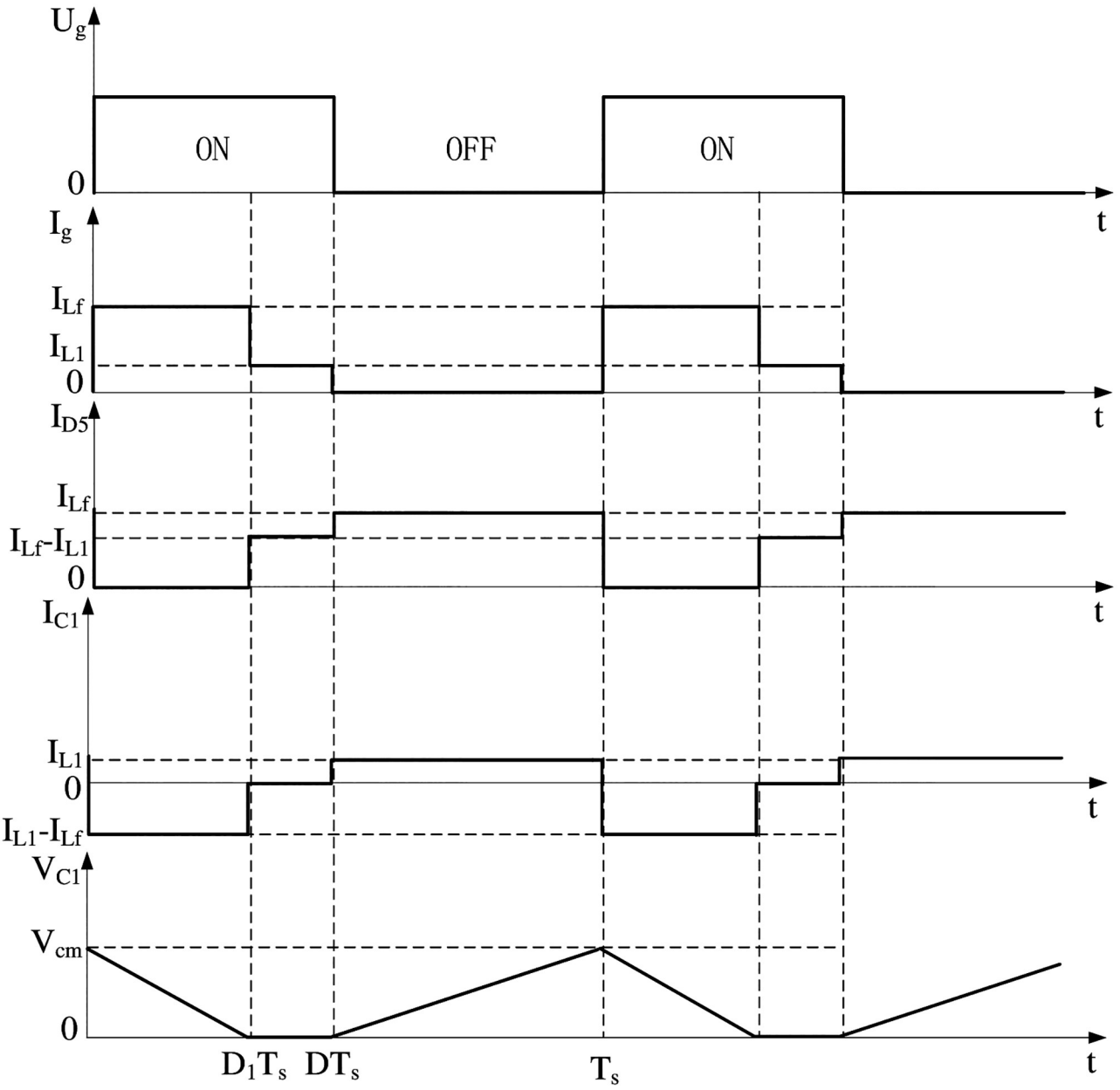

Fig 2. Working waveforms of Buck PFC circuit in DCVM mode.

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Based on the above assumptions, the circuit operates only when the input voltage is greater than the output voltage. There is an edge conduction time t_{edge}, which can be expressed as:

$$t_{edge} = \frac{1}{w_L}\arcsin\frac{V_o}{V_1} = \frac{1}{w_L}\arcsin M_s \tag{5}$$

where $M_s=V_o/V_1$ is the ratio of the output voltage to the sinusoidal input voltage peak.

Therefore, it can be inferred that the circuit can operate normally only when $t \in (t_{edge}, T/2 - t_{edge})$ during half a power frequency period, and the primary-side rectifier diodes D_1 and D_4 can turn on normally.

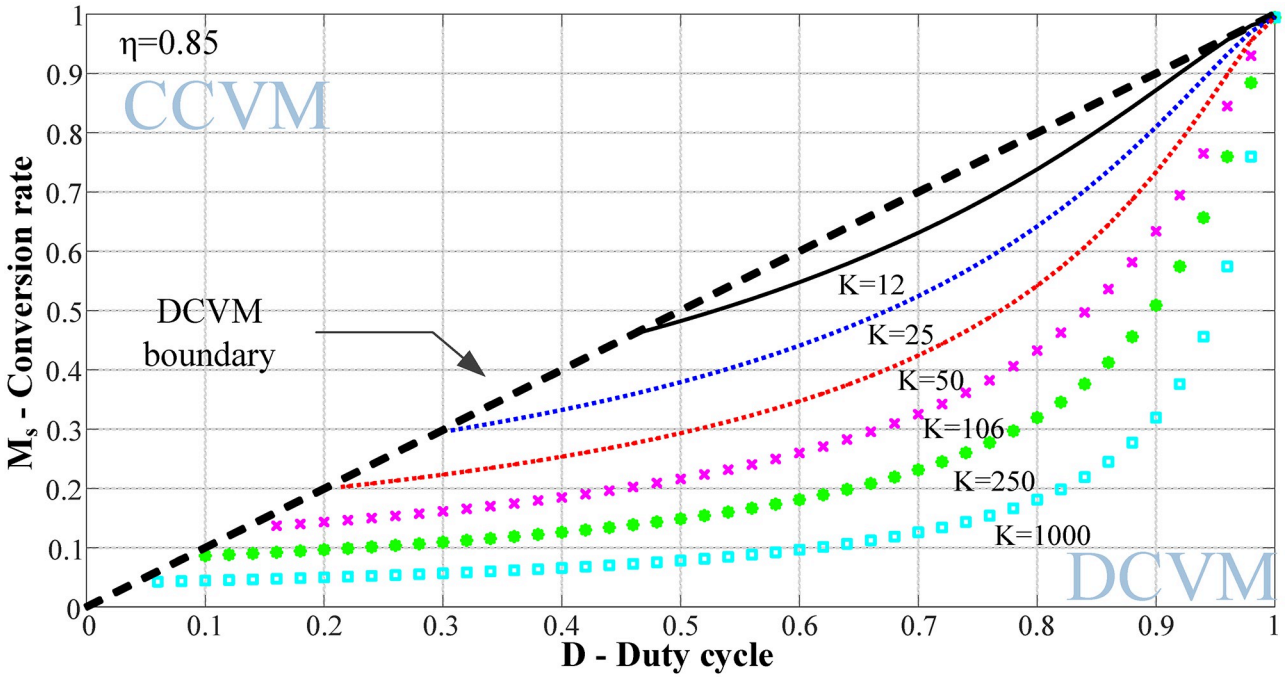

Fig 3. M_s-D **curve at efficiency** η **=0.85.**

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According to the law of energy conservation and conversion efficiency, the relationship between the output energy and input energy is $W_2 = \eta W_1$, which can be obtained as

$$\frac{KM_s^2(1\text{-}D)^2}{4} = \eta[\frac{1}{2}\text{-}\frac{1}{\pi}\arcsin M_s\text{-}\frac{M_s\sqrt{1\text{-}M_s^2}}{\pi}] \tag{6}$$

where K is the parameter, K=$2T_s$ / ($R_L C_1$).

Eq (6) contains four variables K, D, η, and M_s, where K, D, and η can be regarded as independent variables and M_s can be regarded as dependent variables. Different values of M_s can be obtained by assigning different values to K, D, and η. Thus, the relationship curve of the voltage conversion rate M_s with the duty cycle D at different K values at a certain efficiency can be drawn.

(Fig 3) shows the M_s-D curve when η =0.85. The black double dashed line is the system boundary curve indicating whether the circuit can operate in the DCVM mode. When parameter K increases, the curve moves downward, and the effective duty cycle adjustment range of the circuit increases.

However, different values of K affect the voltage stress of the MOSFET. The maximum time of the MOSFET voltage stress was the time of the input voltage peak. At this time, the voltage across the MOSFET was.

$$V_{ds} = \frac{2(V_1\text{-}V_o)}{1\text{-}D} \tag{7}$$

The ratio of the voltage borne by the MOSFET to the peak input sinusoidal voltage is defined as K_s=V_{ds} / V_1. Substituting the K_s expression into Eq (7), we obtain

$$K_s = \frac{2(1\text{-}M_s)}{1\text{-}D} \tag{8}$$

Where D is eliminated by combining Eqs (6) and (8), the expressions for K, M_s, K_s, and η can be obtained:

$$K(M_s\text{-}M_s^2)^2\text{-}K_s^2\eta[\frac{1}{2}\text{-}\frac{1}{\pi}\arcsin M_s\text{-}\frac{M_s\sqrt{1\text{-}M_s^2}}{\pi}] = 0 \quad (9)$$

In Eq (9), K and η are considered as constants, while M_s and K_s are considered as independent and dependent variables, respectively. (Fig 4) shows the curves of the relationship between M_s and K_s corresponding to different parameters K and efficiency η.

(Fig 4) shows that for the same conversion ratio M_s, the larger the value of K, the higher is the voltage stress borne by the MOSFET. As the efficiency of the circuit decreased, the voltage stress increased. To reduce the voltage stress, the value of parameter K should be as small as possible. However, considering the M_s-D curve, the value of K should be as large as possible to ensure that the circuit has a larger range of load regulation. Therefore, when determining parameter K, it is necessary to comprehensively consider the MOSFET voltage stress and duty cycle regulation range to determine the optimal value of parameter K.

2.2 Determination of Buck PFC circuit parameters in DCVM mode

The specific design parameters of the circuit are listed in Table 1 for the design requirements of a small power converter.

Referring to the design parameter requirements in Table 1, we can calculate the parameters of the Buck PFC circuit operate in DCVM mode. Considering that the input voltage range is 90-264 VAC, that is, there is a limit to the value range of M_s. Substituting it into Eq (5), the value interval of M_s can be obtained as

$$0.064 \leq M_s \leq 0.189 \quad (10)$$

Additionally, it is important to consider the circuit performance when the RMS of the input voltage is 220V, that is $M_s = 0.077$.

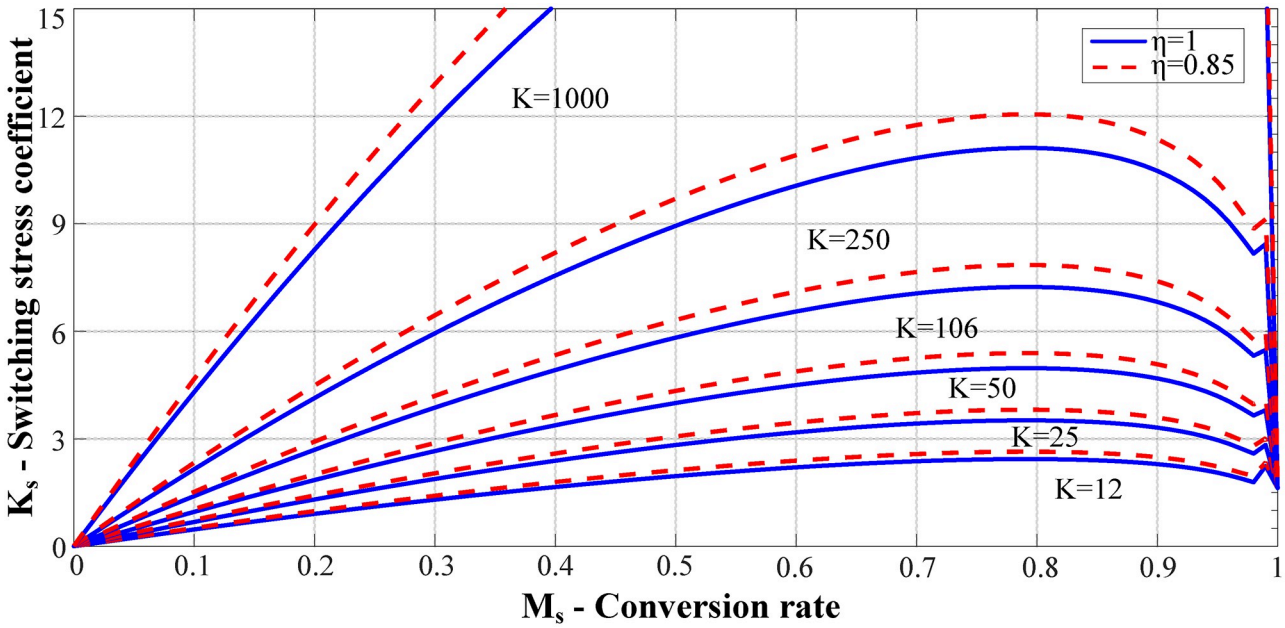

Fig 4. M_s-K_s curve under different parameter K and η.

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Table 1. Design parameters of Buck PFC circuit.

Design parameters	Reference values
Input voltage	90-264 VAC
Output voltage	24 VDC
Rated power	100 W
Output voltage ripple	≤5%
Input current THD	IEC61000-3-2 Class C
Input side PF	≥95%

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Here, M_s is 0.064, 0.077, and 0.189, respectively. The corresponding duty-cycle values under different K values and whether the circuit can operate in the DCVM mode are listed in Table 2.

From Table 2, to ensure that the circuit operates in the DCVM mode, the value of K should be greater than or equal to 500. Combined with the M_s-K_s relationship curve, for the same voltage conversion ratio M_s, reducing the value of parameter K can reduce the voltage stress on the MOSFET. Therefore, after a comprehensive consideration, K = 500.

Substituting the switching frequency f_s = 100kHz and equivalent load R_L = 6 Ω into $K=2T_s/(R_LC_1)$, we calculated C_1 = 6.67 nF.

Inductor L_1 should ensure that the current flowing through it in a switching cycle is continuous. Basically, the resonant period of the resonant current flowing through L_1 is significantly larger than the switching period of the MOSFET. This satisfies the following formula:

$$2\pi\sqrt{L_1C_1} \gg (1-D)T_s \tag{11}$$

However, the value of L_1 is not too large, thus inductance L_1 can be ignored from the input side. Therefore, this value should satisfy the following requirements:

$$R_1 \gg \frac{2\pi L_1}{T} \tag{12}$$

Combining Eqs (4), (11) and (12), the value range of L_1 can be obtained as

$$\frac{(1-D)^2T_s^2}{4\pi^2C_1} \ll L_1 \ll \frac{T_sTV_{rec}(1-D)^2}{4\pi C_1(V_{rec}-V_o)} \tag{13}$$

By substituting into the circuit parameters when V_{rms} = 220 V and K = 500, the value range of L_1 can be calculated. Based on a comprehensive consideration, L_1 = 3.2 mH.

Inductance L_f can be determined using the derivation method of L_1. When the MOSFET is turned on, the current flowing through inductor L_f is guaranteed to be continuous in one

Table 2. Analysis of circuit operating characteristics under different *K* values at η =0.85.

K	1000	900	800	700	600	500	400	350	300
Duty cycle *D* when M_s=0.064	0.38	0.35	0.31	0.26	0.20	0.13	0.02	-0.04	-0.13
Duty cycle *D* when M_s=0.077	0.49	0.46	0.43	0.39	0.34	0.28	0.19	0.14	0.07
Duty cycle *D* when M_s=0.189	0.81	0.79	0.78	0.77	0.75	0.73	0.69	0.67	0.65
Whether it can operate in DCVM	Y	Y	Y	Y	Y	Y	N	N	N

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switching cycle, which can be obtained as

$$2\pi\sqrt{\frac{L_1 L_f C_1}{L_1+L_f}} \gg DT_s \tag{14}$$

Further:

$$L_f \gg \frac{D^2 T_s^2 L_1}{4p^2 L_1 C_1 - D^2 T_s} \tag{15}$$

Eq (15) describes only the lower limit of inductance L_f. The determination of L_f also should comprehensively consider factors such as inductor current ripple and finally select L_f = 250 μH. The determination of capacitor C_f should comprehensively consider the output voltage ripple and the voltage holding time, and finally select C_f = 20 mF.

3 Analysis and design of rear-stage full-bridge DC/DC converter

3.1 Analysis of operating characteristics of Full-Bridge converter with clamping diode

Traditional full-bridge converters can achieve soft-switching of the primary-side MOSFET, but the transformer leakage inductance resonates with the junction capacitance of the diode during circuit operation. This phenomenon leads to the output oscillation and voltage spike of the rectifier bridge, which affects the selection of the rectifier diode. Therefore, this study selected a full-bridge converter with a clamping diode in series on the primary side of the transformer [21,22], as shown in (Fig 5).

To realize a MOSFET zero-voltage switch (ZVS), there should be enough energy to meet three conditions:

1. Release the energy stored in the parasitic capacitance of the MOSFET to be turned on.
2. Charge the parasitic capacitance of the MOSFET turned off at the same leg.
3. Considering the influence of the parasitic parameters of the transformer, a part of the energy is required to release the energy stored in the distributed capacitance of the transformer winding.

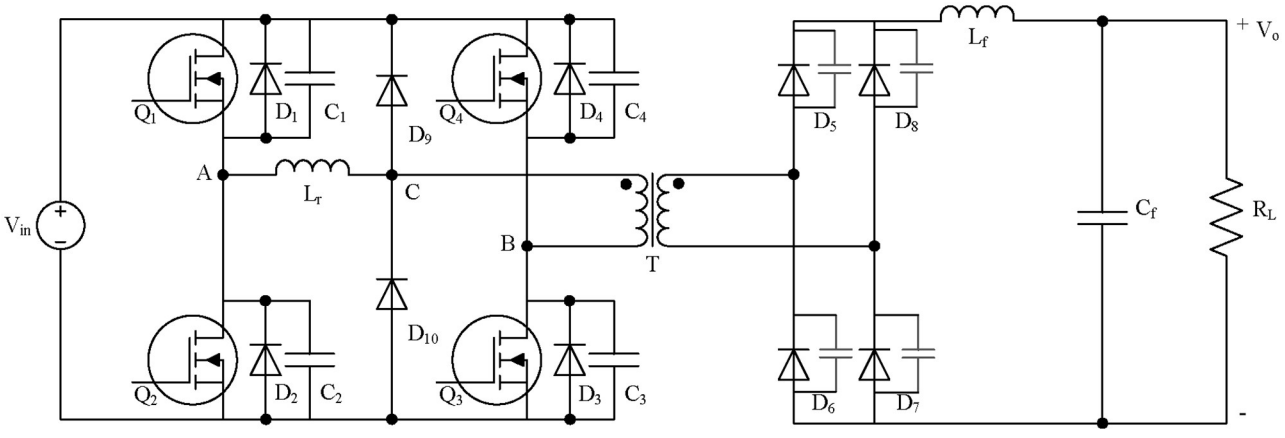

Fig 5. Full-Bridge DC/DC converter with primary clamping diode.

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Therefore, the energy provided by the inductor should meet:

$$E > \frac{1}{2}C_i V_{in}^2 + \frac{1}{2}C_i V_{in}^2 + \frac{1}{2}C_{Tr} V_{in}^2 = C_i V_{in}^2 + \frac{1}{2}C_{Tr} V_{in}^2 \quad (16)$$

where C_i is the parasitic capacitance in parallel with the MOSFET(i=1,2,3,4), and C_{Tr} is the distributed capacitance of the transformer winding. For the leading leg, the resonant inductance L_r and output filter inductance L_f work in the equivalent series mode, and the value of L_f is usually large. Therefore, the two inductors together provide the energy required by the MOSFETS ZVS, which can easily meet the requirements of the above equation.

However, during the operation of the lagging leg, because the secondary rectifier diodes were all turned on, the transformer voltage was limited to 0 V, and the secondary side of the circuit was in a short-circuit state. At this time, the circuit is divided into two parts, and the output filter inductance L_f can no longer be converted to the primary side. The energy stored in the parasitic capacitance C_i and the transformer distributed capacitance C_{Tr} should be completely released by the resonant inductance L_r. Therefore, the realization of MOSFET ZVS should satisfy the following requirements:

$$\frac{1}{2}L_r I_{Lr}^2 > C_i V_{in}^2 + \frac{1}{2}C_{Tr} V_{in}^2 \quad (17)$$

where I_{Lr} is the resonant inductance current.

It can be observed that soft switching of the lagging-leg is more difficult to be achieved. On the premise of not considering the change in transformer core parameters, only a reasonable setting of the parameter of the resonant inductance L_r can realize the ZVS of the MOSFET on both legs.

3.2 Parameter determination of Full-Bridge converter with primary clamping diode

The design parameters of the full-bridge DC/DC converter are listed in Table 3.

3.2.1 MOSFET and rectifier diode selection. First, the maximum input current on the primary side should be calculated:

$$I_{in\_max} = \frac{P_{in\_max}}{V_{in\_min} D_{max}} \quad (18)$$

where P_{in_max} is the maximum input power, V_{in_min} is the minimum input voltage, and D_{max} is the maximum duty cycle for the entire machine operation.

Considering the target efficiency of more than 90%, P_{in_max}= 111.11 W was calculated from the output power. Owing to the loss of duty-circle in the full-bridge converter, let D_{max}= $2D_s$. Substituting it into Eq (18) we obtain I_{in_max}= 6.613A. From this, the maximum current

Table 3. Design parameters of Full-Bridge DC/DC converter.

Design parameters	Minimum value	Typical value	Maximum value	Unit
Rated output power P_{out}	--	100	--	W
Input voltage V_{in}	24	24	26	V
Output voltage V_{out}	12	14	14	V
Output voltage ripple ΔV_{out}	-5	--	+5	%
Operating frequency f_s	--	50	--	kHz
Operating maximum duty cycle D_s	--	35	--	%
Target efficiency η	--	90	--	%

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flowing through the MOSFET can be calculated as

$$I_{\text{mos\_rms}} = I_{\text{in\_max}} \times \sqrt{\frac{D_{\max}}{2}} = 3.912\ \text{A} \tag{19}$$

In full-bridge converters, the voltage of a single MOSFET is the primary input voltage. Based on the requirements of 1.5 times the withstand voltage and three times the overcurrent, we selected an N-channel MOSFET with an overcurrent of 18 A and a withstand voltage of 40 V, model LNL04R075.

The selection of the rectifier diode can be based on the selection method of the MOSFET. First, we calculated the RMS value of the maximum current flowing through the diode.

$$I_{\text{dio\_rms}} = I_{\text{out\_nom}} \sqrt{\frac{D_{\max}}{2}} = \frac{P_{\text{out}}}{V_{\text{out}}} \sqrt{\frac{D_{\max}}{2}} = 4.226\ \text{A} \tag{20}$$

where $I_{\text{out\_nom}}$ is the rated output current.

Considering a margin of 1.5 times, this value is too large for a single diode; therefore, two diodes were used in parallel. Therefore, the current flowing through a single diode was 3.2 A. When the diode was cut off, the reverse voltage of the single diode was the output voltage. Based on the margin of 1.2 times, the selected rectifier diode should have at least 17V reverse withstand voltage. In summary, this study chose a fast recovery Schottky diode of type MBRD6U60CT as the rectifier diode on the secondary side.

3.2.2 Selection of primary clamp diode. The clamping diode was selected according to the selection method for the rectifier diode. The reverse voltage of the clamp diode was the input voltage of the power supply. Considering a margin of 1.5 times, the clamping diode should withstand at least 36 V. Because the current flowing through the clamp diode is the difference between the resonant current and the primary current, the value is relatively small; therefore, the overcurrent requirement for the primary clamp diode can be appropriately lowered. In summary, this study chose a fast recovery diode of type ES2A as the primary clamp diode.

3.2.3 High frequency transformer design. The transformer ratio should consider the situation when the input voltage is the lowest and the duty cycle is the largest.

$$N_{\text{ps}} = \frac{V_{\text{in\_min}} D_{\max}}{V_{\text{out\_nom}} + V_{\text{F}} + 0.5\text{V}} \tag{21}$$

Let $D_{\max} = 0.7$, the conduction voltage drop in the rectifier diode $V_{\text{F}} = 0.65$ V, and then consider the line voltage drop of 0.5 V, then substitute into the calculation to obtain $N_{\text{ps}} = 1.109$. Here, the transformation ratio was set as 1.1.

3.2.4 Design of resonant inductor. From the analysis of the full-bridge converter soft-switching implementation conditions, it is clear that the soft-switching of the MOSFETs in the lagging-leg is more difficult to achieve; therefore, the resonant inductor parameter values should be reasonably designed. Considering the distributed capacitance of the transformer and the output parasitic capacitance of the MOSFET, the equivalent parasitic capacitance C_{r} within a switching cycle is expressed as:

$$C_{\text{r}} = 2 \times C_{\text{i}} + C_{\text{Tr}} \tag{22}$$

By consulting the datasheet of LNL04R075 and estimation of the transformer stray capacitance, we obtained $C_{\text{i}} = 316$ pF and $C_{\text{Tr}} = 100$ pF, and by calculation we obtain $C_{\text{r}} = 732$ pF.

When the input voltage is the highest, the maximum energy stored by the equivalent parasitic capacitance is

$$E_{Cr} = \frac{1}{2} \times C_r \times V_{in\_max}^2 = 247.416\ \text{nJ} \tag{23}$$

Taking 2% of the switching period as the switching state transition time, the resonant inductance L_r can be determined using the following equation:

$$L_r = \frac{2\% \times \frac{1}{f_s}}{2} \times \frac{V_{in\_nom} N_{ps}}{I_{out\_nom}} = 0.745\ \mu\text{H} \tag{24}$$

Let L_r=1 μH, based on the actual situation. therein, the minimum primary current required to realize soft-switching is calculated as

$$I_{ZVS} = \sqrt{\frac{E_{Cr}}{L_r}} = 0.497\ \text{A} \tag{25}$$

According to Eq (25), the current is far less than the primary current value of the circuit under normal operation; therefore, the selected resonant inductor can ensure that the MOSFET operates in the soft-switching state.

3.2.5 Design of output filter inductor and filter capacitor. Because the full-bridge converter can be regarded as a derivative circuit of the Buck converter, the design of its LC filter can refer to the design method of the buck circuit, as shown in the following equation:

$$L_f = \frac{V_{out\_nom}}{(2f_s)20\% I_{out\_nom}} \left[1 - \frac{V_{out\_nom}}{\frac{V_{in\_max}}{N_{ps}} - V_D - V_{Lf}}\right] \tag{26}$$

where V_{out_nom} is the rated output voltage, f_s the switching frequency, V_{in_max} the maximum input voltage, N_{ps} the transformer ratio, V_D the diode voltage drop, and V_{Lf} the filtered inductive voltage drop. Considering actual conditions, L_f =50 μH.

The design of the output filter capacitor mainly should consider the output voltage ripple requirements, as analyzed based on the following equation:

$$C_f = \frac{V_{out\_min}}{8L_f(2f_s)^2 \Delta V} \left[1 - \frac{V_{out\_min}}{\frac{V_{in\_max}}{N_{ps}} - V_D - V_{Lf}}\right] \tag{27}$$

where ΔV is the output voltage ripple.

Let ΔV = 5%, V_{out_nom} = 0.7V, and calculate C_f = 2 μF. To eliminate the high-frequency component of the output voltage, it is necessary to ensure that the turning frequency of the output filter is less than 10 times the switching frequency.

$$\frac{1}{2p\sqrt{L_f C_f}} < \frac{f_s}{10} \tag{28}$$

In summary, C_f = 100μF.

4 Control strategy of two-stage AC/DC converter

4.1 Control strategy design

The two-stage AC/DC converter control strategy is illustrated in (Fig 6).

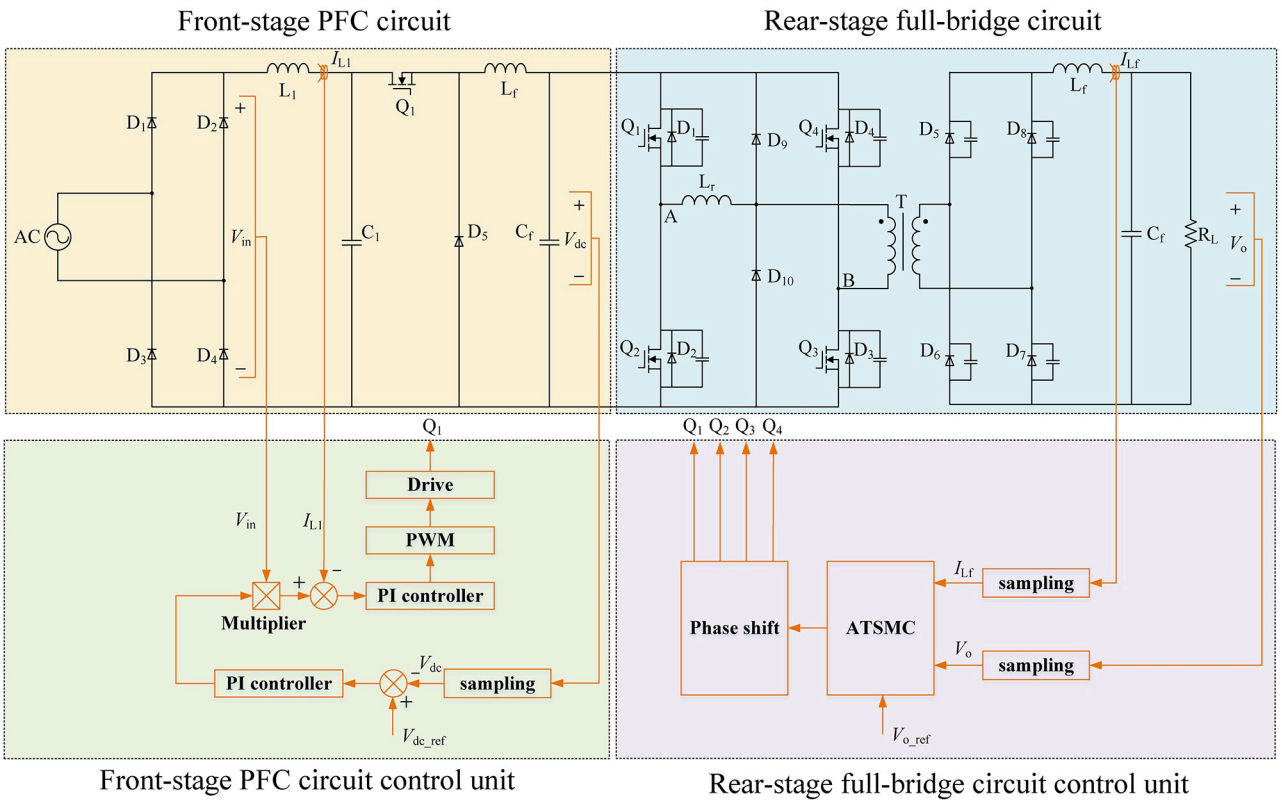

Fig 6. Control strategy of two-stage AC/DC converter.

https://doi.org/10.1371/journal.pone.0275056.g006

The front-stage PFC circuit adopts a PI double-closed-loop control strategy [23]. The output voltage, input voltage, and input current were collected as the control variables. The given value of the outer loop voltage was obtained by comparing the output voltage V_{dc} with the reference voltage V_{dc_ref} in real time. After calculation by the voltage PI controller, it was multiplied by the input voltage V_{in} to obtain the current reference whose phase was consistent with the input voltage. Then, the current reference was compared with the input current I_L as the given value of the current inner loop. After calculation by the current PI controller, it was output to the PWM generator to generate the driving waveform to control Q_1. This strategy realized the tracking of the current phase and the stabilization of the output voltage.

The rear-stage full-bridge circuit adopts a parameter adaptive terminal sliding mode control (ATSMC) strategy [24–26]. The full-bridge converter was derived from the Buck circuit, so the equivalent circuit topology is shown in (Fig 7).

Q^* represents the equivalent MOSFET of the full-bridge converter. Based on the state-space averaging method, the equation describing the working state of the circuit can be obtained as follows:

$$\frac{di_L}{dt} = \frac{V_{in}}{N_{ps}L_f}u - \frac{V_o}{L_f} \tag{29}$$

$$\frac{dV_o}{dt} = \frac{i_{Lf}}{C_f} - \frac{V_o}{R_L C_f} \tag{30}$$

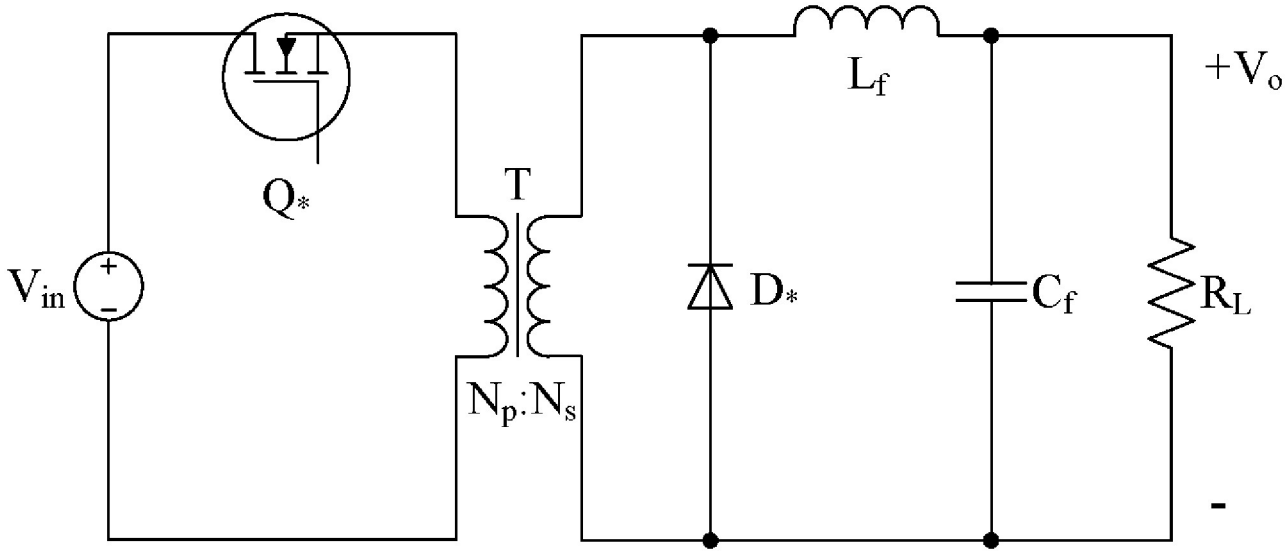

Fig 7. Buck circuit equivalent model of full-bridge converter.

https://doi.org/10.1371/journal.pone.0275056.g007

where u is the equivalent switching control law of switch Q *. When $u = 1$, switch Q * is on, and when $u = 0$, it is OFF. N_{ps} represents the transformer ratio, $N_{ps}=N_p/N_s$.

The output voltage error x_1 and its rate of change x_2 are defined as follows:

$$x_1 = V_o - V_{ref} \tag{31}$$

$$x_2 = \dot{x}_1 = \dot{V}_o - \dot{V}_{ref} \approx \dot{V}_o \tag{32}$$

where V_{ref} is the reference value of the output voltage, $\dot{x}_1$ represents the derivative of x_1 to time.

Subsequently, the equivalent mathematical model of the full-bridge converter is expressed as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\dfrac{1}{L_f C_f} & -\dfrac{1}{R_L C_f} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \dfrac{uV_i - N_{ps} V_{ref}}{N_{ps} L_f C_f} \end{bmatrix} \tag{33}$$

To make the system state tracking error approach zero in a finite time, a nonlinear function was introduced in the design of the sliding surface. Sliding surface function S is defined as follows:

$$S = \dot{x}_1^{\gamma} + k_a x_1^{\gamma} + k_b \int_0^t x_1^{\gamma} d\tau \tag{34}$$

$$k_a < 0, k_b < 0, 0 < \gamma < 1 \tag{35}$$

where K_a and K_b are sliding mode coefficients.

According to the Lyapunov stability criterion, to ensure that the system state trajectory can reach and remain on the sliding surface, the system state should satisfy the following

requirements:

$$S\dot{S} < 0 \tag{36}$$

Here, the Lyapunov function was selected as $V = \frac{1}{2}S^2$, then $\dot{V} = S\dot{S}$. Taking the derivative of Eq (34) and substituting Eq (33) into it, we can get:

$$\dot{S} = \frac{\gamma V_{in}}{N_{ps}L_f C_f^{\gamma}}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{\gamma-1} u - \frac{\gamma V_o}{L_f C_f^{\gamma}}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{\gamma-1} - \frac{\gamma}{R_L C_f^{\gamma+1}}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{\gamma} + k_a \gamma x_1^{\gamma-1}\frac{1}{C_f}\left(i_{Lf} - \frac{V_o}{R_L}\right) + k_b x_1^{\gamma} \tag{37}$$

When u=1, S<0, need $\dot{S} > 0$

$$\dot{S} = \frac{\left(V_{in} - N_{ps}V_o\right)\gamma}{N_{ps}L_f C_f^{\gamma}}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{\gamma-1} - \frac{\gamma}{R_L C_f^{\gamma+1}}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{\gamma} + k_a \gamma x_1^{\gamma-1}\frac{1}{C_f}\left(i_{Lf} - \frac{V_o}{R_L}\right) + k_b x_1^{\gamma} > 0 \tag{38}$$

When u=0, S>0, need $\dot{S} < 0$

$$\dot{S} = -\frac{\gamma V_o}{L_f C_f^{\gamma}}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{\gamma-1} - \frac{\gamma}{R_L C_f^{\gamma+1}}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{\gamma} + k_a \gamma x_1^{\gamma-1}\frac{1}{C_f}\left(i_{Lf} - \frac{V_o}{R_L}\right) + k_b x_1^{\gamma} < 0 \tag{39}$$

If the values of k_a and k_b satisfy the above inequality equations, the Lyapunov stability condition can be satisfied. Let $\gamma \approx 1$, $i_{Lf} \approx 0$, the value range of k_a and k_b can be deduced as

$$\frac{1}{R_L C_f} - \frac{R_L}{L_f} < k_a < 0 \tag{40}$$

$$\frac{(R_L C_f)^2 - 1 + R_L C_f k_a}{(R_L C_f)^3} < k_b < 0 \tag{41}$$

When S=0, the system is in sliding mode. Let $\dot{S} = 0$, and the equivalent control law u_{eq} can be deduced from Eq (37).

$$u_{eq} = \frac{N_{ps}}{V_{in}}\left[V_o + \frac{L_f}{R_L C_f}\left(i_{Lf} - \frac{V_o}{R_L}\right) - k_a L_f C_f^{\gamma-1} x_1^{\gamma-1}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{2-\gamma} - \frac{L_f k_b}{\gamma}(C_f x_1)^{\gamma}\left(i_{Lf} - \frac{V_o}{R_L}\right)^{1-\gamma}\right] \tag{42}$$

In summary, the system control law can be written as

$$u = \begin{cases} 1 & S < 0 \\ u_{eq} & S = 0 \\ 0 & S > 0 \end{cases} \tag{43}$$

In addition, different values of γ have a significant influence on the system performance. When the value of γ increases, the response speed of the system increases, however this also leads to a large voltage overshoot. Conversely, when the value of γ decreases, the overshoot decreases in the system startup phase; however, the voltage drop increases when a disturbance occurs. This is in contrast to the desired control effect. It can be observed that a fixed γ value cannot guarantee the optimal control effect of the system. Therefore, an improved adaptive algorithm for the γ parameter is proposed, as presented in Eq (44).

$$\gamma = \frac{1}{\pi}\arctan(\lambda x_1 - 1) + 0.5 \quad (\lambda > 0) \tag{44}$$

To improve the rapidity of the system, the λ factor was introduced to improve the approach speed of the γ-adaptive algorithm in different situations to adjust the dynamic performance of the system and achieve stable voltage output.

4.2 Simulation of front-stage PFC circuit

The system is simulated based on MATLAB. By engineering turning method, the voltage outer-loop coefficients were determined as K_p=0.1 and K_i=0.5, and the current inner-loop coefficients were K_p=0.08 and K_i=4.

(Fig 8) shows the input voltage and current waveform of the circuit, where the peak value of the input voltage was 311 V. At this time, the power factor reached 99.03%, which meets the design requirements.

(Fig 9) shows the input current waveform. From the figure, the input current still has a certain degree of waveform distortion at the switching time of the positive and negative half cycles. The total harmonic distortion of the current is 16.46%, but each harmonic distortion meets the IEC61000-3-2 Class C standard, meeting the design requirements.

To verify the system recovery effect under a load disturbance, two typical conditions of load surge and load drop were simulated. The output voltage waveform of the circuit when the load surges is shown in (Fig 10). Through quantitative analysis, the output voltage can be adjusted within 100 ms, regardless of the load surge or drop. The absolute value of the maximum voltage fluctuation does not exceed 1.2V, and the output voltage ripple at the steady state is less than 5%. Therefore, the design requirements were met.

4.3 Simulation of rear-stage full-bridge converter

Based on the previous analysis, considering the stability and rapidity of the system, $\lambda = 4$, $k_a = -4 \times 10^4$, and $k_b = -3 \times 10^{10}$ were selected.

(Fig 11) shows a comparison of the output voltage waveform between γ with a fixed value and the adaptive algorithm when the system is started. Clearly from the figure, compared to

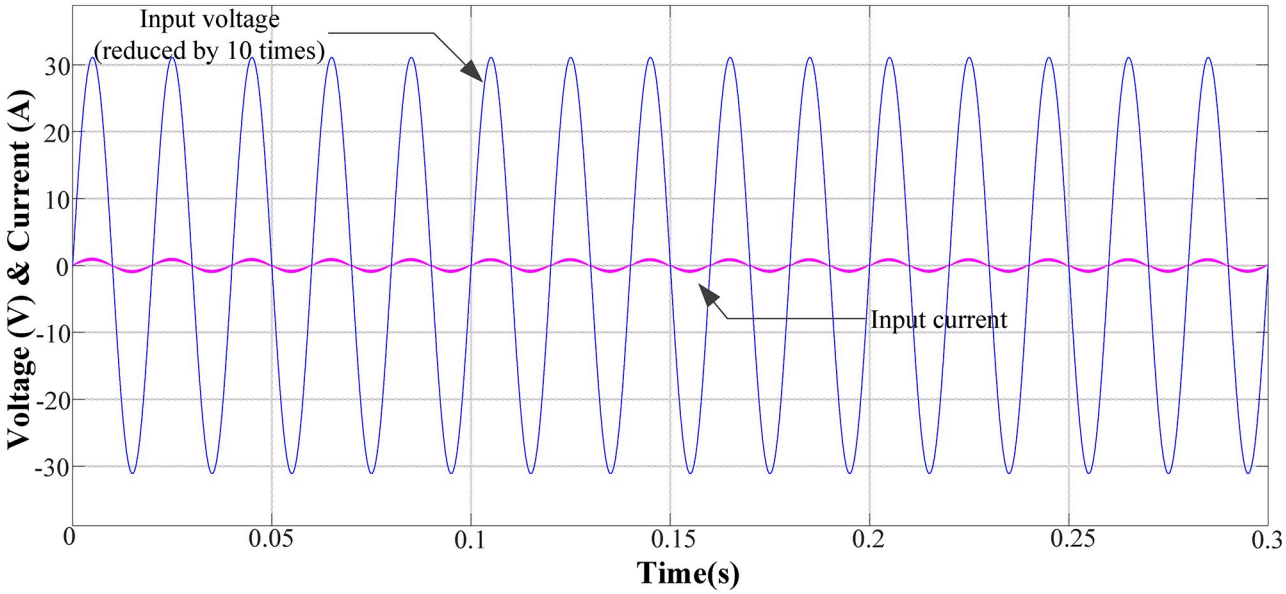

Fig 8. Input voltage and current waveforms in normal operation mode.

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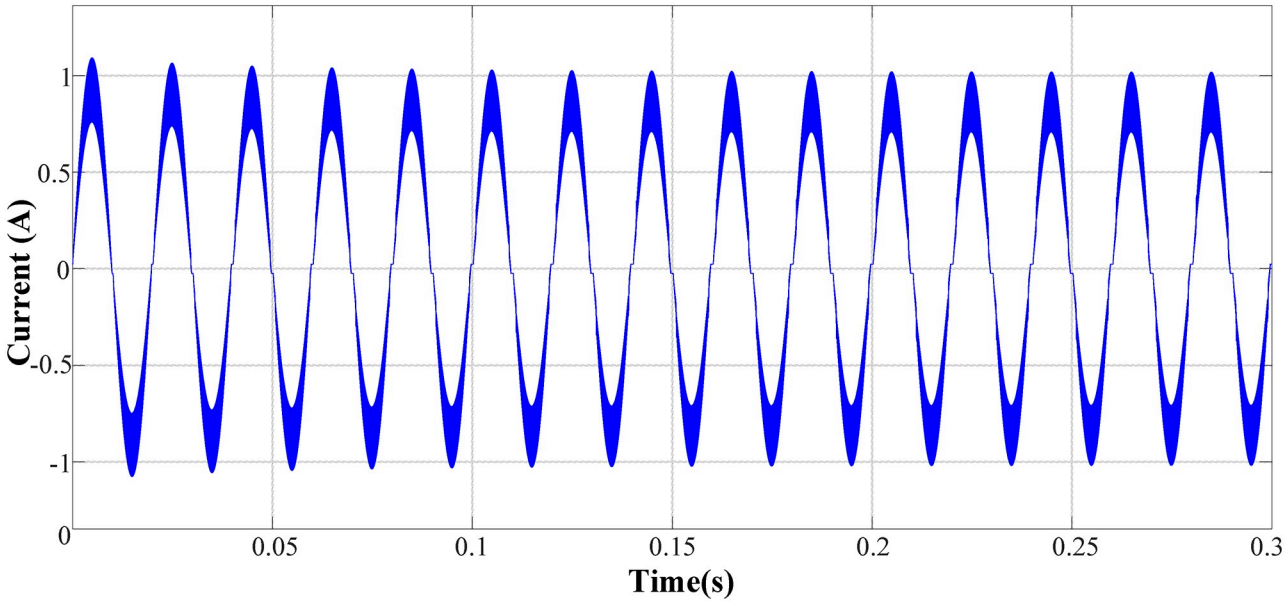

Fig 9. Input current waveform in normal operation mode.

https://doi.org/10.1371/journal.pone.0275056.g009

using a fixed γ value, the output can better track the system state using an adaptive algorithm to obtain γ value, which improves the response speed while considering system stability.

(Fig 12) shows a comparison of the output voltage waveform with a fixed γ value and the adaptive algorithm when the load generates a disturbance. The load disturbance was observed at 0.01 s. Under the adaptive algorithm, the system output voltage drop was smaller, the disturbance recovery time was shorter, and the system robustness was significantly enhanced.

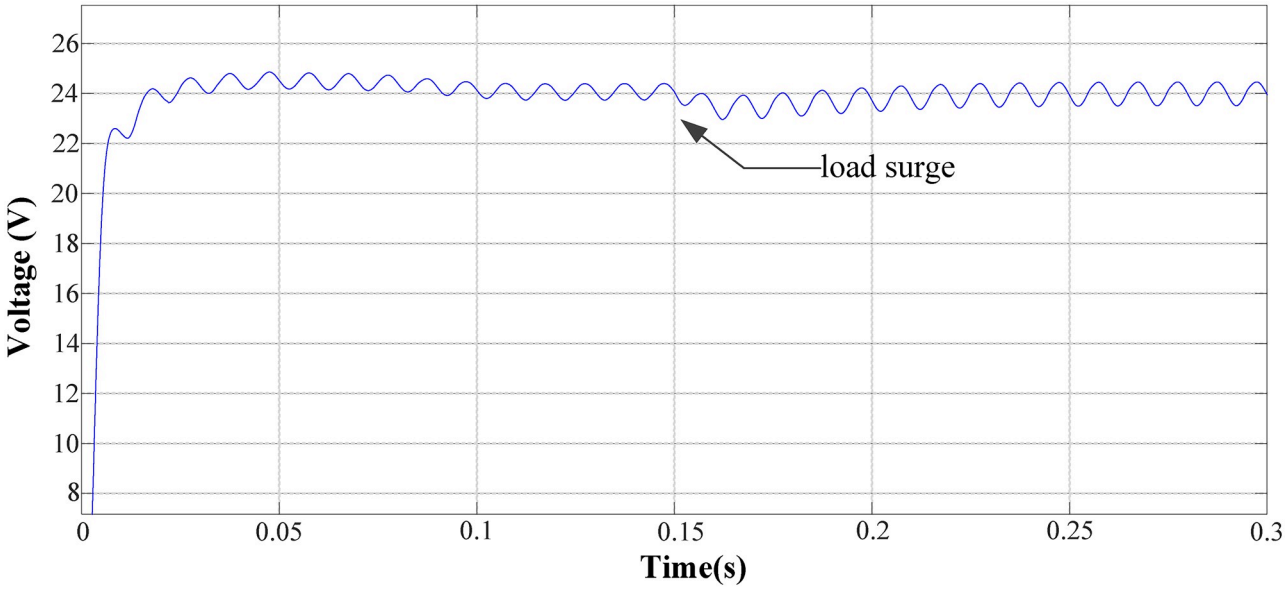

Fig 10. System output voltage waveform under load surge.

https://doi.org/10.1371/journal.pone.0275056.g010

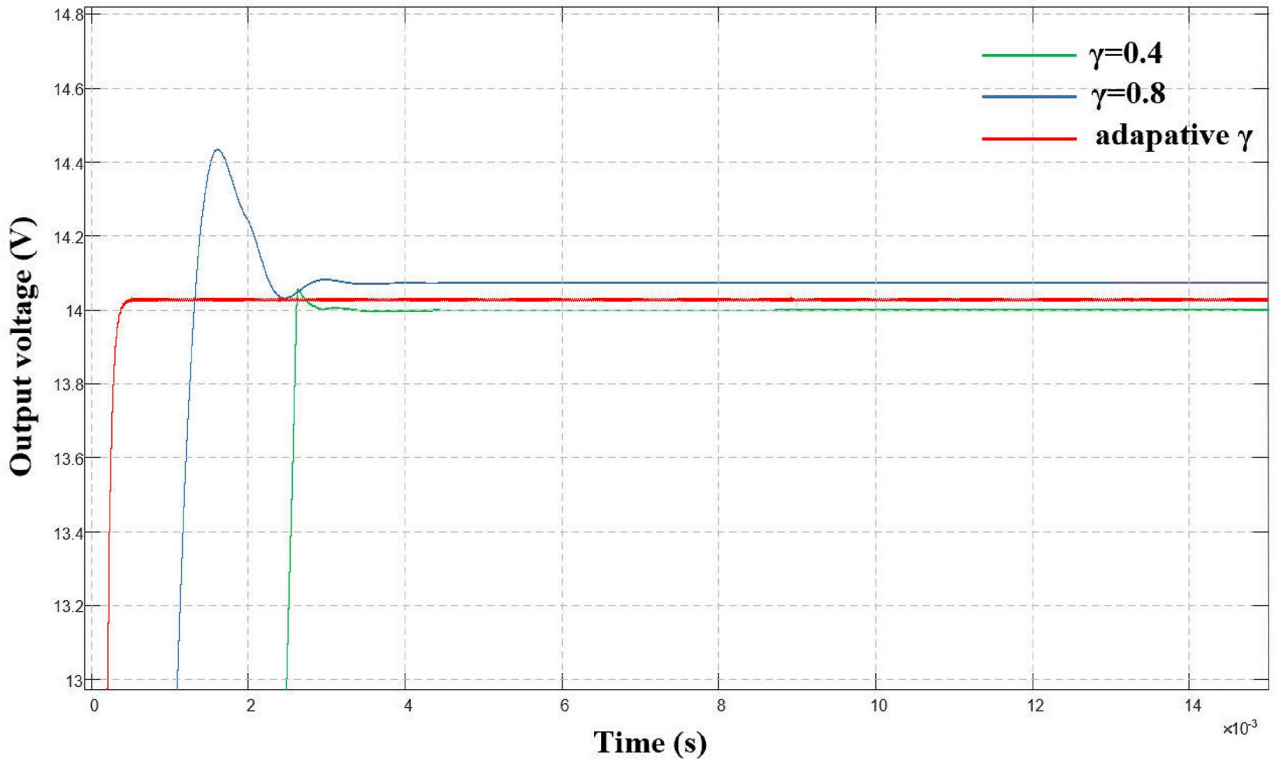

Fig 11. Comparison of output voltage waveforms at system startup.

https://doi.org/10.1371/journal.pone.0275056.g011

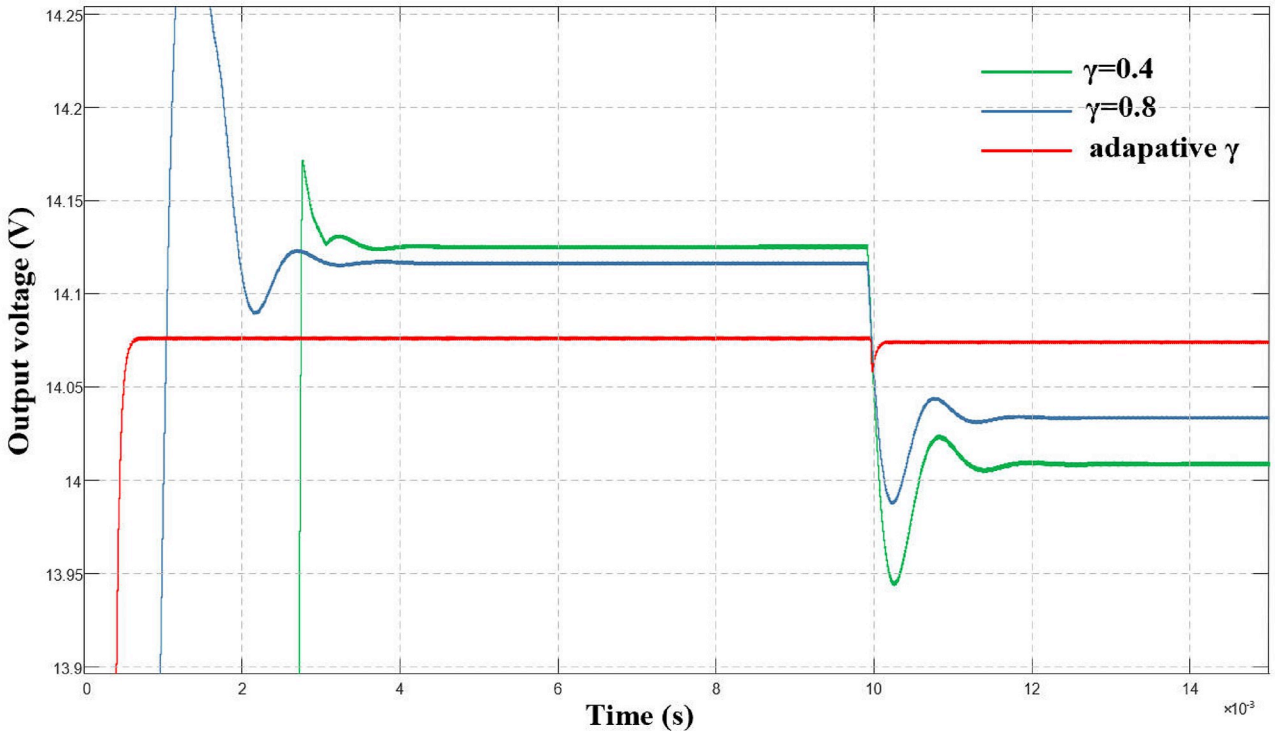

Fig 12. Comparison of output voltage waveform under load disturbance.

https://doi.org/10.1371/journal.pone.0275056.g012

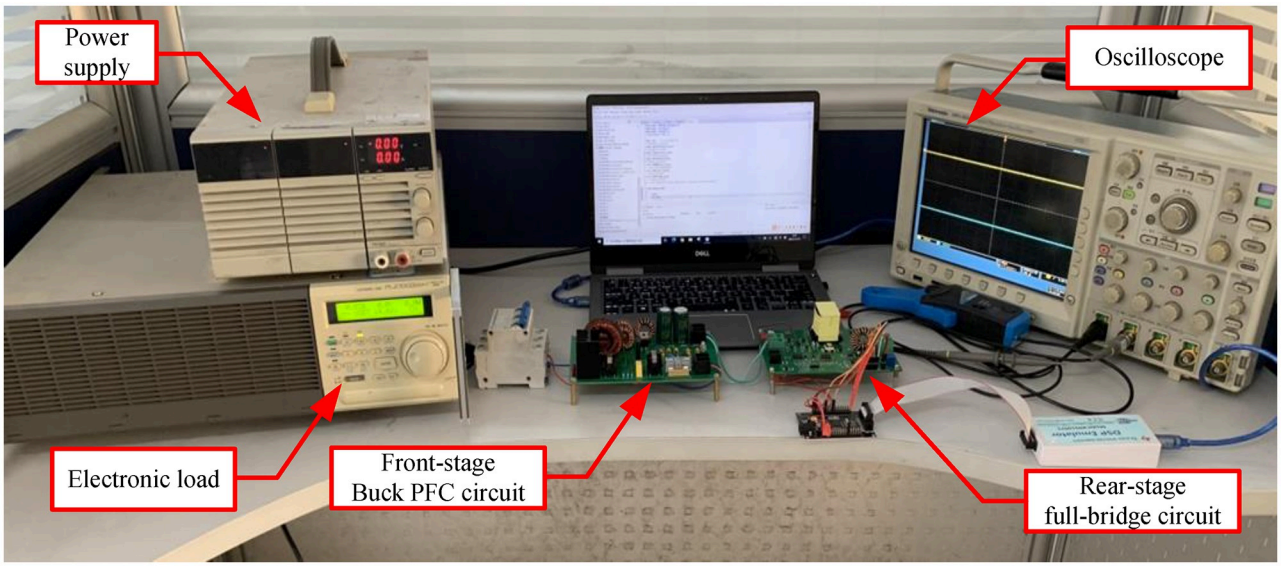

Fig 13. Prototype platform of two-stage AC/DC converter.

https://doi.org/10.1371/journal.pone.0275056.g013

5 Experimental verification

Based on the previous analysis, an experimental prototype of a two-stage isolated AC/DC converter was built. The experimental setup is illustrated in (Fig 13).

The control strategy is realized digitally by DSP. The control flow is shown in (Fig 14). TMS320F28035 is used as the main chip because of its powerful performance and its accompanying ADC module and EPWM module. The sampled voltage and current signals first enter the ADC module for processing. After the DSP calculation, the PWM drive signal is output to the isolation drive circuit through the EPWM module, and finally the control of the MOSFET is realized.

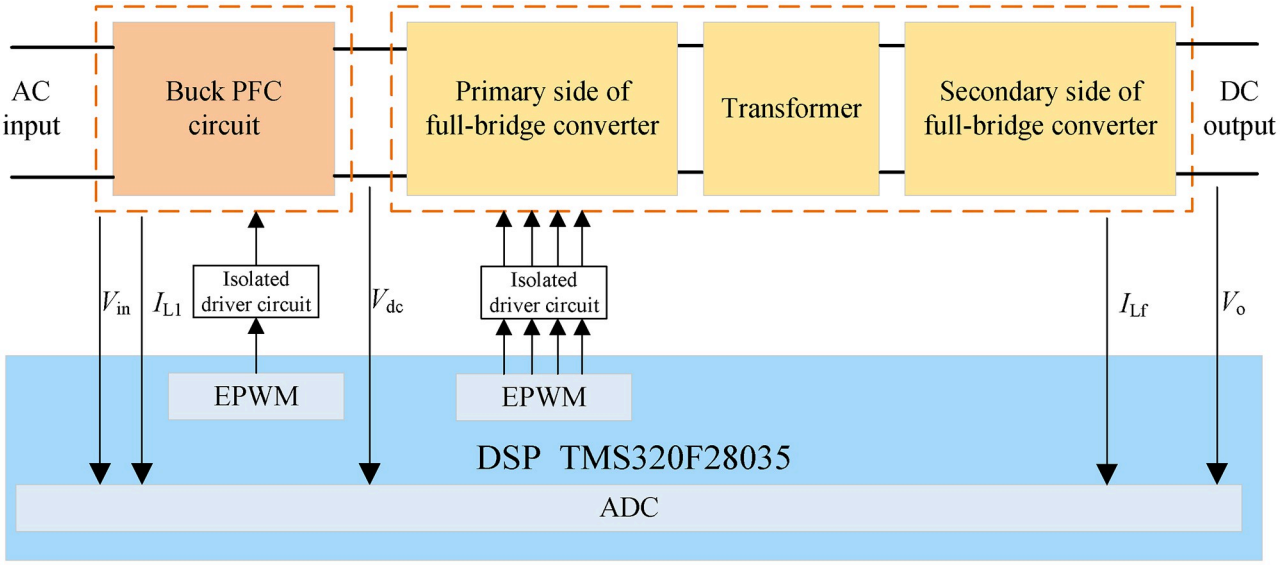

Fig 14. Software and hardware control flow chart.

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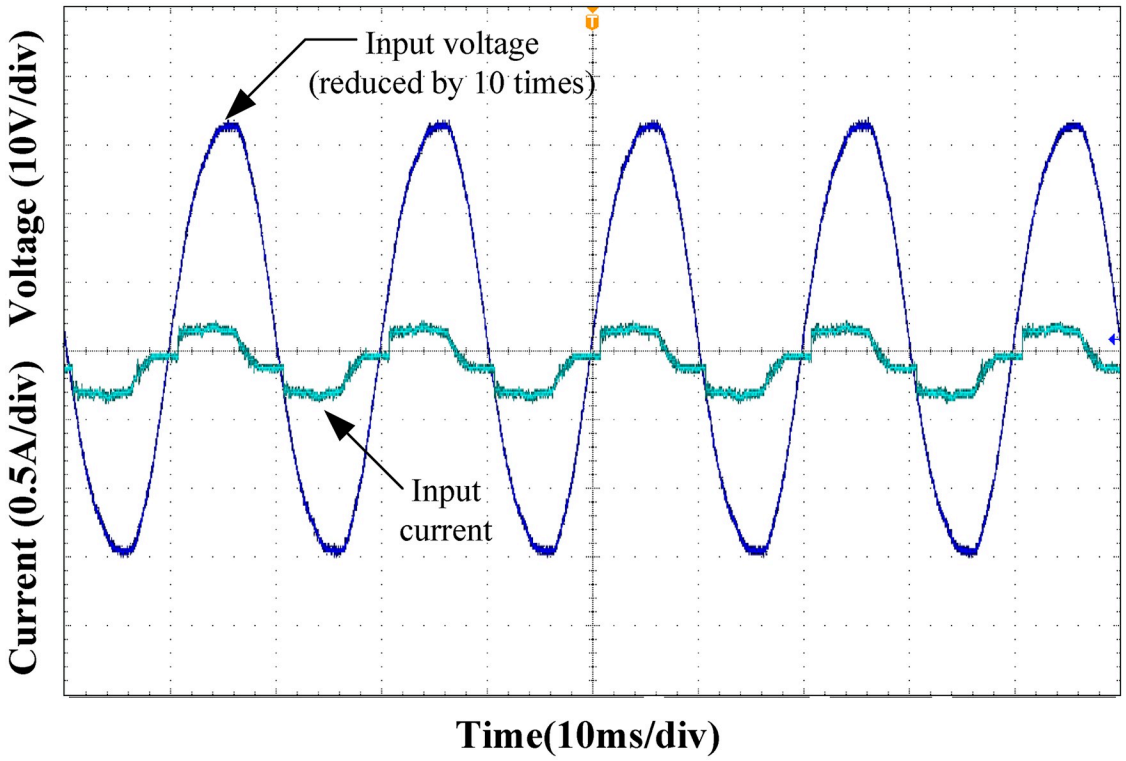

Fig 15. Input voltage and current at 25% load.

https://doi.org/10.1371/journal.pone.0275056.g015

Figs 15–18 show the input voltage and current waveforms under different load conditions. Clearly from the figure, the designed Buck PFC circuit can achieve power factor correction under different operating conditions. As the load power increased, the input current THD decreased, and the power factor of the system increased, satisfying the input requirements of the rear-stage DC/DC converter.

Figs 19 and 20 show the zero-voltage turn-on waveforms of the leading and lagging legs, respectively. As shown from the figure, when the control signal of the MOSFET arrives, the drain-source voltage drops to zero, realizing the ZVS of the MOSFET.

(Fig 21) shows the driving waveforms of MOSFET Q_1 and Q_2 in the leading-leg. By introducing dead-time, the shoot-through of the MOSFET is avoided, and sufficient time is reserved for the ZVS. (Fig 22) shows the driving waveforms of MOSFET Q_1 and Q_3 of the leading and lagging legs. It can be observed that the driving waveform has a certain phase difference, based on which the output voltage can be adjusted.

Figs 23 and 24 show the comparison of the converter startup waveforms under the PI and ATSMC control strategies, respectively. Using the new sliding-mode control strategy, it only takes 196ms to reach the steady state. Therefore, the new control strategy has a faster response speed and better dynamic performance during the startup phase.

Figs 25 and 26 show the output voltage steady-state waveform under the PI and ATSMC control strategies, respectively. According to the output voltage waveform analysis, the output voltage ripple under the PI control strategy is 800mV, which is larger than that under the ATSMC control strategy. Therefore, the output voltage accuracy of the ATSMC strategy was higher.

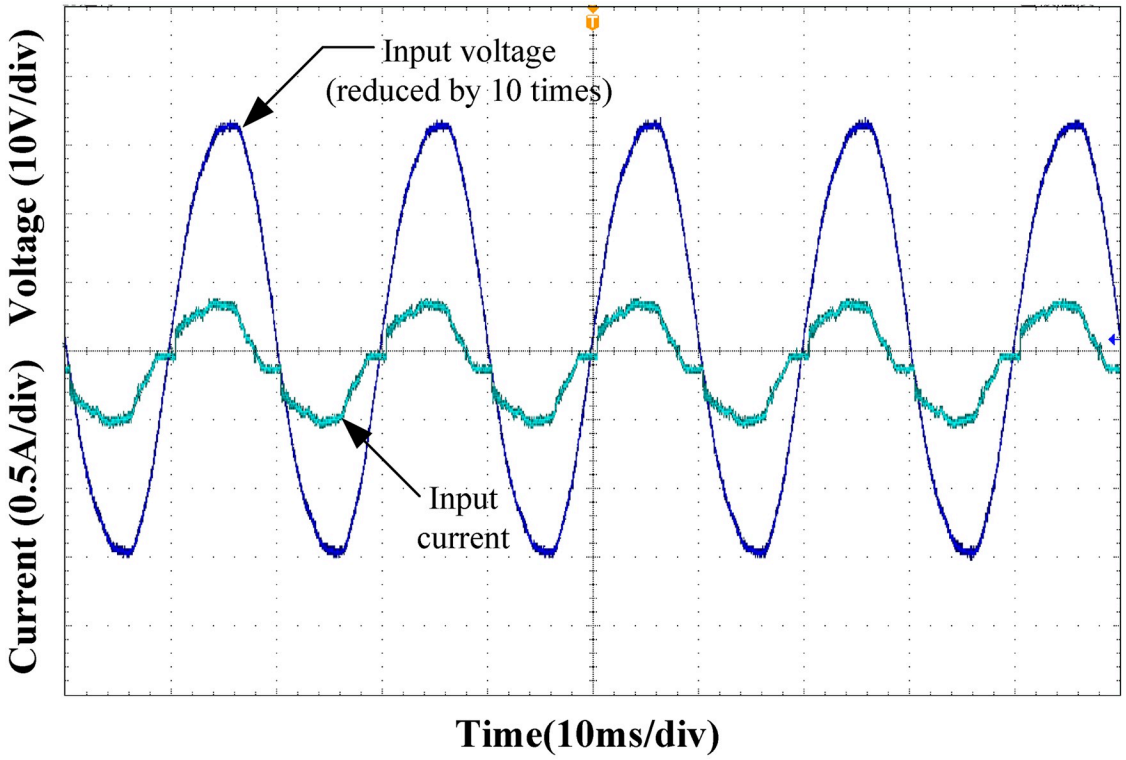

Fig 16. Input voltage and current at 50% load.

https://doi.org/10.1371/journal.pone.0275056.g016

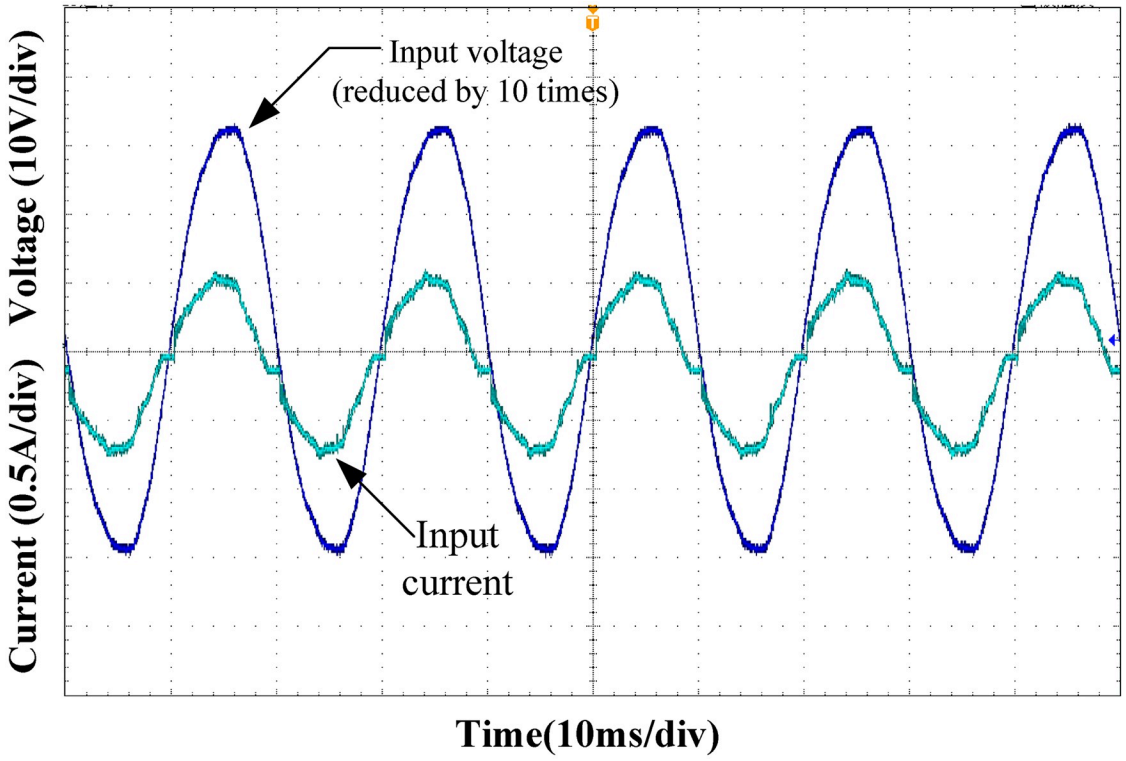

Fig 17. Input voltage and current at 75% load.

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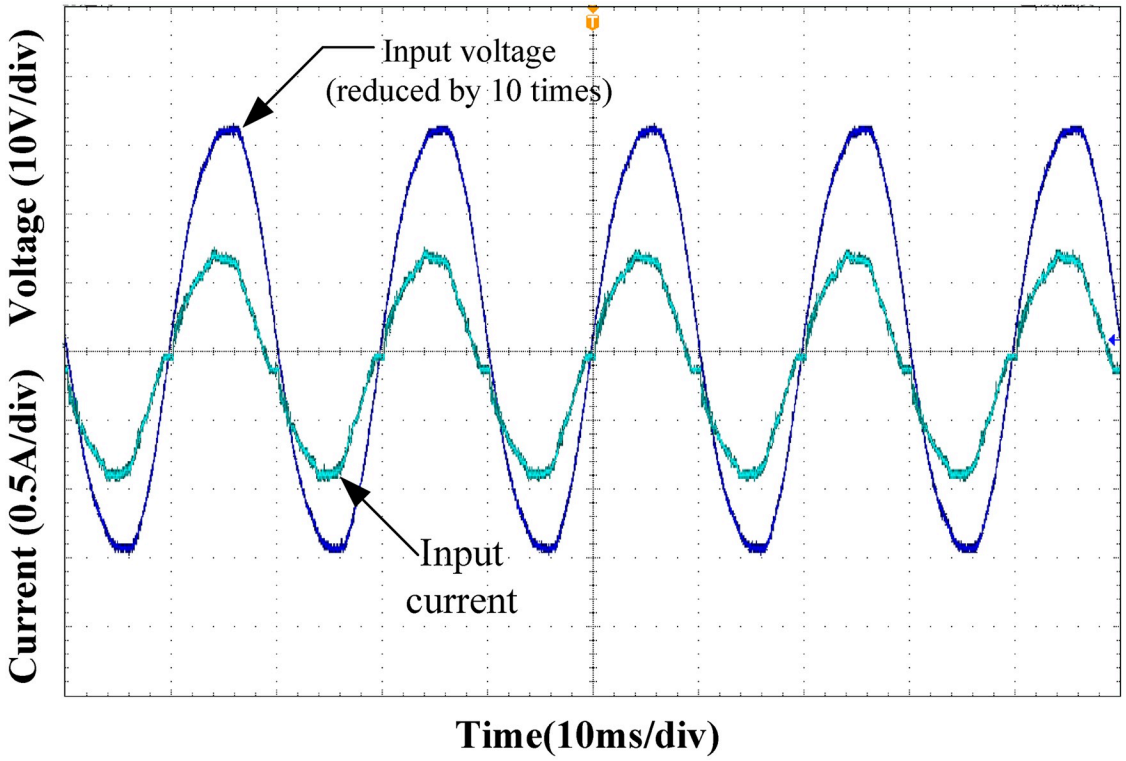

Fig 18. Input voltage and current at full load.

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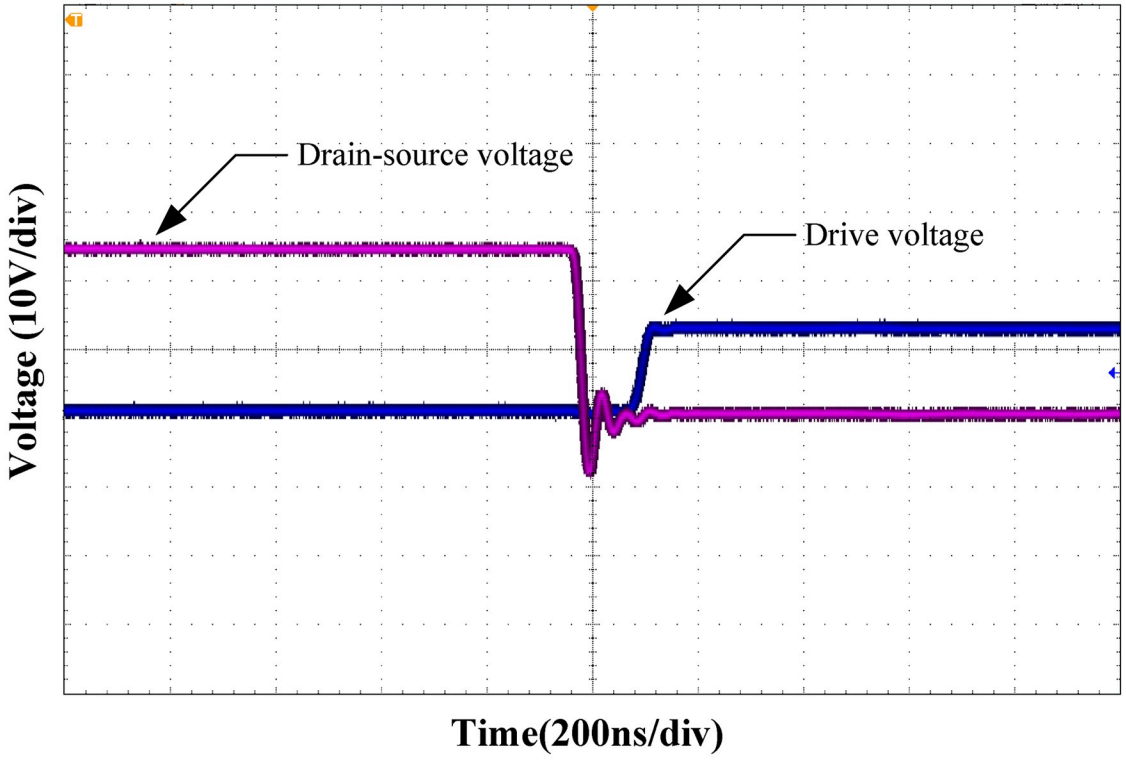

Fig 19. Zero-voltage turn-on waveform of the leading-leg.

https://doi.org/10.1371/journal.pone.0275056.g019

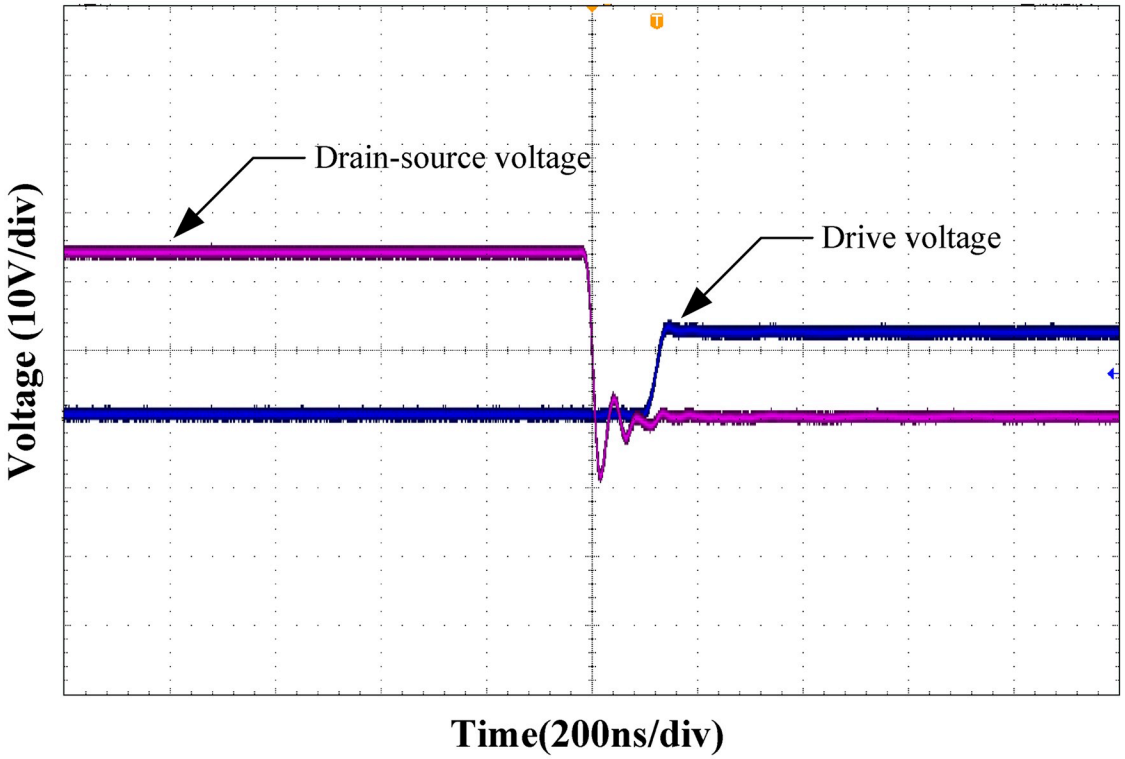

Fig 20. Zero-voltage turn-on waveform of the lagging-leg.

https://doi.org/10.1371/journal.pone.0275056.g020

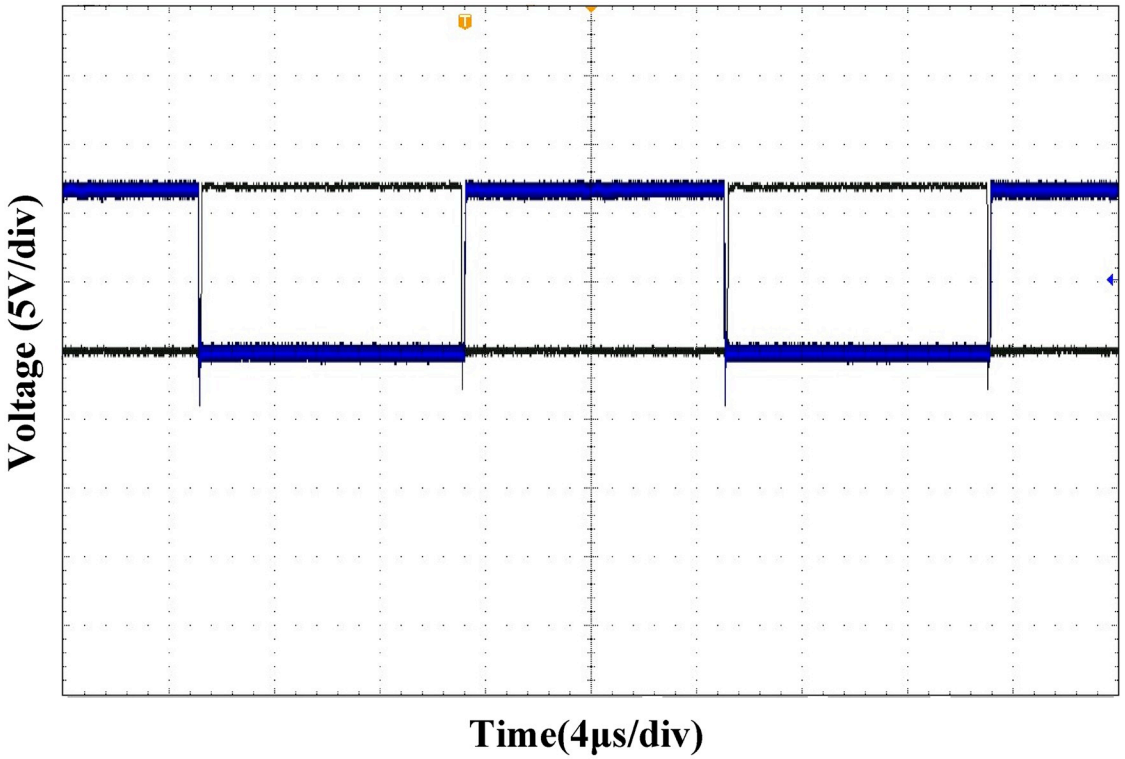

Fig 21. MOSFET driving waveform of the leading-leg.

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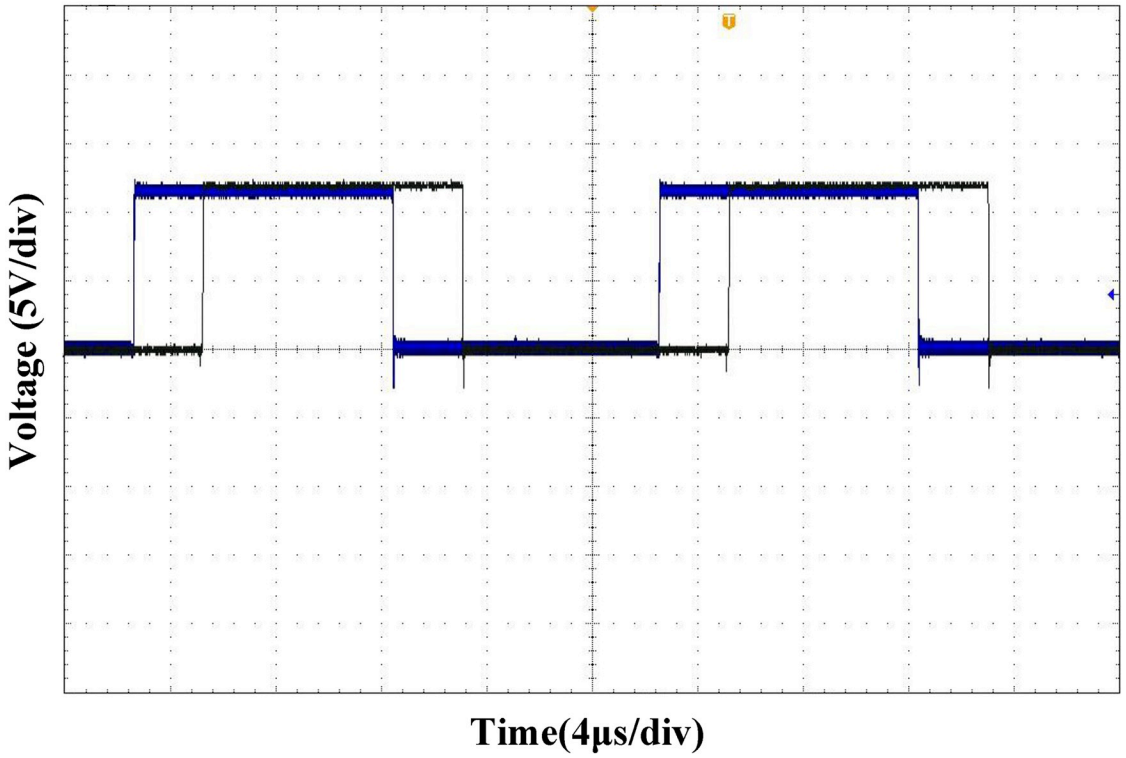

Fig 22. MOSFET driving waveforms of the leading-leg and lagging-leg.

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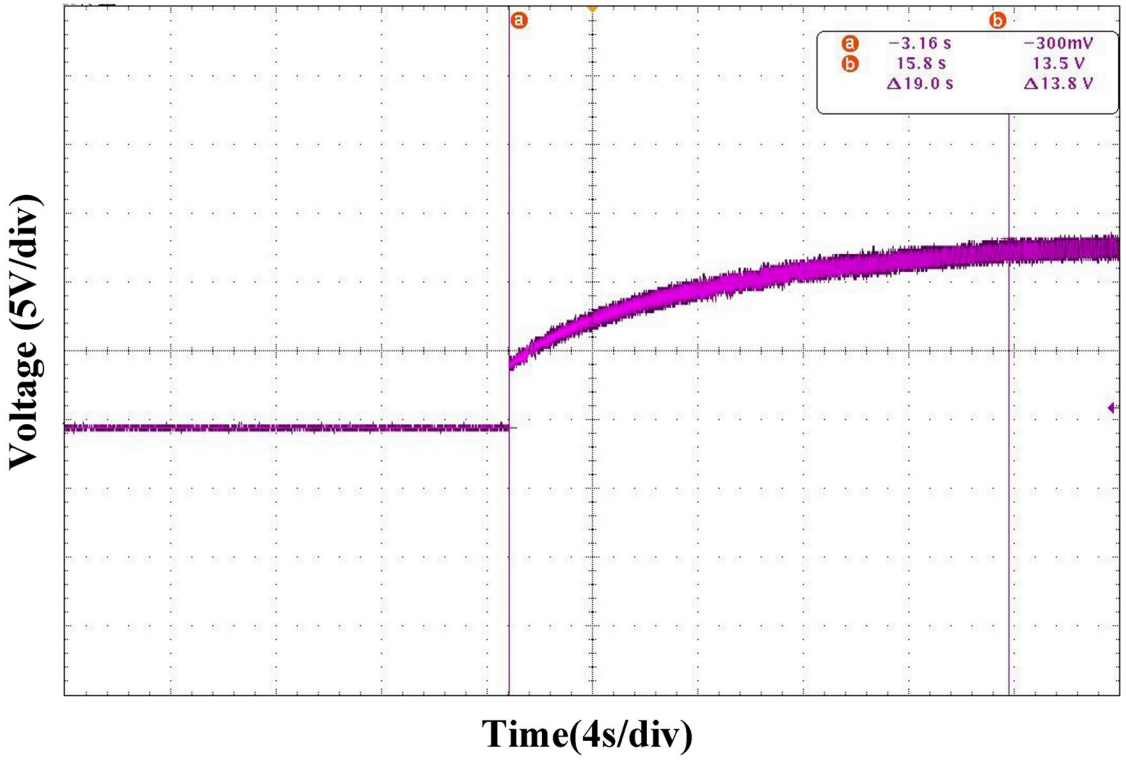

Fig 23. Startup waveform under PI control strategy.

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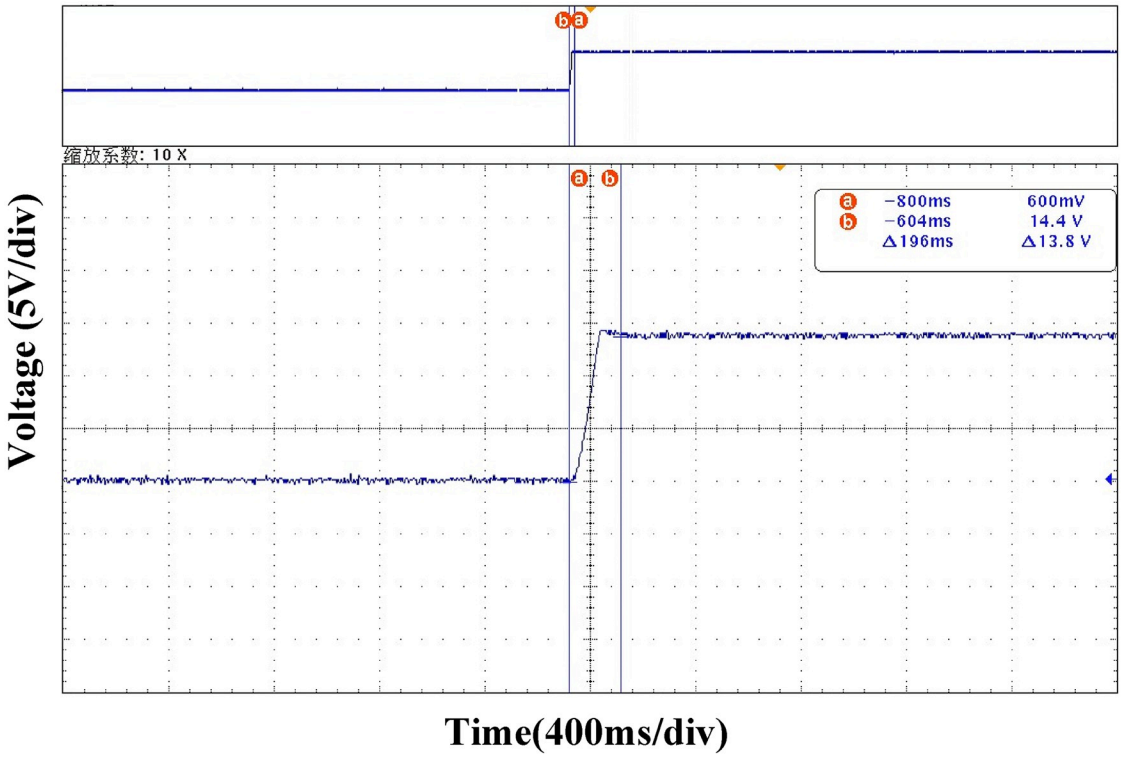

Fig 24. Startup waveform under ATSMC control strategy.

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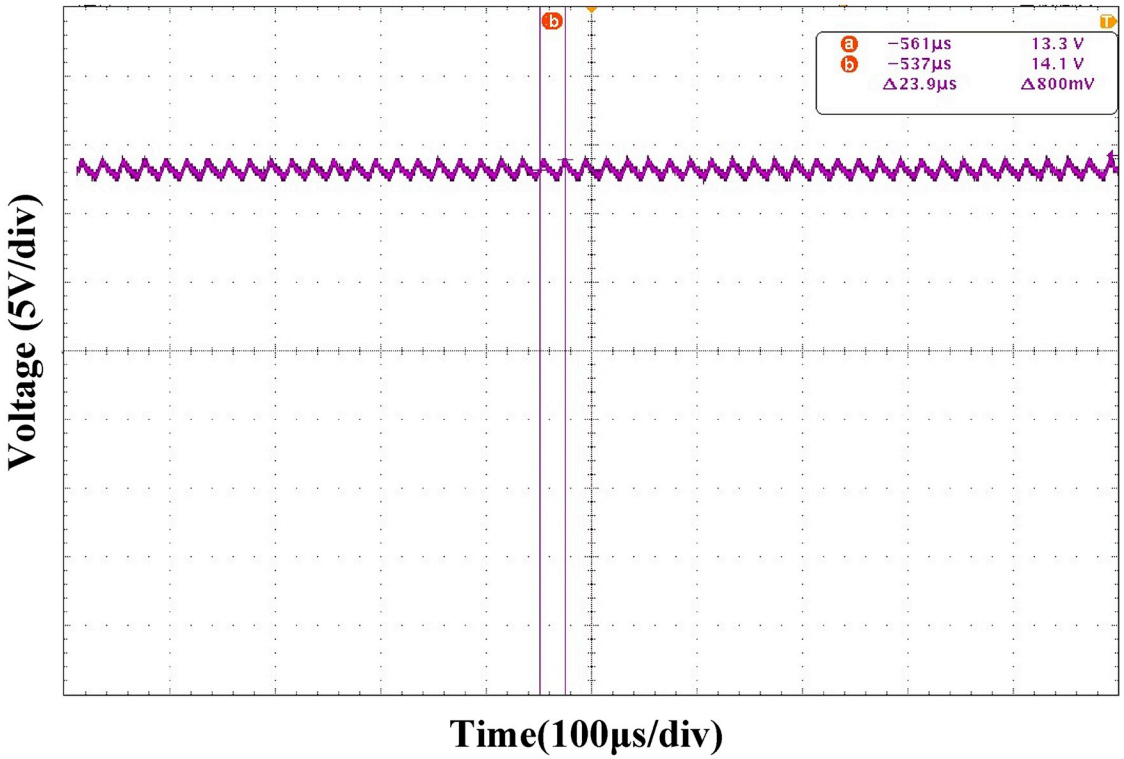

Fig 25. Output voltage waveform under PI control strategy.

https://doi.org/10.1371/journal.pone.0275056.g025

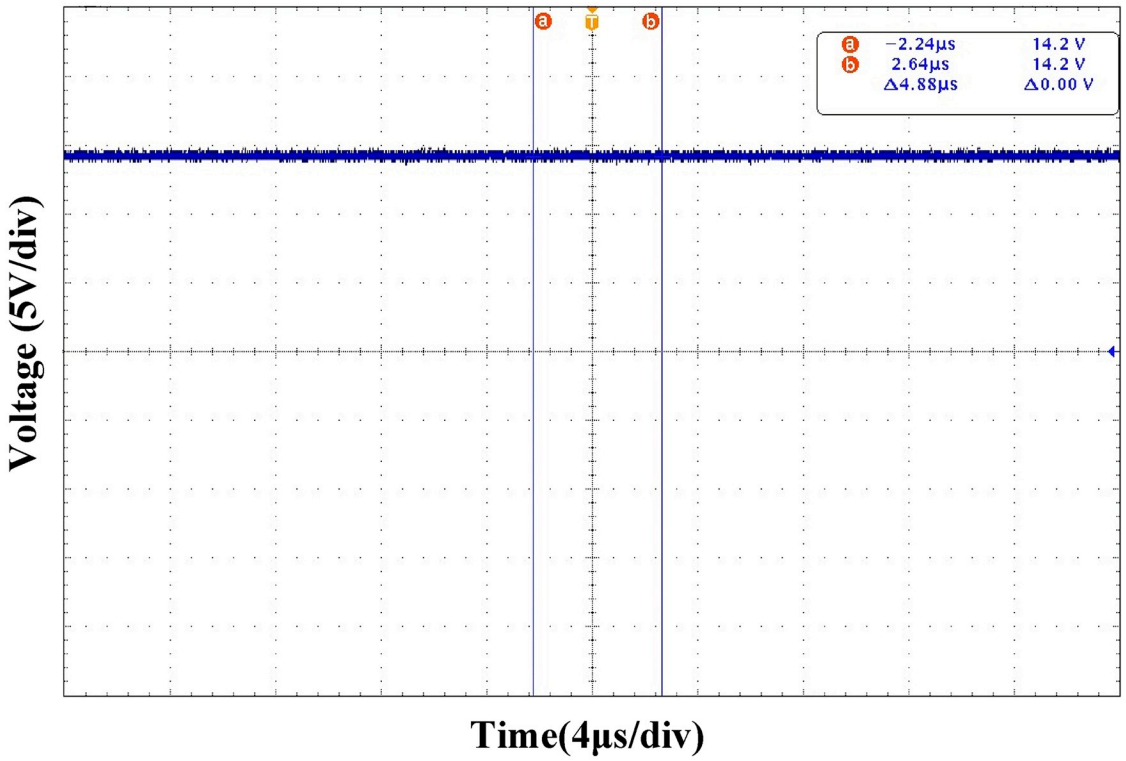

Fig 26. Output voltage waveform under ATSMC control strategy.

https://doi.org/10.1371/journal.pone.0275056.g026

Figs 27 and 28 show the output voltage waveform comparison between the PI and ATSMC control strategies when the load is switched. Compared with PI control, when the same degree of load change occurred, under the ATSMC control strategy, the system adjustment time was shorter, the instantaneous voltage change was smaller, and the system robustness was stronger.

(Fig 29) shows the efficiency curve of the front-stage Buck PFC circuit under different input voltages. (Fig 30) shows the efficiency curves of the rear-stage full-bridge converter under different loads. Multiplying the efficiencies of the front and rear stages under rated conditions shows that the combined efficiency of the two-stage converter is above 85%.

6 Conclusion

In this study, a two-stage AC/DC converter was designed. The front stage uses a Buck PFC circuit operating in discontinuous capacitor voltage mode, and the rear-stage uses a full-bridge converter. The parameters of the circuit components were obtained through theoretical analysis and calculations. The PI control strategy and parameter adaptive terminal sliding mode control strategy were adopted for the front-stage and rear-stage circuits, respectively. The control effect was verified through simulation, and finally, a physical circuit was built. Experiments show that the circuit realized a power-factor correction. The corrected system power factor exceeded 90% under full-load conditions, and 98% under rated conditions. The rear-stage full-bridge circuit realized zero-voltage conduction of MOSFETs. Compared with traditional PI control, the response speed of the circuit startup phase was faster, and the output voltage accuracy was higher. When the load changes, the system exhibits a faster adjustment speed, less voltage fluctuation, and stronger system robustness.

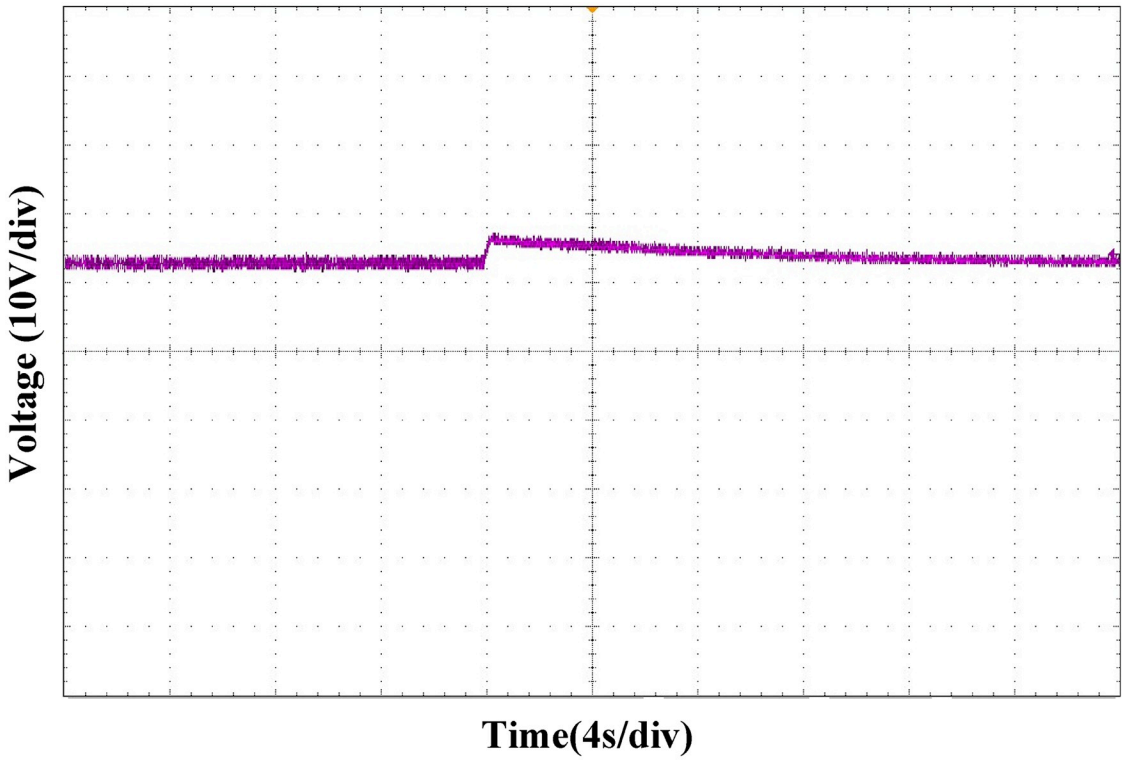

Fig 27. Load switching waveform under PI control strategy.

https://doi.org/10.1371/journal.pone.0275056.g027

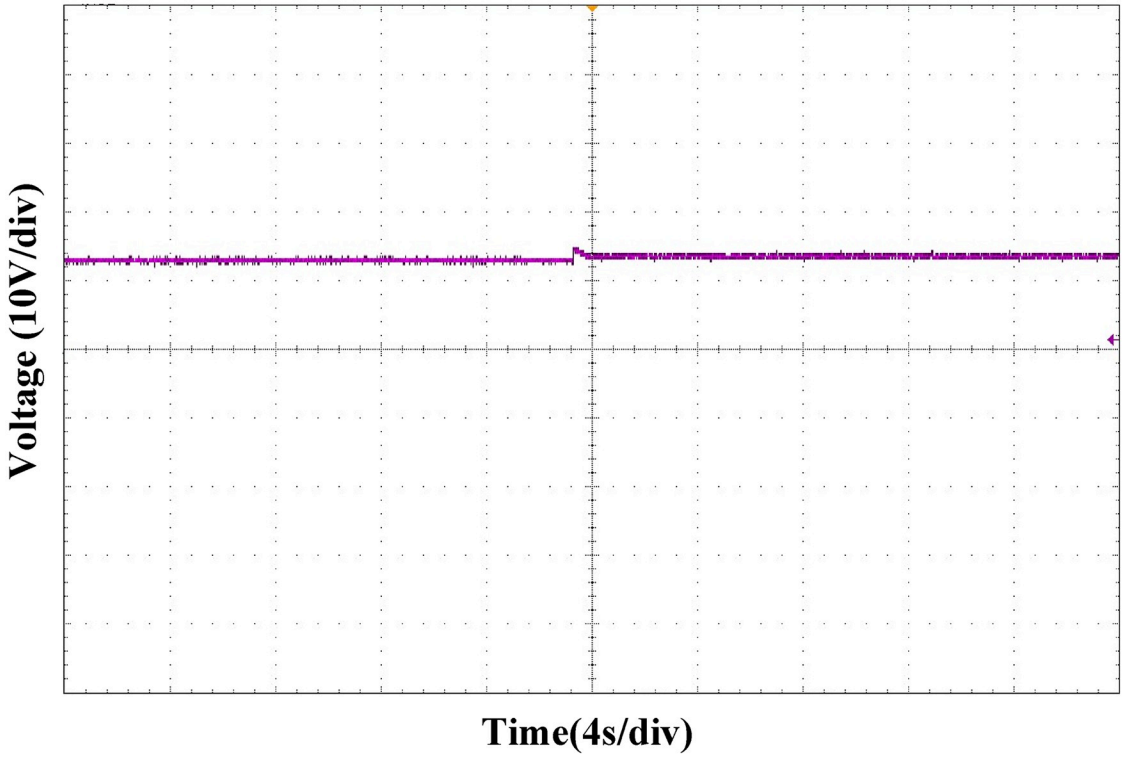

Fig 28. Load switching waveform under ATSMC control strategy.

https://doi.org/10.1371/journal.pone.0275056.g028

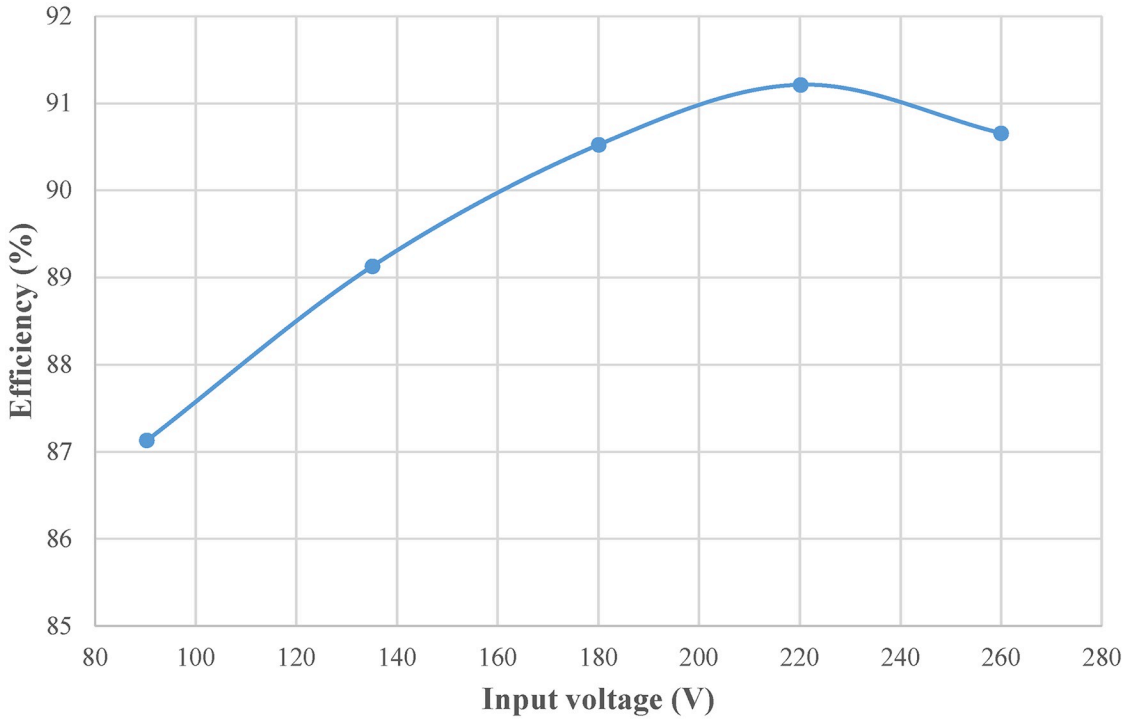

Fig 29. Efficiency curve of front-stage Buck PFC converter.

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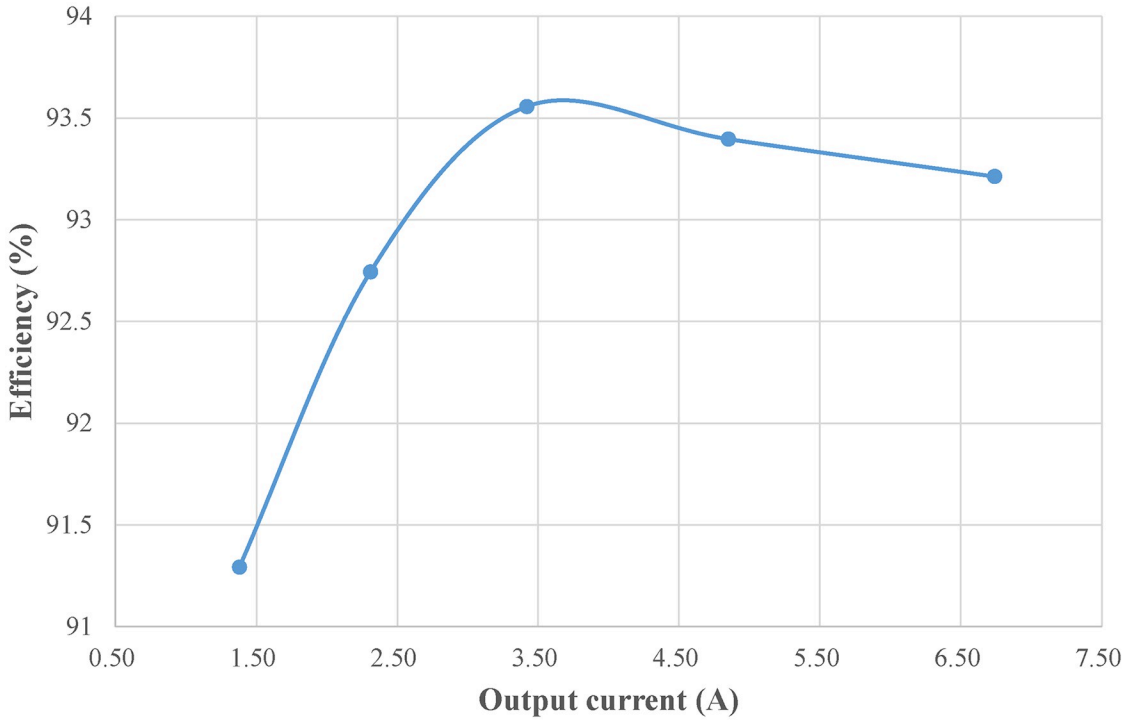

Fig 30. Efficiency curve of rear-stage full-bridge converter.

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Author Contributions

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Methodology: Kai Zhou, Da Teng, Chengxiang Yuan.

Software: Da Teng.

Supervision: Kai Zhou, Chengxiang Yuan.

Writing – review & editing: Da Teng.

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