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0.3-Volt Rail-to-Rail DDTA and Its Application in a Universal Filter and Quadrature Oscillator

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Abstract: This paper presents the extremely low-voltage supply of the CMOS structure of a differential difference transconductance amplifier (DDTA). With a 0.3-volt supply voltage, the circuit offers rail-to-rail operational capability. The circuit is designed for low-frequency biomedical and sensor applications, and it consumes 357.4 nW of power. Based on two DDTAs and two grounded capacitors, a voltage-mode universal filter and quadrature oscillator are presented as applications. The universal filter possesses high-input impedance and electronic tuning ability of the natural frequency in the range of tens up to hundreds of Hz. The total harmonic distortion (THD) for the band-pass filter was 0.5% for 100 mV_{pp} @ 84.47 Hz input voltage. The slight modification of the filter yields a quadrature oscillator. The condition and the frequency of oscillation are orthogonally controllable. The frequency of oscillation can also be controlled electronically. The THD for a 67 Hz oscillation frequency was around 1.2%. The circuit is designed and simulated in a Cadence environment using 130 nm CMOS technology from United Microelectronics Corporation (UMC). The simulation results confirm the performance of the designed circuits.

Keywords: universal filter; quadrature oscillator; differential difference transconductance amplifier; analog signal processing

Citation: Khateb, F.; Kumngern, M.; Kulej, T.; Biolek, D. 0.3-Volt Rail-to-Rail DDTA and Its Application in a Universal Filter and Quadrature Oscillator. *Sensors* **2022**, *22*, 2655. https://doi.org/10.3390/s22072655

Academic Editor: Haruo Kobayashi

Received: 24 February 2022
Accepted: 26 March 2022
Published: 30 March 2022

1. Introduction

In recent years, extremely low-voltage operation capability and low-power consumption became inevitable requirements in modern, battery-operated, portable electronics and self-powered systems. In modern nanoscale complementary metal–oxide–semiconductor (CMOS) technologies, scaling the power supply voltage sustains the reliability and performance improvement of digital circuits; however, it causes performance degradation in the analog part. This poses a continual challenge for analog circuit designers to maintain acceptable performance for applications and systems-on-chip. The main impact of reducing the voltage supply on analog circuit performance, such as an operational amplifier (Op-Amp) or transconductance amplifier (TA or OTA), is the reduced input voltage swing, the transconductance value, and the voltage gain. A conventional design technique used to increase the input voltage swing is rail-to-rail circuits composed of both PMOS and NMOS differential pairs. However, these circuits are complex due to the additional differential pair, current branches, and circuitry used to maintain constant transconductance over the whole input voltage range. Therefore, non-conventional techniques, such as bulk-driven

(BD) [1–14], floating-gate (FG), and quasi-floating-gate (QFG) [15,16], are suitable candidates for circuits operating with low supply voltages. They may reduce the threshold voltage or even remove it from the signal path, resulting in an extended input voltage range. Multiple-input MOS transistor (MI-MOST) is an alternative technique to the FG. However, unlike the FG, the MI-MOST: (a) does not need two polysilicon technologies; hence, it can be implemented in any standard CMOS technology; (b) it can process both AC and DC signals; and (c) there is no gate floating, and hence no issue associated with removing the initial charge trapped as in the case of FG. The multiple-input can be applied to the gate, to the bulk, or to their combination [17–27]. From the realization point of view, analog filter applications with MI-MOST may reduce the count of needed active devices [17–24,28,29]. This leads to simplified filter circuitry and reduced power consumption and chip area.

The universal filter and oscillator are important blocks for analog signal processing. Their applications include communication, control, and instrumentation systems [30–32]. Biquadratic filters and oscillators can be applied to biomedical systems [33–35]. Therefore, low-voltage supply and low-power consumption are mainly considered for these applications.

The differential difference transconductance amplifier (DDTA) is a useful analog block for filter applications [36–40]. It combines the features of a differential difference amplifier (DDA) with unity gain, like addition and subtraction voltage ability, high-input impedance, a low number of components, and the advantages of a operational transconductance amplifier (OTA), such as electronic tuning ability and simple circuitry. There are DDTA-based universal filters and oscillators available in the literature [36–40]. However, these DDTAs are not suitable for extremely low-voltage supply (i.e., $\leq$0.3 V) applications. Their structures are standard; hence, reducing their voltage supply leads to significant performance degradation, for instance a reduced input voltage swing. Focusing on recently published universal filters and/or oscillators [41–47], only the circuit in [48] can work with sub-volt supply ($\pm$0.3 V) and low-power consumption (5.77 μW).

Therefore, this paper presents an innovative CMOS structure for DDTA capable of working under a 0.3 V supply voltage with a rail-to-rail input voltage swing without degrading the other circuit's performance. As an application of DDTA, a multiple-input, multiple-output (MIMO) universal filter is presented. The filter employs two DDTAs and two grounded capacitors. A variety of filter responses can be obtained by suitably applying the input signal and suitably choosing the output terminal. The natural frequency of filter responses can be electronically controlled. The proposed universal filter has also been modified to work as a quadrature oscillator. The frequency of oscillation can be controlled electronically. The proposed universal filter and quadrature oscillator can be applied to biomedical and sensor systems due to their extremely low voltage supply and low power consumption.

This paper is organized as follows: In Section 2, the DDTA and its innovative CMOS structure are presented; Section 3 presents its application in the voltage-mode universal filter and the quadrature oscillator; Section 4 presents the simulation results; and Section 5 concludes the paper.

2. DDTA and Its CMOS Structure

The symbol of the DDTA is shown in Figure 1. In the ideal case, this active component is described by the following equations:

$$\left.\begin{array}{c} V_w = V_{y1} - V_{y2} + V_{y3} \\ I_o = g_m\left(V_w - V_{y4}\right) \end{array}\right\} \quad (1)$$

The CMOS structure of the proposed DDTA is shown in Figure 2. The circuit consists of two main blocks, namely, the differential-difference amplifier operating in a unity feedback configuration, thus forming a differential-difference current conveyor (DDCC), and the transconductance amplifier (TA). Both circuits are based on non-tailed differential amplifiers [1], which allow for operation in an ultra-low-voltage environment with rail-to-rail input swing.

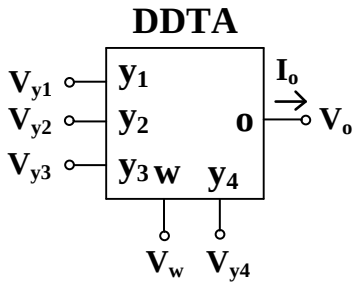


Figure 1. Symbol of DDTA.

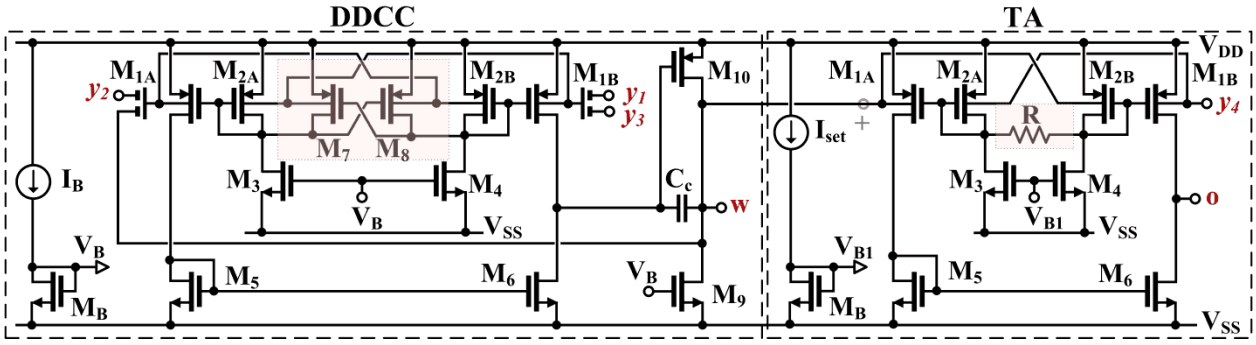


Figure 2. Proposed CMOS structure of DDTA.

The DDCC block consists of two stages, the input differential amplifier, M_1–M_6, and the class-A output stage, M_9–M_{10}. The capacitance C_C is used for frequency compensation. Its value can be calculated in the same way as that for a two-stage operational amplifier. The input stage of the DDCC circuit can be seen as a non-tailed differential pair with an additional partial positive feedback (PPF) circuit. The solution, first presented in [2] and experimentally validated in [3], has been adopted here. The transistors, M_7 and M_8, generate negative conductances, $-g_{m7}$ and $-g_{m8}$, which partially compensate for the positive conductances of the diode-connected transistors, $M_{2A,B}$ ($\approx g_{m2}$), thus increasing the resistances at the gate-drain nodes of these transistors, and consequently the voltage gain from inputs to the gate terminals of $M_{1A,B}$. This improves the overall transconductance and voltage gain of the first stage.

In the proposed realization, the input transistors $M_{1A,B}$ have been replaced by bulk-driven MI-MOST transistors. The symbol and CMOS realization of these devices are shown in Figure 3. This approach allows design simplification and the decreasing of the total dissipation power by removing one differential stage of the conventional DDCC. This is the result of the fact that summation of input signals is realized using the passive voltage divider/summing circuit composed of the capacitances C_{Bi} (see Figure 3b). The capacitances are shunted by large resistances, R_{MOSi}, that allow proper DC biasing of the bulk terminals of $M_{1A,B}$. The resistors are realized as the antiparallel connection of two MOS transistors operating in a cutoff region, as shown in Figure 3c.

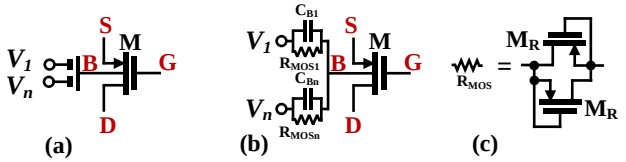


Figure 3. Bulk-driven MI-MOST: (**a**) symbol, (**b**) its realization, and (**c**) realization of RMOS.

The low-frequency open-loop voltage gain of the DDCC, from one differential input, with the second input grounded for AC signals, can be expressed as follows:

$$A_{vo} = G_m(r_{ds1}||r_{ds6})g_{m10}(r_{ds9}||r_{ds10}) \quad (2)$$

where G_m is the transconductance of the input differential stage given by:

$$G_m \cong \beta \frac{2g_{mb1}}{(1-m)} \tag{3}$$

where β is the voltage gain of the input capacitive divider, equal to $\frac{1}{2}$ if all capacitances C_{Bi} are equal to each other and the input capacitance of the MOS transistor from its bulk terminal can be neglected. The factor m represents the absolute value of the ratio of negative to positive conductances at the gate/drain nodes of $M_{2A,B}$:

$$m = \frac{g_{m7,8}}{g_{m2} + g_{ds2} + g_{ds3} + g_{ds7,8}} \cong \frac{g_{m7,8}}{g_{m2}} \tag{4}$$

Note that the transconductance G_m as well as the voltage gain A_{vo} tend to infinity, as m tends to unity, namely, when the negative conductances generated by M_7 and M_8 fully compensate the positive conductances of M_2, thus leading to infinite voltage gain from inputs to the drain/gate nodes of $M_{2A,B}$. However, when the difference between g_{m2} and $g_{m7,8}$ is decreasing, namely when m is increasing to unity, then the circuit sensitivity to transistor mismatch is increasing as well, which limits the maximum value of m. The second limitation is associated with the location of the parasitic pole associated with the PPF circuit, which is given by the formula

$$\omega_p \cong \frac{g_{m2}(1-m)}{C_\Sigma} \tag{5}$$

where $C_\sum$ is the total capacitance associated with the gate/drain nodes of $M_{2A,B}$. Note that the frequency of this pole decreases with increasing m, namely, as the total resistance at the gate/drain nodes of M_2 increases with increasing positive feedback. For stable operation, the pole should be located well above the GBW product of the internal DDA, which is

$$\omega_{GBW} = \frac{G_m}{C_C} \tag{6}$$

In view of the above considerations, the output signal at the W terminal for low frequencies can be expressed as

$$V_w = \frac{A_{vo}}{1 + A_{vo}}(V_{y1} - V_{y2} + V_{y3}) \tag{7}$$

Note that accuracy of this function is improved thanks to the impact of the PPF, which enlarges the low-frequency voltage gain A_{vo}. The 3 dB frequency of this function is approximately equal to ω_{GBW}. The low-frequency output resistance at the W terminal is given as follows:

$$r_{outW} = \frac{r_{ds9} || r_{ds10}}{1 + A_{vo}} \tag{8}$$

Thus, the resistance r_{outW} is also improved (decreased) thanks to the larger value of A_{vo}.

The second block of the proposed DDTA is the linear transconductance amplifier, TA. The circuit applied here was first proposed and validated experimentally in [4]. It can be considered as a non-tailed BD pair [1], linearized with an additional linear resistance R, which significantly improves the linearity of the circuit. Thanks to its non-tailed architecture, the circuit can operate from a very low-voltage supply.

Assuming that transistor M_B is identical with M_3 and M_4, the DC transfer characteristic of the TA in Figure 2 can be described by the formula [4]

$$I_O = 2I_{set}[\sinh(x) - (\mathrm{Ax})\cosh(x)] \tag{9}$$

where

$$A = \frac{n_p U_T}{I_{set}\left(R + \frac{2}{g_{m1,2}}\right)} \tag{10}$$

$$x = \frac{\eta\left(V_w - V_{y4}\right)}{n_p U_T} \tag{11}$$

and n_p is the subthreshold slope factor for a p-channel MOS, U_T is the thermal potential, and $\eta = (n_p - 1) = g_{mb1,2}/g_{m1,2}$ is the bulk-to-gate transconductance ratio for transistors M_1 and M_2.

As it was shown in [4], if the following condition holds

$$R = \frac{1}{g_{m1,2}} \tag{12}$$

then the circuit exhibits an optimum linearity. However, even for the non-optimal case, the linearity of Equation (9) is much better than for the original circuit without the resistance, R; therefore, the TA can be tuned using the current source I_{set}, while still maintaining good linearity of its transfer characteristic.

The small-signal transconductance g_m of the TA in the general case is

$$g_m \cong 2g_{mb1,2}\left[\frac{R + \frac{1}{g_{m1,2}}}{R + \frac{2}{g_{m1,2}}}\right] \tag{13}$$

thus, in the optimum case, ($R = 1/g_{m1,2}$), it is equal to $4g_{mb1,2}/3$.

3. Proposed Applications

3.1. Proposed Universal Filter

Figure 4 shows the proposed voltage-mode MIMO universal filter. The topology employs two DDTAs and two grounded capacitors. The terminals V_{in1}, V_{in2}, V_{in3}, V_{in4}, and V_{in5} provide high-input impedances, and the terminals V_{o1} and V_{o3} low-output impedances, whereas the terminals V_{o2} and V_{o4} require external buffer circuits if a low-impedance load is applied.

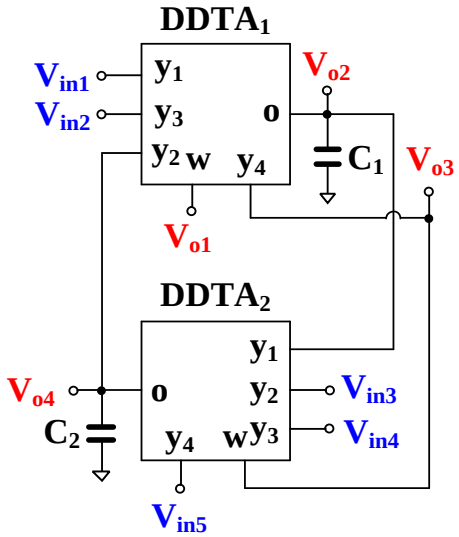


Figure 4. MIMO universal filter using DDTAs.

Using (1) and nodal analysis, the output voltages of Figure 4 can be expressed as follows:

$$V_{o1} = \frac{\left(s^2C_1C_2 + sC_2g_{m1}\right)(V_{in1} + V_{in2}) + sC_1g_{m2}(V_{in3} - V_{in4}) + (sC_1g_{m2} + g_{m1}g_{m2})V_{in5}}{s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}} \quad (14)$$

$$V_{o2} = \frac{sC_2g_{m1}(V_{in1} + V_{in2}) + (sC_2g_{m1} + g_{m1}g_{m2})(V_{in3} - V_{in4}) - g_{m1}g_{m2}V_{in5}}{s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}} \quad (15)$$

$$V_{o3} = \frac{sC_2g_{m1}(V_{in1} + V_{in2}) + s^2C_1C_2(V_{in4} - V_{in3}) + g_{m1}g_{m2}V_{in5}}{s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}} \quad (16)$$

$$V_{o4} = \frac{g_{m1}g_{m2}(V_{in1} + V_{in2}) + sC_1g_{m2}(V_{in4} - V_{in3}) - (sC_1g_{m2} + g_{m1}g_{m2})V_{in5}}{s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}} \quad (17)$$

From (14)–(17), the low-pass (LP), band-pass (BP), high-pass (HP), band-stop (BS), and all-pass (AP) responses can be obtained by properly applying the input signal and choosing the output terminals as shown in Table 1. The input terminals that are not used should be connected to ground. In the case of the all-pass filtering response, the circuit requires an inverting-type input signal, which can be obtained using additional DDTA.

The natural frequency (ω_o) and the quality factor (Q) of the filter can be respectively expressed as

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (18)$$

$$Q = \sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}} \quad (19)$$

From (18) and (19), the natural frequency and the quality factor can be designed, as the quality factor can be given by C_1/C_2 by letting $g_{m1} = g_{m2}$ whereas the natural frequency can be obtained electronically by adjusting g_m ($g_m = g_{m1} = g_{m2}$).

Table 1. Obtaining variant filtering functions of the proposed filter.

Filtering Function		Input	Output
LP	Non-inverting	$V_{in4} = V_{in5}$	V_{o1}
	Non-inverting	V_{in5}	V_{o2}
	Inverting	$V_{in1} = V_{in4}$	V_{o2}
	Non-inverting	V_{in5}	V_{o3}
	Non-inverting	V_{in1}	V_{o4}
	Non-inverting	V_{in2}	V_{o4}
	Inverting	$V_{in4} = V_{in5}$	V_{o4}
BP	Non-inverting	V_{in3}	V_{o1}
	Inverting	V_{in4}	V_{o1}
	Non-inverting	V_{in1}	V_{o2}
	Non-inverting	V_{in2}	V_{o2}
	Inverting	$V_{in4} = V_{in5}$	V_{o2}
	Non-inverting	V_{in1}	V_{o3}
	Non-inverting	V_{in2}	V_{o3}
	Non-inverting	V_{in4}	V_{o4}
	Inverting	V_{in3}	V_{o4}
	Inverting	$V_{in1} = V_{in5}$	V_{o4}
HP	Non-inverting	$V_{in1} = V_{in4}$	V_{o1}
	Inverting	V_{in3}	V_{o3}
	Non-inverting	V_{in4}	V_{o3}
BS	Non-inverting	$V_{in4} = V_{in5}$	V_{o3}
AP	Non-inverting	$-V_{in2} = V_{in4} = V_{in5}$	V_{o3}

3.2. Proposed Quadrature Oscillator

The proposed universal filter in Figure 4 was modified to work as a quadrature oscillator as shown in Figure 5. It can be obtained by using a non-inverting BP filtering response and a feedback connection. Using (14), the transfer function between V_{o1} and V_{in3} can be expressed as follows:

$$\frac{V_{o1}}{V_{in3}} = \frac{sC_1g_{m2}}{s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}} \tag{20}$$

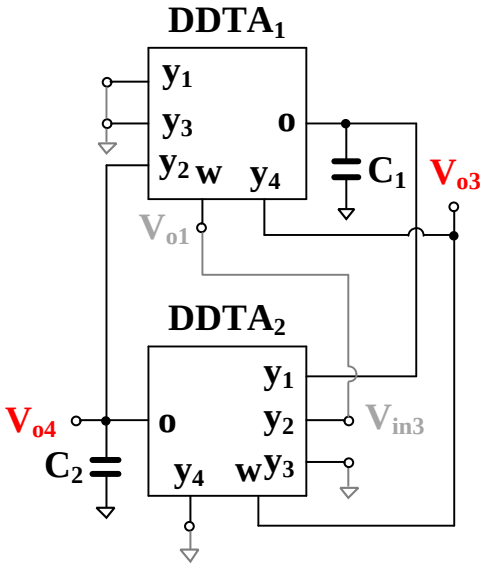


Figure 5. The quadrature oscillator.

Letting $V_{o1}/V_{in3} = 1$, the oscillator characteristic can be derived as

$$s^2C_1C_2 + s(C_2g_{m1} - C_1g_{m2}) + g_{m1}g_{m2} = 0 \tag{21}$$

Letting $g_{m1} = g_{m2} = g_m$, the condition of oscillation (CO) is

$$C_1 = C_2 \tag{22}$$

and the frequency of oscillation (FO) is

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{23}$$

Thus, the CO of the oscillator can be controlled by C_1 and/or C_2, and letting $g_{m1} = g_{m2}$, the FO can be controlled electronically by g_m ($g_m = g_{m1} = g_{m2}$). Therefore, the FO and CO of the oscillator can be orthogonally controlled. The nodes V_{o3} and V_{o4} provide quadrature output signals. It can be confirmed by the relationship between V_{o3} and V_{o4}:

$$\frac{V_{o4}}{V_{o3}} = \frac{g_{m2}}{sC_2} \tag{24}$$

Thus, the phase difference between V_{o3} and V_{o4} is 90°. After setting $s = j\omega_0$ into (24) and taking into account Equations (22) and (23) and the condition $g_{m1} = g_{m2}$, the ratio (24) is one; thus, if oscillation condition (22) is accomplished, the oscillator provides equal amplitudes of both quadrature signals independently of the oscillation frequency.

3.3. Non-Idealities Analysis

Considering non-idealities of the DDTA, (1) can be rewritten as:

$$\left.\begin{array}{c} V_w = \beta_{i1}V_{y1} - \beta_{i2}V_{y2} + \beta_{i3}V_{y3} \\ I_o = g_{mni}(V_w - V_{y4}) \end{array}\right\} \tag{25}$$

where β_{i1} denotes the voltage gain from V_{y1} to V_w of i-th DDTA, β_{i2} denotes the voltage gain from V_{y2} to V_w of i-th DDTA, and β_{i3} denotes the voltage gain from V_{y2} to V_w of i-th DDTA. Ideally, the voltage gains β_{i1}, β_{i2}, and β_{i3} are unity. The g_{mni} is the non-ideal transconductance gain of the DDTA, whose frequency dependence is given by parasitic capacitance C_o and resistance R_o at o-terminal. In the frequency range near the cutoff frequency, g_{mni} can be approximated as [48]

$$g_{mni}(s) \cong g_{mi}(1 - \mu_i s) \tag{26}$$

where $\mu_i = 1/\omega_{gmi}$, ω_{gi} denotes the first-order pole.

Using (25), the output voltages of Figure 4 can be rewritten to the form

$$V_{o1} = \frac{\begin{array}{c}(s^2C_1C_2 + sC_2g_{mn1}\beta_{21})(\beta_{11}V_{in1} + \beta_{13}V_{in2}) + sC_1g_{mn2}\beta_{12}(\beta_{22}V_{in3} - \beta_{23}V_{in4}) \\ +(sC_1g_{mn2}\beta_{12} + g_{mn1}g_{mn2}\beta_{12}\beta_{21})V_{in5}\end{array}}{s^2C_1C_2 + sC_2g_{mn1}\beta_{21} + g_{mn1}g_{mn2}\beta_{12}\beta_{21}} \tag{27}$$

$$V_{o2} = \frac{\begin{array}{c}sC_2g_{mn1}(\beta_{11}V_{in1} + \beta_{13}V_{in2}) + (sC_2g_{mn1} + g_{mn1}g_{mn2}\beta_{12})(\beta_{22}V_{in3} - \beta_{23}V_{in4}) \\ -g_{mn1}g_{mn2}V_{in5}\end{array}}{s^2C_1C_2 + sC_2g_{mn1}\beta_{21} + g_{mn1}g_{mn2}\beta_{12}\beta_{21}} \tag{28}$$

$$V_{o3} = \frac{sC_2g_{mn1}\beta_{21}(\beta_{11}V_{in1} + \beta_{13}V_{in2}) + s^2C_1C_2(\beta_{23}V_{in4} - \beta_{22}V_{in3}) + g_{mn1}g_{mn2}\beta_{12}\beta_{21}V_{in5}}{s^2C_1C_2 + sC_2g_{mn1}\beta_{21} + g_{mn1}g_{mn2}\beta_{12}\beta_{21}} \tag{29}$$

$$V_{o4} = \frac{\begin{array}{c}g_{mn1}g_{mn2}\beta_{21}(\beta_{11}V_{in1} + \beta_{13}V_{in2}) + sC_1g_{mn2}(\beta_{23}V_{in4} - \beta_{22}V_{in3}) \\ -(sC_1g_{mn2} + g_{mn1}g_{mn2}\beta_{21})V_{in5}\end{array}}{s^2C_1C_2 + sC_2g_{mn1}\beta_{21} + g_{mn1}g_{mn2}\beta_{12}\beta_{21}} \tag{30}$$

Considering the denominator D(s) of (27)–(30), the modified parameters ω_o and Q can be expressed by:

$$\omega_o = \sqrt{\frac{g_{mn1}g_{mn2}\beta_{12}\beta_{21}}{C_1C_2}} \tag{31}$$

$$Q = \sqrt{\frac{g_{mn2}C_1\beta_{12}}{g_{mn1}C_2\beta_{21}}} \tag{32}$$

From (27), the modified oscillator characteristic can be expressed as

$$s^2C_1C_2 + (sC_2g_{mn1}\beta_{21} - sC_1g_{mn2}\beta_{12}\beta_{22}) + g_{mn1}g_{mn2}\beta_{12}\beta_{21} = 0 \tag{33}$$

The modified CO and FO of the oscillator are then

$$C_1\beta_{12}\beta_{22} = C_2\beta_{21} \tag{34}$$

$$\omega_o = \sqrt{\frac{g_{mn1}g_{mn2}\beta_{12}\beta_{21}}{C_1C_2}} \tag{35}$$

Since this work is focused on circuits that operate at low frequency, Equation (26) is not taken in consideration. In the case that the universal filter and the quadrature oscillator operate in the frequency range in which the frequency dependence of g_m asserts its influence, then (26) should be used to refine the error analysis.

4. Simulation Results

The DDTA circuit and its applications were designed in a Cadence environment, using 130 nm CMOS technology from UMC. The transistor's aspect ratio and values of passive devices are included in Table 2. The voltage supply is 0.3 V ($V_{DD} = -V_{SS} = 0.15$ V), the bias current of the DDCC $I_B = 50$ nA, and the nominal value of the setting current of the TA $I_{set} = 500$ nA. The nominal power consumption of the DDTA is 357.4 nW (DDCC = 70.21 nW, TA = 287.2 nW). The input and compensation capacitors are highly linear metal–isolator–metal capacitors (MIM). The linear resistor R is a high-resistance poly-resistor.

Table 2. Transistor aspect ratios of the DDTA.

Device	W/L (μm/μm)
M_{1A}, M_{2A}, M_{1B}, M_{2B}	20/3
M_7, M_8	15/3
M_3–M_6, M_B	10/3
M_9	6 × 10/3
M_{10}	6 × 20/3
M_R	5/3
MIM capacitor: C_B = 0.2 pF, Cc = 4 pF	
Poly-resistor R = 90 kΩ	

The open-loop gain of the DDCC (i.e., without the unity gain feedback) was simulated as 73.9 dB, and the phase margin was 56.2° for 20 pF load capacitor. The simulated magnitude characteristics of the DDCC are shown in Figure 6. The low-frequency gain for V_W/V_{Y1} (=V_W/V_{Y3}) and V_W/V_{Y2} is 14 mdB and 57.29 mdB, while the −3 dB bandwidth is 22.24 kHz and 22.23 kHz, respectively.

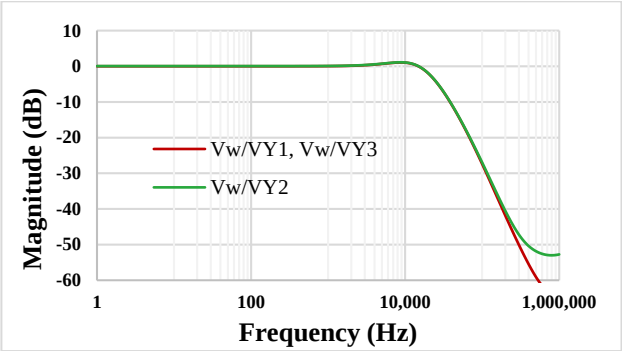


Figure 6. The magnitude characteristics of the DDCC.

The simulated DC transfer characteristics of the DDCC are shown in Figure 7. As is evident, the DDCC enjoys rail-to-rail operation for all its inverting and non-inverting inputs. This rail-to-rail operation capability is a design achievement.

The simulated gain and phase characteristics for the TA with I_{set} = 0.5 μA and 20 pF load capacitance are shown in Figure 8. The low DC gain is 23.2 dB, and the bandwidth (BW) is 19.65 kHz, while the phase error is 3.8°.

Figure 9a,b shows the DC characteristic of the output current and the transconductance versus fully differential input voltage V_{in} ($V_{in} = V_+ - V_{y4}$) for the TA for I_{set} = 0.125 μA, 0.25 μA, and 0.5 μA. The rail-to-rail operation with high linearity is evident.

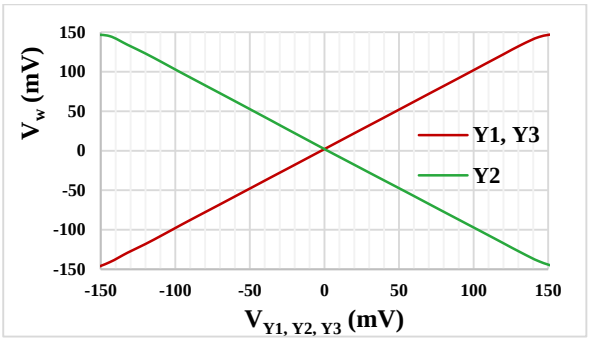


Figure 7. The DC transfer characteristics of the DDCC.

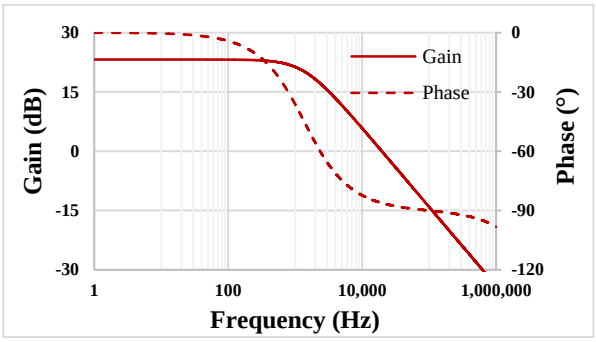
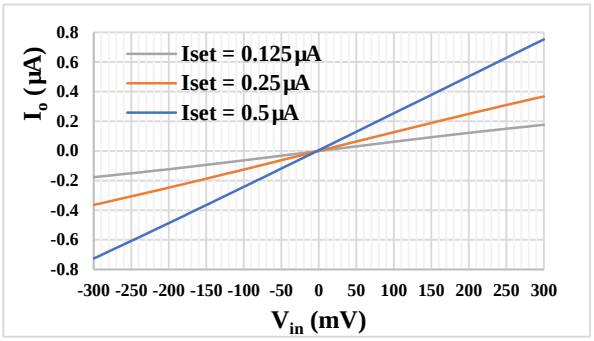
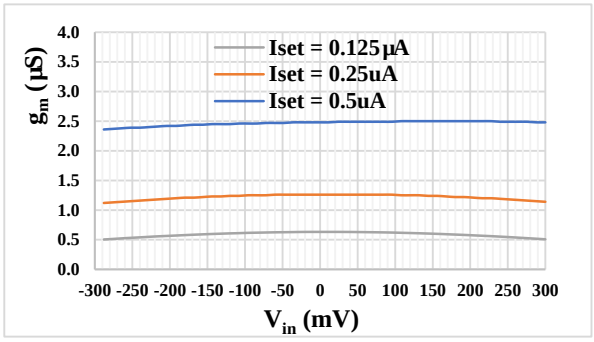


Figure 8. The gain and phase characteristics of the TA.



(**a**)



(**b**)

Figure 9. The DC output current (**a**) and transconductance g_m (**b**) characteristics of the TA versus input voltage.

To determine the impact of mismatch and process variation on the circuit's performance, Monte Carlo (MC) simulations (200 runs) were carried out. As the histograms show in Figure 10, the impact of mismatch and process variation on the gain and −3 dB BW of the DDCC is low. The impact is also low on the gain and phase error of the TA as shown in Figure 11.

The process, voltage, temperature (PVT) corners analysis was also provided on the proposed DDTA. The MOS transistor corners were slow-slow, slow-fast, fast-slow, and fast-fast, the voltage supply corners were ($V_{DD} - V_{SS}$) ± 10%, and the temperature corners were −20 °C and 70 °C. Tables 3 and 4 show the results of the minimum, nominal, and maximum values of the gain, −3 dB BW for the DDCC, and gain and phase error for the TA. The impact of the PVT corners in all cases is acceptable.

Table 3. The PVT corner analysis results for the DDCC.

DDCC	min.	nom.	max.
	P/V/T		P/V/T
Gain V_W/V_{Y1} [mdB]	−75.3/9.8/−224	14	29.4/14/14
Gain V_W/V_{Y2} [mdB]	−14.1/45.8/−75	57	101/67.3/57
−3 dB V_W/V_{Y1} [kHz]	20.2/22/21	22.24	25.2/22.1/23.7
−3 dB V_W/V_{Y2} [kHz]	20.1/22/20.8	22.23	25/22.7/23.4

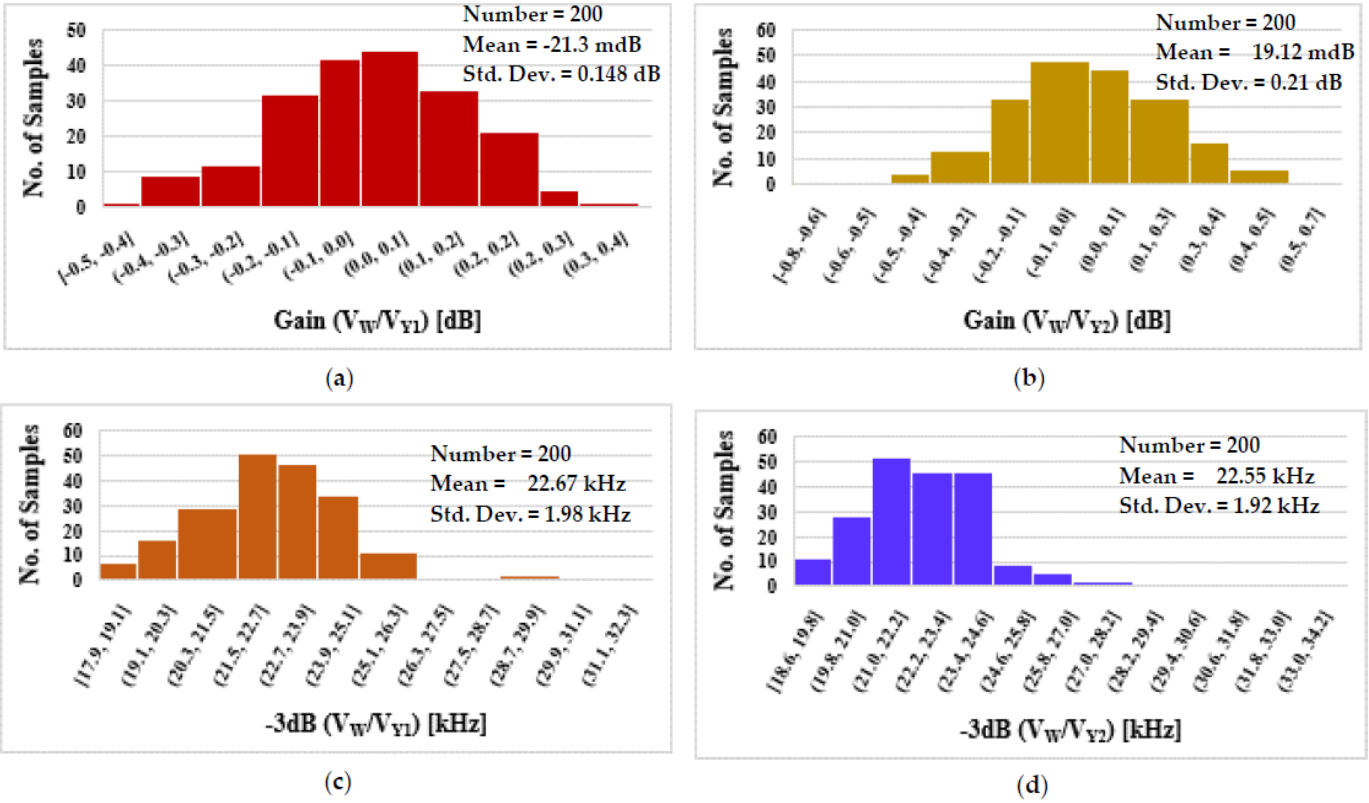
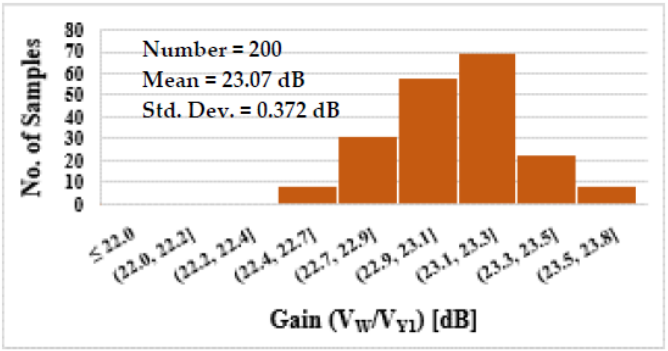
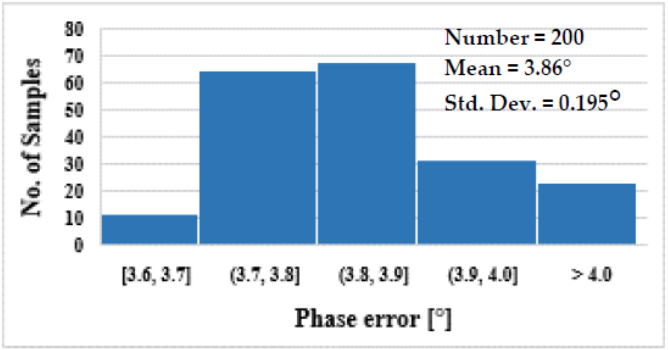


Figure 10. The DDCC histogram of the gain V_w/V_{Y1} (**a**), V_w/V_{Y2} (**b**), and the −3 dB BW V_w/V_{Y1} (**c**), and V_w/V_{Y2} (**d**).



(**a**)



(**b**)

Figure 11. The TA histogram of the gain (**a**) and phase error (**b**).

Table 4. The PVT corner analysis results for the TA.

TA	min.	nom.	max.
	P/V/T		P/V/T
Gain [dB]	23/20.6/21.9	23.19	23.2/25.2/24
Phase error [°]	3.7/2.9/3.4	3.8	3.8/5.1/4.3
G_m [µS]	2.2/2.2/2.2	2.48	2.5/2.5/2.4

The universal filter in Figure 4 was simulated for $C_1 = C_2 = 5$ nF, which are off-chip capacitors. The magnitude characteristics of the LPF, HPF, BPF, BSF, and APF are shown in Figure 12. The simulated natural frequency (f_o) is around 81.47 Hz. It is worth mentioning that, due to the limited value of the output resistance of the TA, which is around 5.1 MΩ, the attenuations of the HPF and BPF are degraded at low frequencies. Therefore, if an application demands higher attenuation, then the output resistance could be increased, employing the MOS transistor self-cascode technique.

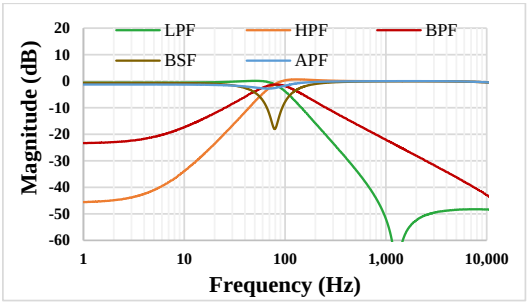


Figure 12. The magnitude characteristics of the universal filter.

The BPF was tested by applying a sine wave signal V_{in} = 100 mV_{pp} @ 81.47 Hz. The waveforms of the input and output voltages are shown in Figure 13a. The spectrum of the

output signal is shown in Figure 13b, where the total harmonic distortion (THD) of the BPF output is 0.5%.

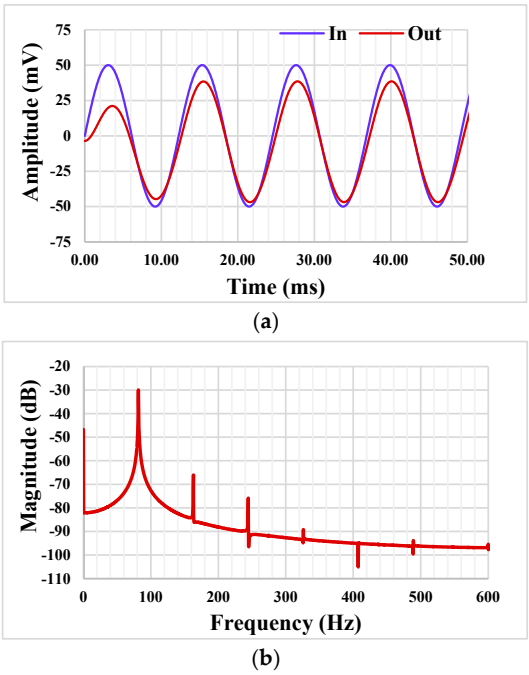


Figure 13. The transient response of the BPF (**a**) and the spectrum of the output signal (**b**).

The electronic tuning capability of the LPF, BPF, HPF, and BSF with different bias currents, I_{set} = 0.125, 0.25, 0.5, and 0.75 µA, is shown in Figure 14. The f_o was in the range of 21.11 Hz, 41.63 Hz, 81.47 Hz, and 115.74 Hz, respectively.

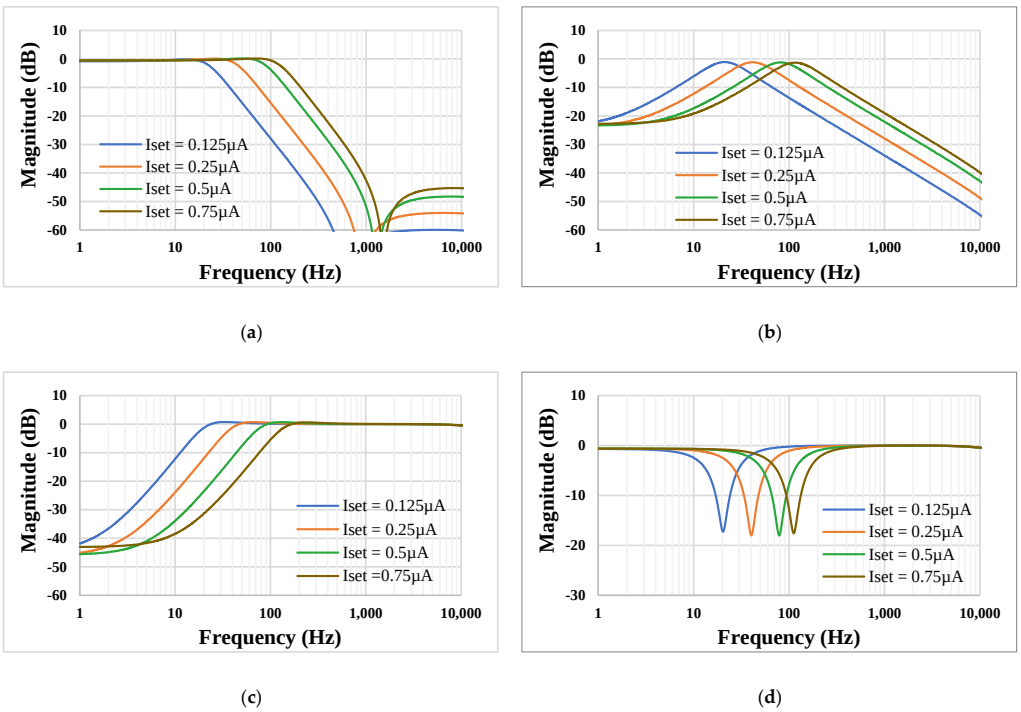
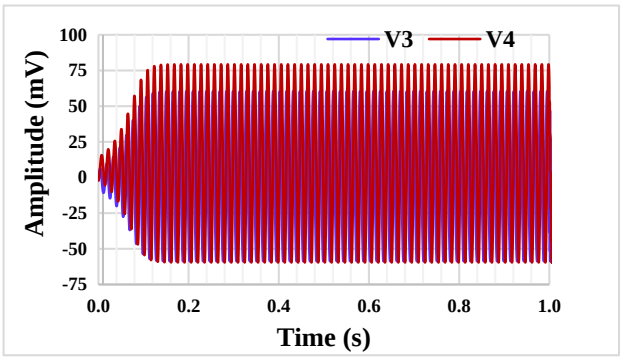
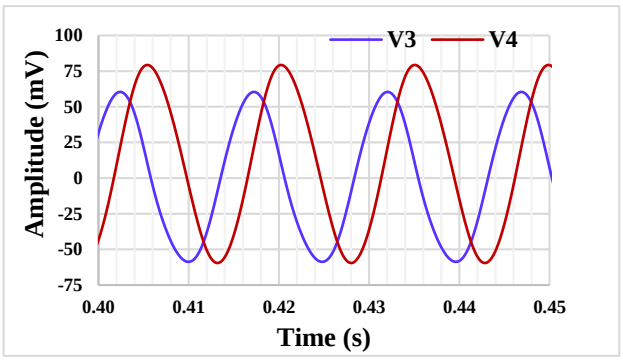


Figure 14. Magnitude characteristics showing the tuning capability of the LPF (**a**), BPF (**b**), HPF (**c**), and BSF (**d**) with different bias currents.

The simulation results showing the start of the oscillation and the steady state of the quadrature oscillator from Figure 5 are given in Figure 15. The oscillation frequency is 67 Hz, and the THD for outputs V_3 and V_4 are 1.2% and 1.29%, respectively.



(**a**)



(**b**)

Figure 15. Starting the oscillation (**a**) and the steady state (**b**).

Finally, Table 5 provides the comparison of the proposed filter with others in the literature [23,41,42,44,46,47]. It is evident that the proposed filter offers the highest number of filtering functions with lowest power supply and power consumption, thanks to the innovative CMOS structure of the DDTA.

Table 5. Comparison table with other universal filters.

Features	Proposed	Ref. [23]	Ref. [41]	Ref. [42]	Ref. [44]	Ref. [46]	Ref. [47]
Active and passive elements	2 DDTA, 2 C	5 OTA, 2 C	5 OTA, 2 C	4 OTA, 2 C	3 CFOA, 2 C, 4 R	3 VDBA, 2 C, 1 R (Figure 2)	8 OTA, 2 C (Figure 3)
Realization	CMOS structure (130 nm)	CMOS structure (180 nm) & commercial IC	commercial IC	commercial IC	CMOS structure (180 nm)	CMOS structure (180 nm)	CMOS structure (180 nm)
Filter type	MIMO	MISO	MIMO	MIMO	MOMO	MISO	MIMO
Number of filtering functions	22 (VM)	11 (VM)	13 (VM)	9 (VM)	5 (VM)	20 (Mixed-mode)	20 (Mixed-mode)
Offer universal filter and oscillator	Yes	Yes	Yes	Yes	Yes	No	No

Table 5. *Cont.*

Features	Proposed	Ref. [23]	Ref. [41]	Ref. [42]	Ref. [44]	Ref. [46]	Ref. [47]
Electronic control of parameter ω_o	Yes	Yes	Yes	Yes	No	Yes	Yes
Natural frequency (kHz)	0.08147	1	217	144.7	757.88.	16.631×10^3	5.77
Total harmonic distortion (%)	0.5@100 mV_{pp}	1.67@600 mV_{pp}	1.93@200 mV_{pp}	3.83@170 mV_{pp}	3.18@1.2 V_{pp}	<3@500 mV_{pp}	<2@200 mV_{pp}
Power supply voltages (V)	0.3	1.2	±15	±15	±0.9	±1.25	±0.3
Simulated power consumption (µW)	0.715	96	860×10^3	0.92×10^6	5.4×10^3	5.482×10^3	5.77
Verification of result	Sim	Sim/Exp	Sim/Exp	Sim/Exp	Sim/Exp	Sim/Exp	Sim

Note: VDBA = voltage differencing buffered amplifier, VM = voltage-mode.

5. Conclusions

This paper presents an innovative structure of a DDTA capable of operating under an extremely low voltage supply of 0.3 V while offering a rail-to-rail input voltage swing. As an application, a universal filter and quadrature oscillator based on two DDTAs and two grounded capacitors are presented. The simulation results including Monte Carlo and PVT analysis confirm the good functionality of the proposed circuits.

Author Contributions: Conceptualization: F.K. and M.K.; Methodology: F.K., M.K., T.K. and D.B.; Validation: F.K., M.K. and T.K.; Formal Analysis: M.K., T.K., F.K. and D.B.; Investigation: F.K. and M.K.; Writing—Original Draft Preparation: F.K., M.K., T.K. and D.B.; Writing—Review and Editing: F.K., M.K., T.K. and D.B. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the School of Engineering, King Mongkut's Institute of Technology Ladkrabang, under Grant 2565-02-01-005, and by the University of Defence Brno within the Organization Development Project VAROPS.

Conflicts of Interest: The authors declare no conflict of interest.

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