Review

Functional Devices from Bottom-Up Silicon Nanowires: A Review

Tabassom Arjmand [1,2,3]**, Maxime Legallais** [1,2]**, Thi Thu Thuy Nguyen** [1]**, Pauline Serre** [1,3]**, Monica Vallejo-Perez** [1]**, Fanny Morisot** [1]**, Bassem Salem** [3] **and Céline Ternon** [1,*]

[1] Univ. Grenoble Alpes, CNRS, Grenoble INP (Institute of Engineering Univ. Grenoble Alpes), LMGP, F-38000 Grenoble, France; tabassom.arjmand@grenoble-inp.fr (T.A.); maxime.legallais@cea.fr (M.L.); thuthuynguyen2004@gmail.com (T.T.T.N.); pauserre@gmail.com (P.S.); monica.vallejop@gmail.com (M.V.-P.); morisotf@gmail.com (F.M.)
[2] Univ. Grenoble Alpes, CNRS, Grenoble INP (Institute of Engineering Univ. Grenoble Alpes), IMEP-LAHC, F-38000 Grenoble, France
[3] Univ. Grenoble Alpes, CNRS, CEA/LETI-Minatec, Grenoble INP (Institute of Engineering Univ. Grenoble Alpes), LTM, F-38000 Grenoble, France; bassem.salem@cea.fr
[*] Correspondence: celine.ternon@grenoble-inp.fr

Abstract: This paper summarizes some of the essential aspects for the fabrication of functional devices from bottom-up silicon nanowires. In a first part, the different ways of exploiting nanowires in functional devices, from single nanowires to large assemblies of nanowires such as nanonets (two-dimensional arrays of randomly oriented nanowires), are briefly reviewed. Subsequently, the main properties of nanowires are discussed followed by those of nanonets that benefit from the large numbers of nanowires involved. After describing the main techniques used for the growth of nanowires, in the context of functional device fabrication, the different techniques used for nanowire manipulation are largely presented as they constitute one of the first fundamental steps that allows the nanowire positioning necessary to start the integration process. The advantages and disadvantages of each of these manipulation techniques are discussed. Then, the main families of nanowire-based transistors are presented; their most common integration routes and the electrical performance of the resulting devices are also presented and compared in order to highlight the relevance of these different geometries. Because they can be bottlenecks, the key technological elements necessary for the integration of silicon nanowires are detailed: the sintering technique, the importance of surface and interface engineering, and the key role of silicidation for good device performance. Finally the main application areas for these silicon nanowire devices are reviewed.

Keywords: nanowires; nanonets; transistor; integration process; silicon

1. Introduction

The study of nano-objects reveals a new world in which the observed properties may differ from those of bulk materials. When the size of structures reaches the nanoscale, the ratio of surface to volume of the structures increases drastically [1]. Since the number of atoms on the surface becomes comparable to the number in the volume, the physico-chemical properties of nanostructures are modified and even controlled by surface effects. These surface effects induce new properties compared to the bulk material that multiply the field of investigation. Over time, the study of nano-objects has increasingly become a scientific and technological revolution. Nanowires (NWs) can be defined as nanostructures that have diameters towards the nanometer scale (<100 nm).

Nanowires are still in an experimental stage and have not yet been used in real applications [2,3]. However, there is a graceful evolution in NW-based technology and investigations suggest that they can be used as the building blocks for the next-generation electronics and very sensitive biosensors [2,4,5]. Another possible real application of

nanowires is nano-electromechanical systems (NEMS) due to their high Young's moduli [2,6]. Nanorobots can also be aided by nanowires in the generation and conduction of their required energy [7].

In this review, we focus on synthesized silicon nanowires (bottom-up NWs) and do not consider nanowires formed by any etching techniques. These nanowires can be used vertically attached directly to their growth substrate [8,9], or detached from it to be transferred elsewhere and integrated into devices [10,11]. The mastery of the synthesis techniques allows obtaining nanowires of very small diameters, with controlled crystallinity and doping. In addition, surface engineering allows good control of their surface properties. Their quasi-one-dimensional characteristic gives them remarkable properties for many applications—such as electronic, optoelectronic, energy, and biomedical applications. In 1998, Morales and Lieber succeeded in synthesizing the first silicon and germanium nanowires with diameters of less than 20 nm for lengths greater than 1 μm [12]. This major breakthrough was an immediate success within the scientific community as a new field of research in nanoelectronics.

It is possible to make conducting (e.g., Ni, Pt, Au), semiconducting (e.g., Si, InP, GaN), and insulating (e.g., SiO_2, TiO_2) nanowires which can find different possible real applications [2,13–15]. Among these nanowires, silicon nanowires (SiNWs) are considered as popular nanomaterials due to their exceptional electrical and mechanical properties and their conductivity can be controlled by the field effect behavior [2,16–18]. In addition, their synthesis is very well controlled due to broad study in the literature, their integration in transistors takes benefits from the technological knowledge related to the manufacture of MOSFET, particularly for the production of electrical contacts [19,20]. Finally, NWs have a very high length-to-diameter ratio called form factor. Because of this one-dimensional shape, which is comparable to some biological molecules, NWs are the ideal transducer for bio-detection. In 2001, Lieber's group was the first to highlight the promising potential of SiNWs as biosensors [21]. This technology still arouses curiosity today, and silicon nanowires are still potential candidates for field effect transistors and advanced sensors [22,23].

To appreciate the attractiveness of silicon nanowires (SiNWs) in a broad sense, we have shown in Figure 1 the result of a search on the Of Knowledge website with the keyword "Si or Silicon" AND "nanowire*" in the title. The first decade of the 21st century saw an explosion in the number of publications on silicon nanowires (Figure 1), as their potential appeared extremely promising. These publications are mainly concerned with the synthesis, formation, characterization, and integration into functional devices that are mostly composed of a single nanowire or several nanowires in parallel. From 2012 onwards, we observe a steady decrease in the number of publications. This can be attributed on the one hand to the less innovative aspect of the topic over the years with increasingly complete coverage of knowledge on this material. On the other hand, the difficulty of producing functional devices in a reproducible and efficient manner with technologies that are transferable to industry and at reasonable costs tends to blunt the appeal of these materials. A few years ago, and based on this observation, some groups [24–30] started to work on nanowire assemblies, also called nanowire networks and referred to as nanonets. Indeed, such assemblies benefit from advantageous nanometric properties, as well as easy connection to macroscopic objects thanks to their large dimension.

In this review, properties, growth, and transfer methods of SiNWs—either singularly, or in the form of a network—are reported. To have a better view of devices based on these materials, technological key parameters were discussed. Afterward, SiNW-based transistors are explored as building blocks for most of the applications depicted in different common forms—in particular, single NW field effect transistors (SiNW-FETs), nanonet field effect transistors (SiNN-FETs), and multi-parallel channel field effect transistors (MPC-FETs). Ultimately, it is shown that SiNWs, owing to their unique physical and chemical properties, are promising candidates for the wide range of applications that differ from those of bulk silicon material.
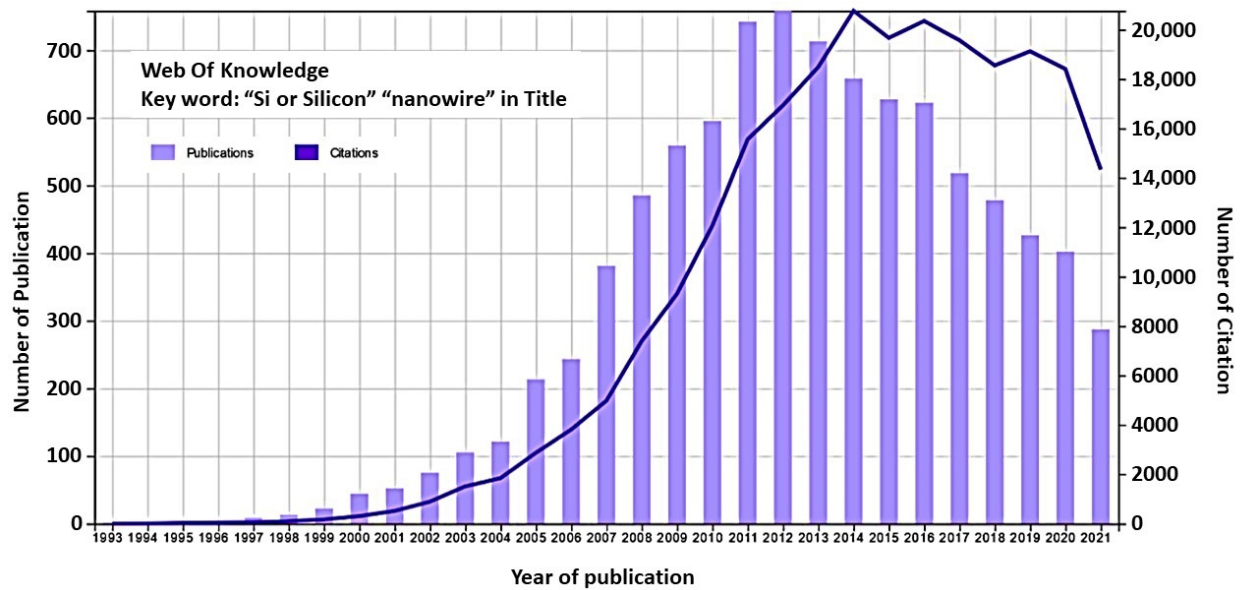
Figure 1. Number of articles published per year and the number of citations based on a search using the keyword "Si or Silicon Nanowire" on the website Of Knowledge.

2. From Nanowire-Based to Nanonet-Based Silicon Devices

There are a broad variety of nanowire-based devices—such as single nanowire, crossed nanowires, forest of upright nanowires, and two- and three-dimensional (2D and 3D) nanonet based devices—as schematically summarized in Figure 2. Crossed nanowire device architectures, more complex than single NW devices, can open up new opportunities that differentiate NW-based devices from conventional paradigms. Depending on the choice of NWs, the structure can yield a variety of critical device elements, including transistors and diodes [31]. Forest-like and 3D-NW structures, combining the properties of 1D and 3D nanostructures, could have more interesting properties than simple arrays of in-plane nanowires because of their higher porosity and specific surface area [32]. However, in this review, we will focus on single NW field effect transistors (SiNW-FETs), nanonet field effect transistors (SiNN-FETs), and multi-parallel channel field effect transistors (MPC-FETs).
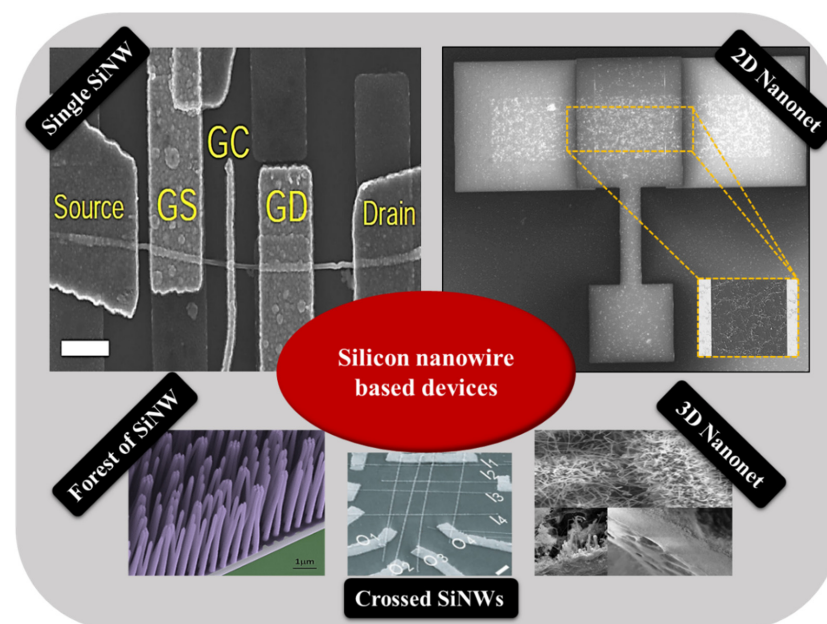
Figure 2. Different types of nanowire-based samples [33,34].

Today, single nanowire devices and parallel nanowire devices are well known to the scientific community and widely reported in the literature. Nanonet-based devices, on the other hand, are less well known, especially in the context of semiconductor nanowires. Nanonet, an acronym for NANOstructured NETwork, is a term that was introduced by George Grüner in 2006 [35,36]. It refers to a network of one-dimensional, randomly oriented nanostructures on the surface of a substrate. Two types of nanonets can be distinguished according to the thickness of the film formed. On one hand, three-dimensional nanonets have a thickness comparable to or larger than the length of the nanostructures (Figure 3a). On the other hand, two-dimensional nanonets are defined by a film thickness comparable to the diameter of the nanostructures (Figure 3b).
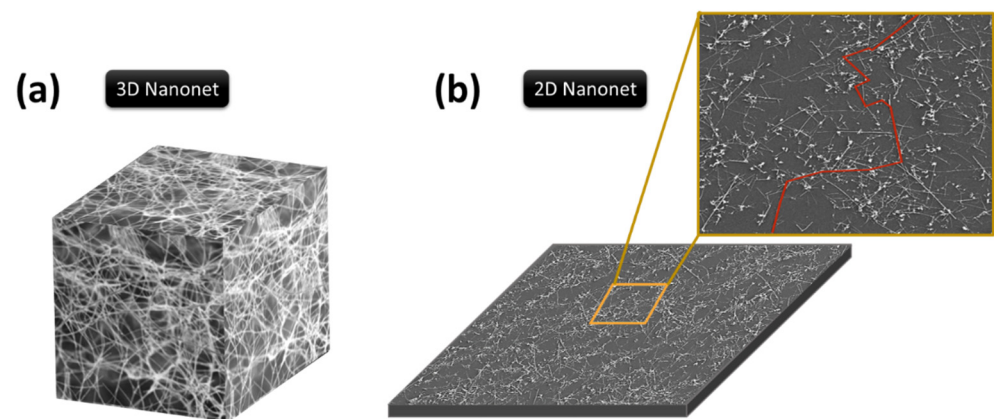
Figure 3. Schematic made by SEM images for representation of a nanonet (**a**) three-dimensional (3D nanonet) and (**b**) two-dimensional (2D nanonet). A top view and percolation path in red are highlighted in image (**b**).

Considering the electronic properties, such three-dimensional or two-dimensional networks are governed by percolation theory. Percolation is associated with a system in which randomly distributed objects of a given geometry may or may not form connections with each other [37,38]. A nanonet is then defined as percolating when a network of infinite size can communicate (e.g., conduct current) over the entire network via percolation paths that involve nanostructures and connections between nanostructures (Figure 3b). The density of nanostructures is a key parameter to control this communication (conduction in the current, etc.) via the interconnections between nanostructures. As a result, there is a critical density, called the percolation threshold, at which percolation pathways can be used to ensure communication in the nanonet. The manufacture of functional electrical devices from nanonets requires densities above the percolation threshold. Besides, nanonets are highly interesting because once the nanostructures are gathered to form the network, new properties appear and multiply the number of degrees of freedom. These properties are separated according to the intrinsic properties of the nanostructures and the macroscopic properties that come from the nanonet itself [36,39]. The particular properties of the nanonets are described in Section 4 in detail.

The literature on silicon nanonets remains scarce, despite the very well-controlled growth of NWs and excellent carrier mobility in bulk materials [40,41]. One of the plausible reasons for the lack of interest in these nanonets is the formation of an oxide that forms around the NWs when they are exposed to air. This native oxide is an electrical insulator and thus limits conduction across the junctions between NWs and the fabrication of long channel devices [42]. As a consequence, there is a deep-seated belief in the scientific community that it would be impossible to produce functional electrical devices based on Si-NW networks. To overcome this major disadvantage, Heo et al. [42] used intermediate metal contacts in the transistor channel to allow current to flow despite insulating junctions between SiNWs, but such a solution has a profound impact on the nanonet and the advantages arising from the geometry of the nanonets are probably lost. The Lieber group [43] also made devices

with arrays of silicon NWs; however, the length of the NWs remains close to the length of the channel and therefore the current can flow directly from one contact to another without using junctions between NWs. Furthermore, SiNNs have also been studied by the Unalan group for photodetection applications [44]. According to their observations, light makes it possible to reduce the height of the energy barrier at the level of the junctions between NWs, thus allowing the passage of current through the devices. However, even in that study, the length of the channel remains comparable to that of the NWs, limiting the junction number to one maximum. As a result, few NW/NW junctions are involved in the conduction of the nanonet, which prevents the full benefits of network geometry from being exploited.

Generally, semiconducting nanonets—in comparison with metallic ones—are much less studied and, most of the time, when dealing with NWs, the reported work is an isolated study that is not followed by any other publication [24,44–46]. We believe that the reason for this lies in the great sensitivity of semiconducting nanonets to their environment, which makes electrical properties unstable and weakly reproducible at first sight. However, Ternon's group has demonstrated that appropriate surface engineering and optimization of the effects resulting from the nanometric scale allow addressing this instability and low reproducibility. As a consequence, sensitivity can be controlled instead of endured [47]. As a result, they developed a process for sintering junctions that makes nanonets insensitive to oxidation in the long term [48] making their integration into electronic devices possible.

Among NWs, SiNWs are considered one of the most popular one-dimensional materials due to their functionality for nanoscale electronics without the need for complex and costly fabrication facilities. The main obstacles to the mass production of single NW devices, including high-resolution lithography technologies or elaborated process technology, are still valid. There are a huge number of papers on single SiNWs, but not all the other class of SiNW assemble like silicon nanonets, although they indicate being a good alternative for single NWs due to their easier integration and production in large-scale electronics. These types of materials combine the advantage of NWs, such as high sensitivity, with the ability to be transferred on any kind of substrates, whether rigid or flexible.

3. Silicon Nanowire Properties

3.1. Mechanical Properties

Mechanical properties of nanowires are of considerable significance in device processing since changes in temperature, induced strain, and external stress can change the electrical conductivity of the nanowire due to internal dislocations or flexoelectricity [49,50]. The processing of VLSI (very large-scale integration) induces compressive and tensile stresses via deposition of different materials which can cause failure in devices mainly due to delamination and electro-migration [51]. Moreover, due to the Si NW ability to relax strain, it presents the possibility to also combine lattice mismatched materials (e.g., Ge) in axial heterostructures without the formation of misfit dislocations. Nanowires, which are 1D systems, are expected to have interesting mechanical properties due to their high aspect ratio compared to bulk materials and reduced number of defects per unit length [6,51]. However, manipulating these materials for mechanical measurements is a challenging task [51,52]. The main methods which are used to investigate their mechanical properties are mechanical resonance, atomic force microscopy (AFM), and nanoindentation [18,52]. The resonance method is used only for the determination of the elastic properties and is not easy to measure the applied force. On the other hand, nanoindentation has very good force and displacement resolution and control [52].

Experiments based on the AFM-based nanoindentation showed that the stiffness of silicon nanowires is well described by the Herz theory [18]. Therefore, the wires with diameters in the range of 100 nm to 600 nm have elastic modulus values which are independent of the wire diameter and are more or less identical to those of bulk silicon [18]. This implies that the elastic characteristics of silicon nanowires with diameters larger than 100 nm are not affected by the finite size effect. Furthermore, the elastic modulus of nanowires with diameters of less than 100 nm was found to decrease with diameter [18]. In contrast, com-

putational studies do not support any size dependence of Young's modulus for SiNWs with a diameter greater than 10 nm [53,54]. In fact, some experimentalists disagree on the evolution of Young's modulus as a function of size [55]. In many cases, experimentally depicted structures and the analogous theoretically simulated models have different dimensions, surface contours, or passivation. Therefore, it has been speculated that the surface effects should have a certain influence on the difference between experimental and theoretical data. Importantly, the experimental proofs of possible sources of such misconceptions have been provided, at least for the resonance and tensile tests [56–60].

Moreover, NWs can be used in the field of sensors and nano-electromechanical systems (NEMS) [18,51]. This is because, according to their tensile strength and Young's modulus, they are very robust materials and have the ability to store elastic energy [51,61]. Then, nanoscale resonators can be built from silicon nanowires with high oscillation frequencies (100 MHz up to 1 GHz) because of their excellent elastic properties [18,51]. The detection of molecules at atomic resolution was achieved with these nanoscale resonators [18].

3.2. Electrical Properties

The small sizes of SiNWs make their electronic and electrical properties strongly dependent on growth direction, size, morphology, and surface reconstruction. A well-known example is the size dependence of the electronic bandgap width of SiNWs irrespective of wire direction. As the nanowire diameter, d, decreases below 10 nm, the band gap of the nanowire widens and deviates from that of bulk silicon gradually (Equation (1)) [62]. Moreover, the orientation of the NW axis and the surface have a great effect on the electronic properties of SiNWs [63].

$$\text{Band Gap} \propto \frac{1}{d^n}; \ 1 \leq n \leq 2 \tag{1}$$

Therefore, the electronic properties—such as the band gap, valley splitting, and effective mass—are also functions of the diameter [64]. These affect the transport properties of the nanowires [65]. Hydrogen and oxygen terminated SiNWs have also been studied to gain an understanding of their optical and electronic properties [66–68].

In the presence of perfect crystalline SiNW with four atoms per unit cell, three conductance channels are found corresponding to three *s* bands crossing the Fermi level [69]. Conductance variations are observed if one or two atoms are added or removed. Thus, the conductance is affected by the crystalline structure of the nanowire [23]. Furthermore, variations in the surface conditions, such as scattering phenomena of carriers in nanowires, cause changes in conductivity [23,51]; meanwhile, it is also seen that scattering phenomena are NW diameter dependent [23,70].

The large aspect ratio of nanowires makes their conductivity very sensitive to surface excitation by external charges [6,23,61]. As it is seen in Figure 4, a small surface perturbation can influence the entire section of the nanowire, whereas in the case of a thin film, only a fraction of its surface is influenced. This important property is the reason why silicon nanowires are so electrically sensitive to surface events. Thus, this phenomenon is the basis for the detection of single molecules and the use of silicon nanowires in biosensors [17,22,61,71].

It has been shown that threshold voltage (V_{th}) can be significantly tuned by the NW diameter (d) [72,73]. V_{th} is linearly proportional to d in an NW field effect transistor (NWFET) due to the greater influence of the surface scattering processes. NWFETs based on thin nanowires exhibit a steep subthreshold slope with a small threshold voltage, but low conductivity in comparison with NWFETs with larger diameters in which—due to high short-channel length effects—they experience a moderated subthreshold slope with a larger threshold voltage [74].
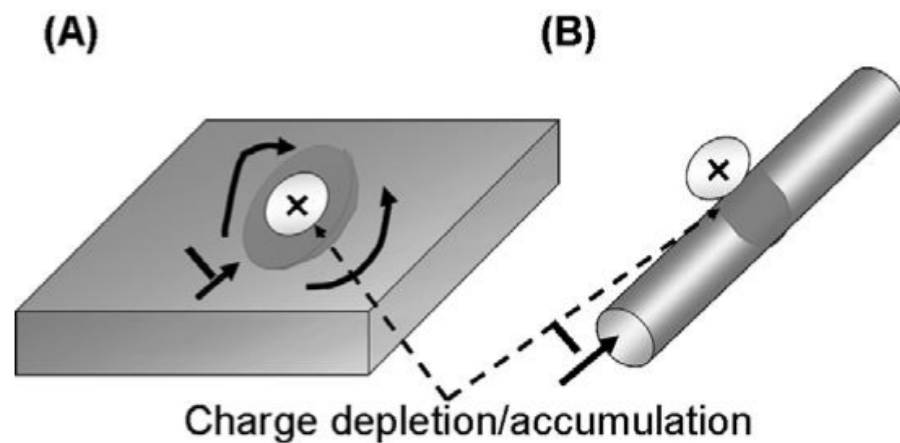
Figure 4. The major advantage of 1D nanostructures (**B**) over 2D thin film (**A**). Binding to 1D nanowire leads to depletion or accumulation in the 'bulk' of the nanowire as opposed to only the surface in the 2D thin-film case. Reproduced from [61].

Additionally, the free carrier concentration in silicon nanowires depends on the size of the structure. It was shown that the donor ionization energy of silicon nanowires increases with decreasing nanowire diameter. Therefore, the free carrier density can be profoundly modified at diameter values much larger (>10 nm) than those at which quantum and dopant surface segregation effects are set in [16].

Thus, silicon nanowires exhibit charge trapping behavior and transport properties, tunable by surface engineering, that make them attractive for use in electronic devices such as MIS (metal–insulator–semiconductor) structures and field effect transistors (FET). Therefore, SiNWs are attractive for designing a wide range of functional devices such as flash memory, logic devices, as well as chemical and biological sensors [51,62,75–78].

3.3. Surface Chemistry

As for bulk silicon, silicon nanowires are subject to surface oxidation when exposed to an oxidizing atmosphere such as air. This native oxide is of poor quality and is accompanied by many oxygen-derived defects. Moreover, native oxides are a contamination source by metallic impurities [79] and are poorly stable in aqueous media [80]. Native oxide can be easily removed by using either chemical reactants—such as buffer oxide etching (BOE) solution, diluted hydrofluoric acid (HF), HF vapor, and gaseous ammonia (NH_3)—or by physical etching method including argon (Ar) plasma etching. Most of these methods provide hydrogenated surfaces that are an interesting starting point for further functionalization in the frame of sensor applications [79,81].

In contrast to bulk silicon or thin films, the oxidation kinetics of H-terminated silicon nanowires is very slowed down regardless of the oxidation temperature (ambient—900 °C) compared to planar structures [82–85]. Moreover, it has been shown that—below 100 nm in diameter—the smaller the diameter of the nanowires, the slower the phenomenon [83]. This change in kinetics is commonly explained by compressive stress at the SiO_2/Si interface retarding the interfacial reaction [82,83]. Then, this effect becomes more significant for a more curved surface [86]. On this basis, Fazzini et al. propose that since oxidation retardation is inversely proportional to nanowire diameter, this property can be used to homogenize the diameter of a given nanowire population [87]. Such a slowing down of oxidation is an extremely interesting phenomenon when it comes to making functional devices. Indeed, this unwanted oxidation has detrimental effects on the electronic properties of nanowires. Preventing oxidation during silicon processing is an important task in all microelectronic processing. Thus, thanks to this slowing down of oxidation, silicon nanowires with a diameter lower than 10 nm can remain several days in the ambient air without oxidizing and can then be easily processed without any special precautions against oxidation [84].

3.4. Optical Properties

Remarkably, small diameter (<6 nm) SiNWs grown along most of the crystallographic orientations have a direct band gap [88], meaning that the maximum of the valence band and the minimum of the conduction band occur at the same point in the reciprocal space. This property has allowed envisaging the use of SiNWs as optically active materials for photonics applications [89]. Silicon nanowires exhibit strong antireflective properties and are capable of enhancing optical absorption over that of bare bulk crystalline silicon [90]. Nanowires can exhibit mechanical strain effects if exposed to light which has a wavelength comparable to their energy bandgap. This is due to their photoelastic properties [18].

In all, as yet it has been shown that SiNWs are found to process such remarkable optical properties as visible photoluminescence (PL) [91,92], very low total reflection [92,93], enhancement of Raman scattering [92–94], coherent anti-Stokes light scattering [95], inter-band PL [93,96], and efficiency of generation of third harmonics whereby light is generated at a wavelength which is one-third of the pump wavelength [92,97].

3.5. Thermal Properties

SiNWs could have applications in nano- and micro-scale thermoelectric power generators [98,99]. Therefore, it is important to study their thermal conductivity. However, for a major increment in the Seebeck coefficient, nanowires with a diameter of less than 5 nm are required [100]. The optimal diameter of NWs for good thermoelectric properties is between 30 and 100 nm. The thermal conductivity can be very small if rough nanowires are fabricated, while electrical conductivity and the Seebeck coefficient are very close to the bulk silicon [101]. Two opposite phenomena compete within the nanowires with respect to the thermal conductivity. On the one hand, as the diameter of the nanowires decreases, the surface-to-volume ratio increases, which increases the surface scattering effects and thus decreases the thermal conductivity of the nanowires. On the other hand, it has been predicted that for very small diameters (<1.5 nm), by a quantum confinement phonons effect, the thermal conductivity increases [102,103].

One has to note that silicon nanowires, when used within applications or experiments, may have a curved-like shape and not be straight. As the phonon transport can be affected by their curvature, their thermal conductivity then changes. There is an additional obstructive mechanism to phonon transport, particularly in the ballistic regime, thanks to the deviation of phonon from the main heat flow direction due to its curvature. Therefore, thermal conductivity is reduced when the radius of the nanowire curvature increases [5]. The effect of the curvature on the thermal impedance has a greater effect when the radius of the curvature is one order smaller than the phonon mean free path [5].

This observation is interesting since the thermal conductivity of silicon nanowires can be controlled by the proper shaping of the wire. For instance, the thermal conductivity of NWs with large roughness is found to be significantly below the prediction [5,104]. This is important in the use of silicon nanowires in next-generation electronics because the shrinking of electronic devices towards the nanoscale region demands an increase in power dissipation per unit area [99,105].

4. Silicon Nanonet Properties

Two-dimensional (2D) nanonets are very promising because, by an averaging effect, the structure provides an increase in the reproducibility of nanonet properties by minimizing the disparities existing between the NWs. It also compensates for potential failures in operation to the extent that NWs from the network, which are not initially involved in conduction paths, can contribute to a new conduction path to bypass the failed NWs. Nanonets offer undisputed advantages thanks to the wise combination of the intrinsic properties of nanostructures with those of the nanonet. According to Zhao and Grüner, the 'nanonet' morphology can be regarded as a fourth material phase in addition to monocrystalline, polycrystalline, and amorphous structures [106]. Finally, because of the coexistence of NWs and junctions within a conduction path, it is expected that the switching of the

transistors from 'off' state to the 'on' state will be even more abrupt as the number of junctions increases [107]. However, to allow these advantages to be revealed and exploited, it is important that the dimensions of the nanonet be much larger than the length of the NWs and that the number of NWs involved in conduction is sufficiently large. Here, important parameters impacting nanonet-based devices besides ones from individual NWs are the morphological quality of the nanonets, the density of NWs within the nanonet, the size of the nanonet, and particularly the distance between the two electrodes of the device compared to the length of NWs. Such degrees of freedom in nanonet create vast opportunities in future applications.

4.1. Electrical Conductivity

Above the percolation threshold, the current is likely to flow through percolation paths (also called conduction paths) that involve nanostructures and connections between nanostructures. These junctions between nanostructures appear as an energy barrier for carriers and are therefore likely to be more resistive than nanostructures [36,108]. In that case, they can control conduction within the nanonet. As mentioned earlier, these junctions generate additional resistance, so they can enormously affect percolation transport in nanowire network [107,109]. Such a two-dimensional network is normally governed by the theory of percolation. Percolation is often defined as a system in which randomly distributed objects of a given geometry can form, or not form, connections between each other [37,110,111]. A nanonet is then defined as a percolating system when a network of infinite size can communicate (e.g., conduct current) over the entire network via percolation paths that involve nanostructures and connections between nanostructures. The density of nanostructures is a key parameter to control the communication in the medium via the interconnections between nanostructures. As a result, there is a critical density—called the percolation threshold—above which percolation paths allow for communication in the nanonet. The fabrication of functional electrical devices from nanonets requires the use of densities above the percolation threshold.

4.2. Porosity and Optical Transparency

Due to the very high aspect ratio of nanostructures, and by playing with the density and diameter of NWs, NNs can reach even 90% of optical transparency as illustrated in Figure 5.

Indeed, for low-density percolating networks, nanonets are essentially composed of voids. In the case of metallic NWs, this property makes nanonets particularly attractive as transparent electrodes [26]. With the same idea, in the case of semiconductor NWs, nanonets would be particularly attractive to form transparent transistors and transparent electronics in general. Moreover, the high porosity of the nanonet can allow the insertion of functional materials [108], which is of high value when dealing with biosensors.

### 4.3. Mechanical Strength and Flexibility

Based on the excellent flexibility in individual nanowires which is diameter dependent, and for diameters less than 100 nm is remarkable when these nanostructures are assembled as a nanonet, the entire network is capable of being subjected to mechanical deformation [112] (Figure 5) and can adapt to the substrate morphology [112,113]. The flexibility in the choice of nanostructures and the unique structure of the network suggests a broad spectrum of applications for nanonets, as we will see in the following.
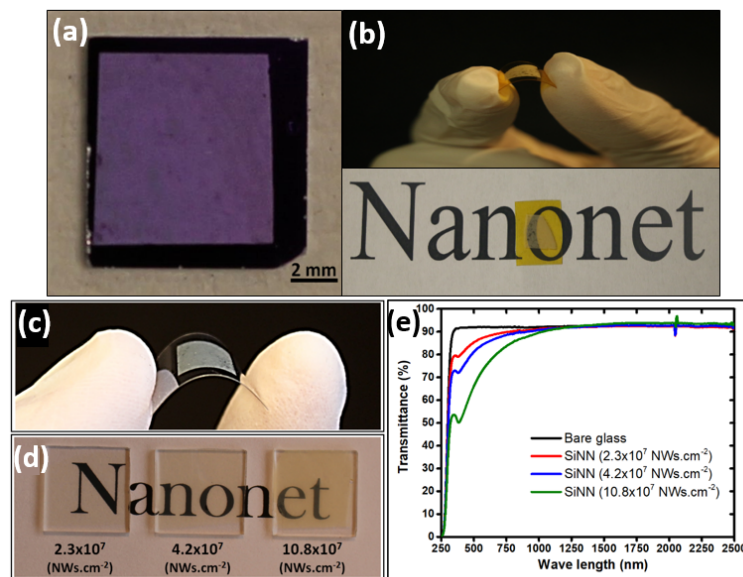
Figure 5. Silicon nanowire nanonets manufactured by vacuum filtration and then transferred to (**a**) Silicon/Si$_3$N$_4$, (**b**) Kapton, (**c**) plastic, and (**d**) glass substrates. (**e**) The transmittance of SiNN with the three densities were shown in image (**e**), the transmittance of the substrate (bare glass) is also reported. Reproduced from [114].

4.4. Fault Tolerance and Reproducibility

For electrical devices, conduction in a nanonet is ensured by multiple percolation paths that connect the two metallic contacts. Then, the number of conduction paths is greater but the presence of junctions within each path ultimately implies a reduction in current. Therefore, for a given electric field, the amount of current is generally lower in nanonet than in single nanowire devices (Figure 6). However, if one path is faulty, many other conduction paths remain and can guarantee the functionality of the device [36].
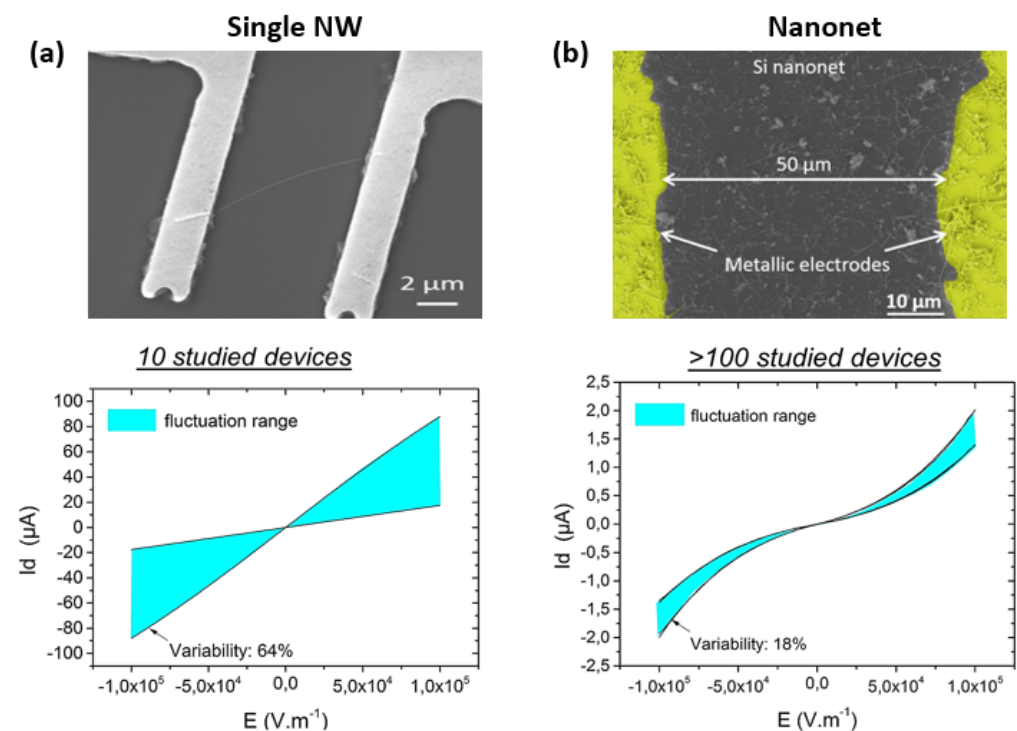
Figure 6. SEM image and fluctuation range in the current of (**a**) single nanowire and (**b**) nanonet-based resistors. Reproduced from ref. [28].

Moreover, the macroscopic properties of a given nanonet are the result of a considerable number (for 1×1 cm^2 e.g., 10^6–10^8 NWs) of nanostructures which makes it possible to smooth out the disparities that may exist from one NW to another. Therefore, the properties of the nanonets show less disparity than those of the population of nanowires that constitute it. This can be demonstrated by studying the electrical characteristics of the single nanowire or nanonet devices based on the same nanowire population, as Pauline Serre has done. With a technological work based on heavily doped NWs (degenerated), she produced single SiNW resistors and Si NN resistors (Figure 6) [28,39]. By studying numerous devices (10 single SiNW resistors, >100 SiNN resistors), evidence of averaging effect is proven for nanonets. Indeed, the dispersion in the current of these two types of devices is clearly different: 64% for single NW resistors, against 18% for SiNN resistors. As a consequence, one of the main drawbacks of the single NW-based devices, lack of reproducibility, can be eliminated by the nanonet geometry.

5. Silicon Nanowire Growth

There are two major approaches to form nanowires. The 'top-down' approach starts from bulk silicon in the form of a substrate or thin film silicon with the use of SOI substrate with the objective to etch the material until reaching the formation of high aspect ratio structures called nanowires, but which section is not necessarily circular. Besides, the 'bottom-up' approach is used to grow nanowires, either vertically on the substrate or in-plane lying on the substrate. In the past few decades, there has been extensive research on synthetic nanowire strategies focused on a bottom-up approach to understand the growth of nanostructures, tune the geometrical dimensions during growth, and form heterostructures. Here, we focus on bottom-up approaches that give the opportunity to detach the NWs and to collect them with the objective to form a nanonet by assembling the NWs. Then, targeted bottom-up syntheses are additive and can be done in two phases: vapor and solution phase.

5.1. Vapor Phase

5.1.1. Low Pressure

In the frame of low-pressure chemical growth, silicon nanowires are synthesized using the vapor–liquid–solid (VLS) mechanism (see Figure 7A) on a silicon substrate <111> from a metal catalyst (Au [115,116], In [117], Pt [118], Sn [119], etc.) in a CVD reactor. To allow the NW growth, the catalyst must be present on the surface of the substrate in the form of nanoparticles. For this purpose, it is possible to disperse a solution of colloids on the surface of the substrate [11] or to deposit a thin film that forms nanoparticles by thermal dewetting [117]. Then the growth of the Si nanowires is carried out in the presence of silane, SiH$_4$, used as a precursor to silicon. The Si atoms incorporate into the metallic droplets and when it reaches saturation, the excess silicon crystallizes at the interface between the droplet and the substrate. This process continues as long as the system is supplied with gaseous precursors and thus forms silicon nanowires.

Silicon nanowires can be doped during growth by adding boron (p-doping) or phosphorus (n-doping) in gaseous form. Phosphine, PH$_3$, is used for n-type doping and diborane, B$_2$H$_6$, for p-type doping [120]. The concentration of dopants in nanowires is directly related to the ratio between the concentration of dopant gas and the concentration of silane [121], which allows the doping of nanowires to be controlled with great precision during the growth. Two other gases can also be added during the synthesis of nanowires: hydrogen, H$_2$, which is used as a carrier gas; and hydrogen chloride, HCl, which is used to prevent the diffusion of gold on the surface of the nanowires and thus inhibit the lateral and branch growth of the structures [121–123]. The silicon nanowires produced by VLS are of good crystal quality and can have a very high length at low costs. The length of the nanowires is controlled by the time of the growth and diameter of the nanowires depending on the size of the metallic nanoparticles [21].
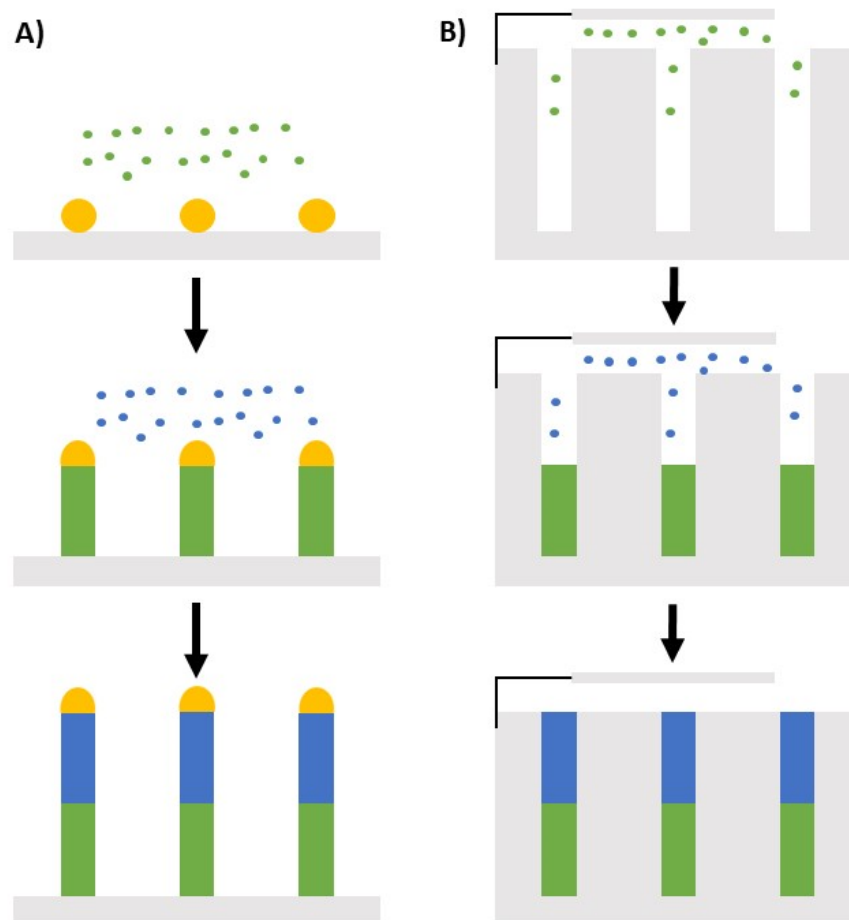
Figure 7. Schematic representation of two bottom-up synthesis methods. (**A**) Vapour-Liquid-Solid Chemical Vapor Deposition (VLS-CVD). Segmentation in composition is possible by the modulation of the gaseous precursor. (**B**) Electrochemical deposition in solution into anodic aluminum oxide. Segmentation is also possible.

5.1.2. High Pressure

The patented SyMMES technique [124] is similar to the CVD method and it aims to make its industrial scaling simpler, by limiting the hazard of the reactants, facilitating reactor design, and producing nanowires in large quantities.

In Figure 8, this method is shown for the solvent-free chemical synthesis of thin (10 ± 3 nm) SiNWs using diphenylsilane as a Si source and small (1–2 nm) gold nanoparticles (AuNP) as a catalyst in a sealed reactor at 420 °C and with a pressure < 10 bar. The catalyst nanoparticles are immobilized on micron-sized salt (NaCl) powder, which acts as a sacrificial 3D substrate which is easily removable by washing with water after NW growth. Pure SiNWs are obtained at a high production yield of 1 mg cm^{-3} of reactor volume and with a 70% chemical yield. In this method, n-type doping of the SiNWs is achieved by adding diphenylphosphine at concentrations of 0.025 to 1.5% as the dopant source [125]. Recently, the impact of the size/shape of SiNWs grown by this technique is also demonstrated on the electrochemical performance of conventional Li-ion batteries [126].
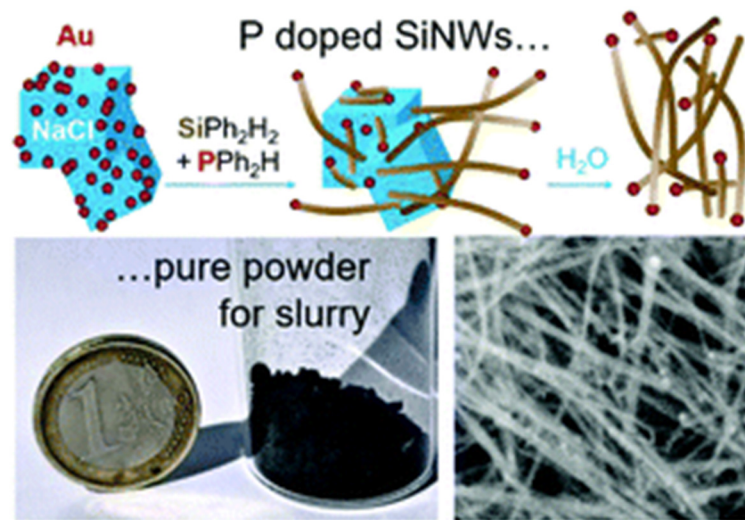
Figure 8. Schematic of the growth principle of SiNWs, and SEM image of as grown silicon nanowires Reproduced from [125].

5.2. Liquid (Solution) Phase

The first liquid phase technique for SiNW growth is the direct counterpart of the VLS technique. Then the solution–liquid–solid (SLS) mechanism is fully similar to that of VLS, except that nanowire precursors are dissolved into a high-boiling liquid, such as squalene ($C_{30}H_{62}$), and the catalysts are suspended therein, as described by Heitsch et al. [127].

The second method in liquid involves electrochemical phenomena. Here, anodic aluminum oxide (AAO) substrates are used for templated solution growth, using electrochemical deposition to fill the channels as shown in Figure 7B [128]. Drawing upon the solution-phase synthesis of nanoparticles, redox reactions can also be used to produce nanowires [129]. Seed particles are first grown by a rapid reduction of a dissolved precursor with a strong reducing agent such as sodium borohydride. Secondary growth is achieved with a weaker reducing agent, such as L-ascorbic acid, to prevent additional seed particle production. The nanowire anisotropy is achieved by controlling surface chemistry [123].

5.3. Summary on Growth

Table 1 gives a simple comparison between the different techniques used for SiNW growth. We studied the various methods currently used in bottom-up SiNW growth. Gold is the most widely used catalyst for SiNW growth by CVD under VLS mechanism, as it offers a good size control. However, the recent advances in the mentioned SiNW growth techniques are still in their early stages. The most appropriate method for the growth will ultimately be determined by a number of factors, including the desired application, as well as the available process control and associated costs. SiNW properties can be finely tuned for the desired application using the various growth methods available.

Table 1. Comparison between different NW growth methods including low pressure VLS (LP VLS), high pressure VLS (HP VLS), SLS, and electrochemical.

Method	Diameter Range	Crystallinity	Doping	Yield	Scalability	Homogeneity	Catalyst	Freestanding
LP VLS	>30 nm	Monocrystalline	Highly controlled	Medium	Good	Generally dispersed	Yes	No
HP VLS	<30 nm	Polycrystalline	Controlled	High	Very good	Homogeneous	Yes	Yes
SLS	Between 20 and 30 nm	Monocrystalline	Controlled	Medium	Good	Dispersed	Yes	No
Electrochemical	Limited by template	Polycrystalline	Controlled	High	Good	Highly homogeneous	Yes	No

6. SiNW Collective Handling

After growth, the nanowires are detached from the substrate and dispersed in solution to allow collective manipulation (colloidal suspension). Depending on the chosen assembly technique, it is possible to form arrays with a preferred orientation which are then not necessarily percolating or to form randomly oriented arrays. The common points of all these methods are the low thermal budget (less than 200 °C) and the easy scalability. In the frame of electronic application and functional device formation, the formation of the percolating network is mandatory. As a consequence, when the applied method leads to a preferential orientation, a two-step process has to be used to allow the crossing of the NWs that is required to allow charge carrier displacement.

6.1. Network with Preferential Orientation

6.1.1. Drop-Casting

The drop-casting is the simplest method to deposit NWs on top of a substrate. In this approach, a drop of a NW suspension is first deposited (literally 'drop-casted') on the surface. Second, a drying process is applied to evaporate the liquid. The clear advantage of this approach is its simplicity and versatility. There is also an opportunity to even mix different nanowires in a suitable solvent via ultrasonication before drop-casting. The main drawback is related to the homogeneity of the NW distribution on the substrate surface. Indeed, the drying process often induces shear forces that impact the NW positioning. As a consequence, drop-casting is well dedicated when the needs in terms of positioning or density are not too restrictive.

6.1.2. Fluidic Directed Assembly

In this method, nanowires can be assembled into parallel arrays with the control of average separation as well as complex crossed nanowires arrays. In this technique, the nanowires are suspended in a solution such as ethanol. Then, the suspension is sent through fluidic channel structures formed between poly(dimethylsiloxane) (PDMS) molds and a flat substrate. As a consequence, the NWs tend to align in the flow direction. In this way, by building the appropriate fluidic channel, parallel and crossed arrays of NWs can be readily achieved with single and sequential crossed flows (Figure 9), respectively, for the assembly [130]. The same result can be obtained with chemically patterned substrate that preferentially attracts the NWs in the functionalized region (Figure 9A).

The fluidic phase poses a challenge for single-nanowire control, accompanied to some extent by issues related to spacious microfluidic and large footprint electrodes [130].
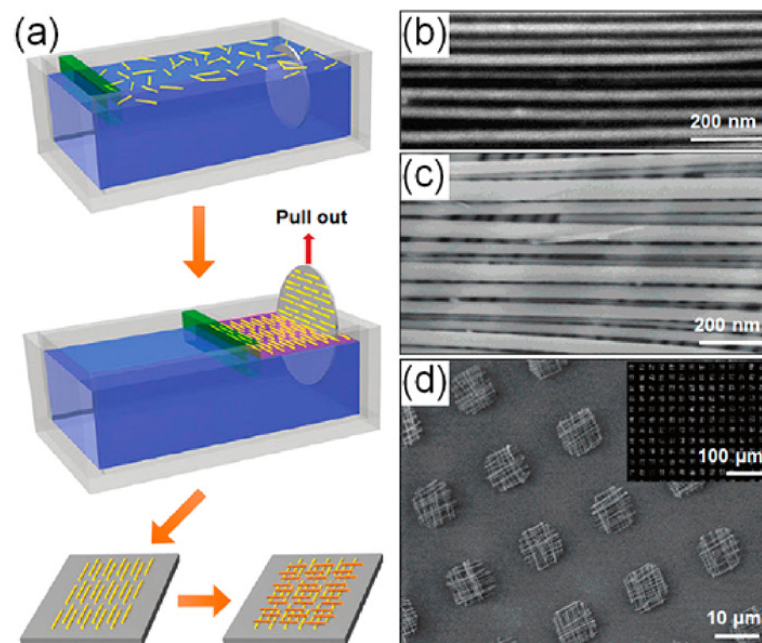
6.1.3. Langmuir–Blodgett Assembly

Another promising method to produce aligned arrays of NWs on various substrates is the Langmuir–Blodgett (LB) technique [43,131–134]. In this technique, NW suspension is densely packed using a compression trough at an air–liquid interface. Dip coating can be then used to transfer the NWs onto receiver substrates by van der Waals, hydrophobic-hydrophilic, or electrostatic interactions when the substrate is lowered and withdrawn from the system, in the vertical direction as shown in Figure 10a.

This technique is frequently used in the assembly of highly ordered nanomaterials. By repeating the assembly process with a changed orientation of the substrate, hierarchical nanowire structures can also be produced as shown in Figure 10b–d [131].

The density of nanowires can be improved by adapting LB techniques to align the nanowires. Limitations of this technique include reorganization of the nanowires during dip coating that leads to overlapping features and gaps within the dense arrays of nanowires [43,133,134].
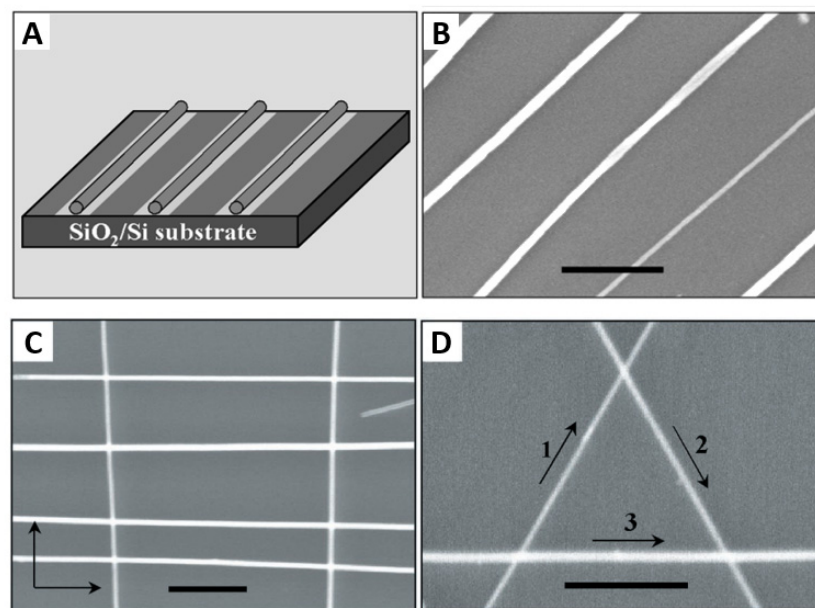
Figure 9. Assembly of periodic NW arrays and layer-by-layer assembly of crossed NW arrays. (**A**) Schematic view of the assembly of NWs onto a chemically patterned substrate. The light gray areas correspond to NH_2-terminated surfaces, whereas the dark gray areas correspond to either methyl-terminated or bare surfaces. NWs are preferentially attracted to the NH_2-terminated regions of the surface. (**B**) Parallel arrays of GaP NWs with 500-nm separation obtained with a patterned SAM surface. (**C**) Typical SEM images of crossed arrays of InP NWs obtained in a two-step assembly process with orthogonal flow directions for the sequential steps. Flow directions are highlighted by arrows in the images. (**D**) An equilateral triangle of GaP NWs obtained in a three-step assembly process, with 60° angles between flow directions, which are indicated by numbered arrows. The scale bars correspond to 500 nm in (**B**–**D**) Reproduced from [130].

Figure 10. Langmuir−Blodgett assembly of nanowires. (**a**) Schematic illustration of the Langmuir−Blodgett assembly process. Reproduced from [134]. (**b**,**c**) SEM images of a high-density parallel nanowire array (**b**) and crossed nanowire array (**c**) on the substrates. (**d**) SEM images at different magnifications for patterned crossed nanowire arrays. Reproduced from [43].

6.1.4. Blown-Bubble Films

An approach with the potential for large scale transfer of well aligned NWs is the so-called blown-bubble film assembly (BBF) (Figure 11). This approach involves the preparation of homogeneous polymer suspension of NWs, followed by the expansion of polymer suspension using a circular die, and finally the breaking by an external force and the transfer of the bubble film to the desired substrate. By tuning the preliminary concentration, well aligned, and controlled density NWs over large areas are achievable [135–137].
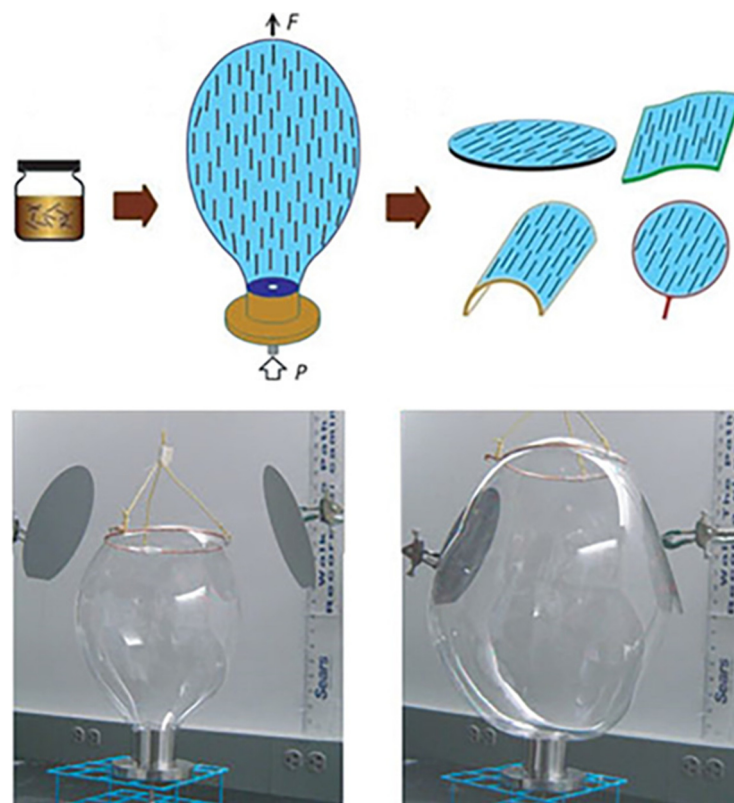

Figure 11. Illustration of blown bubble films method and photographs of the directed bubble expansion process in the early and final stages. Reproduced from [137].

Blow-bubble approach is inexpensive and can be adapted to patterning nanowires on many different types of substrates (e.g., flexible, flat, or curved). However, a challenge for these techniques is to control the viscosity of the bubble film in balance with a compatible surface coating on the nanowires, which has so far limited this demonstration to films of epoxy. Another challenge for this technique and for the alignment achieved using microfluidic flow is to precisely control the position of the deposited nanowires [43,136,137]. This method is highly attractive in a technology where device fabrication costs must be kept to a minimum and for transferring and aligning a variety of nanomaterials including SiNWs and CNTs [136,137].

6.1.5. Contact Printing

'Printing' has usually been used to describe a method by which a layer of ink is transferred from a stamp to a substrate through a reversing reaction [138,139]. Figure 12 contains an illustration of two different printing apparatuses. Printing methods thus include flexographic printing, offset printing, gravure printing, screen printing, and ink-jet printing. In the printing method, the choice of the solvents for ink preparation has been identified as an important parameter for active layer surface morphology [139–142].

Gravure printing   Ink-jet printing
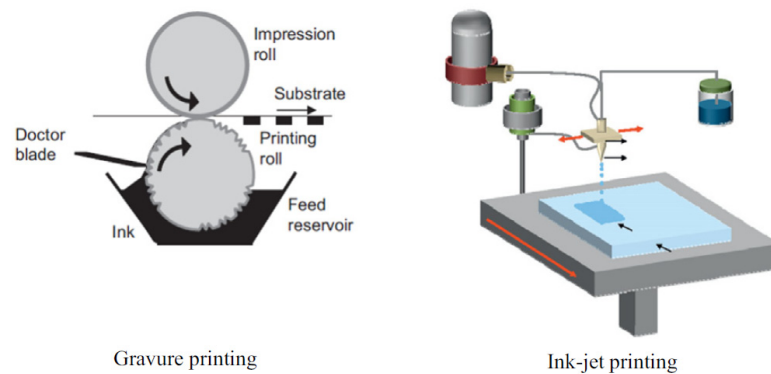
**Figure 12.** Illustration of printing apparatus. Reproduced from [139].

A simple but promising method is the contact printing (CP) technique developed by Javey et al. Here, the particularity is that the NWs are kept on their growth substrate until the transfer, no need to form a suspension. Therefore, during CP, nanowires are mechanically transferred by a shearing motion between the growth and the target substrate. In order to maximize the nanowire density and the alignment yield, the use of lubricants—such as mineral oil—is essential [143].

Yao et al. have significantly developed the nanowire alignment in CP by nanoscale combing technique [144,145]. In this technique, patterned resist windows opened by lithography are utilized to store the nanowires partially within the so-called anchoring regions [143,144,146], see Figure 13.
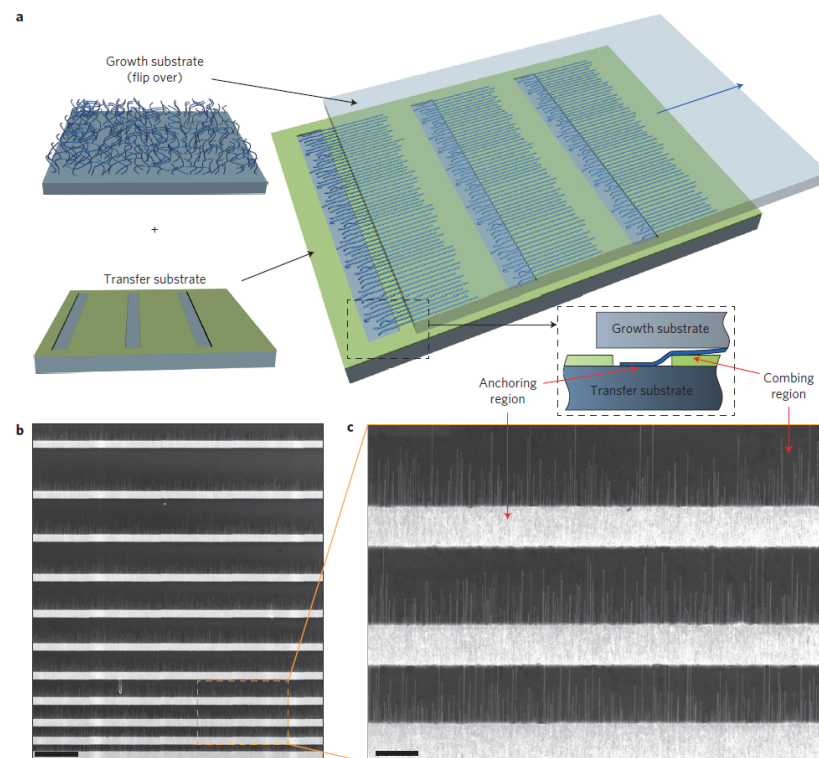
Figure 13. Schematics and demonstration of nano-combing. (**a**) Schematics of the nano-combing process. The blue arrow indicates the traveling direction of the growth substrate with respect to the target substrate, which yields a combing/aligning force that is parallel and opposite to the anchoring force. The dashed window at the right bottom shows a side view of the nano-combing process. (**b**,**c**) SEM images of silicon nanowires on the combing (resist) surface at different magnifications. The thickness of the resist (S1805) layer was 70 nm. Scale bars: 50 μm (**b**), 10 μm (**c**) Reproduced from [144].

Inspired by this CP technique, Robkopf and Strehle expand the current scope by focusing on the low-density nanowire assemblies and on dry friction to confine the nanowire deposition during CP [143]. Their motivation for dry friction was based on the fact that lubricants might act as a source of contamination in micro-device fabrication [147]. Therefore, they developed the concept of surface-controlled contact printing (SCCP) to avoid the need for lubricants, patterned resist, and post-print resist removal procedures. SCCP method is based on the frictional force between an individual nanowire on the growth substrate and the target surface, as shown in Figure 14. It has been shown that the material of the surface, the surface roughness, elevated structures, and nanoparticles can, in principle, be effective in the positioning of nanowires.
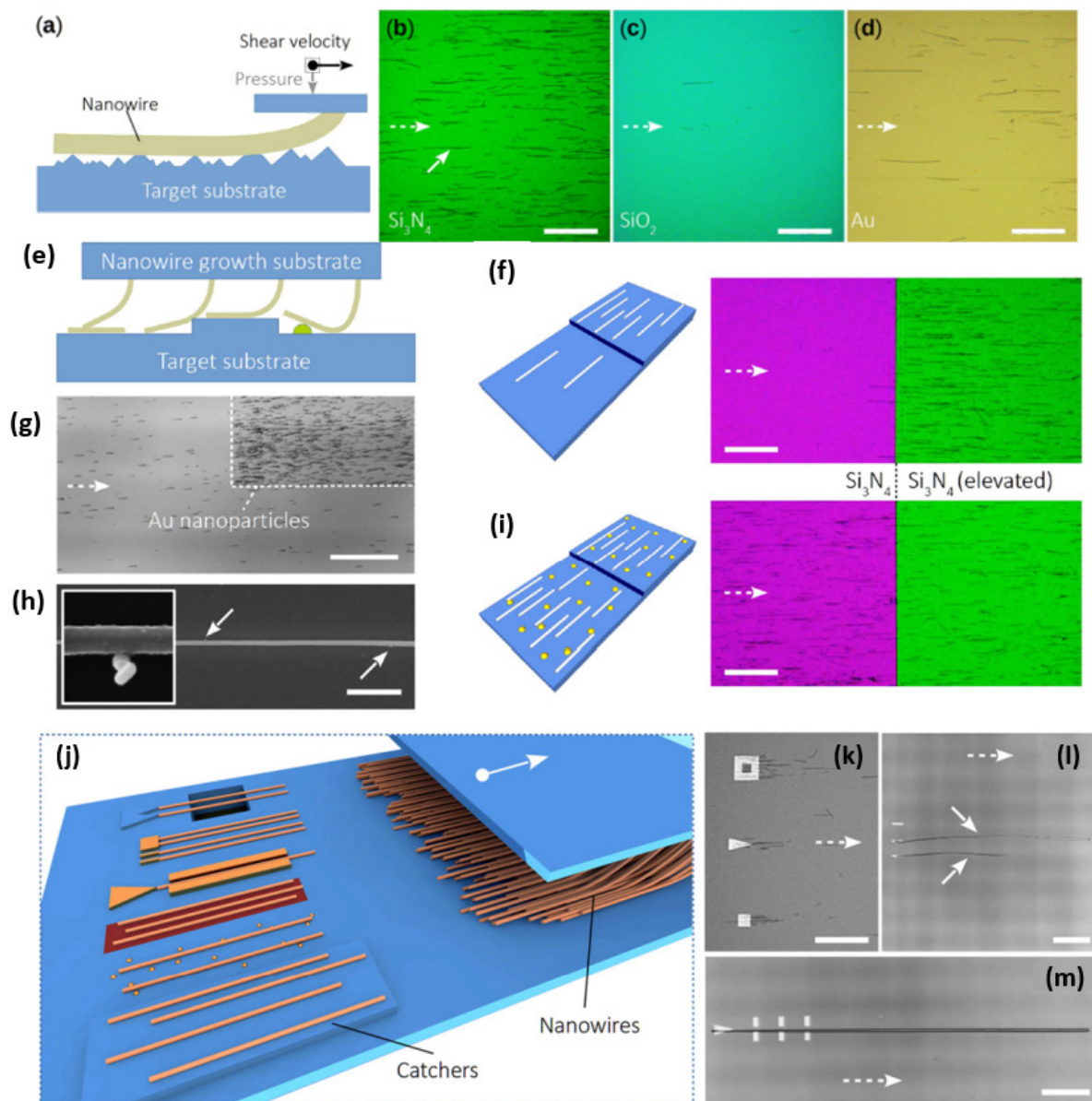
Figure 14. (**a–d**) Friction-based SCCP concept. (**a**) Schematic illustration of a nanowire in mechanical contact with a surface. The frictional force is predominantly influenced by the shear velocity vector, applied load, contact morphology, and materials of the nanowire and the target substrate. (**b–d**) Optical microscopy images of nanowires transferred in a lubricant-free manner (exemplified by the solid arrow in (**a**)) onto Si_3N_4, SiO_2, and Au surfaces. The dashed arrow represents the shear direction of the growth substrate. (**e–i**) Influence of local surface features on SCCP. (**e**) Schematic illustration showing the interaction of a nanowire with a previously deposited nanowire (left), the interactions of

nanowires with a step (center), and the interaction of a nanowire with a nanoparticle (right). (**f**) Schematic and optical images of an 80 nm step in Si_3N_4, revealing that nanowires are preferentially deposited onto the elevated area. (**g**) Optical micrograph depicting an area decorated locally with Au nanoparticles of 50 nm in diameter. The nanoparticles increase the frictional force acting on the nanowires and, therefore, significantly increase the deposited nanowire density. (**h**) SEM image of a nanowire on a surface decorated with Au nanoparticles of 20 nm in diameter. The arrows indicate the positions of nanoparticles. The inset shows a magnified region containing a nanowire and Au nanoparticles. (**i**) The effect of the step, as shown in (**f**), is masked when Au nanoparticles (here, 50 nm in diameter) are present. The shear direction of the growth substrate is indicated in all images by a dashed arrow. The scale bars for (**f–i**) represent 100 μm, and that for (**h**) represents 1 μm. (**j–m**) Towards SCCP nano-device fabrication. (**j**) Schematic illustration of various catcher concepts, listed from front to back: elevated plateaux, nanoparticles, changes in surface roughness or material composition, catchers with selectivity or guiding rails, catchers for single and multiple-nanowire positioning, and catchers fabricated out of the substrate material with nanowires spanning a trench. (**k**) Catchers on SiO_2 of different lateral shapes, leading to an increased nanowire density adjacent to the catcher. The dashed arrow indicates the shear direction of the nanowire growth substrate. (**l**) Gold catchers on Si_3N_4 with the ability to position single nanowires (see white arrows). The width of a single structure is 300 nm. (**m**) Optical image of one triangular and six rectangular Au structures for single-nanowire positioning. When the triangular structure catches a single nanowire, the rectangular structures appear to assist, serving a function similar to that of a guiding rail, as revealed by experiments. Reproduced from [143].
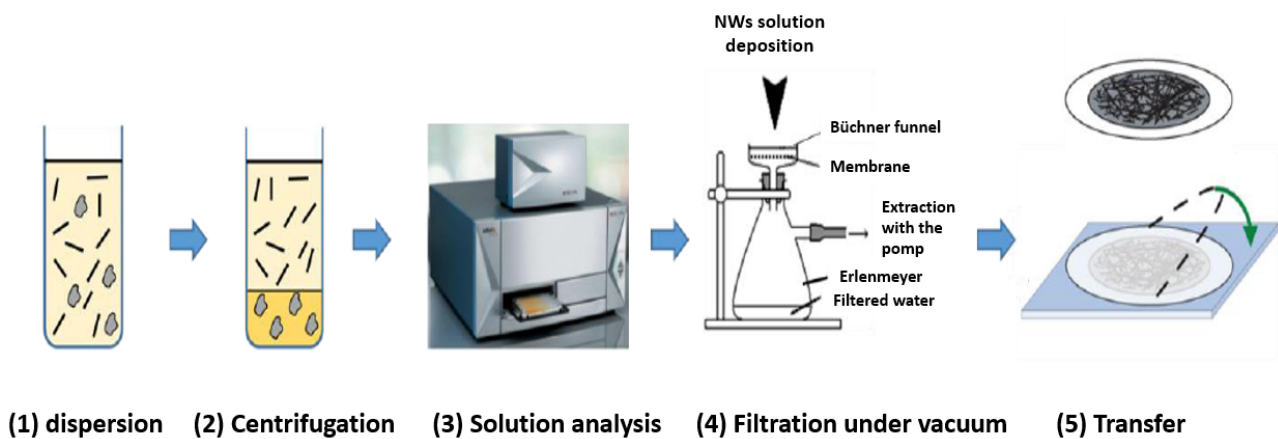
Contact printing can be a promising alternative to transfer highly controllable single-NWs, but using lubricant is still necessary for that. SCCP provides further possibilities to control the positioning of nanowires by lubricant free or dry friction interaction. The reduction in nanowire densities and lower alignment yields are still some drawbacks of this method [143,144].

6.2. Random Networks

6.2.1. Vacuum Filtration

Vacuum filtration [148,149] is widely used in the literature as it allows the production of homogeneous nanostructured networks at low cost and over large areas. During solution filtration, the nanostructures are randomly trapped on the surface of a porous filter. In the frame of Si nanonet assembling, Pauline Serre [28] and Maxime Legallais [27] have shown that the process consists in five main steps that are: (1) dispersion of the silicon NWs in solution, (2) purification of the suspension by centrifugation, (3) analysis of the suspension by absorption spectroscopy, (4) assembly of the NWs into nanonets by vacuum filtration, and finally, (5) transfer of the nanonet onto a substrate, as shown in Figure 15.

Since the properties of nanonets are influenced by NW density, it is important to be able to control the density of nanonet. As the density of nanowires in nanonets is directly related to the number of nanowires in the suspension, the mastery of a technique of quantification of NWs is necessary. In Ternon's group, several techniques—such as Raman, infrared, fluorescence, and absorption spectroscopy—have been tested. Only the latter has made it possible to obtain a measurement that is directly proportional to the number of nanowires in the solution [28,36,150]. Then, for a given absorbance and a given NW geometry, the NN density is directly linked to the volume of the filtered suspension with high reproducibility. The greater the volume of filtered suspension, the greater the density in the nanonets (see Figure 16).

(1) dispersion   (2) Centrifugation   (3) Solution analysis   (4) Filtration under vacuum   (5) Transfer

Figure 15. Overview of the protocol for manufacturing nanonets. This process consists of five main steps: (**1**) dispersion of the silicon NWs in solution, (**2**) purification of the NW suspension by centrifugation, (**3**) analysis of the suspension by absorption spectroscopy, (**4**) assembly of the NWs into nanonets by vacuum filtration, and (**5**) transfer of the nanonet onto a substrate. Reproduced from [27].
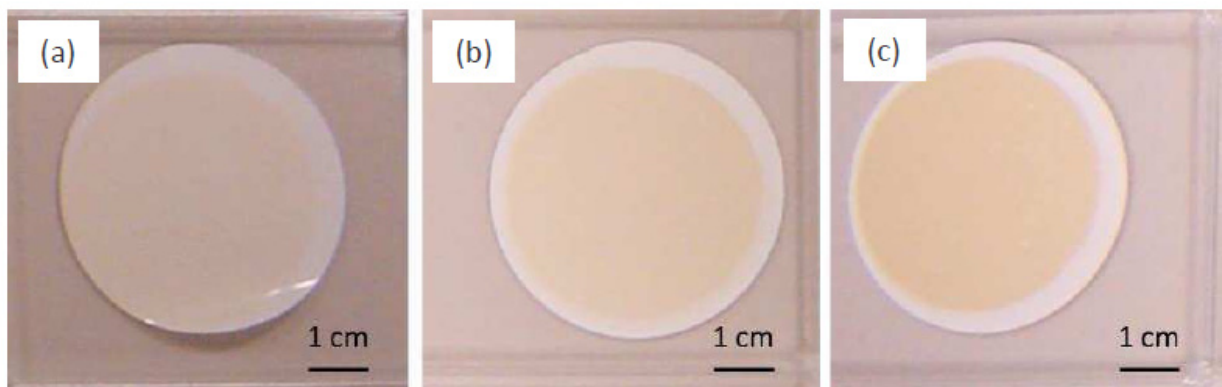
Figure 16. Membranes obtained after vacuum filtration of nanowires having the same arbitrarily fixed absorbance (0.06 at 400 nm) and different filtered volumes (**a**) 10 mL, (**b**) 20 mL, and (**c**) 35 mL. Reproduced from [28].

Once the nanowire solution has been analyzed, the silicon nanowires can be assembled by the filtration method with the schematic equipment in Figure 15 (step 4) [28,151,152]. The nanowire suspension is filtered for a few minutes through a nitrocellulose membrane. The progressive accumulation of the nanostructures on the filter surface decreases the flow velocity in these areas and induces an increase in flow in the areas devoid of nanostructures. These different flow velocities involved are at the origin of the self-assembly mechanism and the homogeneity of the nanonet.

When the nanowire suspension is not homogeneous—i.e., it contains aggregates from growth defects or clusters of NWs—it is possible to remove some of these elements by centrifugation as demonstrated by M. Legallais [27].

After filtration, NN can be transferred to the desired substrate either by the dissolution of the filter [148] or by direct contact [153]. For instance, Serre et al. [28] and Legallais et al. [27] demonstrated that this transfer can be carried out via a wet process by dissolving the membrane produced by vacuum filtration in an acetone bath. The adhesion of the nanonets to the surface of the substrates is simply due to van der Waals forces [27,28]. This process is well dedicated for SiNN [44,154] and can be adapted for a wide variety of nanostructures—such as NWs of zinc oxide [155], germanium [156], or carbon nanotubes (CNTs) [148,152]. Furthermore, the size of the nanonet is only conditioned by the size of the filter used and can therefore be easily enlarged. Finally, the formed nanonets can be

transferred onto different types of substrates either rigid or flexible, insulating or conductive, opaque or transparent, as shown in Figure 5, depending on the characterization and the intended application. Still, there is some difficulty such as finding a flexible substrate which is compatible with acetone.

Vacuum filtration is a low-temperature process in film production which affords films with some advantages such as surface uniformity and controllable thickness. Transferring NWs to a flexible substrate after being deposited on the filter depends on the substrate endurance towards acetone as most of the flexible substrates are attacked by it [27,157].

6.2.2. Spray Coating

One of the simple and efficient routes for the deposition of randomly dispersed nanowires or highly ordered and highly aligned even on a wide range of receiver substrates is spray coating. Spray coating is a technique in which nanowire suspension is electrostatically forced through a nozzle whereby a fine aerosol will be formed [158,159]. The spray coating system consisted of a hot plate for controlling the temperature of the substrate, a pressure flow spray nozzle element, a nozzle movement, and an angle control module. Normally, the spray coating system is designed by taking to account the viscosity of NW suspension, the NW suspension supply, and other process variables [158] (see Figure 17). Ossama Assad et al. [158] showed that by controlling these conditions and provided that the size of the generated droplet is comparable to the length of the single NW, the shear-driven elongation of the droplet results is likely in the alignment with the confined NW in the spraying direction.
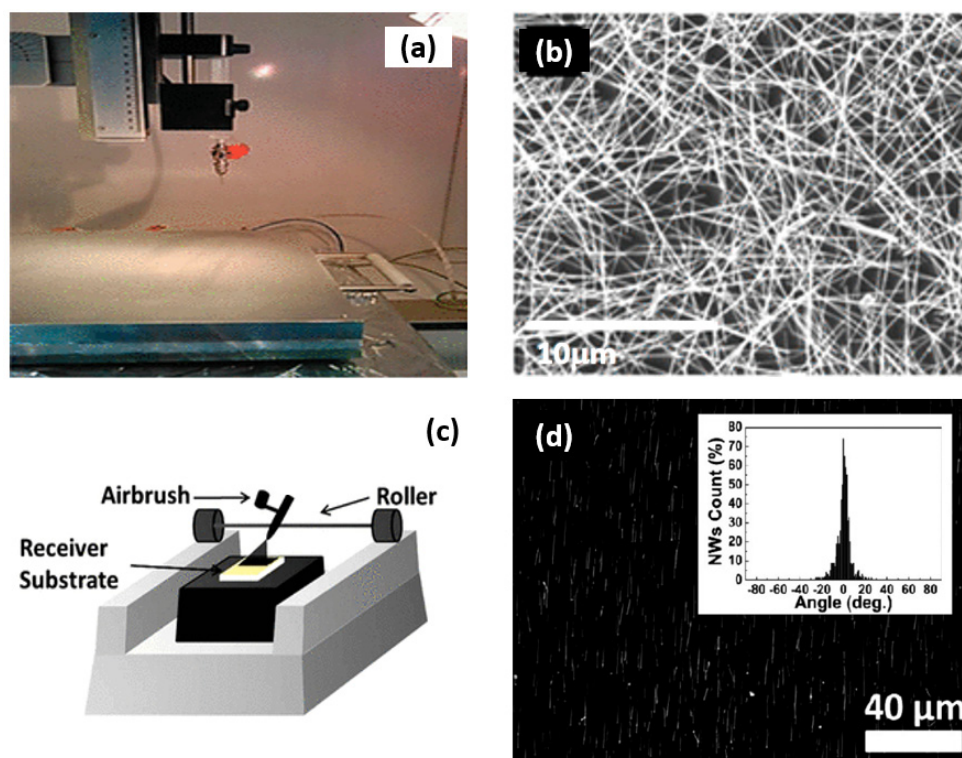
Figure 17. (**a**) Image of the electrostatic spray system step. Reproduced from [159]. (**b**) SEM image of the electrostatic spray deposited nanowire network. Reproduced from [159]. (**c**) Schematic of the spray coating apparatus. Reproduced from [158]. (**d**) representative dark-field optical image of spray-coated SiNWs on the SiO$_x$/Si substrate and the constituent analysis of 700 SiNWs with respect to the flow direction. Reproduced from [158]. Spray coating method can be controlled under conditions of temperature, droplet size, spray coating angle, and airflow which makes this method interesting either in the well-aligned or well controlled density in large size of nanonet with a small lack in control over the low density of nanonets.

Since this technique has no limitation in substrate size, it has great potential for large scale production and can replace spin-coating which is a conventional method [139]. However, the main concerns of utilizing the spray coating belong to higher film thickness and roughness.

As already mentioned, one of the key parameters in nanonet assembly is density. In spray coating, by controlling the concentration of the nanowire suspension or at the same time regulating the flow duration, it is possible to adjust the density of deposited NWs—e.g., for having high density deposited NWs, we should increase the spray coating duration. The level of density control over deposited NWs in this approach is similar to other techniques such as blown-bubble and contact transfer techniques, while in these two techniques we are dealing with just aligned nanowires.

Spray coating facilitates a low-cost uniform coverage over a large area which has a potential for immediate implementation in the industry and/or line production. In this technique, NWs film making by the spray coating method depends on the nozzle speed, diameter, and length of nanowires and is more beneficial for high densities and large-scale fabrication [158,159].

6.3. Advantages and Disadvantages of Each Technique

As already discussed, semiconductor NWs have demonstrated excellent performance for nanoscale electronics and due to their great mechanical flexibility, high yield, and low-cost bottom-up synthesis; they have outstanding potential to be used in flexible electronics. As the assembly of NWs remains a challenge for practical large-scale application, various innovative NW assembly technologies have been investigated [160]. As a result below in Table 2, there is a simple comparison between different techniques of transferring nanowires into a variety of substrates from rigid to flexible ones.

Table 2. Advantages and disadvantages of each NWs transferring technique.

Technique	NWs Uniformity	Random/ Aligned	Density (Percolation Regime)	NWs Layer Thickness (Low Density)	Versatile in Substrate	Scalability	Localized/ Large Scale	Complexity
Drop-casting	Low	Random/ Aligned	Low	Low	High	Low	Localized	Low
Fluidic directed	Medium	Aligned	Low	Low	Low	Low	Localized	Medium
Langmuir-Blodgett	High	Aligned	Medium	High	High	Medium	Localized/ Large scale	Medium
Blown-bubble	High	Aligned	Medium	Low	High	Low	Localized	
Contact printing	Medium	Aligned	Medium	Medium	Medium	Low	Localized	Medium
Vacuum filtration	High	Random	High	High	Medium	Medium	Large scale	Low
Spray coating	High	Random/ Aligned	Medium	Low	High	High	Large scale	Low

In order to fabricate devices based on a single SiNW, the best option in terms of simplicity and adaptability to varieties of substrates is drop-casting, but still this technique is not efficient and the number of devices out of each NW transfer is trivial and negligible. However, other techniques—such as Langmuir–Blodgett, blown-bubble, contact printing, and fluidic directed—are the best choices for multiple-parallel channel devices. Each technique has its advantages but still, Langmuir–Blodgett seems to be a better option over others. Finally, in order to have nanonet (assembly of randomly oriented nanowires), we deal with mostly two methods, vacuum filtration and spray coating in the other technique several transfer process in different angles are needed to produce arrays of nanowires with junctions so these latter methods are complex with low yield. Although in vacuum filtration technique, density regulation is much easier and the process is inexpensive, spray coating

can prevail over vacuum filtration because it is easily applicable on different substrates, at large scale, and it allows the selection of a random or aligned nanowire array.

Generally, though all these methods have an advantage over direct growth methods, these methods extend the assembly procedures, which increase the risk of additional contamination and destruction of the intrinsic properties.

7. Silicon Nanowire-Based Transistors

The small size and unprecedented ability to combine semiconductors with very different lattice parameters provide exciting new opportunities for devices. At the beginning of the 20th century, nanowire device researchers face the exciting challenge of deciding which devices, and thus which future applications, hold particular promise for this new class of material [161,162]. Among the many possibilities, the field effect transistor (FET) stands out as the modern workhorse of the semiconductor industry. Not surprisingly, most of the efforts in nanowire devices have focused on the fabrication of nanowire field effect transistors, as it is the building block of modern electronics and the most frequently fabricated device in history. FET is the dominant semiconductor device in digital and analog integrated circuits (ICs), and the most common power device [163]. It is a compact transistor that has been miniaturized and mass-produced for a wide range of applications.

Silicon transistor technology, especially metal–oxide–semiconductor (MOS) technology, is scaling down as predicted by Moore's Law [18,164]. Originally, transistors had a three-dimensional active region (solid silicon substrate) then it was reduced to a two-dimensional geometry (silicon ultra-thin film on insulator (SOI)) to finally reach a one-dimensional structure with the introduction of nanowires (FinFET on SOI) [165,166], as schematically illustrated in Figure 18.
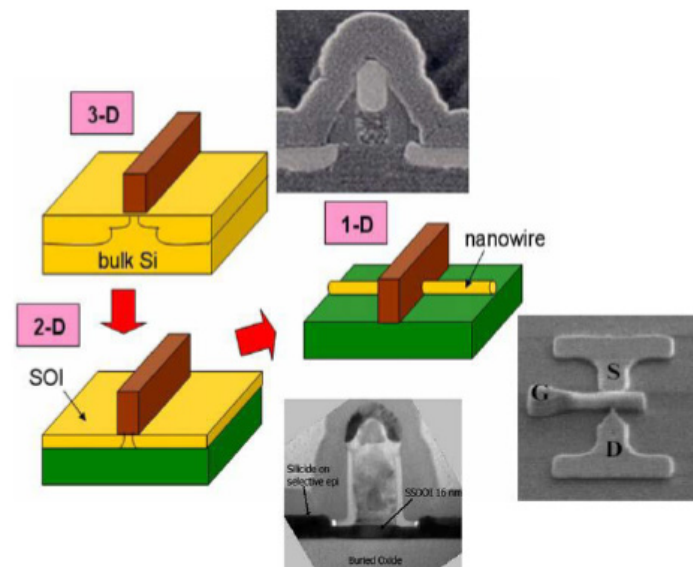

Figure 18. Continued scaling of silicon complementary metal–oxide–semiconductor (CMOS) transistor into nanometer regime requires the corresponding reduction in device active layer dimensionality. Reproduced from [6].

However, this scaling of the typical silicon transistor technology has almost reached its limits [22,51]. Despite the advanced capabilities of fabrication tools, many physical effects can prevent the tools from performing satisfactorily when the device size is scaled down to the nanoscale. In addition, transistor scalability, performance, and power dissipation are three fundamental issues facing aggressive miniaturization. Furthermore, the leakage mechanisms associated with the size reduction of conventional silicon transistors down to the nanoscale include direct gate dielectric tunneling, band-to-band tunneling, and short channel effects. Finally, silicon has almost reached its intrinsic switching speed limit. Other semiconducting materials with higher carrier mobility could solve the problem,

but the required power dissipation levels in the nanoscale structure do not allow further downscaling [6].

Nevertheless, one-dimensional (1D) structures are the smallest structures that can be used for efficient transport of electrons [6,61,167]. Semiconductor nanowires fall into this category and are obvious candidates to replace ultrathin-film SOI transistors [168]. Among semiconductor NWs, silicon nanowires have been studied more and are considered the most suitable for implementing nanowire transistors, as silicon dominates the semiconductor industry and its structure and doping can be precisely controlled [168]. However, the smaller the footprint of the manufactured devices, the higher the manufacturing cost and the more complicated it is to observe good reproducibility and homogeneity of the device characteristics. Nevertheless, being able to introduce nanometric structures into the devices is extremely interesting because it allows new properties and functionalities to emerge. In this, nanonet devices are extremely promising because they are made of nano components while having a large enough footprint to lower the cost and complexity of production. They are clearly not part of the miniaturization dynamics of the 'More Moore' trend, but rather contribute to the 'More-than-Moore' trend or even to a paradigm shift (Figure 19a).
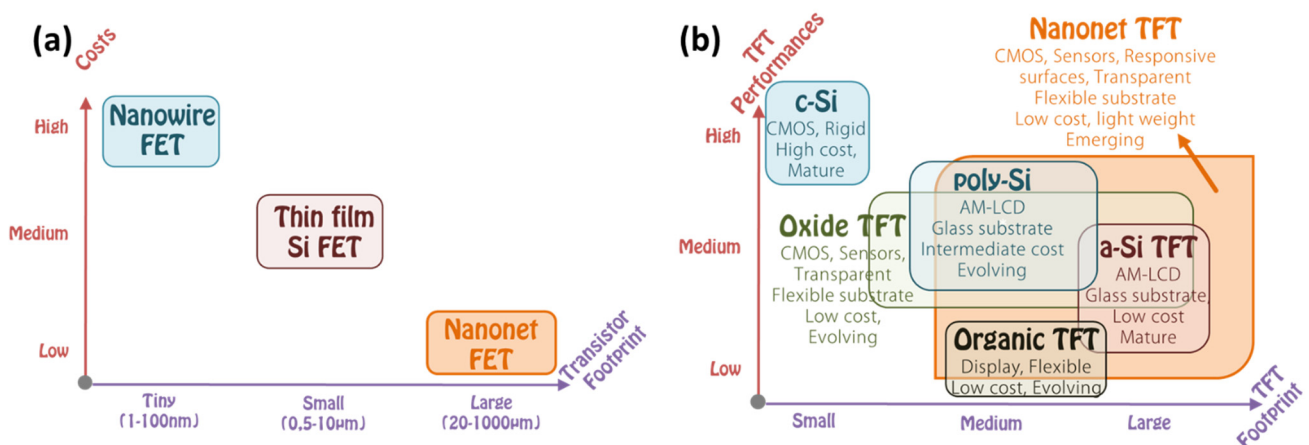
Figure 19. (**a**) Simple comparison between single SiNW-, thin film Si- and SiNN-FETs with respect to the industrial size and fabrication costs related. (**b**) Positioning (Nanonet TFT) in terms of thin-film transistor (TFT) performance versus footprint in comparison with the existing technologies (TFT based on: cSi: monocrystalline Si; poly-Si: polycrystalline Si; a-Si: amorphous Si; Organic: organic material; Oxide: metal oxide film).

Nanonet based transistors belong to the category of thin film transistors that provide numerous functionalities for various applications such as CMOS circuits, sensors, responsive surfaces, and flexible and transparent electronics. They compete not only with other materials such as oxides or organics but also with other forms of silicon, amorphous, polycrystalline, or monocrystalline. In this context, Figure 19b shows the performance of these devices according to their footprint.

In this section, we focus on nanowire transistors with the simplest geometry—namely, a source electrode, a drain electrode, a channel consisting of a single nanowire, parallel nanowires, or a nanonet, as well as a full back gate or localized top-gate. Thus, we will present the most basic integration processes and then the typical electrical characteristics.

7.1. Integration Process

7.1.1. Single Nanowire FETs (Single-SiNW-FETs)

Whether the approach is bottom-up or top-down, there is a phenomenal variety of integration processes and device geometries in the literature. There is a large number of studies presenting the fabrication of transistors with the simplest geometry, which we will describe in the rest of this paragraph [10,11,169], to the most complex transistors with variable doping along the nanowires and gate multiplicity allowing an electrostatic control

of the doping and thus the control of the nature of the channel (P or N) [170,171]. Even for the simplest geometry, there are integration subtleties that impact the properties of the manufactured transistor. A simple silicon nanowire transistor can be built as shown in Figure 20a. The two gold cubes represent the source (labeled S) and drain (labeled D) contacts of the transistor respectively whereas the gate is on the backside of the substrate. The dark blue cylinder represents the nanowire which is the channel of the transistor. The channel can be doped p-type or n-type. The top-gate of the transistor is shown in Figure 20b,c as a rectangular-like plate labeled with G. The gate can be placed in a semi-cylindrical shape on the top of the nanowire or all around the nanowire [168]. SiNW transistors manufactured with a gate that surrounds the whole nanowire (all-around-gate) allow better current control through the channel and thus higher current densities can be controlled compared to a planar device. What is more, the all-around-gate allows the devices to be shrunk even more (down to 10 nm) due to the excellent control of short-channel effects and leakage [51].
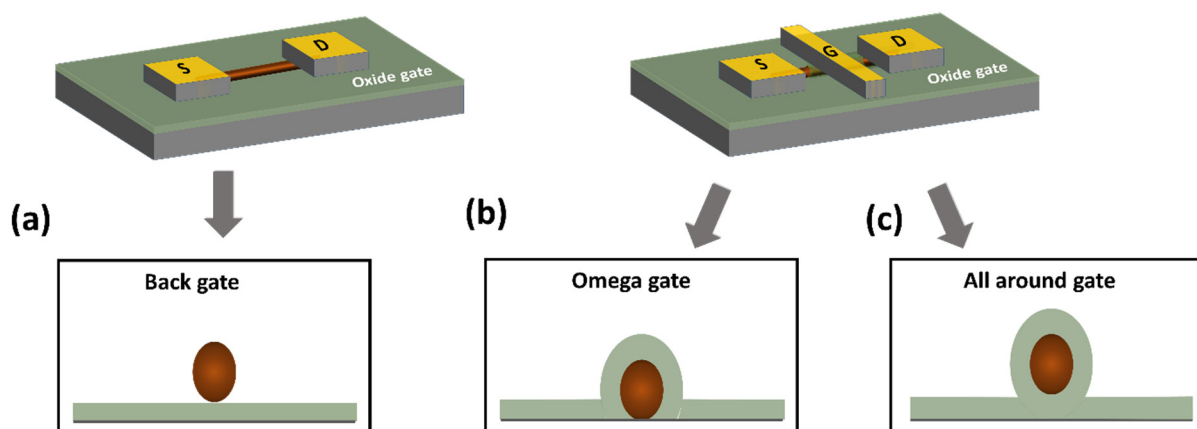

Figure 20. Schematic of NWFETS with (**a**) back gate, (**b**) semi-cylindrical top gate, and (**c**) cylindrical gate-all-around configurations. The nanowire is brown, gate-dielectric is light green, and source (S), drain (D), and top-gate (G) electrodes are gold. Insets show device cross section at the midpoint between source and drain.

The bottom-up approach, which is the subject of this paper, has caught our attention because it provides great flexibility in that nanowire growth and integration are two completely independent steps. Thus, it is easy to choose the material, length, diameter, type, and concentration of the dopants, and the orientation of the crystals because all these parameters can be adjusted during the synthesis. Today, the main limitation of this approach is the complexity of developing a method for large-scale transistor integration with high reproducibility.

For the simplest geometry (Figure 20a), the bottom-up processes start with as-grown SiNWs in both bottom-up (Figure 21i) as described in Section 5. Subsequently, the as-synthesized SiNWs have to be transferred onto the desired substrate, generally including the back-gate, by using the simple drop-casting or one of the methods described in Section 6 (Figure 21ii). In some works, SiNWs are passivated in order to preserve them from the environment sensibility, low efficiency, and short lifetime [27,172,173]. Thereafter, a photo- or electron-beam lithography process (Figure 21iii) followed by metallization (Figure 21iv) and lift-off (Figure 21v) are utilized to pattern metallic electrodes to the SiNWs [3,169,174]. Silicidation which is a process of the intermetallic compound formed by the reaction of metal and silicon can be performed in order to lower the access and/or series resistance of the device in contacts [11,175,176]. Eventually if desired, a top-gate can be added by an additional photolithography step.
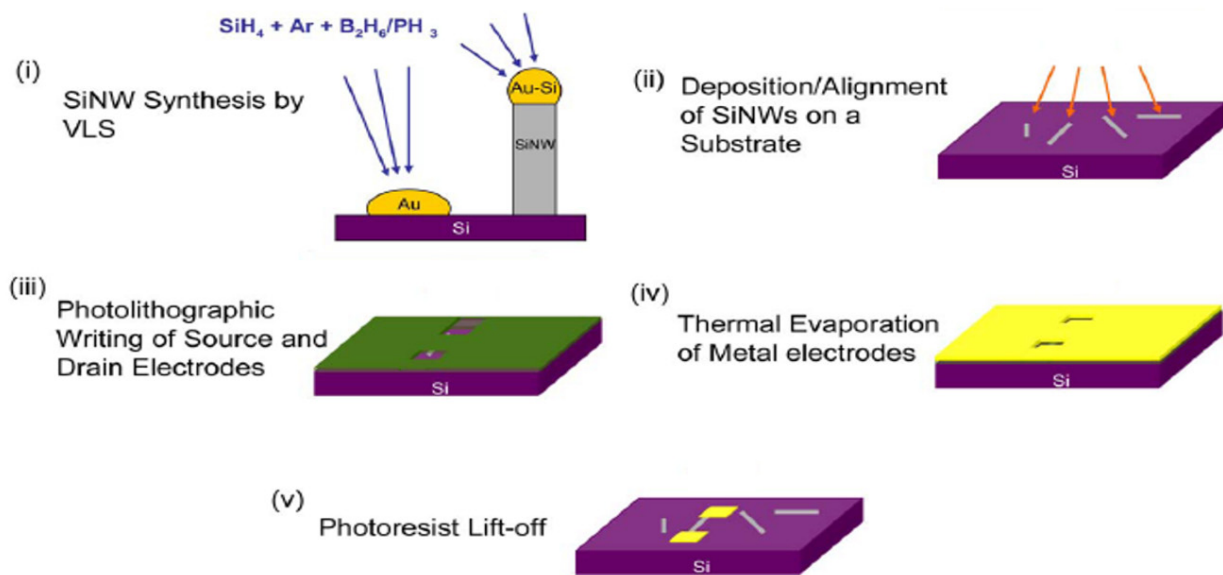
Figure 21. (**i**) The growth of SiNWs in CVD reaction via the VLS mechanism. (**ii**) Deposition/alignment of SiNWs on a silicon substrate. (**iii**) A photomask pattern to define source/drain electrodes. (**iv**) Thermal evaporation to deposit the source/drain contacts. (**v**) Lift-off the remaining photoresist with Remover PG. Adapted from [174].

Generally, this type of integration process, based on drop-casting, yields only a low success rate in obtaining nanowire devices without allowing large statistical studies. However, this is sufficient to study the fundamental properties of single SiNW devices. Furthermore, this method is clearly not suitable for the low-cost, mass production of SiNW devices. Therefore, the use of the techniques described in Section 6 that allow the assembly of SiNWs with controlled orientation and spacing over large areas is essential for the fabrication of complex logic circuits and high-performance devices.

7.1.2. Silicon Nanonet FETs (SiNN-FETs)

To qualify as a nanonet device, the geometry of the transistor must be such that the length of the channel is greater than the length of the nanowires so that no nanowires are able to bridge the two electrodes directly. The current flows from one contact (source) to another (drain) via percolation paths that involve NWs as well as junctions between NWs. Typical devices are illustrated in Figure 22.
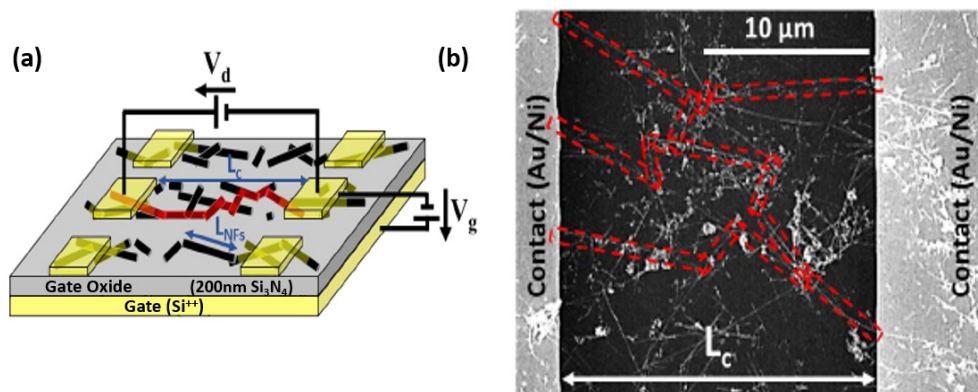
Figure 22. (**a**) Schematic and (**b**) SEM image of SiNN transistor studied. The schematic (**a**) refers to long channel transistors for which the length of the NWs (L_{NFs}) is less than the channel length (L_c). Conversely, the SEM image (**b**) refers to the possible conduction paths involving NW–NW junctions are indicated in red. Reproduced from [27].

Thus, the fabrication starts with the assembly of the nanonets on the surface of the substrate including the back gate according to one of the methods described in Section 6. Then the fabrication process of back-gated SiNN-FETs can be broken down into four main steps:

- Sintering of the NW–NW junctions and passivation of the NN to stabilize electrical properties (see Section 8.1 Sintering and Section 8.2 Surface and Interface).
- NN patterning to define the channel geometry (Figure 23i-0–i-5).
- Deposition of the source/drain contacts (Figure 23ii-0-ii-5).
- Silicidation of the source/drain contacts (see Section 8.3 Silicidation).
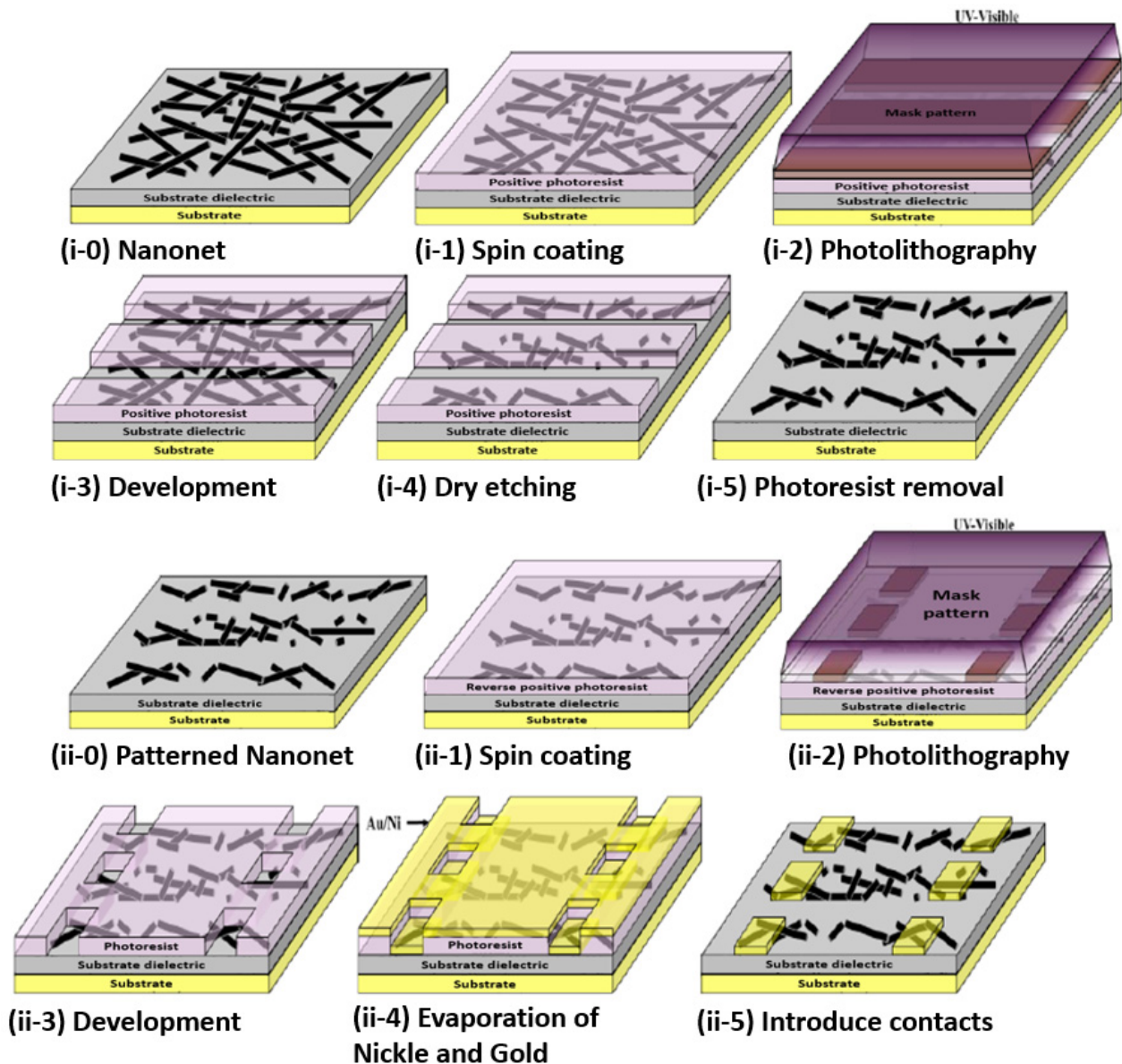
Figure 23. Main steps in the isolation of nanonets. (**i-0**) Fabrication of nanonets. (**i-1**) Deposition of the positive photoresist by the spin-coating technique. (**i-2**) Photolithography with the UV–visible through the mask. (**i-3**) Photoresist development. (**i-4**) Dry etching of the NWs by a sulfur hexafluoride plasma. (**i-5**) Photoresist removal. Main steps for the formation of source/drain contacts. (**ii-0**) Nanonet after isolation. (**ii-1**) Deposition of inversion photoresist using the spin-coating technique. (**ii-2**) Photolithography in the UV–visible through the mask aligned with the isolated nanonet. (**ii-3**) Photoresist development. (**ii-4**) Electron beam evaporation of nickel and gold. (**ii-5**) Revelation of the source/drain contacts after lifting of the photoresist (lift-off).

By doing the silicidation step, back-gate SiNN-based FETs are achieved. These steps can be modified due to the need and application. For example, one might need a local top-gate instead of a full back-gate hence some procedures will be added such as deposition of the gate oxide, lithography of top-gate, and metal evaporation step to introduce top-gate. In Figure 24, SiNN-based FETs with two different designs are demonstrated.
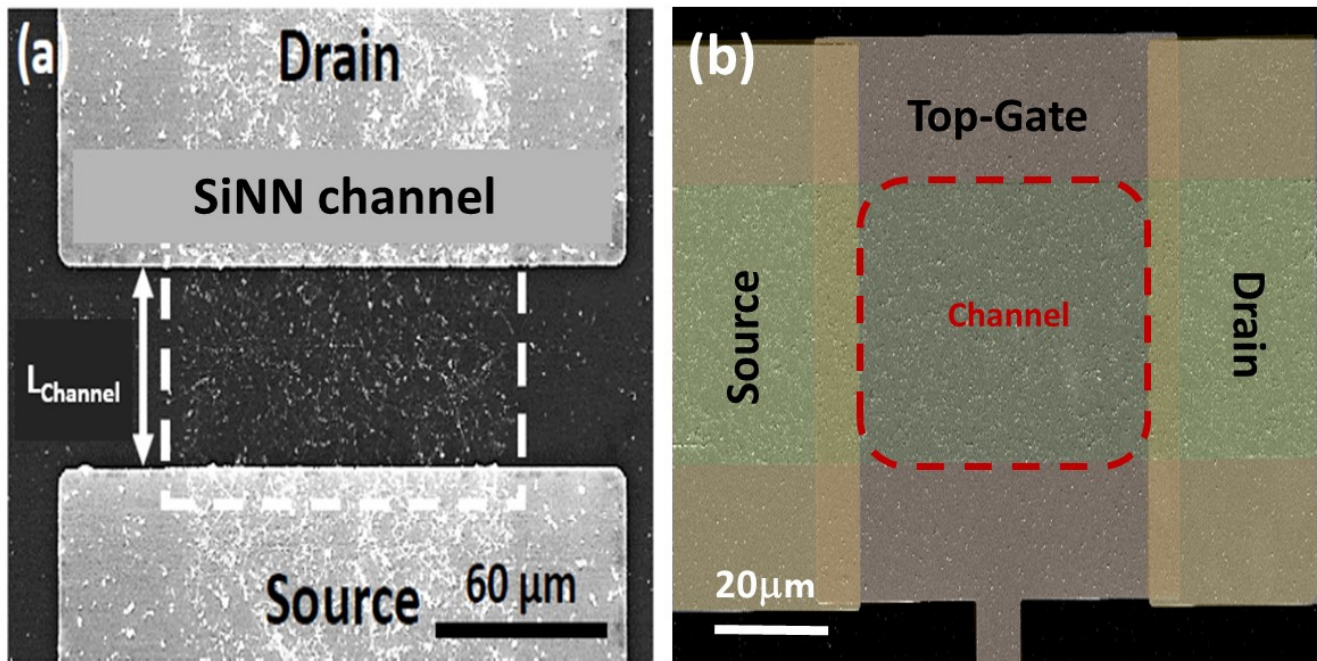

Figure 24. (**a**) SEM image final full back-gate FET based on SiNN. The length of the Si nanonet channel is 50 μm for a width of 120 μm. The square contacts measure 200 μm on each side. (**b**) SEM image final local top-gate FET based on SiNN. The length of the Si nanonet channel is 50 μm for a width of 100 μm. The square contacts measure 200 μm on each side. Although this integration process involves only simple and mastered steps, such integration has proven to be challenging since, to date, very few papers have presented the fabrication of this type of device. Moreover, to date, there are works based on the SiNN devices on rigid substrates, especially resistors and transistors but there is a great potential in the field of flexibility that is still unproven.

7.1.3. Multiple-Parallel-Channel FETs (MPC-FETs)

The realization of a multiple-parallel-channel field effect transistor (in reference to multiple parallel NWs as channels) can arise from two strategies. First, by choosing an appropriate technique (Section 6), it is possible to align nanowires parallel to each other and then apply the integration process presented for single nanowire transistors which will then result in an MPC FET since the channel will consist of nanowires in parallel (Figure 25a,b). The second strategy consists in producing a nanonet on the surface of the substrate and then applying the dedicated integration technique while choosing a geometry such that the length of the channel is smaller than the length of the NWs. As a consequence, several NWs are able to bridge the two electrodes, forming an MPC-FET (Figure 25c,d).
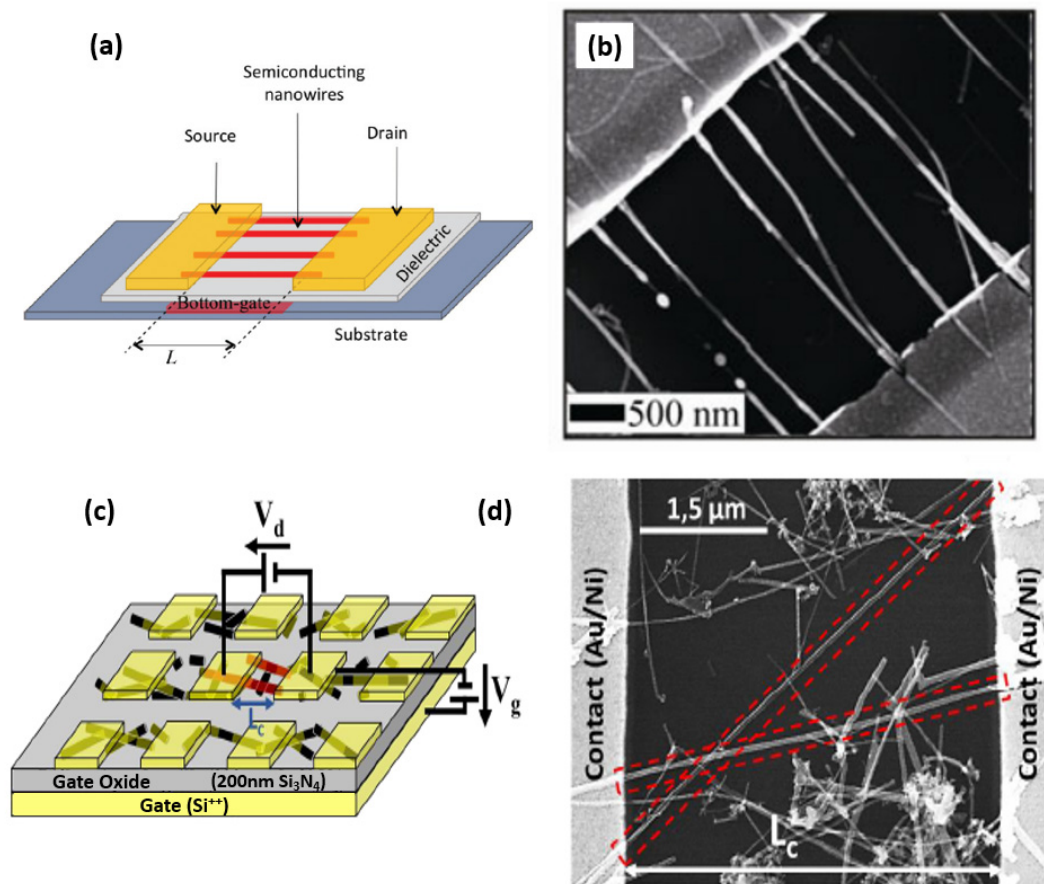
Figure 25. (**a**) Schematics of bottom-gate of multi parallel array silicon nanowires. Reproduced from [177] (**b**) SEM image of as fabricated parallel channels FETs with intruded NiSi$_2$ Schottky barrier contacts. Reproduced from [178]. (**c**) Refer to the schematic of the short channel transistor (Nanowire length higher than channel length) (**d**) SEM image of MPC-FETs based on short-channel SiNN and the possible conduction paths involving with without-NW–NW junctions are indicated in red. Reproduced from [27].

### 7.2. Electrical Characteristics of Single SiNW-, SiMPC-, and SiNN-FETs

The operation of a single SiNW-based transistor is similar to that of a typical FET transistor. If the SiNWs are p-type and a positive/negative voltage is applied to the gate (G), then the carriers are depleted/accumulated; conversely, if the SiNWs are n-type and positive/negative voltage is applied to the gate, then the carriers are accumulated/depleted (Figure 26). Therefore, the variation of the SiNW conductance via the field-effect action allows for the transistor action to be implemented with SiNWs [17,31].

P-type SiNWs have attracted greater interest than n-type ones. P-type SiNWs were fabricated and showed high performance characteristics. Their transconductance was about 10 times greater than typical planar devices and the holes' mobility was an order of magnitude larger too. Both the transconductance and mobility increased after surface modification of the SiNW. This implies that some of the electrical characteristics of the SiNW transistors can be controlled by proper surface modification as described in the next section. Therefore, the performance of SiNW transistors can exceed that of typical devices [51].
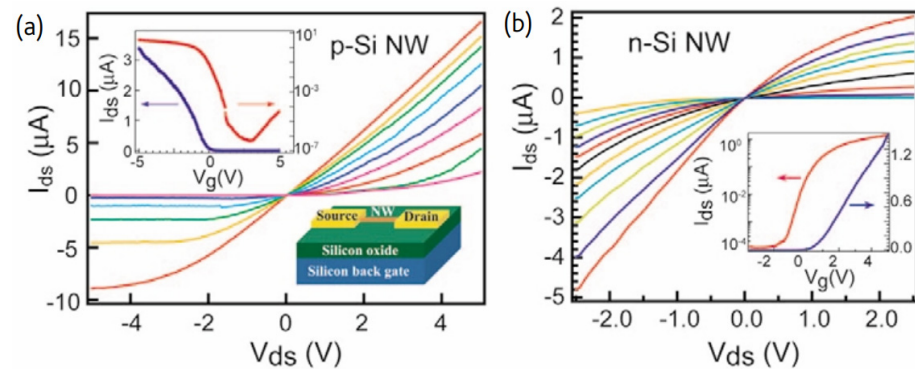
Figure 26. SiNW-FETs: a family of current versus drain-source voltage (I_{ds}-V_{ds}) plots for a representative (**a**) 20 nm p-Si NW device (channel length of 1 μm; from red to pink, V_g = −5 V to 3 V); and (**b**) 20 nm n-Si NW device (channel length of 2 μm; from yellow to red, V_g = −5 V to 5 V) in a standard back-gated NW-FET geometry as illustrated. Insets in (**a**,**b**) are current versus gate–voltage (I_{ds}-V_g) curves recorded for NWFETs plotted on linear (blue) and log (red) scales at V_{ds} = −1 V and 1 V, respectively. Reproduced from [31].

In addition, one of the major gains in 1D nanostructures is depletion or accumulation in the bulk of nanowires while in 2D structures such as thin film is happening only on the surface which causes lateral current shunting. This property provides sensing with label-free and direct detection when the nanowire is used as a sensor to make real-time detection possible [22,61]. Based on this advantage in nanowires, Li et al. [75] depicted an efficient strategy through surface functionalization to build a single silicon nanowire field-effect transistor-based biosensor that is capable of directly detecting protein adsorption/desorption at the single-event level (see Figure 27).
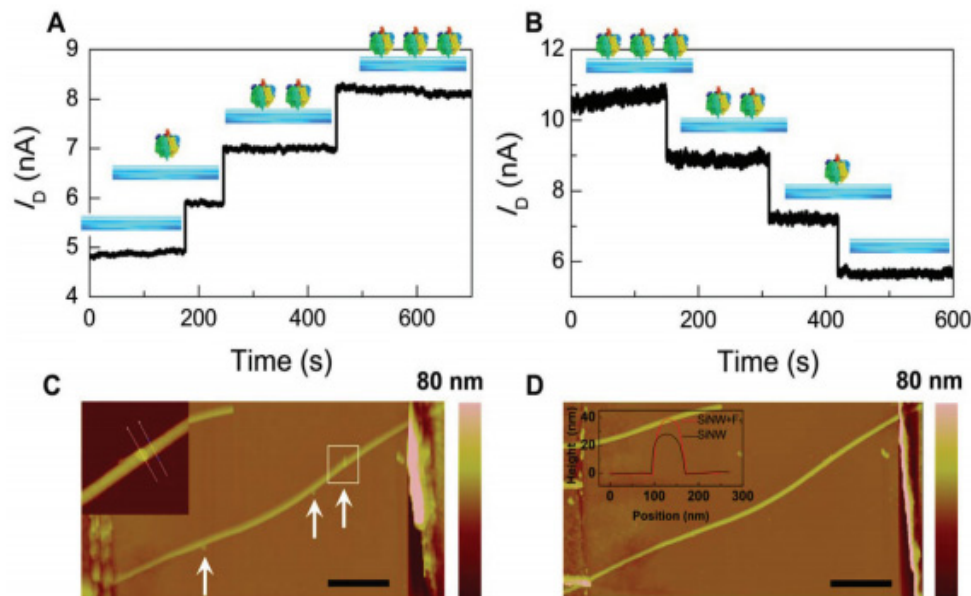
Figure 27. Sensing properties. (**A**,**B**) Real-time recordings of the absorption/desorption processes of F1-ATPases, showing the gradual changes in ID with three steps. Drain voltage, V_D = 0.1 V and gate voltage, V_G = 0 V. (**C**,**D**) Corresponding AFM images after protein delivery ((**C**), inset shows an enlarged image of a single F1 protein) and after further EDTA treatment ((**D**) inset is the height profile of the bare silicon nanowire and the nanowire with an adsorbed F1 protein particle in (**C**) inset. The total height of F1 is ~12 nm including a ~2 nm linkage). The scale bar is 1 μm. Reproduced from [75].

As will be discussed in the following section, the contact resistance of SiNW-FETs affects their performance significantly. Devices with titanium (Ti) source-drain contacts

revealed variations in their transconductance and mobility after thermal annealing effects. Other materials for the contacts, such as silicide and nickel monosilicide, can reduce this variation in the performance of the device [11,51].

That is why the MPC-FETs and NN-FETs are particularly interesting, as they can maintain the nanosize of the components while increasing the amount of current for a given voltage [178].

In the case of MPC-FETs, fabricated from aligned parallel NWs, Figure 28 depicts the off-current as a function of the on-current for different inter-electrode (IE) spacing (2.5–5.5 μm). It can be seen that the current output can clearly exceed the μA range and that it increases when the inter-electrode (IE) spacing is reduced. However, the off-current increases when the on-current increases, and accordingly, the on/off current ratio drops with decreasing IE spacing. Since channel length (L_c) of individual nanowires varies in the parallel array due to dispersion in nanowire alignment as shown in Figure 28b, though a small number of nanowires with short channels will be found in the ensemble, affected by quasi short channel effect (SCE), these nanowires will degrade the total on/off current ratio. This apparent quasi short channel effect for parallel array devices at such a large electrode spacing is not observed for single nanowires [178].
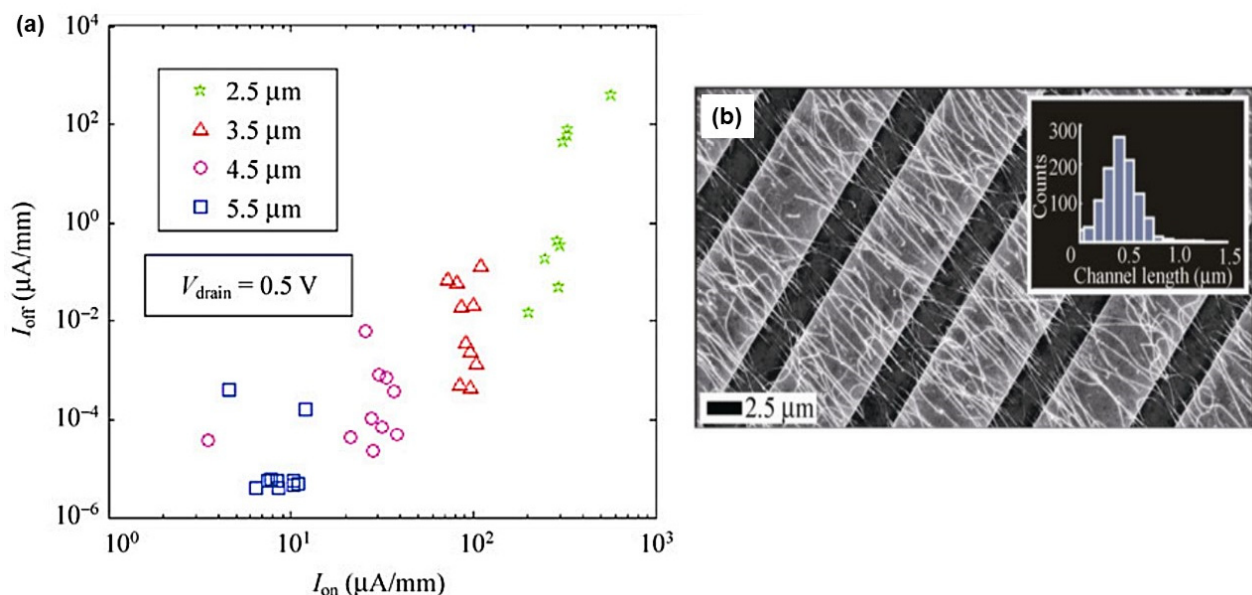

Figure 28. (**a**) Source-drain voltage V_{sd} versus a gate voltage V_g statistics of 36 nanowire parallel array FET devices. Each device consists of 500–1000 nanowires. Off-current versus on-current per mm electrode width for $V_{sd} = 0.5$ V. The on/off ratio is shown for devices with four different inter-electrode spacing but the same silicidation process (green/stars 2.5 μm; red/triangles 3.5 μm; purple/circles 4.5 μm; blue/sq. 5.5 μm). Reproduced from [178]. (**b**) High density nanowires are contacted by nickel electrodes. The inset displays the histogram of channel lengths of individual nanowires after silicidation for a device with 2.5 μm inter-electrode spacing. Reproduced from [178].

When MPC-FETs are obtained from a randomly oriented nanowire network, the same trend is observed: by decreasing the channel length, the on and off current increase (Figure 29A,B, 5 and 10 μm). Moreover, from this figure, one can notice a surprising and significant degradation of the subthreshold swing.

Then MPC-FETs are interesting to increase the on-current, but at the same time, off-current also increases and the commutation ability degrades. Such behavior can be explained by the intrinsic disparity of the nanowire population. Indeed, whatever the method of bottom-up synthesis of NWs, it is possible to observe variations of diameters, doping, or surface properties from one nanowire to another. Such variations are responsible for different electrical behaviors for each NW. Thus, there is a dispersion of on-current, off-current, sub-threshold slope, and threshold voltages [179,180]. While this is not a major

problem for the on-current, the existence of a single nanowire with a high off current will result in a high off current for the MPC FET. Similarly, if all of the nanowires making up the MPC-FET switch successively, this will result in the MPC FET switching over a wide range of gate voltages [72].
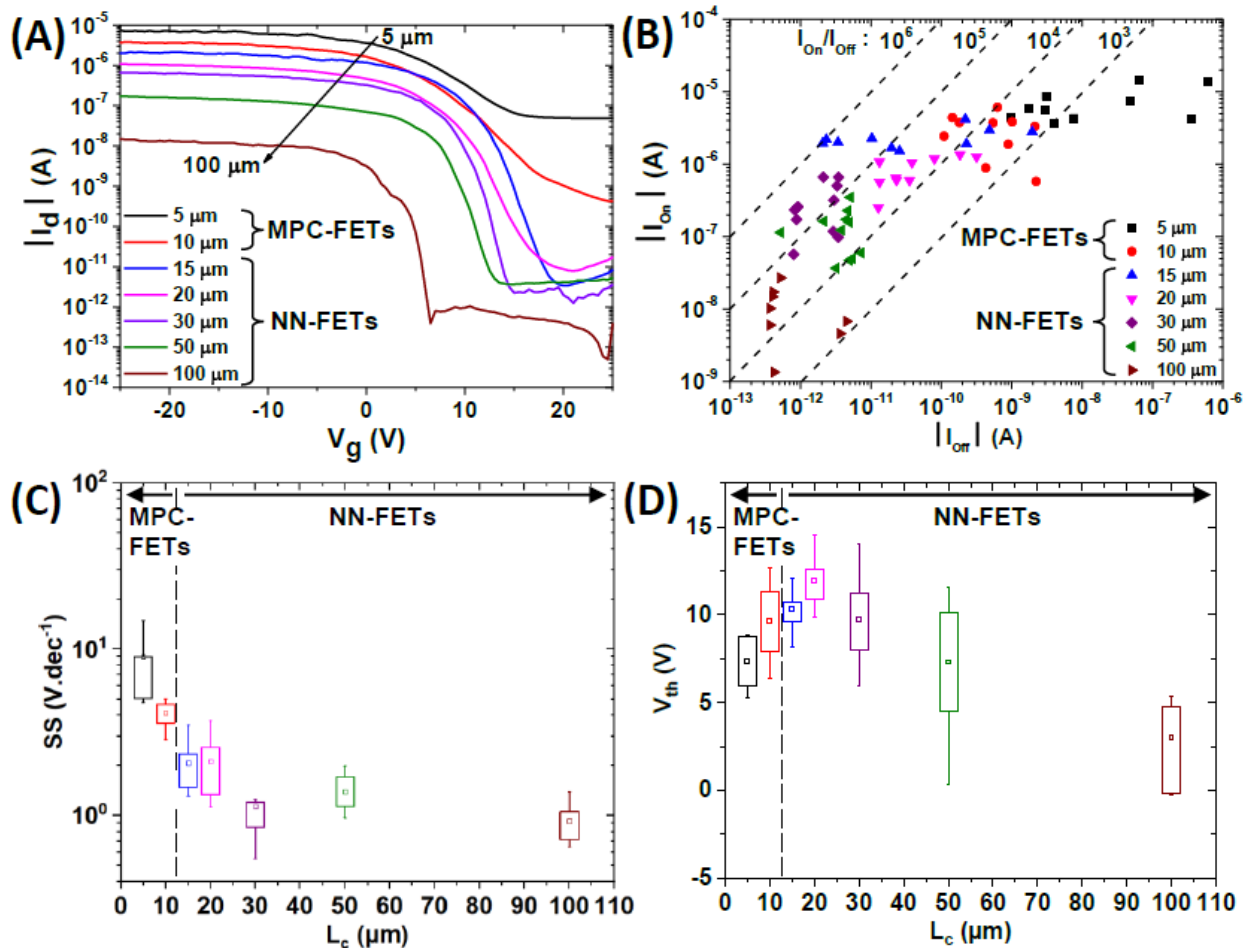

Figure 29. Study of transistor electrical properties for various channel lengths. (**A**) Typical transfer characteristics from 5 to 100 µm at $V_d = -4$ V. (**B**) On current (I_{on}) as a function of off current (I_{off}). The on current is defined as I_d at $V_g = -25$ V, $V_d = -4$ V, (**C**) subthreshold slope (SS), and (**D**) threshold voltage (V_{th}) for various channel lengths extracted for about seventy transistors. For (**B**) the on-to-off ratio (I_{on}/I_{off}) is indicated by the dashed lines. Reproduced from [72].

In this context, NN-FETs appear to be promising for reconciling high current, high I_{on}/I_{off} ratio, and fast switching, as illustrated in Figure 29 (15–100 µm). In Figure 29B, by measuring over 70 NN-based transistors with different channel lengths, an interesting trend in the I_{on}/I_{off} curve is observed. On one hand, the NN-FETs with the smallest length (15–20 µm) have a quite dispersed current while the current is almost stable. On the other hand, for the longer (>20 µm), current is almost fixed with a reduction in current by increasing the channel length. As a consequence, this leads to a drastic change in the on-to-off ratio and the observation of an optimum on-to-off ratio as high as 10^5 [72].

In order to have a better understanding of the differences inherent to these three types of nanowire-based devices, Figure 30 presents the transfer characteristics of a single-SiNW FET, an MPC FET, and an NN FET. All previous observations are summarized on that graph. The MPC-FET clearly exhibits the highest on-current, but all other transistor parameters are poor. In contrast, and against all expectations, the NN FET maintains very good performance with fast switching and very low off-current while exhibiting an on-current up to 100 times higher than that of the single nanowire device, even though its

channel is over 10 times longer. As a consequence, an NN-FET could be as interesting, and even more than a single SiNW-FET.
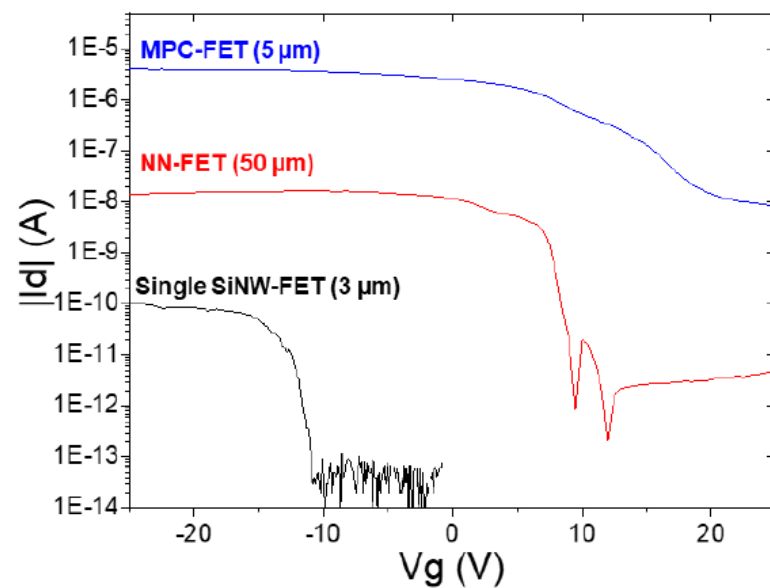
Figure 30. Typical transfer characteristic at $V_d = -1$ V for single SiNW-FET with $L_c = 3$ μm (black), MPC-FET with $L_c = 5$ μm (blue), SiNN-FET with $L_c = 50$ μm (red). Reproduced from [72].

The statistical summary in Figure 31 presents a comparison between the performance, in terms of I_{on}/I_{off} ratio and subthreshold slope, of single SiNW FETs from the literature and SiNN as a function of channel length. It is important to mention that, for SiNN based transistors, each point on the graph results from measuring the performances of several devices (average and variability): on the order of 15 devices for channel lengths below 300 μm and 3 to 6 devices for longer ones.
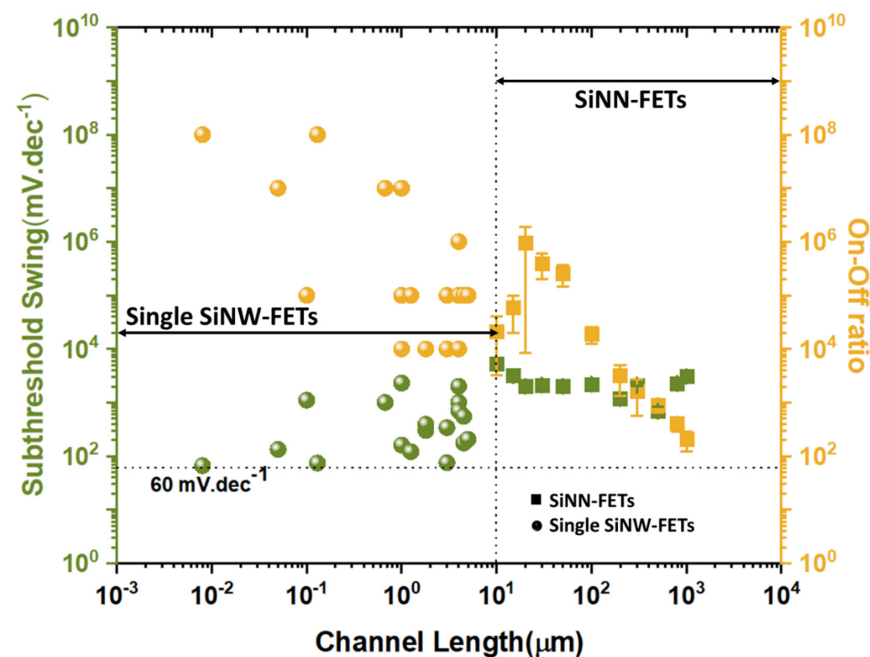
Figure 31. A comparison between single SiNW-FETs [11,33,175,181–190] and SiNN-FETs with respect to the channel length (SiNN density is about 0.6 NWs μm^{-2}). Squares of SiNN-FETs segment show the average of several devices' performances in which bars are representative of deviation in measured parameters for a certain L_c.

Such a graph clearly shows that single-nanowire devices exhibit highly dispersed performance, even for a given channel length, while NN devices show much lower dispersion.

In conclusion, despite having lots of resistive junctions, SiNN based devices have good performance. Then the NW/NW junctions, which might initially appear to be a weakness of this type of system, are in fact an asset that allow good performance, good reproducibility, and high fault tolerance.

## 8. Technological Key Elements for SiNW-Based Device Integration

8.1. Sintering

When silicon is exposed to air, silicon dioxide (SiO_2)—commonly known as native oxide—is systematically formed on its surface. This oxidation is self-limiting at ambient temperature and the SiO_2 formed stops growing once it has reached a certain thickness of a few nanometers. According to high-resolution transmission electron microscopy (HRTEM) analyses, the NWs are covered with about 2 nm native oxide [28]. With a permittivity dielectric of 3.9, the silica layer—of amorphous structure—has good electrical insulating properties. The native thickness formed around the NWs is sufficient to inhibit the possible conduction by tunneling from one NW to another and makes it impossible to fabricate percolating devices with SiNNs [42]. Subsequently, Pauline Serre showed that in the absence of oxide, current can flow from one nanowire to the other via the junctions [39]. To do this, she studied the behavior of resistors based on NNs. Thus, as long as the devices are stored under nitrogen after deoxidation by hydrofluoric acid (HF) treatment, significant conduction is observed across the resistor. As soon as they are exposed to air, conductance decreases exponentially with air exposure time due to the progressive reoxidation of the NWs as shown in Figure 32a. Such a decrease in current observed in Figure 32a is explained by the progressive growth of SiO_2 at the junctions between NWs as indicated by the passage from step (1) to (1.a) in Figure 32b. With a time constant of 2.2 days, the silica shell formed is thick enough to electrically isolate the NW–NW junctions and prevent current flow through the nanonet. The use of the SiNNs is then jeopardized as a functional device under air. Nevertheless, when low-temperature annealing (400 °C) is performed just after removal of SiO_2 by treatment with hydrofluoric acid (HF), the conductance shown in Figure 32a decreases by only 20% and then stabilizes for several months [48].
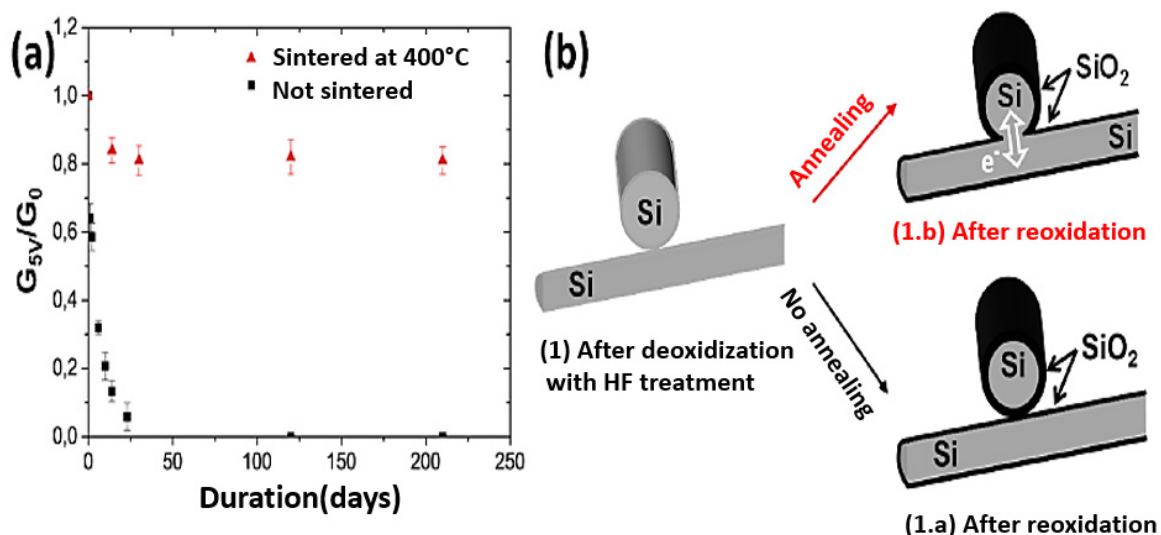
Figure 32. (**a**) Evolution of the conductance over time of Si nanonets based on not-annealed degenerated NWs and annealed at 400 °C after deoxidation. The conductance at 5 V was normalized to the initial conductance just after deoxidation. (**b**) Diagrams illustrating, after deoxidation, the reoxidation under air of an NW–NW junction (1.a) without annealing or (1.b) with annealing at 400 °C under nitrogen. Reproduced from [27].

HRTEM analysis, presented in Figure 33a.1 with its equivalent diagram (a.2), reveals the presence of a neck at the junction between two NWs. On this micrograph, the visible dislocation shows a continuity of crystalline planes between the two NWs. This crystal lattice continuity explains the stabilization of the current observed in Figure 32a even after several months of exposure to air. The 20% decrease in current after a few days is explained by the progressive reduction of the neck by the growth of the native oxide. However, when the reoxidation stops for a SiO_2 thickness of about 2 nm, the neck size stabilizes and the current is then constant even under air (Figure 32b, step (1.b)).
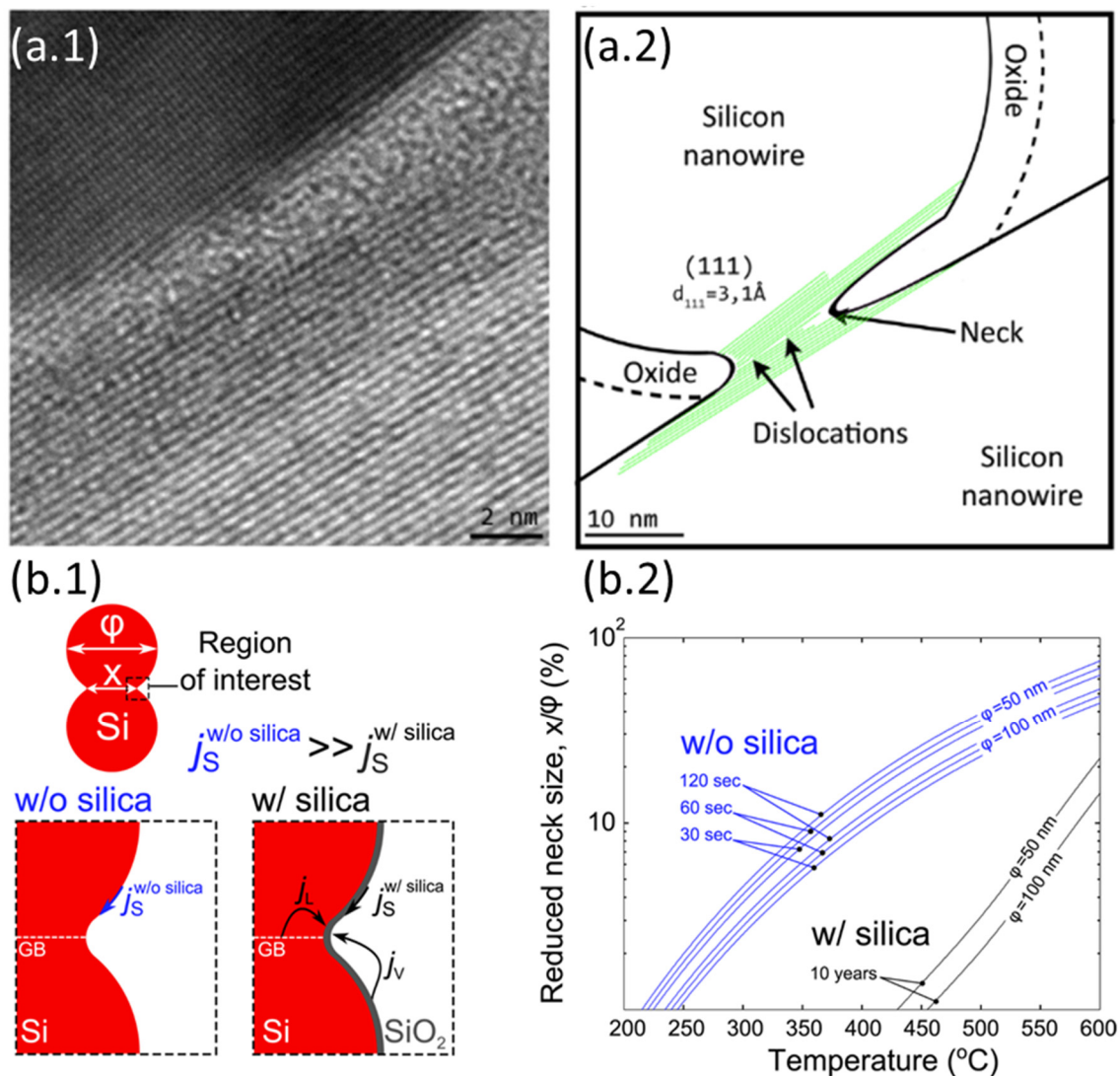
Figure 33. (**a.1**) High-resolution TEM image realized after re-oxidation of a junction between two NWs annealed at 400 °C under nitrogen. (**a.2**) Schematic representation of the TEM image showing the formation of a dislocation and a neck delimited by SiO_2 at the NW–NW junction. (**b.1**) Modeling of the sintering between two silicon nanoparticles with (w/) and without (w/o) the native oxide. Surface diffusion (j_s), volume diffusion from the grain boundary (j_L), and vapor diffusion (j_v) are the material transports considered. X and φ represent the shot size and diameter of the nanoparticles, respectively. (**b.2**) Sintering map representing the neck size relative to the initial nanoparticle size as a function of temperature for different annealing times. Reproduced from [48].

8.2. Surface and Interfaces

8.2.1. Modulation Thanks to Interface Surrounding the Channel

The quality of the interface surrounding the channel is a key parameter for all electronic devices such as FETs as it influences many parameters, from high to low frequency noise [191,192]. For example, a mechanism for filling or emptying traps at the NW/oxide interface leads to a memory effect as this gate dependency could compromise the operation of the transistor. According to the literature, the most commonly used oxides for passivation of silicon nanowires are silicon oxide (SiO_2), aluminium oxide (Al_2O_3), and hafnium oxide (HfO_2) [47,193]. It has been shown that Al_2O_3 offers better chemical stability than silicon oxide while maintaining excellent sensitivity in the case of using them as sensors [194,195].

In their early work, Legallais et al. studied SiNN FETs passivated by the native silicon dioxide layer which systematically grows when the silicon is exposed to air [47]. It is known this native SiO_2 provides poor-quality interfaces and induces the formation of a high density of dangling bonds at the interface. On the basis of the foregoing, they opted for an alumina encapsulation layer as it is fully compatible with the integration process and can be easily etched before contact deposition, using HF treatment [47]. Atomic layer deposition (ALD) was chosen for alumina deposition since it involves a self-limiting growth mechanism that enables the formation of high quality and homogenous thin film. Moreover, this technique provides a conformal coating and properly encapsulates SiNWs while preserving the sintered NW–NW junctions (Figure 34).
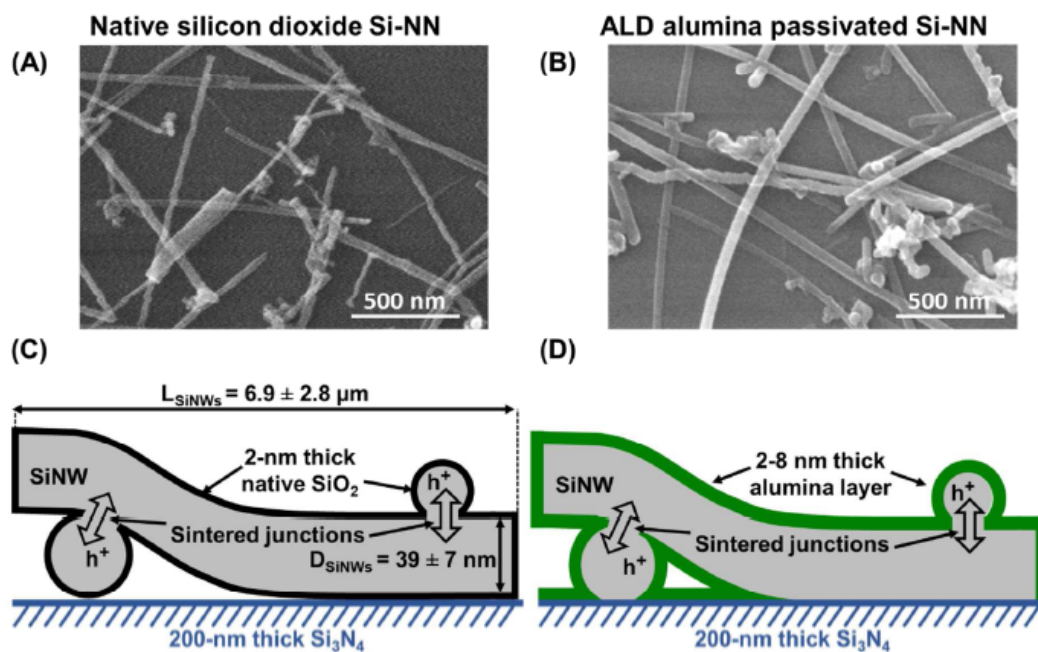
Figure 34. Comparison between sintered SiNN coated by (**A,C**) natively grown silicon dioxide and passivated by (**B,D**) alumina deposited using ALD. (**A**, **B**) Refer to top-view SEM images of nanonets, while (**C**, **D**) are sectional schemes of three coated SiNWs: one sectioned in the length and two according to the diameter. For (**C**), the mean and standard deviation of SiNW length (L_{SiNWs}) and diameter (D_{SiNWs}) are indicated. For (**D**), due to conformal coating with ALD, alumina is deposited simultaneously on SiNWs and onto the substrate whereas SiNW–SiNW junction and underneath SiNW portions are considered alumina-free. Reproduced from [47].

As native SiO_2 has a high density of dangling bonds at the interface, this interruption in the periodic lattice structure acts as interface traps for carriers. These traps are responsible for the reduction of transistor performances. On the contrary, alumina provides a better quality interface and improved electrical characteristics, as clearly shown in Figure 35A,B.
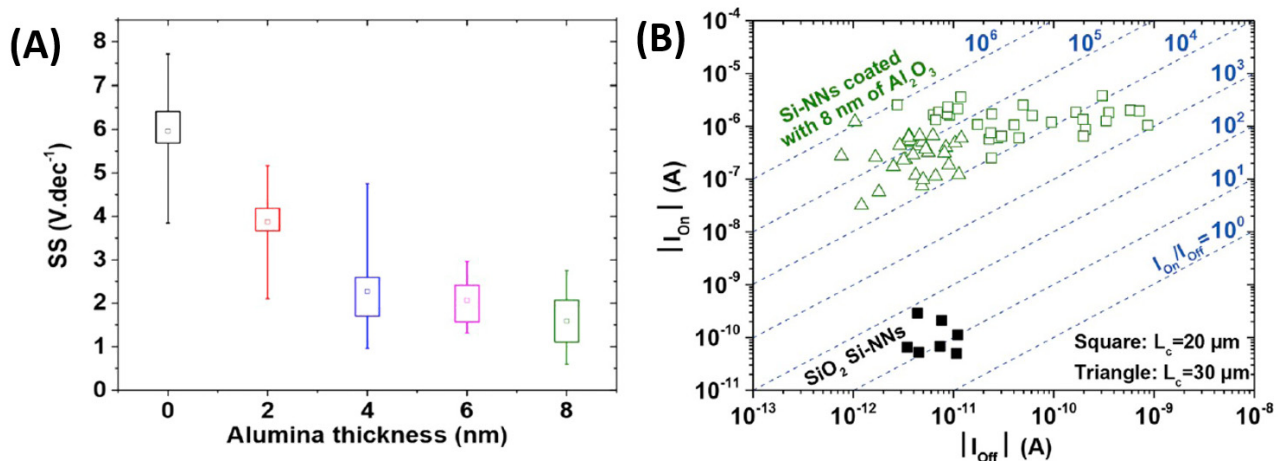
Figure 35. (**A**) Effect of the alumina thickness on the subthreshold slope (SS). 0 nm of alumina corresponds to a 2-nm thick layer of native SiO_2. For all transistors, the channel length (L_c) is 20 µm and the drain voltage (V_d) was set at -4 V. The boxes show the 25th and 75th percentiles, whereas the whiskers represent the 5th and 95th percentiles. The empty square in the boxes shows the mean value. (**B**) Reproducibility of the on and off current for transistors based on native SiO_2 SiNNs (full symbol) and 8-nm alumina encapsulated SiNNs (empty symbol) for 20 µm (square) and 30 µm (triangle) long channel. For native SiO_2 SiNN based devices, no current is observed when the channel length is 30 µm. The on-to-off ratio ($I_{on} = I_{off}$) is indicated by the dashed line. I_{on} and I_{off} were extracted at -25 V and $+25$ V, respectively. Reproduced from [47].

As a result, this study shows that proper material engineering of nanonets via alumina encapsulation can drastically enhance the electrical characteristics of back-gate FETs.

At the same time, although silicon nanowires are considered promising for future biomedical sensors, their limited stability under physiological conditions is a challenge for sensor development. Solving this issue by surface engineering as described above opens up new possibilities for sensor improvements [81,196,197].

However, as with thin films, the nanostructures composing the nanonet can be functionalized with, for example, molecules or proteins. DNA sensors based on SiNN have been achieved by chemically modifying the surface of nanonet with 3-aminopropyl-triethoxysilane (APTES) silanization [28] or (3-glycidyloxypropyl)trimethoxysilane (GOPS) [198]. Particularly, GOPS functionalization enables DNA electrical detection with SiNN-FETs [199]. Additionally, silicon nanonet field effect transistors (SiNN-FETs) were biomodified using thrombin-binding aptamer (TBA-15) [200] with the aim to detect thrombin protein. As an illustration, Figure 36 shows the shift in threshold voltage induced by aptamer probes grafting on the SiNN surface. As a result, again it has been demonstrated that the surrounding material can drastically change the characteristics of the SiNN-FETs.

8.2.2. Modulation Thanks to Functionalization under the Channel

As previously stated, the complex electronic mechanisms involved in electronic devices are highly dependent not only on the energy barriers to conquer but also on the interface traps, which can induce modification of the charge carrier density thus changing the performances of the devices. The phenomena are poorly understood, and the roots of changes are numerous ranging from the neutralization of surface defects, the modification of the surface energy, and even the creation of interface dipoles. Celle et al. focused on the control of the chemical nature of the interface between the gate oxide and the semiconductor, the place where the conduction channel is established in FETs (back gate-bottom contact structure Figure 37) [201].
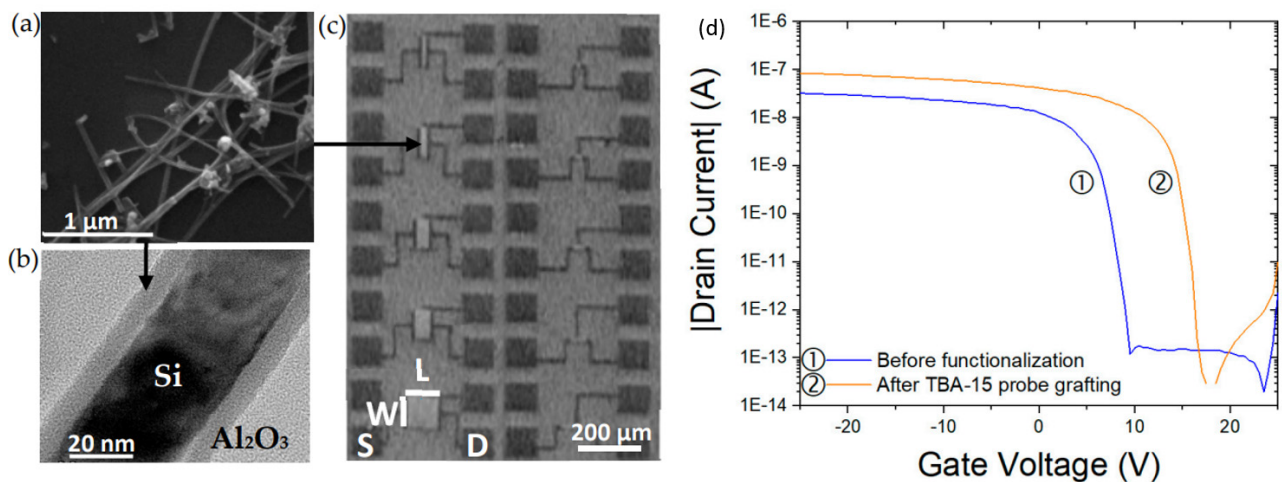
Figure 36. (**a**) SEM image of the Si nanonet (NN) after transfer on heavily doped Si substrate covered with a 200 nm thick Si_3N_4. (**b**) High-resolution TEM (HRTEM) image displaying an Al_2O_3 passivated Si nanowire. (**c**) Optical image of Al_2O_3 passivated SiNN field effect transistors (FETs) presenting different channel geometries. (**d**) Transfer characteristics were obtained for an L = 100 μm, W = 100 μm NN-FET at a drain voltage of V_{ds} = −2 V before and after functionalization with thrombin-binding aptamer (TBA-15). Reproduced from [200].
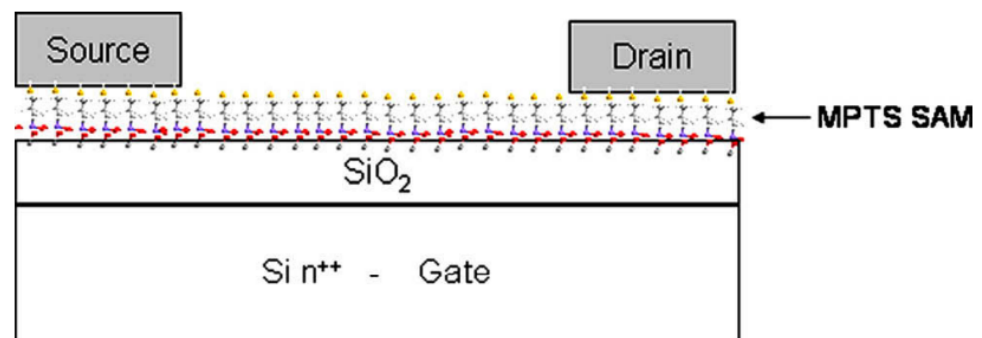
Figure 37. Schematic structure of the devices with MPTS as anchoring layer for gold electrodes. Reproduced from [201].

They show that thiolated self-assembled monolayer (SAMs) can be used to anchor source-drain gold electrodes on the substrate, leading to excellent electronic performances of the organic field-effect transistor (OFET) on the same level as those using a standard electrode process. It has been demonstrated that the threshold voltage is tunable while keeping the other electrical properties nearly unchanged by functionalization of the surface of the substrate under the channel (Figure 38). These self-assembled monolayers strongly modify the OFET characteristics, leading notably to charge carrier mobility [201,202].

SAMs are known to generate a built-in electric field, which modifies the carrier density in the transistor channel. For instance, it is seen that fluorinated SAMs have the tendency to generate a local electric field that accumulates holes, and on the contrary, devices with 3-aminopropyl-triethoxysilane (APTS), or triarylamine triethoxysilane derivative (TAATS) accumulate electrons, leading to the need for a very large negative gate bias to turn on organic semiconductor which is polytriarylamine (PTAA), into hole accumulation mode. They have shown that this local electric field is related to the dipole moment of the molecules [201,202].
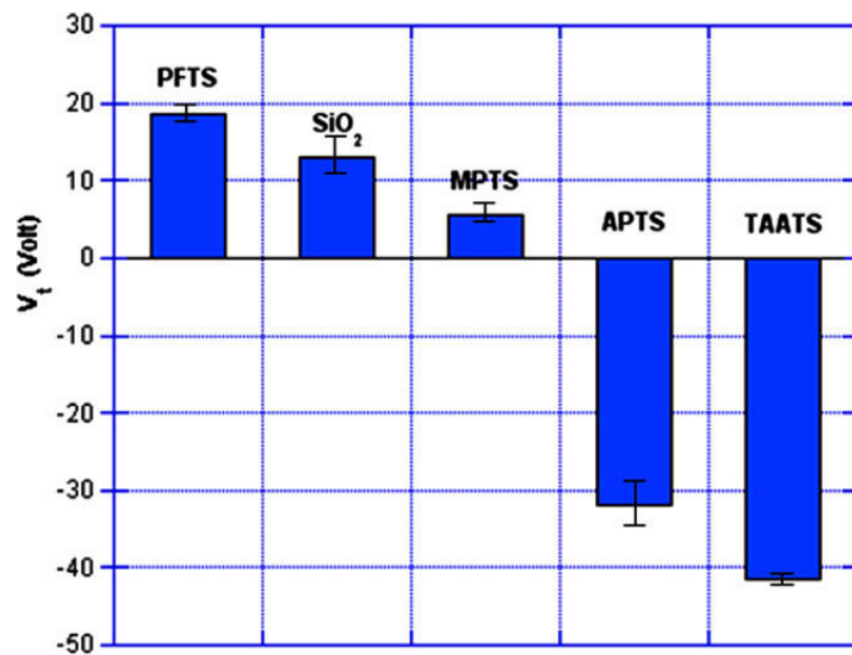
Figure 38. V_t as a function of the channel modification. Reproduced from [201].

8.3. Silicidation

Silicidation was commonly used since the 1980s in MOSFETs in forming an alloy between metal and silicon during an annealing process in order to decrease the electrical contact resistance between the two materials. During this step, solid-state reactions occur by diffusion and/or nucleation processes of the thermally activated species. Depending on the experimental annealing conditions, different stable crystalline phases called silicides can form and are denoted M_xSi_y with M the metal used. Silicon has the particularity of associating with many metals, some of which are grouped in Table 3. Historically, the silicides $TiSi_2$, $CoSi_2$, and more recently NiSi have been the most used by the microelectronics industry for their low electrical resistivity ranging from 10 to 25 $\mu\Omega$.cm [203]. Nevertheless, Ti- and Co-based alloys require higher temperature annealing which may be responsible for the deactivation of the dopants contained in the silicon and implies an increase in contact resistance at the interface between silicide and Si [204]. Moreover, for some Co silicides, Si is the dominant diffusion species, which causes the formation of gaps or voids in the silicon. Following this phenomenon, the diffusion of Si gaps can also become considerable. Thus, simultaneous flows of matter in one direction and of vacancies in the other lead to the appearance of porosities within the silicon, a phenomenon commonly known as the Kirkendall effect. This is probably one of the reasons why a high increase in the electrical resistance of Co silicides is observed when the channel length of MOSFETs is below 50 nm [205,206].

Table 3. Properties of different silicides used in the microelectronics industry. Table adapted from references [205,207,208]. Φ_{bh} corresponds to the barrier height on N-type silicon.

Silicide	Formation Temperature (°C)	Crystalline Structure	Resistivity ($\mu\Omega$.cm)	Φ_{bh} (eV)
$TiSi_2$	650	Orthorhombic	13–16	0.60
$CoSi_2$	450	Cubic	18–20	0.64
PtSi	300	Orthorhombic	28–35	0.87
NiSi	400	Orthorhombic	10.5–18	0.75

For the reasons stated above, NiSi silicide is today widely used due to its low electrical resistivity (10.5–18 $\mu\Omega$.cm) as well as its lower formation temperature (400 °C). Further-

more, Ni-based silicidation is a diffusion process in which Ni is the dominant diffusion species [206]. While, contrary to Co silicides, the gaps generated during thermal annealing are located in the metallic contact and avoid the appearance of porosities within the silicon. Nevertheless, the complexity of the Ni-Si phase diagram presented in Figure 39 indicates the difficulty to control, during annealing, the formation of the desired NiSi phase. Indeed, many crystalline and stable phases at room temperature are likely to form [209]. Note that the variations in resistivity from one phase to another are very large, ranging from 7 to 150 $\mu\Omega$.cm (Table 4).
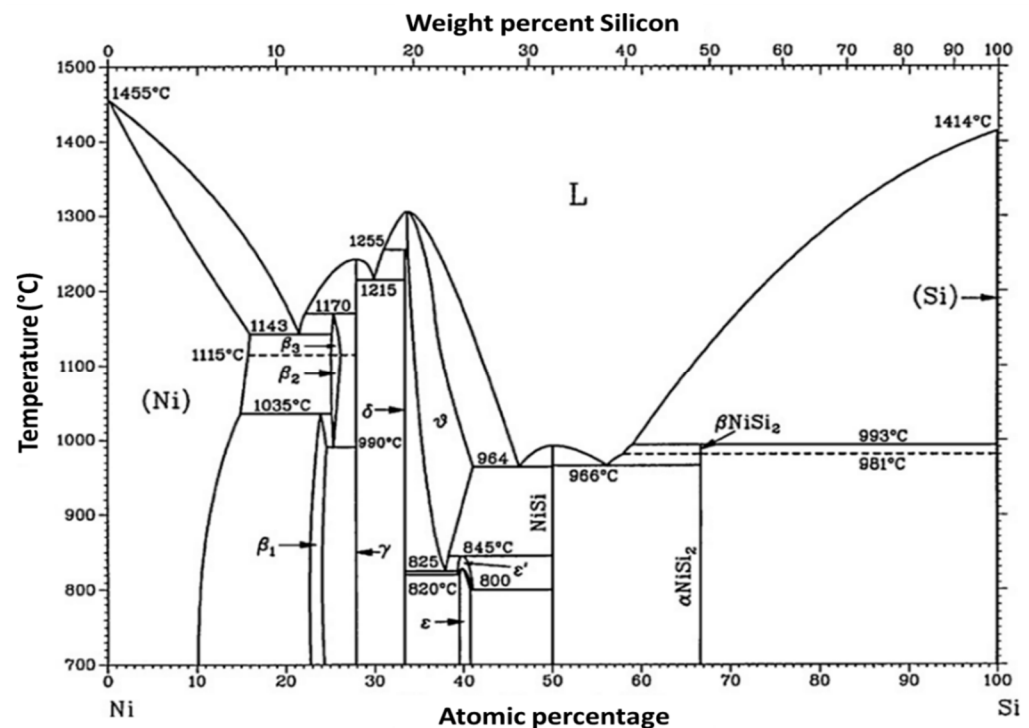

Figure 39. Binary phase diagram of the nickel–silicon pair. Reproduced from [209].

Table 4. Formation temperature, crystallographic structure, electrical resistivity, unit cell volume per Si atom ($V_{Ni_xSi_i/Si}$), and the ratio of this volume to that of Si ($V_{Ni_xSi_i/Si}/V_{Si}$) of each room temperature stable Ni_XSi_y silicide [205,208]. UNK is the acronym for unknown.

Phase	Formation Temperature (°C)	Crystalline Structure	Resistivity (μΩ.cm)	$V_{Ni_xSi_i/Si}$ (Å^3)	$V_{Ni_xSi_i/Si}/V_{Si}$
Ni	-	Cubic	7–10	-	-
Ni_3Si	UNK	Cubic	80–90	43.08	2.15
$Ni_{31}Si_{12}$	UNK	Hexagonal	90–150	39.46	1.97
Ni_2Si	200	Orthorhombic	24–30	32.15	1.61
Ni_3Si_2	UNK	Orthorhombic	60–70	28.73	1.44
NiSi	400	Orthorhombic	10.5–18	24.12	1.21
$NiSi_2$	800	Cubic	34–50	19.75	0.99
Si	-	Cubic	Depend on doping	20.01	1

Currently, the salicidation process [210] (a portmanteau for 'self-aligned silicide') is used to achieve simultaneous silicidation of the source, drain. This technique consists in forming the Ni_2Si phase by diffusion of Ni during the first annealing between 270 and 350 °C. Then, after etching the excess of unreacted nickel, the NiSi silicide is formed after second annealing between 400 and 550 °C [211]. According to Ottaviani, NiSi can only be formed after consumption of the entire metal reservoir, which explains the need to etch the excess Ni after the first annealing [212].

It was shown that the NiSi phase can form a low resistive Si-Ni interface for a thermal budget compatible with the specifications of today's microelectronics industry.

Silicidation of Silicon Nanowires with Nickel

For silicon nanowires, the formation of a silicide also makes it possible to form an abrupt interface over the entire cross-section of the nanowire between the silicide and the nanowire, which facilitates the injection of the carriers. Indeed, the nickel penetrates over the entire volume of the SiNW and then diffuses longitudinally. Otherwise, for non-silicided nanowires, the injection of the carriers is less efficient since it is done radially through the edges of the SiNWs. In addition, Chou et al. studied the kinetics of NiSi formation between 450 and 750 °C by in-situ transmission electron microscopy analyses [213,214].

Nevertheless, the NiSi phase is often accompanied by a Ni-rich phase that forms at lower temperatures [215–217]. Other crystallographic studies have shown the possibility of obtaining Ni-rich phases such as $Ni_{31}Si_{12}$ and Ni_2Si for temperatures between 400 and 450 °C [176,218]. More surprisingly, $NiSi_2$ silicide has been stabilized at low temperatures between 440 and 550 °C while it forms at about 800 °C for bulk materials [175,176,218–220]. In order to evaluate the phases likely to form for a given temperature, Figure 40 represents the minimum and maximum temperatures of formation of the different Ni_xSi_y silicides in silicon nanowires from references reported in the literature.
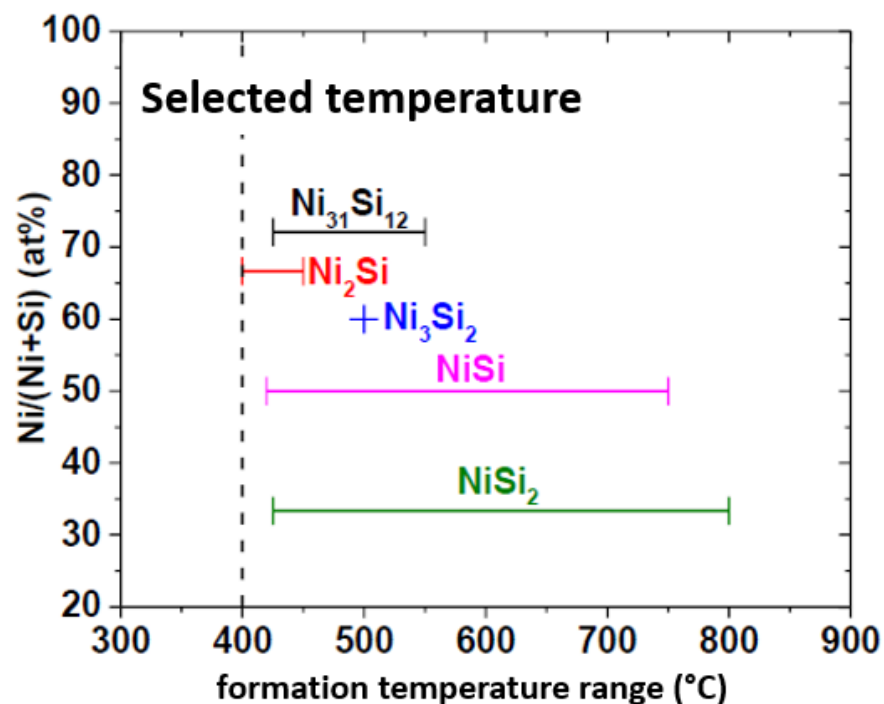
Figure 40. Temperature range of formation of different Ni_xSi_y silicides in SiNWs reported in the literature from 15 references [175,176,182,213,214,216–224].

According to Figure 40 based on SiNWs, for an annealing temperature of about 400–450 °C, we can see that the $Ni_{31}Si_{12}$, Ni_2Si, NiSi, and $NiSi_2$ phases are likely to form, i.e., a variation in electrical resistivity between 10.5 and 150 µΩ.cm (Table 4). Thus, obtaining the NiSi phase in SiNWs is complex and the silicidation involves many parameters such as the crystal orientation [176,218], the diameter of the nanowire [217], the thickness of the nickel film [225], or the thickness of the oxide surrounding the nanowire [221]. According to the work of Ogata et al. [220], the diffusion length of silicide in SiNW evolves with the square root of the annealing time.

According to the literature carried out previously, the desired NiSi silicide of low electrical resistivity is formed at a temperature of about 400 °C for massive materials

(Table 4). In the context of NW silicidation, the complex growth mechanisms involved do not allow to conclude on an optimal temperature and time for the formation of the NiSi phase despite a rich literature on this subject. Nevertheless, according to the work of Ternon et al. [48] and the studies of Byon et al. [182], an optimum of the electrical properties can be distinguished for annealing at 400 °C which is consistent with the NiSi formation temperature. Moreover, this temperature does not exceed the maximum temperature allowed for integration on the back-end of a reading circuit.

To complete the silicidation study, the impact of silicide existence on the electrical characteristics of SiNWs was also considered [226]. The main advantage of silicide contacts over non-silicided contacts is better device performance by modifying the nature of the metal–semiconductor interface, thus reducing series resistance [11,214,215,227]. Guillaume Rosaz showed that the NiSi silicide, formed at 400 °C in the nanowires, lowers the height of the Schottky barrier, thus favoring the injection of the carriers. The performance of the transistors is significantly improved by an increase in current accompanied by a decrease in subthreshold swing [3,11]. The thermally activated intrusion of nickel into the SiNW is an inexpensive and robust, but not fully controlled, process. They demonstrated that the silicidation reaction seems to be self-limited (see Figure 41c).
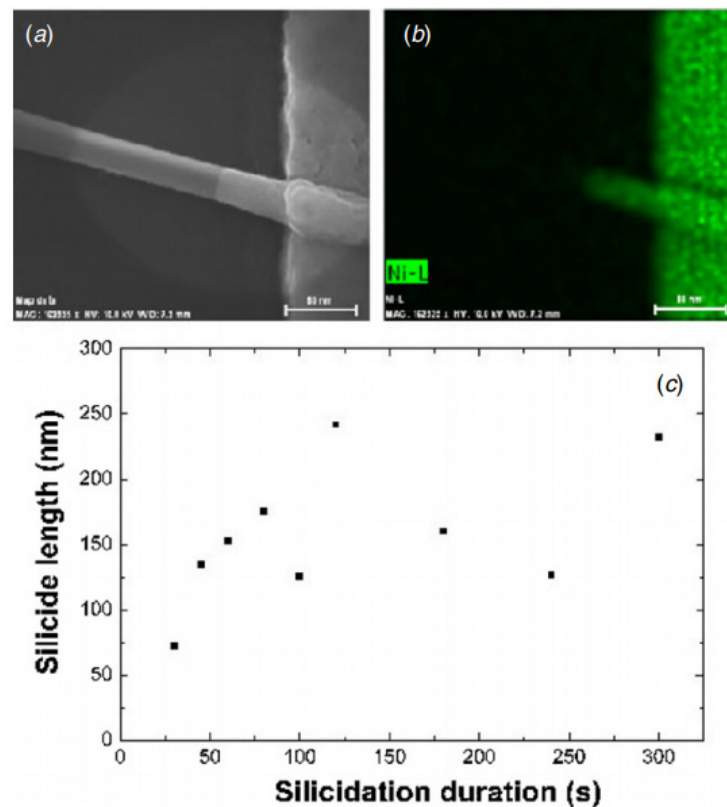
Figure 41. (**a**) SEM view of a silicided contact after annealing at 400 °C under nitrogen gas during 300 s. The scale bar is 80 nm. (**b**) EDX picture of the contact presented in (**a**). Green color indicates the presence of nickel. One can notice the propagation of the nickel in the SiNW after the annealing step leading to the formation of a silicide. (**c**) Length of the silicided section obtained at 400 °C under nitrogen gas in an RTA furnace as a function of the annealing time. Reproduced from [11].

The silicide region lessens the resistance of the contacts in two ways. First, the low sheet resistance of the silicide layer reduces the in-plane contact resistance, and second, the silicide reaction leads to an intimate and more reliable metal–semiconductor (MS) contact and transforms the contact surface initially on the surface of the NW into a contact surface on the cross-section of the NW. As a result, in terms of performance, the most substantial properties of a silicide material are its low electrical resistivity and its lower Schottky

barrier height [227,228]. Byon et al. also studied the impact of silicidation on the electrical properties of transistors and observed an optimum between 400 and 450 °C after successive annealing from 250 to 500 °C [182].

　　　Figure 42 presents the transfer characteristics before and after annealing of a 20 μm channel SiNN-FET elaborated with a density of 42×10^6 NWs cm^{-2} (drain-source bias of -4 V). Before annealing, the device exhibits and the state of 9 nA and 0.7 pA respectively, resulting in an on/off ratio of 10^4. After annealing, the state reaches 170 nA while the state remains constant, corresponding to an enlarged on/off ratio $>10^5$ Such improvement by one order of magnitude confirms the formation of a low resistive phase, enhancing hole injection at the metal/SiNW contact.
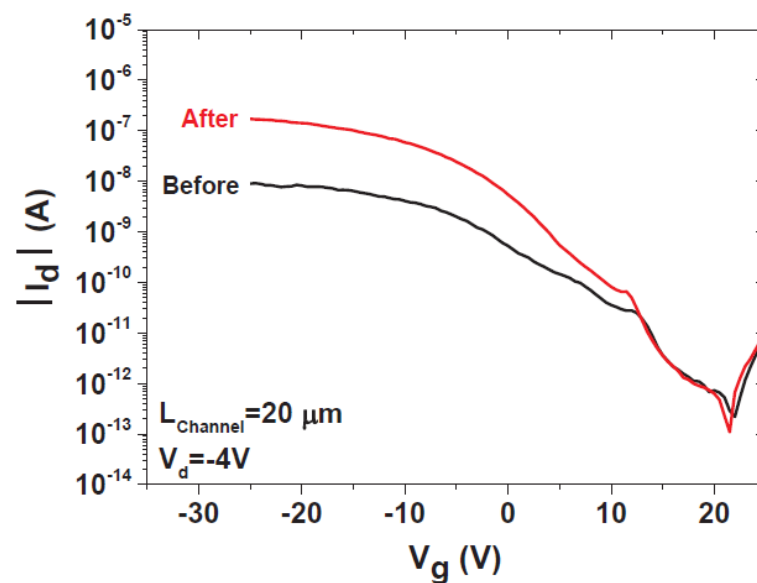
Figure 42. Transfer characteristics before and after silicidation (400 °C, for 60 s) of a 20 μm channel Si nanonet FET elaborated with 18 mL of filtered SiNW solution (with 42×10^6 NWs cm^{-2} corresponding density). The drain-source bias was set at -4 V. Reproduced from [226].

9. Applications

　　　Silicon nanowires can be exploited in many ways in electronic devices and can find numerous real applications such as displays, data storage, 3-D computing, lasers, smart cards, wearable electronics, high efficiency programming, ring oscillators [6,31,168]. They have so far shown promising applications in areas ranging from biological sensors, thermo-electric convertors, opto-mechanical devices, piezoelectric sensors, and solar cells among others. Describing all the potential applications is detail is far beyond the scope of this review. However, dealing with devices without describing applications would leave a taste of unfinished business. As a consequence, in this section, without being exhaustive, we choose to summarize some basic applications for the simplest SiNW-based devices (resistor, transistors, and diodes).

9.1. Photodetectors

　　　Optical properties of SiNWs have allowed envisaging the use of SiNWs as optically active materials for photonics application. The ease of bandgap conversion from indirect to direct band due to dimension, crystallography, mechanical strain, and alloying allows SiNWs to be used in the optical applications—e.g., photodetectors (PDs) and light emitters (LEs). Since silicon nanowires have a superior ability to tune absorption with morphology, Um et al. reported that SiNWs with a coating of an indium oxide layer on it, lead to efficient carrier separation and collection, resulting in an improvement of quantum efficiency and by controlling the nanowire radii, can create a multispectral detector [229].

9.2. Memories

A self-alignment technique can be used to position the silicon nanowires, which could allow for lower production costs than current flash memory cards. SiNW-based memory devices showed better stability at higher temperatures, no power consumption in the off-state, and very small switching energy (10^{-14} J) [230].

With the advent of new CMOS compatible fabrication methods for silicon nanowires, it is now feasible to build memory and memristive devices. The SiNW-FET based dielectric charge-trapping flash-like memories have been fabricated and fully characterized by Zhu et al. (Figure 43c,d) [231].

These non-volatile memory devices exhibited fast programming/erasing speed, excellent retention, and endurance, indicating the advantages of integrating the multilayer of charge-storage stacks on the nanowire channel. Such high-performance flash-like non-volatile memory can be integrated into the microprocessor chip as the local memory which requires high density and good endurance [231–233].
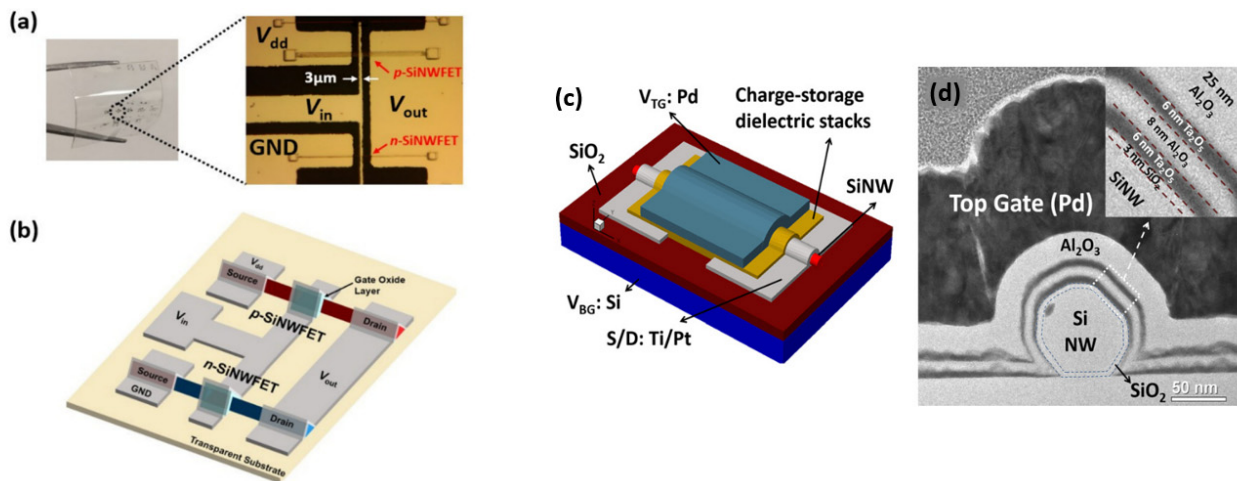
Figure 43. (**a**) Optical images and (**b**) schematic illustration of the SiNW CMOS inverter on a transparent substrate. Reproduced from [234]. (**c**) Schematic of a SiNW-FET-based charge-trapping non-volatile flash memory; (**d**) TEM image of the cross section of a MATATOS device. Inset demonstrates the typical thickness of the top gate stack. Reproduced from [231].

9.3. Biosensors

Sensors are important tools for life sciences and biochemistry. The use of sensors in these areas leads to the detection and diagnosis of diseases and to the discovery of new drugs [17,71]. Microelectronic sensors based on thin film transistors and ion-sensitive filedeffect transistors (ISFETs) are used since the 1970s. They offered a cheap solution over the chemical sensors and could be integrated on a chip [71]. Nevertheless, the microelectronic sensors did not have the required characteristics to be used as biosensors because of their undesired sensitivity to temperature and light and because their parameters were not fixed over time. Additionally, solid-state electrodes were not reliable and this led to the use of chemical sensors [71]. Currently, the detection of biomolecules at low concentrations is achieved with fluorescent labeling and optical detection methods. However, this technique is expensive and time-consuming and thus silicon nanowires may be an alternative solution [71,235].

Silicon nanowires can almost act as perfect biosensors due to their inherent properties [235]. When used as sensors, their characteristics include ultrahigh sensitivity because the molecule being sensed depletes or accumulates the charges in the bulk of the nanowire [17,235]. In addition, direct label-free detection allows the molecules to be detected in real time which eliminates the time consuming labeling chemistry [17,23,71].

Another important characteristic is that they are non-radioactive and that sensor arrays can allow detection of different molecules in the same solution [23,71].

Although SiNW sensors have great characteristics there are factors that can affect their performance. These include the surrounding environment of the nanowire and the electrostatic screening action of the ions in the solution. The performance of a sensor can be characterized by sensitivity, settling time, and selectivity. A simulation with a silicon nanowire with a length between 2 and 20 μm showed how the sensitivity can be influenced by several factors. The results showed that the sensitivity increases with reduced dopant density and decreased diameter and length. However, it is not possible to reduce these quantities as much as needed to achieve the maximum desired sensitivity due to the dopant fluctuations effect. Furthermore, this simulation revealed that the dielectric constant of the surrounding environment affects the sensitivity of SiNW. If the surrounding media is air then the sensor has greater sensitivity if it is designed to operate in the depletion mode. Finally, parasitic ions in the surrounding solution of the sensor screen the charge of the target molecule and reduce sensitivity [71].

Experimental applications of SiNW sensors include the detection of proteins, DNA, pH, drug discovery, single viruses, glucose, and arrays for parallel molecule detection, as shown in Figure 44 [17,61,236].
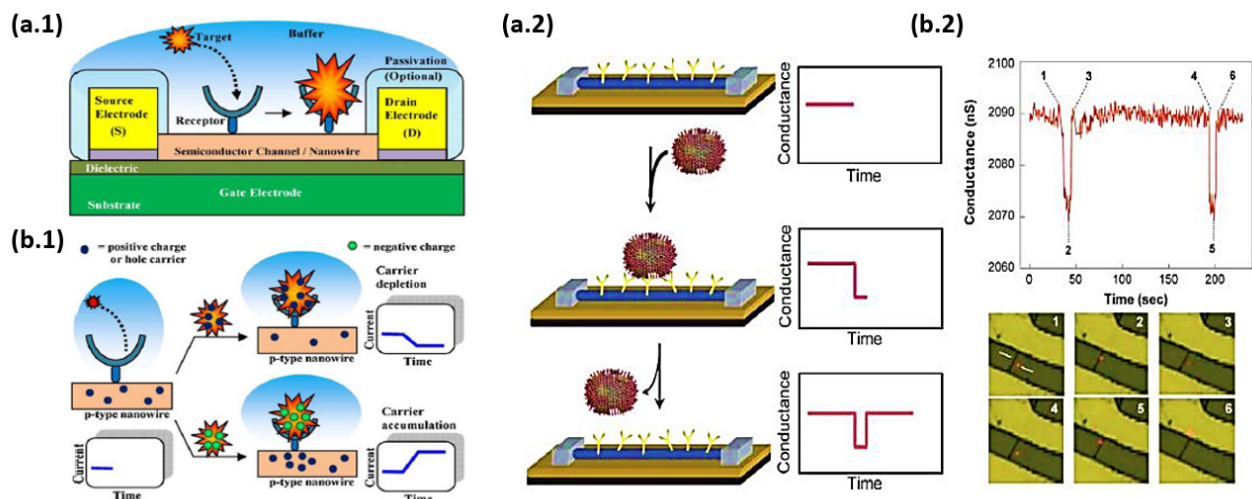
Figure 44. (**a.1**) The illustration of a nanoscale FET biosensor with a cross-sectional view. (**b.1**) When positively charged target molecules bind the receptor modified on a p-type NW, positive carriers (holes) are depleted in the NW, resulting in a decrease in conductance. Conversely, negatively charged target molecules captured by the receptor would make an accumulation of hole carriers, causing an increase in conductance. Reproduced from [174]. (**a.2**) Schematic of a single virus binding and unbinding to the surface of a SiNW device modified with antibody receptors and the corresponding time-dependent change in conductance. (**b.2**) Simultaneous conductance and optical data recorded for a Si nanowire device after the introduction of influenza A solution. The images correspond to the two binding/unbinding events highlighted by time points 1–3 and 4–6 in the conductance data, with the virus appearing as a red dot in the images. Reproduced from [17].

9.4. Gas Sensor

Silicon nanowires can find applications as gas sensors too. As an example, this was demonstrated for H_2 sensing when the surface of an n-type SiNW was coated with palladium nanoparticles (Pd particles). Good selectivity was demonstrated as no response was observed when exposed to NH_3 or N_2O gases. However, when H_2 gas flowed over the sensor, the current flowing through was increased, as shown in Figure 45. Furthermore, the SiNW sensor responded faster (2.3 s) than an ordinary macroscopic Pd wire sensor (more than 10 s) [236].
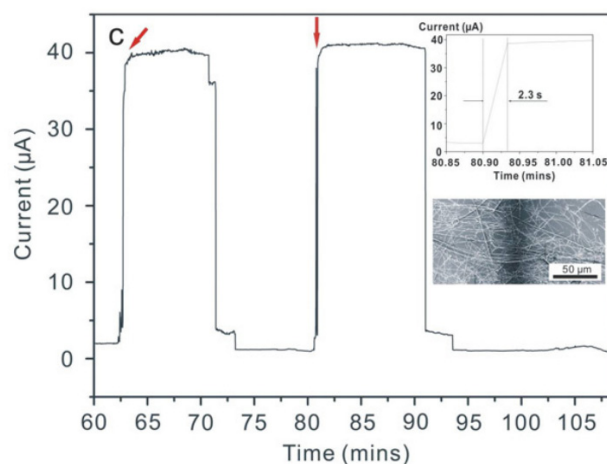
Figure 45. Real time current response of Pd coated SiNWs in 5% H$_2$. The inset images show the enlarged current response (**upper**) and an SEM image (**below**) of the device. Note that, the sensor was inside a chamber with a pressure of 0.01 Torr, and a voltage of 2 V was applied across it. Reproduced from [236].

9.5. Thermoelectric Application

Thermoelectric devices can convert heat directly into electrical power, and vice versa, and they have a broad range of applications: energy recovery and green energy harvesting; energy micro-harvesting (scavenging) for the capillary supply of small systems, such as sensor nodes for Internet of Things (IoT); powering of systems in remote and harsh environments typical, for example, of spatial exploration; localized and optimized cooling of small systems, where the reliability and the compactness can play a fundamental role [101, 237,238]. Unfortunately, the available materials with thermoelectric properties good enough for an acceptable thermal-to-electrical conversion efficiency limit all of the potentialities offered by thermoelectric devices at the current state of the art.

The observed high electrical and low thermal conductivity of highly doped SiNWs arrays, shows that SiNWs arrays represent a promising material for thermoelectric applications. Hence, it could make a significant contribution in the fundamental fields of energy micro-harvesting (scavenging) and macro-harvesting [101,237,238].

10. Conclusions

Semiconductor nanowires, especially silicon nanowires, have aroused a lot of scientific interest over the past 25 years and have been considered a promising material for nanoscale devices and integrated circuits. Key parameters in realizing application through a bottom-up paradigm include chemical composition, structure, size, morphology, and doping which have been fully controlled in semiconductor NW systems. Among semiconductor NWs, silicon NWs—owing to their unique physical and chemical properties—show promise for a wide range of applications, including FETs. However, such devices based on single SiNWs face complicated fabrication processes and low reproducibility of their electrical characteristics which originate from various issues such as dispersion in length, diameter, and doping of individual nanowires, wire surface passivation, poorly controlled gate length, or silicidation with the silicide length and quality arising from annealing step.

Researchers tried to solve these issues with multi-channel SiNW-based devices which have better stability and reproducibility in comparison with single SiNW-based devices. Apart from increased on-current in MPC-FETs, some other parameters include on-to-off ratio or subthreshold swing degrade. This degradation occurs due to intrinsic disparities of all parameters which have already been mentioned for single SiNWs such as length, diameter, doping, and surface properties.

Silicon nanonets are networks of randomly oriented silicon nanowires. Due to its flexibility, transparency, and reproducibility, this material is highly attractive as an alterna-

tive to amorphous silicon or organic materials for various macro-electronic applications involving sensors and displays. Based on the easy integration process simply relying on standard photolithography, it has demonstrated successful workability, reproducibility, and excellent air stability along with interesting performance for device channel length ranging from micrometer to millimeter scales. SiNN-FETs also displayed good stability and reproducibility which differentiates them from single SiNW- and MPC-FETs and which are the results of averaging effect over thousands of nanowires and their junctions.

According to literature, the nanonet-based thin film transistor technology has the respective advantages of poly-Si, a-Si, or organic material, without their particular drawbacks, along with being flexible. Moreover, low-cost and large-scale technology is an important asset of this material, in comparison to the issues surrounding the poly-Si option. Furthermore, using nanostructures—such as a network of nanowires—allows electronics to be smaller, more powerful, and more efficient. Finally, in conclusion, nanonets can address the need for cost-effective, reproducible, and efficient systems to exploit nanoscale properties while being easily manipulated and compatible with large-scale integration and opening up many opportunities, both in terms of applications and fundamental studies, in short, a new field of research.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Ramgir, N.S.; Yang, Y.; Zacharias, M. Nanowire-Based Sensors. *Small* **2010**, *6*, 1705–1722. [CrossRef] [PubMed]
2. Wu, B.; Heidelberg, A.; Boland, J. Mechanical properties of ultrahigh-strength gold nanowires. *Nat. Mater.* **2005**, *4*, 525–529. [CrossRef] [PubMed]
3. Rosaz, G. Intégration 3D de Nanofils Si et SiGe Pour la Réalisation de Transistors Verticaux à Canal. 2012. Available online: https://www.theses.fr/2012GRENT108 (accessed on 9 February 2022).
4. Lu, W.; Xiang, J. Semiconductor Nanowires: From Next-Generation Electronics to Sustainable Energy. *R. Soc. Chem.* **2015**, *39*. Available online: http://stacks.iop.org/0022-3727/39/i=21/a=R01 (accessed on 8 February 2022).
5. Liu, L.-C.; Huang, M.-J.; Yang, R.; Jeng, M.-S.; Yang, C.-C. Curvature effect on the phonon thermal conductivity of dielectric nanowires. *J. Appl. Phys.* **2009**, *105*, 104313. [CrossRef]
6. Yu, B.; Meyyappan, M. Nanotechnology: Role in emerging nanoelectronics. *Solid-State Electron.* **2006**, *50*, 536–544. [CrossRef]
7. How Nanowires Work. 2014, pp. 1–5. Available online: https://science.howstuffworks.com/nanowire.htm (accessed on 11 January 2022).
8. Ternon, C.; Dupas, F.; Stein, S.; Aguirre, C.; Dhalluin, F.; Baron, T. Carbon Nanotube Sheet as Top Contact Electrode for Nanowires: Highly Versatile and Simple Process. *J. Nanosci. Nanotechnol.* **2015**, *15*, 1669–1673. [CrossRef] [PubMed]
9. Rosaz, G.; Salem, B.; Pauc, N.; Potié, A.; Gentile, P.; Baron, T. Vertically integrated silicon-germanium nanowire field-effect transistor. *Appl. Phys. Lett.* **2011**, *99*, 193107. [CrossRef]
10. Arjmand, T.; Legallais, M.; Haffner, T.; Bawedin, M.; Ternon, C.; Salem, B. Development of a robust fabrication process for single silicon nanowire-based omega gate transistors on polyamide substrate. *Semicond. Sci. Technol.* **2020**, *36*, 025003. [CrossRef]
11. Rosaz, G.; Salem, B.; Pauc, N.; Gentile, P.; Potié, A.; Solanki, A.; Baron, T. High-performance silicon nanowire field-effect transistor with silicided contacts. *Semicond. Sci. Technol.* **2011**, *26*, 085020. [CrossRef]
12. Morales, A.M.; Lieber, C.M. A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires. *Science* **1998**, *279*, 208–211. [CrossRef]
13. Yu, P.; Wu, J.; Liu, S.; Xiong, J.; Jagadish, C.; Wang, Z.M. Design and fabrication of silicon nanowires towards efficient solar cells. *Nano Today* **2016**, *11*, 704–737. [CrossRef]
14. Chen, L.; Lu, W.; Lieber, C.M. Chapter 1. Semiconductor Nanowire Growth and Integration. In *Semiconductor Nanowires: From Next-Generation Electronics to Sustainable Energy*; Royal Society of Chemistry: London, UK, 2014; pp. 1–53. [CrossRef]
15. Appenzeller, J.; Member, S.; Knoch, J.; Björk, M.T.; Riel, H.; Schmid, H.; Riess, W. Toward nanowire electronics. *IEEE Trans. Electron Devices* **2008**, *55*, 2827–2845. [CrossRef]
16. Björk, M.T.; Schmid, H.; Knoch, J.; Riel, H.; Riess, W. Donor deactivation in silicon nanostructures. *Nat. Nanotechnol.* **2009**, *4*, 103–107. [CrossRef] [PubMed]
17. Patolsky, F.; Lieber, C.M. Nanowire nanosensors. *Mater. Today* **2005**, *8*, 20–28. [CrossRef]

18. Sohn, Y.-S.; Park, J.; Yoon, G.; Song, J.; Jee, S.-W.; Lee, J.-H.; Na, S.; Kwon, T.; Eom, K. Mechanical Properties of Silicon Nanowires. *Nanoscale Res. Lett.* **2009**, *5*, 211–216. [CrossRef] [PubMed]

19. Dasgupta, N.P.; Sun, J.; Liu, C.; Brittman, S.; Andrews, S.C.; Lim, J.; Gao, H.; Yan, R.; Yang, P. 25th Anniversary Article: Semiconductor Nanowires—Synthesis, Characterization, and Applications. *Adv. Mater.* **2014**, *26*, 2137–2184. [CrossRef]

20. Schmidt, V.; Wittemann, J.V.; Senz, S.; Gösele, U. Silicon Nanowires: A Review on Aspects of their Growth and their Electrical Properties. *Adv. Mater.* **2009**, *21*, 2681–2702. [CrossRef]

21. Cui, Y.; Wei, Q.; Park, H.; Lieber, C.M. Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species. *Science* **2001**, *293*, 1289–1292. [CrossRef]

22. Shao, M.; Ma, D.D.D.; Lee, S. Silicon Nanowires—Synthesis, Properties, and Applications. *Eur. J. Inorg. Chem.* **2010**, *2010*, 4264–4278. [CrossRef]

23. Dhahi, T.S.; Bin Hashim UD, A.; Ahmed, N.M.; Mat Taib, A. A review on the electrochemical sensors and biosensors composed of nanogaps as sensing material. *J. Optoelectron. Adv. Mater.* **2010**, *12*, 1857–1862.

24. Sun, C.; Mathews, N.; Zheng, M.; Sow, C.H.; Wong, L.H.; Mhaisalkar, S.G. Aligned Tin Oxide Nanonets for High-Performance Transistors. *J. Phys. Chem. C* **2009**, *114*, 1331–1336. [CrossRef]

25. Morisot, F.; Nguyen, V.H.; Montemont, C.; Maindron, T.; Munoz-Rojas, D.; Mouis, M.; Langlet, M.; Ternon, C. Al_2O_3, Al doped ZnO and SnO_2 encapsulation of randomly oriented ZnO nanowire networks for high performance and stable electrical devices. *Nanotechnology* **2019**, *30*, 385202. [CrossRef] [PubMed]

26. Langley, D.; Giusti, G.; Mayousse, C.; Celle, C.; Bellet, D.; Simonato, J.-P. Flexible transparent conductive materials based on silver nanowire networks: A review. *Nanotechnology* **2013**, *24*, 452001. [CrossRef] [PubMed]

27. Legallais, M. Conception, Etude et Modélisation d'une Nouvelle Génération de Transistors à Nanofils de Silicium Pour Applications Biocapteurs. Ph.D. Dissertation, Université Grenoble Alpes, Grenoble, France, 2017.

28. Pauline, S. Etude des Propriétés Structurales et électriques de Réseaux Aléatoires de Nanofils de Silicium. 2014. Available online: https://tel.archives-ouvertes.fr/tel-01162345/ (accessed on 9 February 2022).

29. De, S.; Coleman, J.N. The effects of percolation in nanostructured transparent conductors. *Mrs Bull.* **2011**, *36*, 774–781. [CrossRef]

30. Acharya, S.; Panda, A.B.; Belman, N.; Efrima, S.; Golan, Y. A Semiconductor-Nanowire Assembly of Ultrahigh Junction Density by the Langmuir–Blodgett Technique. *Adv. Mater.* **2006**, *18*, 210–213. [CrossRef]

31. Li, Y.; Qian, F.; Xiang, J.; Lieber, C.M. Nanowire electronic and optoelectronic devices. *Mater. Today* **2006**, *9*, 18–27. [CrossRef]

32. Kharisov, B.I.; Kharissova, O.V.; García, B.O.; Méndez, Y.P.; de la Fuente, I.G. State of the art of nanoforest structures and their applications. *RSC Adv.* **2015**, *5*, 105507–105523. [CrossRef]

33. Zhong, Z.; Wang, D.; Cui, Y.; Bockrath, M.W.; Lieber, C.M. Nanowire Crossbar Arrays as Address Decoders for Integrated Nanosystems. *Science* **2003**, *302*, 1377–1379. [CrossRef]

34. Mongillo, M.; Spathis, P.; Katsaros, G.; Gentile, P.; De Franceschi, S. Multifunctional Devices and Logic Gates with Undoped Silicon Nanowires. *Nano Lett.* **2012**, *12*, 3074–3079. [CrossRef]

35. Gruner, G. Carbon nanonets spark new electronics. *Sci. Am.* **2007**, *296*, 76–83. [CrossRef]

36. Gruner, G. Carbon nanotube films for transparent and plastic electronics. *J. Mater. Chem.* **2006**, *16*, 3533–3539. [CrossRef]

37. Hammersley, J.M. Percolation processes. *Math. Proc. Camb. Philos. Soc.* **1957**, *53*, 642–645. [CrossRef]

38. Kirkpatrick, S. Percolation and Conduction. *Rev. Mod. Phys.* **1973**, *45*, 574–588. [CrossRef]

39. Serre, P.; Mongillo, M.; Periwal, P.; Baron, T.; Ternon, C. Percolating silicon nanowire networks with highly reproducible electrical properties. *Nanotechnology* **2014**, *26*, 15201. [CrossRef]

40. Hill, D.J.; Teitsworth, T.S.; Ritchie, E.T.; Atkin, J.M.; Cahoon, J.F. Interplay of Surface Recombination and Diode Geometry for the Performance of Axial p–i–n Nanowire Solar Cells. *ACS Nano* **2018**, *12*, 10554–10563. [CrossRef]

41. Sze, S.; Irvin, J. Resistivity, mobility and impurity levels in GaAs, Ge, and Si at 300° K. *Solid-State Electron.* **1968**, *11*, 599–602. [CrossRef]

42. Heo, K.; Cho, E.; Yang, J.-E.; Kim, M.-H.; Lee, M.; Lee, B.Y.; Kwon, S.G.; Lee, M.-S.; Jo, M.-H.; Choi, H.-J.; et al. Large-Scale Assembly of Silicon Nanowire Network-Based Devices Using Conventional Microfabrication Facilities. *Nano Lett.* **2008**, *8*, 4523–4527. [CrossRef]

43. Whang, D.; Jin, S.; Wu, Y.; Lieber, C.M. Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems. *Nano Lett.* **2003**, *3*, 1255–1259. [CrossRef]

44. Mulazimoglu, E.; Coskun, S.; Gunoven, M.; Butun, B.; Ozbay, E.; Turan, R.; Unalan, H. Silicon nanowire network metal-semiconductor-metal photodetectors. *Appl. Phys. Lett.* **2013**, *103*, 83114. [CrossRef]

45. Rabbani, M.G.; Patil, S.R.; Verma, A.; Villarreal, J.E.; Korgel, B.A.; Nekovei, R.; Khader, M.M.; Darling, R.B.; Anantram, M.P. Zero-bias photocurrents in highly-disordered networks of Ge and Si nanowires. *Nanotechnology* **2015**, *27*, 045201. [CrossRef]

46. Dalal, S.H.; Unalan, H.; Zhang, Y.; Hiralal, P.; Gangloff, L.; Flewitt, A.; Amaratunga, G.A.J.; Milne, W.I. Synthesis of ZnO nanowires for thin film network transistors. *Carbon Nanotub. Assoc. Devices* **2008**, *7037*, 172–178. [CrossRef]

47. Legallais, M.; Nguyen, T.T.T.; Cazimajou, T.; Mouis, M.; Salem, B.; Ternon, C. Material engineering of percolating silicon nanowire networks for reliable and efficient electronic devices. *Mater. Chem. Phys.* **2019**, *238*, 121871. [CrossRef]

48. Ternon, C.; Serre, P.; Lebrun, J.-M.; Brouzet, V.; Legallais, M.; David, S.; Luciani, T.; Pascal, C.; Baron, T.; Missiaen, J.-M. Low Temperature Processing to Form Oxidation Insensitive Electrical Contact at Silicon Nanowire/Nanowire Junctions. *Adv. Electron. Mater.* **2015**, *1*, 1500172. [CrossRef]

49. Shu, L.; Liang, R.; Rao, Z.; Fei, L.; Ke, S.; Wang, Y. Flexoelectric materials and their related applications: A focused review. *J. Adv. Ceram.* **2019**, *8*, 153–173. [CrossRef]

50. Liang, X.; Hu, S.; Shen, S. Effects of surface and flexoelectricity on a piezoelectric nanobeam. *Smart Mater. Struct.* **2014**, *23*, 035020. [CrossRef]

51. Wu, X.; Kulkarni, J.S.; Collins, G.; Petkov, N.; Almécija, D.; Boland, J.J.; Erts, D.; Holmes, J.D. Synthesis and Electrical and Mechanical Properties of Silicon and Germanium Nanowires. *Chem. Mater.* **2008**, *20*, 5954–5967. [CrossRef]

52. Feng, G.; Nix, W.D.; Yoon, Y.; Lee, C.J. A study of the mechanical properties of nanowires using nanoindentation. *J. Appl. Phys.* **2006**, *99*, 74304. [CrossRef]

53. Lee, B.; Rudd, R.E. First-principles calculation of mechanical properties of Si⟨001⟩ nanowires and comparison to nanomechanical theory. *Phys. Rev. B* **2007**, *75*, 195328. [CrossRef]

54. Park, S.; Kim, J.; Park, J.; Lee, J.; Choi, Y.; Kwon, O. Molecular dynamics study on size-dependent elastic properties of silicon nanocantilevers. *Thin Solid Films* **2005**, *492*, 285–289. [CrossRef]

55. Zhu, Y.; Xu, F.; Qin, Q.; Fung, W.Y.; Lu, W. Mechanical Properties of Vapor−Liquid−Solid Synthesized Silicon Nanowires. *Nano Lett.* **2009**, *9*, 3934–3939. [CrossRef]

56. Sadeghian, H.; Yang, C.-K.; Gavan, K.B.; Goosen, J.; Van Der Drift, E.W.J.M.; Van Der Zant, H.S.J.; Bossche, A.; French, P.J.; Van Keulen, F. Some considerations of effects-induced errors in resonant cantilevers with the laser deflection method. *J. Micromech. Microeng.* **2010**, *20*, 105027. [CrossRef]

57. Steighner, M.S.; Snedeker, L.P.; Boyce, B.L.; Gall, K.; Miller, D.C.; Muhlstein, C. Dependence on diameter and growth direction of apparent strain to failure of Si nanowires. *J. Appl. Phys.* **2011**, *109*, 33503. [CrossRef]

58. Sadeghian, H.; Yang, C.-K.; Goosen, J.; Bossche, A.; Staufer, U.; French, P.J.; Van Keulen, F. Effects of size and defects on the elasticity of silicon nanocantilevers. *J. Micromech. Microeng.* **2010**, *20*, 064012. [CrossRef]

59. Röhlig, C.-C.; Niebelschütz, M.; Brueckner, K.; Tonisch, K.; Ambacher, O.; Cimalla, V. Elastic properties of nanowires. *Phys. Status Solidi* **2010**, *247*, 2557–2570. [CrossRef]

60. Kim, Y.-J.; Son, K.; Choi, I.-C.; Park, W.I.; Jang, J.-I. Exploring Nanomechanical Behavior of Silicon Nanowires: AFM Bending Versus Nanoindentation. *Adv. Funct. Mater.* **2010**, *21*, 279–286. [CrossRef]

61. Wanekaya, A.K.; Chen, W.; Myung, N.V.; Mulchandani, A. Nanowire-Based Electrochemical Biosensors. *Electroanalysis* **2006**, *18*, 533–550. [CrossRef]

62. Zhao, X.; Wei, C.-M.; Yang, L.; Chou, M.-Y. Quantum Confinement and Electronic Properties of Silicon Nanowires. *Phys. Rev. Lett.* **2004**, *92*, 236805. [CrossRef] [PubMed]

63. Lu, A. Theoretical Study of Electronic and Electrical Properties of Silicon Nanowires. Public Health, 2007. Available online: http://lbms03.cityu.edu.hk/theses/c_ftt/phd-ap-b22687658f.pdf (accessed on 9 February 2022).

64. Sacconi, F.; Persson, M.P.; Povolotskyi, M.; Latessa, L.; Pecchia, A.; Gagliardi, A.; Balint, A.; Fraunheim, T.; Di Carlo, A. Electronic and transport properties of silicon nanowires. *J. Comput. Electron.* **2007**, *6*, 329–333. [CrossRef]

65. Saitta, A.M.; Buda, F.; Fiumara, G.; Giaquinta, P.V. Ab initiomolecular-dynamics study of electronic and optical properties of silicon quantum wires: Orientational effects. *Phys. Rev. B* **1996**, *53*, 1446–1451. [CrossRef]

66. Matsuda, Y.; Tahir-Kheli, J.; Goddard, W.A. Surface and Electronic Properties of Hydrogen Terminated Si [001] Nanowires. *J. Phys. Chem. C* **2011**, *115*, 12586–12591. [CrossRef]

67. Haick, H.; Hurley, P.T.; Hochbaum, A.I.; Yang, P.; Lewis, N.S. Electrical Characteristics and Chemical Stability of Non-Oxidized, Methyl-Terminated Silicon Nanowires. *J. Am. Chem. Soc.* **2006**, *128*, 8990–8991. [CrossRef] [PubMed]

68. Yuan, G.D.; Zhou, Y.B.; Guo, C.S.; Zhang, W.J.; Tang, Y.B.; Li, Y.Q.; Chen, Z.H.; He, Z.B.; Wang, P.F.; Bello, I.; et al. Tunable Electrical Properties of Silicon Nanowires via Surface-Ambient Chemistry. *ACS Nano* **2010**, *4*, 3045–3052. [CrossRef] [PubMed]

69. Zhao, J.; Buia, C.; Han, J.; Lu, J.P. Quantum transport properties of ultrathin silver nanowires. *Nanotechnology* **2003**, *14*, 501–504. [CrossRef]

70. Wiecha, P.R.; Cuche, A.; Arbouet, A.; Girard, C.; Colas des Francs, G.; Lecestre, A.; Paillard, V. Strongly Directional Scattering from Dielectric Nanowires. *ACS Photonics* **2018**, *4*, 2036–2046. [CrossRef]

71. Nair, P.R.; Alam, M.A. Design Considerations of Silicon Nanowire Biosensors. *IEEE Trans. Electron Devices* **2007**, *54*, 3400–3408. [CrossRef]

72. Legallais, M.; Nguyen, T.T.T.; Cazimajou, T.; Mouis, M.; Arjmand, T.; Salem, B.; Ternon, C. Role played by the nanowire/nanowire junctions in the electrical properties of semiconductor percolating silicon nanowire networks. *J. Appl. Phys.* **2020**, *128*, 204501. [CrossRef]

73. Basori, R.; Samanta, S. Diameter dependent threshold voltage modification of resistive state switching in organometallic single nanowire devices (diameter∼10–100 nm). *Appl. Phys. Lett.* **2018**, *113*, 123507. [CrossRef]

74. Nguyen, B.M.; Taur, Y.; Picraux, S.T.; Dayeh, S.A. Diameter-independent hole mobility in Ge/Si core/shell nanowire field effect transistors. *Nano Lett.* **2014**, *14*, 585–591.

75. Li, J.; He, G.; Ueno, H.; Jia, C.; Noji, H.; Qi, C.; Guo, X. Direct real-time detection of single proteins using silicon nanowire-based electrical circuits. *Nanoscale* **2016**, *8*, 16172–16176. [CrossRef]

76. Feng, S.; Yu, D.; Zhang, H.; Bai, Z.; Ding, Y. The growth mechanism of silicon nanowires and their quantum confinement effect. *J. Cryst. Growth* **2000**, *209*, 513–517. [CrossRef]

77. Baek, E.; Das, N.R.; Cannistraci, C.V.; Rim, T.; Bermúdez, G.S.C.; Nych, K.; Cho, H.; Kim, K.; Baek, C.-K.; Makarov, D.; et al. Intrinsic plasticity of silicon nanowire neurotransistors for dynamic memory and learning functions. *Nat. Electron.* **2020**, *3*, 398–408. [CrossRef]

78. Zhang, H.; Kikuchi, N.; Ohshima, N.; Kajisa, T.; Sakata, T.; Izumi, T.; Sone, H. Design and Fabrication of Silicon Nanowire-Based Biosensors with Integration of Critical Factors: Toward Ultrasensitive Specific Detection of Biomolecules. *ACS Appl. Mater. Interfaces* **2020**, *12*, 51808–51819. [CrossRef] [PubMed]

79. Ahoulou, S.; Perret, E.; Nedelec, J.-M. Functionalization and Characterization of Silicon Nanowires for Sensing Applications: A Review. *Nanomaterials* **2021**, *11*, 999. [CrossRef]

80. Calistri-Yeh, M.; Kramer, E.J.; Sharma, R.; Zhao, W.; Rafailovich, M.H.; Sokolov, A.J.; Brock, J.D. Thermal Stability of Self-Assembled Monolayers from Alkylchlorosilanes. *Langmuir* **1996**, *12*, 2747–2755. [CrossRef]

81. Steinbach, A.M.; Sandner, T.; Nilsen, M.; Hua, X.; Sivakumar, R.; Geiger, D.; Moeinian, A.; Strehle, S. The Electronic Properties of Silicon Nanowires during Their Dissolution under Simulated Physiological Conditions. *Appl. Sci.* **2019**, *9*, 804. [CrossRef]

82. Bashouti, M.Y.; Sardashti, K.; Ristein, J.; Christiansen, S. Kinetic study of H-terminated silicon nanowires oxidation in very first stages. *Nanoscale Res. Lett.* **2013**, *8*, 41. [CrossRef]

83. Liu, B.; Wang, Y.; Ho, T.-T.; Lew, K.-K.; Eichfeld, S.M.; Redwing, J.M.; Mayer, T.S.; Mohney, S.E. Oxidation of silicon nanowires for top-gated field effect transistors. *J. Vac. Sci. Technol. A: Vacuum Surfaces Films* **2008**, *26*, 370. [CrossRef]

84. Ma, D.D.D.; Lee, C.S.; Au, F.C.K.; Tong, S.Y.; Lee, S.T. Small-iameter Silicon Nanowire Surfaces. *Science* **2003**, *299*, 1874–1877. [CrossRef]

85. Bashouti, M.Y.; Sardashti, K.; Ristein, J.; Christiansen, S.H. Early stages of oxide growth in H-terminated silicon nanowires: Determination of kinetic behavior and activation energy. *Phys. Chem. Chem. Phys.* **2012**, *14*, 11877–11881. [CrossRef]

86. Büttner, C.C.; Zacharias, M. Retarded oxidation of Si nanowires. *Appl. Phys. Lett.* **2006**, *89*, 263106. [CrossRef]

87. Fazzini, P.-F.; Bonafos, C.; Claverie, A.; Hubert, A.; Ernst, T.; Respaud, M. Modeling stress retarded self-limiting oxidation of suspended silicon nanowires for the development of silicon nanowire-based nanodevices. *J. Appl. Phys.* **2011**, *110*, 033524. [CrossRef]

88. Harris, C.; O'Reilly, E. Nature of the band gap of silicon and germanium nanowires. *Phys. E Low-Dimens. Syst. Nanostruct.* **2006**, *32*, 341–345. [CrossRef]

89. Guichard, A.R.; Barsic, D.N.; Sharma, S.; Kamins, T.; Brongersma†, M.L. Tunable Light Emission from Quantum-Confined Excitons in TiSi$_2$-Catalyzed Silicon Nanowires. *Nano Lett.* **2006**, *6*, 2140–2144. [CrossRef] [PubMed]

90. Kumar, C. *UV-VIS and Photoluminescence Spectroscopy for Nanomaterials Characterization*; Springer: Berlin, Germany, 2013; pp. 1–599. [CrossRef]

91. Sivakov, V.A.; Voigt, F.; Berger, A.; Bauer, G.; Christiansen, S.H. Roughness of silicon nanowire sidewalls and room temperature photoluminescence. *Phys. Rev. B* **2010**, *82*, 125446. [CrossRef]

92. Gonchar, K.A.; Zubairova, A.A.; Schleusener, A.; Osminkina, L.A.; Sivakov, V. Optical Properties of Silicon Nanowires Fabricated by Environment-Friendly Chemistry. *Nanoscale Res. Lett.* **2016**, *11*, 357. [CrossRef]

93. Osminkina, L.A.; Gonchar, K.A.; Marshov, V.S.; Bunkov, K.V.; Petrov, D.V.; Golovan, L.A.; Talkenberg, F.; Sivakov, V.A.; Timoshenko, V. Optical properties of silicon nanowire arrays formed by metal-assisted chemical etching: Evidences for light localization effect. *Nanoscale Res. Lett.* **2012**, *7*, 524. [CrossRef]

94. Gonchar, K.A.; Golovan', L.A.; Timoshenko, V.Y.; Sivakov, V.A.; Christiansen, S. Effects of light localization in photoluminescence and Raman scattering in silicon nanostructures. *Bull. Russ. Acad. Sci. Phys.* **2010**, *74*, 1712–1714. [CrossRef]

95. Golovan, L.; Gonchar, K.; Osminkina, L.; Timoshenko, V.; Petrov, G.; Yakovlev, V. Coherent anti-Stokes Raman scattering in silicon nanowire ensembles. *Laser Phys. Lett.* **2011**, *9*, 145–150. [CrossRef]

96. Gonchar, K.A.; Osminkina, L.A.; Sivakov, V.; Lysenko, V.; Timoshenko, V. Optical properties of nanowire structures produced by the metal-assisted chemical etching of lightly doped silicon crystal wafers. *Semiconductors* **2014**, *48*, 1613–1618. [CrossRef]

97. Zabotnov, S.V.; Kholodov, M.M.; Georgobiani, V.A.; Presnov, D.E.; Golovan, L.A.; Kashkarov, P.K. Photon lifetime correlated increase of Raman scattering and third-harmonic generation in silicon nanowire arrays. *Laser Phys. Lett.* **2016**, *13*, 35902. [CrossRef]

98. Li, Y.; Wang, G.; Akbari-Saatlu, M.; Procek, M.; Radamson, H.H. Si and SiGe nanowire for micro-thermoelectric generator: A review of the current state of the art. *Front. Mater.* **2021**, *8*, 611078. [CrossRef]

99. Zhan, T.; Yamato, R.; Hashimoto, S.; Tomita, M.; Oba, S.; Himeda, Y.; Mesaki, K.; Takezawa, H.; Yokogawa, R.; Xu, Y.; et al. Miniaturized planar Si-nanowire micro-thermoelectric generator using exuded thermal field for power generation. *Sci. Technol. Adv. Mater.* **2018**, *19*, 443–453. [CrossRef] [PubMed]

100. Pennelli, G.; Macucci, M. Optimization of the thermoelectric properties of nanostructured silicon. *J. Appl. Phys.* **2013**, *114*, 214507. [CrossRef]

101. Pennelli, G.; Dimaggio, E.; Masci, A. Silicon Nanowires: A Breakthrough for Thermoelectric Applications. *Materials* **2021**, *14*, 5305. [CrossRef] [PubMed]

102. Paulo, A.S.; Bokor, J.; Howe, R.T.; He, R.; Yang, P.; Gao, D.; Carraro, C.; Maboudian, R. Mechanical elasticity of single and double clamped silicon nanobeams fabricated by the vapor-liquid-solid method. *Appl. Phys. Lett.* **2005**, *87*, 53111. [CrossRef]

103. Ponomareva, I.; Srivastava, D.; Menon, M. Thermal Conductivity in Thin Silicon Nanowires: Phonon Confinement Effect. *Nano Lett.* **2007**, *7*, 1155–1159. [CrossRef]

104. Feser, J.P.; Sadhu, J.S.; Azeredo, B.P.; Hsu, K.H.; Ma, J.; Kim, J.; Seong, M.; Fang, N.; Li, X.; Ferreira, P.M.; et al. Thermal conductivity of silicon nanowire arrays with controlled roughness. *J. Appl. Phys.* **2012**, *112*, 114306. [CrossRef]

105. Pop, E. Energy dissipation and transport in nanoscale devices. *Nano Res.* **2010**, *3*, 147–169. [CrossRef]

106. Zhao, Y.; Grüner, G. Nanonet as a scaffold with targeted functionalities. *J. Mater. Chem.* **2012**, *22*, 24983–24991. [CrossRef]

107. Cazimajou, T.; Mouis, M.; Legallais, M.; Nguyen, T.; Ternon, C.; Salem, B.; Ghibaudo, G. Analysis of the role of inter-nanowire junctions on current percolation effects in silicon nanonet field-effect transistors. *Solid-State Electron.* **2019**, *168*, 107725. [CrossRef]

108. Hu, L.; Hecht, D.S.; Grüner, G. Carbon Nanotube Thin Films: Fabrication, Properties, and Applications. *Chem. Rev.* **2010**, *110*, 5790–5844. [CrossRef]

109. Fata, N.; Mishra, S.; Xue, Y.; Wang, Y.; Hicks, J.; Ural, A. Effect of junction-to-nanowire resistance ratio on the percolation conductivity and critical exponents of nanowire networks. *J. Appl. Phys.* **2020**, *128*, 124301. [CrossRef]

110. Pike, G.E.; Seager, C.H. Percolation and conductivity: A computer study. I. *Phys. Rev. B* **1974**, *10*, 1421–1434. [CrossRef]

111. Seager, C.H.; Pike, G.E. Percolation and conductivity: A computer study. II. *Phys. Rev. B* **1974**, *10*, 1435–1446. [CrossRef]

112. Cao, Q.; Kim, H.-S.; Pimparkar, N.; Kulkarni, J.P.; Wang, C.; Shim, M.; Roy, K.; Alam, M.A.; Rogers, J.A. Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **2008**, *454*, 495–500. [CrossRef] [PubMed]

113. Ternon, C.; Serre, P.; Rey, G.; Holtzinger, C.; Periwal, P.; Martin, M.; Baron, T.; Stambouli, V.; Langlet, M. High aspect ratio semiconducting nanostructure random networks: Highly versatile materials for multiple applications. *Phys. Status Solidi (RRL)—Rapid Res. Lett.* **2013**, *7*, 919–923. [CrossRef]

114. Nguyen, T.T.T.; Cazimajou, T.; Legallais, M.; Arjmand, T.; Nguyen, V.H.; Mouis, M.; Salem, B.; Robin, E.; Ternon, C. Monolithic fabrication of nano-to-millimeter scale integrated transistors based on transparent and flexible silicon nanonets. *Nano Futur.* **2019**, *3*, 25002. [CrossRef]

115. Den Hertog, M.I.; Rouviere, J.L.; Dhalluin, F.; Gentile, P.; Ferret, P.; Ternon, C.; Baron, T. Gold Catalyzed Silicon Nanowires: Defects in the Wires and Gold on the Wires. In *Microscopy of Semiconducting Materials 2007*; Cullis, A.G., Midgley, P.A., Eds.; Springer Proceedings in Physics; Springer: Dordrecht, The Netherlands, 2008; Volume 120. [CrossRef]

116. Surawijaya, A.; Anshori, I.; Rohiman, A.; Idris, I.; Iskandar, F.; Abdullah, M. Gold Nanoparticles Assisted Silicon Nanowire Growth using Vapor Liquid Solid Method. *AIP Conf. Proc.* **2011**, *1415*, 36–38. [CrossRef]

117. Kumar, R.R.; Rao, K.N.; Phani, A. Growth of silicon nanowires by electron beam evaporation using indium catalyst. *Mater. Lett.* **2012**, *66*, 110–112. [CrossRef]

118. Jeong, H.; Park, T.; Seong, H.; Kim, M.; Kim, U.; Choi, H. Growth kinetics of silicon nanowires by platinum assisted vapour–liquid–solid mechanism. *Chem. Phys. Lett.* **2009**, *467*, 331–334. [CrossRef]

119. Djoumi, S.; Kail, F.; Chahed, L.; i Cabarrocas, P.R. Growth Study of Silicon Nanowires Synthesized Via Plasma-Assisted VLS Using Tin Catalysts. *Mod. Concepts Mater. Sci.* **2020**, *2*, 1–2. [CrossRef]

120. Brouzet, V.; Salem, B.; Periwal, P.; Rosaz, G.; Baron, T.; Bassani, F.; Gentile, P.; Ghibaudo, G. Fabrication and characterization of silicon nanowire p-i-n MOS gated diode for use as p-type tunnel FET. *Appl. Phys. A* **2015**, *121*, 1285–1290. [CrossRef]

121. Cui, Y.; Lieber, C.M. Functional Nanoscale Electronic Devices Assembled Using Silicon Nanowire Building Blocks. *Science* **2001**, *291*, 851–853. [CrossRef]

122. Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J.W.; Empedocles, S.; Goldman, J.L. High-performance thin-film transistors using semiconductor nanowires and nanoribbons. *Nature* **2003**, *425*, 274–278. [CrossRef] [PubMed]

123. Gentile, P.; Solanki, A.; Pauc, N.; Oehler, F.; Salem, B.; Rosaz, G.; Baron, T.; Den Hertog, M.; Calvo, V. Effect of HCl on the doping and shape control of silicon nanowires. *Nanotechnology* **2012**, *23*, 215702. [CrossRef] [PubMed]

124. Burchak, O.; Chenevier, P.; Reiss, P. Procede de Preparation de Nanofils de Silicium. Patent WO2015189827A1, 17 December 2015.

125. Burchak, O.; Keller, C.; Lapertot, G.; Salaün, M.; Danet, J.; Chen, Y.; Bendiab, N.; Pépin-Donat, B.; Lombard, C.; Faure-Vincent, J.; et al. Scalable chemical synthesis of doped silicon nanowires for energy applications. *Nanoscale* **2019**, *11*, 22504–22514. [CrossRef]

126. Keller, C.; Desrues, A.; Karuppiah, S.; Martin, E.; Alper, J.; Boismain, F.; Villevieille, C.; Herlin-Boime, N.; Haon, C.; Chenevier, P. Effect of Size and Shape on Electrochemical Performance of Nano-Silicon-Based Lithium Battery. *Nanomaterials* **2021**, *11*, 307. [CrossRef]

127. Heitsch, A.T.; Fanfair, D.D.; Tuan, H.-Y.; Korgel, B.A. Solution−Liquid−Solid (SLS) Growth of Silicon Nanowires. *J. Am. Chem. Soc.* **2008**, *130*, 5436–5437. [CrossRef]

128. Qin, L.; Park, S.; Huang, L.; Mirkin, C.A. On-Wire Lithography. *Science* **2005**, *309*, 113–116. [CrossRef]

129. Um, H.-D.; Kim, N.; Lee, K.; Hwang, I.; Seo, J.H.; Young, J.Y.; Duane, P.; Wober, M.; Seo, K. Versatile control of metal-assisted chemical etching for vertical silicon microwire arrays and their photovoltaic applications. *Sci. Rep.* **2015**, *5*, 11277. [CrossRef]

130. Huang, Y.; Duan, X.; Wei, Q.; Lieber, C.M. Directed Assembly of One-Dimensional Nanostructures into Functional Networks. *Science* **2001**, *291*, 630–633. [CrossRef] [PubMed]

131. Jia, C.; Lin, Z.; Huang, Y.; Duan, X. Nanowire Electronics: From Nanoscale to Macroscale. *Chem. Rev.* **2019**, *119*, 9074–9135. [CrossRef] [PubMed]

132. Park, J.; Shin, G.; Ha, J.S. Controlling orientation of V_2O_5 nanowires within micropatterns via microcontact printing combined with the gluing Langmuir–Blodgett technique. *Nanotechnology* **2008**, *19*, 395303. [CrossRef] [PubMed]

133. Tao, A.; Kim, F.; Hess, C.; Goldberger, J.; He, R.; Sun, Y.; Xia, A.Y.; Yang, P. Langmuir−Blodgett Silver Nanowire Monolayers for Molecular Sensing Using Surface-Enhanced Raman Spectroscopy. *Nano Lett.* **2003**, *3*, 1229–1233. [CrossRef]

134. Liu, X.; Long, Y.-Z.; Liao, L.; Duan, X.; Fan, Z. Large-Scale Integration of Semiconductor Nanowires for High-Performance Flexible Electronics. *ACS Nano* **2012**, *6*, 1888–1900. [CrossRef]

135. Yu, G.; Cao, A.; Lieber, C.M. Large-area blown bubble films of aligned nanowires and carbon nanotubes. *Nat. Nanotechnol.* **2007**, *2*, 372–377. [CrossRef]

136. Yu, G.; Li, X.; Lieber, C.M.; Cao, A. Nanomaterial-incorporated blown bubble films for large-area, aligned nanostructures. *J. Mater. Chem.* **2008**, *18*, 728–734. [CrossRef]

137. Zhang, J.; Cui, J.; Wang, X.; Wang, W.; Mei, X.; Yi, P.; Yang, X.; He, X. Recent Progress in the Preparation of Horizontally Ordered Carbon Nanotube Assemblies from Solution. *Phys. Status Solidi* **2018**, *215*, 1700719. [CrossRef]

138. Krebs, F.C. Roll-to-roll fabrication of monolithic large-area polymer solar cells free from indium-tin-oxide. *Sol. Energy Mater. Sol. Cells* **2009**, *93*, 1636–1641. [CrossRef]

139. Aziz, F.; Ismail, A.F. Spray coating methods for polymer solar cells fabrication: A review. *Mater. Sci. Semicond. Process.* **2015**, *39*, 416–425. [CrossRef]

140. Kopola, P.; Aernouts, T.; Guillerez, S.; Jin, H.; Tuomikoski, M.; Maaninen, A.; Hast, J. High efficient plastic solar cells fabricated with a high-throughput gravure printing method. *Sol. Energy Mater. Sol. Cells* **2010**, *94*, 1673–1680. [CrossRef]

141. Hoth, C.N.; Choulis, S.A.; Schilinsky, P.; Brabec, C.J. High Photovoltaic Performance of Inkjet Printed Polymer:Fullerene Blends. *Adv. Mater.* **2007**, *19*, 3973–3978. [CrossRef]

142. Voigt, M.M.; MacKenzie, R.; King, S.P.; Yau, C.P.; Atienzar, P.; Dane, J.; Keivanidis, P.; Zadrazil, I.; Bradley, D.D.; Nelson, J. Gravure printing inverted organic solar cells: The influence of ink properties on film quality and device performance. *Sol. Energy Mater. Sol. Cells* **2012**, *105*, 77–85. [CrossRef]

143. Roßkopf, D.; Strehle, S. Surface-controlled contact printing for nanowire device fabrication on a large scale. *Nanotechnology* **2016**, *27*, 185301. [CrossRef]

144. Yao, J.; Yan, H.; Lieber, C.M. A nanoscale combing technique for the large-scale assembly of highly aligned nanowires. *Nat. Nanotechnol.* **2013**, *8*, 329–335. [CrossRef]

145. Bensimon, A.; Simon, A.; Chiffaudel, A.; Croquette, V.; Heslot, F. Alignment and Sensitive Detection of DNA by a Moving Interface. *Science* **1994**, *265*, 2096–2098. [CrossRef]

146. Yao, J.; Yan, H.; Das, S.; Klemic, J.F.; Ellenbogen, J.C.; Lieber, C.M. Nanowire nanocomputer as a finite-state machine. *Proc. Natl. Acad. Sci. USA* **2014**, *111*, 2431–2435. [CrossRef]

147. Holland, L.; Bateman, S.K. Effects of oil vapour contamination on the adhesion of zinc sulphide films to glass and silica. *Br. J. Appl. Phys.* **1960**, *11*, 382–385. [CrossRef]

148. Wu, Z.; Chen, Z.; Du, X.; Logan, J.M.; Sippel, J.; Nikolou, M.; Kamaras, K.; Reynolds, J.R.; Tanner, D.B.; Hebard, A.F.; et al. Transparent, Conductive Carbon Nanotube Films. *Science* **2004**, *305*, 1273–1276. [CrossRef]

149. Aguirre, C.M.; Auvray, S.; Pigeon, S.; Izquierdo, R.; Desjardins, P.; Martel, R. Carbon nanotube sheets as electrodes in organic light-emitting diodes. *Appl. Phys. Lett.* **2006**, *88*, 183104. [CrossRef]

150. Ferrer-Anglada, N.; Kaempgen, M.; Skakalova, V.; Dettlaf-Weglikowska, U.; Roth, S. Synthesis and characterization of carbon nanotube-conducting polymer thin films. *Diam. Relat. Mater.* **2004**, *13*, 256–260. [CrossRef]

151. Muhl, S.; Aguilar Osorio, R.; Martínez Huitle, U.A. Transparent conductive carbon nanotube films. *Rev. Mex. Fis.* **2014**, *63*, 439–447.

152. Hu, L.; Hecht, D.S.; Grüner, G. Percolation in Transparent and Conducting Carbon Nanotube Networks. *Nano Lett.* **2004**, *4*, 2513–2517. [CrossRef]

153. Zhang, D.; Ryu, K.; Liu, X.; Polikarpov, E.; Ly, J.; Tompson, M.E.; Zhou, C. Transparent, Conductive, and Flexible Carbon Nanotube Films and Their Application in Organic Light-Emitting Diodes. *Nano Lett.* **2006**, *6*, 1880–1886. [CrossRef]

154. Serre, P.; Ternon, C.; Chapron, P.; Durlin, Q.; Francheteau, A.; Lantreibecq, A. Role of nanowire length in morphological and electrical properties of silicon nanonets. In Proceedings of the 2014 10th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME), Grenoble, France, 30 June–3 July 2014; pp. 9–12. [CrossRef]

155. Demes, T.; Ternon, C.; Morisot, F.; Riassetto, D.; Legallais, M.; Roussel, H.; Langlet, M. Mechanisms involved in the hydrothermal growth of ultra-thin and high aspect ratio ZnO nanowires. *Appl. Surf. Sci.* **2017**, *410*, 423–431. [CrossRef]

156. Aksoy, B.; Coskun, S.; Kucukyildiz, S.; Unalan, H.E. Transparent, highly flexible, all nanowire network germanium photodetectors. *Nanotechnology* **2012**, *23*, 325202. [CrossRef]

157. Wang, Y.; Feng, T.; Wang, K.; Qian, M.; Chen, Y.; Sun, Z. A Facile Method for Preparing Transparent, Conductive, and Paper-Like Silver Nanowire Films. *J. Nanomater.* **2011**, *2011*, 1–5. [CrossRef]

158. Assad, O.; Leshansky, A.M.; Wang, B.; Stelzner, T.; Christiansen, S.; Haick, H. Spray-Coating Route for Highly Aligned and Large-Scale Arrays of Nanowires. *ACS Nano* **2012**, *6*, 4702–4712. [CrossRef]

159. Kim, T.; Canlier, A.; Kim, G.H.; Choi, J.; Park, M.; Han, S.M. Electrostatic Spray Deposition of Highly Transparent Silver Nanowire Electrode on Flexible Substrate. *ACS Appl. Mater. Interfaces* **2012**, *5*, 788–794. [CrossRef]

160. Wang, M.C.; Gates, B.D. Directed assembly of nanowires. *Mater. Today* **2009**, *12*, 34–43. [CrossRef]

161. Thelander, C.; Agarwal, P.; Brongersma, S.; Eymery, J.; Feiner, L.; Forchel, A.; Scheffler, M.; Riess, W.; Ohlsson, B.; Gösele, U.; et al. Nanowire-based one-dimensional electronics. *Mater. Today* **2006**, *9*, 28–35. [CrossRef]

162. Chen, L.J. Silicon nanowires: The key building block for future electronic devices. *J. Mater. Chem.* **2007**, *17*, 4639–4643. [CrossRef]

163. Valizadeh, P. Field Effect Transistors, A Comprehensive Overview: From Basic Concepts to Novel Technologies. *F Eff. Transistors A Compr. Overv. Basic Concepts Nov. Technol.* **2016**, 1–457. [CrossRef]

164. Moore, G.M. Cramming more components onto integrated circuits with unit cost. *Electronics* **1965**, *38*, 114. Available online: https://newsroom.intel.com/wp-content/uploads/sites/11/2018/05/moores-law-electronics.pdf (accessed on 9 February 2022).

165. Inaba, S.; Okano, K.; Matsuda, S.; Fujiwara, M.; Hokazono, A.; Adachi, K.; Ohuchi, K.; Suto, H.; Fukui, H.; Shimizu, T.; et al. High performance 35 nm gate length CMOS with NO oxynitride gate dielectric and Ni salicide. *IEEE Trans. Electron Devices* **2002**, *49*, 2263–2270. [CrossRef]

166. Iwai, H.; Ohguro, T.; Ohmi, S.-I. NiSi salicide technology for scaled CMOS. *Microelectron. Eng.* **2002**, *60*, 157–169. [CrossRef]

167. Hu, J.; Odom, T.W.; Lieber, C.M. Chemistry and Physics in One Dimension: Synthesis and Properties of Nanowires and Nanotubes. *Accounts Chem. Res.* **1999**, *32*, 435–445. [CrossRef]

168. Lu, W.; Xie, P.; Lieber, C.M. Nanowire Transistor Performance Limits and Applications. *IEEE Trans. Electron Devices* **2008**, *55*, 2859–2876. [CrossRef]

169. Patolsky, F.; Zheng, G.; Lieber, C.M. Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species. *Nat. Protoc.* **2006**, *1*, 1711–1724. [CrossRef]

170. McIntyre, P.; Morral, A.F. Semiconductor nanowires: To grow or not to grow? *Mater. Today Nano* **2019**, *9*, 100058. [CrossRef]

171. Fasoli, A.; Milne, W. Overview and status of bottom-up silicon nanowire electronics. *Mater. Sci. Semicond. Process.* **2012**, *15*, 601–614. [CrossRef]

172. Aouida, S.; Zaghouani, R.B.; Bachtouli, N.; Bessais, B. Hydrogen passivation of silicon nanowire structures. *Appl. Surf. Sci.* **2016**, *370*, 49–52. [CrossRef]

173. Yuan, W.; Tutuncuoglu, G.; Mohabir, A.T.; Thorpe, R.; Feldman, L.C.; Filler, M.A.; Shan, J.W. Reducing Conductivity Variability in Si Nanowires via Surface Passivation for Nanoelectronics. *ACS Appl. Nano Mater.* **2021**, *4*, 3852–3860. [CrossRef]

174. Chen, K.-I.; Li, B.-R.; Chen, Y.-T. Silicon nanowire field-effect transistor-based biosensors for biomedical diagnosis and cellular recording investigation. *Nano Today* **2011**, *6*, 131–154. [CrossRef]

175. Weber, W.M.; Geelhaar, L.; Graham, A.P.; Unger, E.; Duesberg, G.S.; Liebau, M.; Pamler, W.; Chèze, C.; Riechert, H.; Lugli, P.; et al. Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts. *Nano Lett.* **2006**, *6*, 2660–2666. [CrossRef]

176. Dellas, N.S.; Schuh, C.J.; Mohney, S.E. Silicide formation in contacts to Si nanowires. *J. Mater. Sci.* **2012**, *47*, 6189–6205. [CrossRef]

177. Shkunov, M.; Rigas, G.; Constantinou, M. Solution-Processable Nanowire Field-Effect Transistors. In *Nanowires-New Insights*; IntechOpen: London, UK, 2017. [CrossRef]

178. Pregl, S.; Weber, W.M.; Nozaki, D.; Kunstmann, J.; Baraban, L.; Opitz, J.; Mikolajick, T.; Cuniberti, G. Parallel arrays of Schottky barrier nanowire field effect transistors: Nanoscopic effects for macroscopic current output. *Nano Res.* **2013**, *6*, 381–388. [CrossRef]

179. Islam, A.E. Variability and Reliability of Single-Walled Carbon Nanotube Field Effect Transistors. *Electronics* **2013**, *2*, 332–367. [CrossRef]

180. Shin, S.H.; Masuduzzaman, M.; Gu, J.; Wahab, M.A.; Conrad, N.; Si, M.; Ye, P.D.; Alam, A. Impact of nanowire variability on performance and reliability of gate-all-around III-V MOSFETs. *2013 IEEE Int. Electron Devices Meet.* **2013**, *7*, 188–191. [CrossRef]

181. Zheng, G.; Lu, W.; Jin, S.; Lieber, C.M. Synthesis and Fabrication of High-Performance n-Type Silicon Nanowire Transistors. *Adv. Mater.* **2004**, *16*, 1890–1893. [CrossRef]

182. Byon, K.; Tham, D.; Fischer, J.E.; Johnson, A.T. Systematic study of contact annealing: Ambipolar silicon nanowire transistor with improved performance. *Appl. Phys. Lett.* **2007**, *90*, 143513. [CrossRef]

183. Hayden, O.; Björk, M.T.; Schmid, H.; Riel, H.; Drechsler, U.; Karg, S.F.; Lörtscher, E.; Riess, W. Fully Depleted Nanowire Field-Effect Transistor in Inversion Mode. *Small* **2007**, *3*, 230–234. [CrossRef] [PubMed]

184. Rajeev, K.P.; Stolojan, C.O.V.; Constantinou, M.; Shkunov, M. Effect of Nanowire-dielectric Interface on the Hysteresis of Solution Processed Silicon Nanowire FETs. *Nanosci. Nanoeng.* **2017**, *5*, 17–24. [CrossRef]

185. Van, N.H.; Lee, J.-H.; Whang, D.; Kang, D.J. Low-Programmable-Voltage Nonvolatile Memory Devices Based on Omega-shaped Gate Organic Ferroelectric P(VDF-TrFE) Field Effect Transistors Using p-type Silicon Nanowire Channels. *Nano-Micro Lett.* **2014**, *7*, 35–41. [CrossRef] [PubMed]

186. Jung, Y.; Vacic, A.; Perea, D.E.; Picraux, S.T.; Reed, M. Minority carrier lifetime and surface effects in VLS-grown axial p-n junction silicon nanowires. *Adv. Mater.* **2011**, *23*, 4306–4311. [CrossRef]

187. Heo, K.; Park, J.W.; Yang, J.-E.; Koh, J.; Kwon, J.-H.; Jhon, Y.M.; Kim, M.; Jo, M.-H.; Hong, S. Large-scale assembly of highly flexible low-noise devices based on silicon nanowires. *Nanotechnology* **2010**, *21*, 145302. [CrossRef]

188. Celle, C.; Carella, A.; Mariolle, D.; Chevalier, N.; Rouvière, E.; Simonato, J.-P. Highly end-doped silicon nanowires for field-effect transistors on flexible substrates. *Nanoscale* **2010**, *2*, 677–680. [CrossRef]

189. McAlpine, M.; Friedman, R.; Lieber, C. High-Performance Nanowire Electronics and Photonics and Nanoscale Patterning on Flexible Plastic Substrates. *Proc. IEEE* **2005**, *93*, 1357–1363. [CrossRef]

190. Knopfmacher, O.; Tarasov, A.; Fu, W.; Wipf, M.; Niesen, B.; Calame, M.; Schönenberger, C. Nernst Limit in Dual-Gated Si-Nanowire FET Sensors. *Nano Lett.* **2010**, *10*, 2268–2274. [CrossRef]

191. Liu, Y.; Zhu, L.; Guo, L.; Zhang, H.; Xiao, H. Surface Passivation Performance of Atomic-Layer-Deposited Al_2O_3 on p-type Silicon Substrates. *J. Mater. Sci. Technol.* **2014**, *30*, 835–838. [CrossRef]

192. Liang, S.; He, G.; Wang, D.; Qiao, F. Atomic-layer-deposited (ALD) Al_2O_3 passivation dependent interface chemistry, band alignment and electrical properties of HfYO/Si gate stacks. *J. Mater. Sci. Technol.* **2018**, *35*, 769–776. [CrossRef]

193. Noor, M.O.; Krull, U.J. Silicon nanowires as field-effect transducers for biosensor development: A review. *Anal. Chim. Acta* **2014**, *825*, 1–25. [CrossRef] [PubMed]

194. Reddy, B.; Dorvel, B.R.; Go, J.; Nair, P.R.; Elibol, O.H.; Credo, G.M.; Daniels, J.S.; Chow, E.K.C.; Su, X.; Varma, M.; et al. High-k dielectric Al2O3 nanowire and nanoplate field effect sensors for improved pH sensing. *Biomed. Microdevices* **2011**, *13*, 335–344. [CrossRef] [PubMed]

195. Zhou, W.; Dai, X.; Fu, T.-M.; Xie, C.; Liu, J.; Lieber, C.M. Long Term Stability of Nanowire Nanoelectronics in Physiological Environments. *Nano Lett.* **2014**, *14*, 1614–1619. [CrossRef]

196. Klinghammer, S.; Rauch, S.; Pregl, S.; Uhlmann, P.; Baraban, L.; Cuniberti, G. Surface Modification of Silicon Nanowire Based Field Effect Transistors with Stimuli Responsive Polymer Brushes for Biosensing Applications. *Micromachines* **2020**, *11*, 274. [CrossRef]

197. Nikonov, A.M.; Naumova, O.V.; Generalov, V.M.; Safatov, A.S.; Fomin, B.I. Surface Preparation as a Step in the Fabrication of Biosensors Based on Silicon Nanowire Field-Effect Transistors: Review. *J. Surf. Investig. X-ray Synchrotron. Neutron. Tech.* **2020**, *14*, 337–346. [CrossRef]

198. Demes, T.; Morisot, F.; Legallais, M.; Calais, A.; Pernot, E.; Pignot-Paintrand, I.; Ternon, C.; Stambouli, V. DNA grafting on silicon nanonets using an eco-friendly functionalization process based on epoxy silane. *Mater Today Proc.* **2019**, *6*, 333–339. [CrossRef]

199. Nguyen, T.T.T.; Legallais, M.; Morisot, F.; Cazimajou, T.; Stambouli, V.; Mouis, M.; Ternon, C. First evidence of superiority of Si nanonet field effect transistors over multi-parallel Si nanowire ones in view of electrical DNA hybridization detection. *Mater. Res. Express* **2018**, *6*, 016301. [CrossRef]

200. Vallejo-Perez, M.; Ternon, C.; Spinelli, N.; Morisot, F.; Theodorou, C.; Jayakumar, G.; Hellström, P.-E.; Mouis, M.; Rapenne, L.; Mescot, X.; et al. Optimization of GOPS-Based Functionalization Process and Impact of Aptamer Grafting on the Si Nanonet FET Electrical Properties as First Steps towards Thrombin Electrical Detection. *Nanomaterials* **2020**, *10*, 1842. [CrossRef]

201. Celle, C.; Suspene, C.; Simonato, J.; Lenfant, S.; Ternisien, M.; Vuillaume, D. Self-assembled monolayers for electrode fabrication and efficient threshold voltage control of organic transistors with amorphous semiconductor layer. *Org. Electron.* **2009**, *10*, 119–126. [CrossRef]

202. Celle, C.; Suspène, C.; Ternisien, M.; Lenfant, S.; Guerin, D.; Smaali, K.; Lmimouni, K.; Simonato, J.-P.; Vuillaume, D. Interface dipole: Effects on threshold voltage and mobility for both amorphous and poly-crystalline organic field effect transistors. *Org. Electron.* **2014**, *15*, 729–737. [CrossRef]

203. Robert, D.; Yoshio, N. Front Matter. In *Handbook of Semiconductor Manufacturing Technology*, 2nd ed.; CRC Press: Boca Raton, FL, USA, 2007. [CrossRef]

204. Bhaskaran, M.; Sriram, S.; Holland, A.S.; du Plessis, J. Nickel silicide and titanium silicide formation: A comparison. *Smart Struct. Devices Syst. III* **2006**, *6414*, 64141B. [CrossRef]

205. Chen, L.J. *Institution of Electrical Engineers. Silicide Technology for Integrated Circuits*; Institution of Electrical Engineers: London, UK, 2004.

206. Lavoie, C.; D'Heurle, F.; Detavernier, C.; Cabral, C. Towards implementation of a nickel silicide process for CMOS technologies. *Microelectron. Eng.* **2003**, *70*, 144–157. [CrossRef]

207. Murarka, S.P. *Silicides for VLSI Applications*; Academic Press: Cambridge, MA, USA, 1983.

208. Sze, S.M. *Physics of Semiconductor Devices*, 3rd ed.; Wiley: New York, NY, USA, 2006.

209. Connétable, D.; Thomas, O. First-principles study of nickel-silicides ordered phases. *J. Alloys Compd.* **2011**, *509*, 2639–2644. [CrossRef]

210. Zhang, S.; Östling, M.; Zhang, S.; Östling, M. Metal Silicides in CMOS Technology: Past, Present, and Future Trends Metal Silicides in CMOS Technology: Past, Present, and Future Trends. *Crit. Rev. Solid State Mater. Sci.* **2003**, *28*, 1–129. [CrossRef]

211. Ryuji, T. A Study on Formation of High Resistivity Phases of Nickel Silicide at Small Area and its Solution for Scaled CMOS Devices. Ph.D. Thesis, Tokyo Institute of Technology, Tokyo, Japan, 2013.

212. Mongillo, M. Transport Properties and Functional Devices on CVD Grown Silicon Nanowires. Ph.D. Thesis, Université Joseph-Fourier-Grenoble I, Grenoble, France, 2010.

213. Chou, Y.-C.; Wu, W.-W.; Chen, L.-J.; Tu, K.-N. Homogeneous Nucleation of Epitaxial CoSi2 and NiSi in Si Nanowires. *Nano Lett.* **2009**, *9*, 2337–2342. [CrossRef] [PubMed]

214. Chou, Y.-C.; Lu, K.-C.; Tu, K. Nucleation and growth of epitaxial silicide in silicon nanowires. *Mater. Sci. Eng. R Rep.* **2010**, *70*, 112–125. [CrossRef]

215. Katsman, A.; Beregovsky, M.; Yaish, Y.E. Formation and Evolution of Nickel Silicide in Silicon Nanowires. *IEEE Trans. Electron Devices* **2014**, *61*, 3363–3371. [CrossRef]

216. Katsman, A.; Yaish, Y.; Beregovsky, M. From Contact to Diffusion Controlled Growth of Nickel Silicides in Silicon Nanowires. *Defect Diffus. Forum* **2012**, *323–325*, 427–432. [CrossRef]

217. Hsu, H.-F.; Huang, W.-R.; Chen, T.-H.; Wu, H.-Y.; Chen, C.-A. Fabrication of Ni-silicide/Si heterostructured nanowire arrays by glancing angle deposition and solid state reaction. *Nanoscale Res. Lett.* **2013**, *8*, 224. [CrossRef]

218. Dellas, N.S.; Liu, B.Z.; Eichfeld, S.M.; Eichfeld, C.M.; Mayer, T.S.; Mohney, S.E. Orientation dependence of nickel silicide formation in contacts to silicon nanowires. *J. Appl. Phys.* **2009**, *105*, 94309. [CrossRef]

219. Lin, Y.-C.; Chen, Y.; Xu, D.; Huang, Y. Growth of Nickel Silicides in Si and Si/SiOx Core/Shell Nanowires. *Nano Lett.* **2010**, *10*, 4721–4726. [CrossRef]

220. Otaga, K.; Sutter, E.; Zhu, X.; Hofmann, S. Ni-Silicide growth kinetics in Si and Si/SiO2core/shell nanowires. *Nanotechnology* **2011**, *22*, 365305. [CrossRef]

221. Chen, Y.; Lin, Y.-C.; Zhong, X.; Cheng, H.-C.; Duan, X.; Huang, Y. Kinetic Manipulation of Silicide Phase Formation in Si Nanowire Templates. *Nano Lett.* **2013**, *13*, 3703–3708. [CrossRef] [PubMed]

222. Tang, W.; Dayeh, S.A.; Picraux, S.T.; Huang, J.Y.; Tu, K.-N. Ultrashort Channel Silicon Nanowire Transistors with Nickel Silicide Source/Drain Contacts. *Nano Lett.* **2012**, *12*, 3979–3985. [CrossRef] [PubMed]

223. Weber, W.M.; Geelhaar, L.; Unger, E.; Chèze, C.; Kreupl, F.; Riechert, H.; Lugli, P. Silicon to nickel-silicide axial nanowire heterostructures for high performance electronics. *Phys. Status Solidi* **2007**, *244*, 4170–4175. [CrossRef]

224. Chou, Y.C.; Wu, W.W.; Lee, C.Y.; Liu, C.Y.; Chen, L.J.; Tu, K.N. Heterogeneous and Homogeneous Nucleation of Epitaxial NiSi2 in [110] Si Nanowires. *J. Phys. Chem. C* **2011**, *115*, 397–401. [CrossRef]

225. Song, J.; Matsumoto, K.; Kakushima, K.; Kataoka, Y.; Nishiyama, A.; Sugii, N.; Wakabayashi, H.; Tsutsui, K.; Natori, K.; Iwai, H. Resistivity of Ni silicide nanowires and its dependence on Ni film thickness used for the formation. *ECS Trans.* **2013**, *58*, 87–91. [CrossRef]

226. Legallais, M.; Nguyen, T.; Mouis, M.; Salem, B.; Robin, E.; Chenevier, P.; Ternon, C. An innovative large scale integration of silicon nanowire-based field effect transistors. *Solid-State Electron.* **2018**, *143*, 97–102. [CrossRef]

227. Mongillo, M.; Spathis, P.; Katsaros, G.; Gentile, P.; Sanquer, M.; De Franceschi, S. Joule-Assisted Silicidation for Short-Channel Silicon Nanowire Devices. *ACS Nano* **2011**, *5*, 7117–7123. [CrossRef]

228. Yan, H.; Xing, Y.; Hang, Q.; Yu, D.; Wang, Y.; Xu, J.; Xi, Z.; Feng, S. Growth of amorphous silicon nanowires via a solid–liquid–solid mechanism. *Chem. Phys. Lett.* **2000**, *323*, 224–228. [CrossRef]

229. Um, H.-D.; Solanki, A.; Jayaraman, A.; Gordon, R.G.; Habbal, F. Electrostatically Doped Silicon Nanowire Arrays for Multispectral Photodetectors. *ACS Nano* **2019**, *13*, 11717–11725. [CrossRef] [PubMed]

230. Li, Q.; Koo, S.-M.; Edelstein, M.D.; Suehle, J.S.; Richter, C.A. Silicon nanowire electromechanical switches for logic device application. *Nanotechnology* **2007**, *18*, 315202. [CrossRef]

231. Zhu, H.; Bonevich, J.E.; Li, H.; Richter, C.A.; Yuan, H.; Kirillov, O.; Li, Q. Discrete charge states in nanowire flash memory with multiple Ta2O5 charge-trapping stacks. *Appl. Phys. Lett.* **2014**, *104*, 233504. [CrossRef]

232. Baraban, L.; Ibarlucea, B.; Baek, E.; Cuniberti, G. Hybrid Silicon Nanowire Devices and Their Functional Diversity. *Adv. Sci.* **2019**, *6*, 1900522. [CrossRef]

233. Park, S.J.; Jeon, D.-Y.; Piontek, S.; Grube, M.; Ocker, J.; Sessi, V.; Heinzig, A.; Trommer, J.; Kim, G.-T.; Mikolajick, T.; et al. Reconfigurable Si Nanowire Nonvolatile Transistors. *Adv. Electron. Mater.* **2017**, *4*, 1700399. [CrossRef]

234. Yoo, J.; Kim, Y.; Lim, D.; Kim, S. Electrical characteristics of silicon nanowire CMOS inverters under illumination. *Opt. Express* **2018**, *26*, 3527–3534. [CrossRef]

235. Singh, P.; Delhi, N. Properties and Transistor Applications of Silicon Nanowires. *Int. J. Phys. Appl.* **2020**, *12*, 11–19.

236. Chen, Z.H.; Jie, J.S.; Luo, L.B.; Wang, H.; Lee, C.-S.; Lee, S.T. Applications of silicon nanowires functionalized with palladium nanoparticles in hydrogen sensors. *Nanotechnology* **2007**, *18*, 345502. [CrossRef]

237. Pourkiaei, S.M.; Ahmadi, M.H.; Sadeghzadeh, M.; Moosavi, S.; Pourfayaz, F.; Chen, L.; Pour Yazdi, M.A.; Kumar, R. Thermoelectric cooler and thermoelectric generator devices: A review of present and potential applications, modeling and materials. *Energy* **2019**, *186*, 115849. [CrossRef]

238. Fonseca, L.; Donmez-Noyan, I.; Dolcet, M.; Estrada-Wiese, D.; Santander, J.; Salleras, M.; Gadea, G.; Pacios, M.; Sojo, J.-M.; Morata, A.; et al. Transitioning from Si to SiGe Nanowires as Thermoelectric Material in Silicon-Based Microgenerators. *Nanomaterials* **2021**, *11*, 517. [CrossRef] [PubMed]