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# **Steep Subthreshold Swing and Enhanced Illumination Stability InGaZnO Thin-Film Transistor by Plasma Oxidation on Silicon Nitride Gate Dielectric**

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Abstract: In this paper, an InGaZnO thin-film transistor (TFT) based on plasma oxidation of silicon nitride (SiN<sub>x</sub>) gate dielectric with small subthreshold swing (SS) and enhanced stability under negative bias illumination stress (NBIS) have been investigated in detail. The mechanism of the high-performance InGaZnO TFT with plasma-oxidized SiN<sub>x</sub> gate dielectric was also explored. The X-ray photoelectron spectroscopy (XPS) results confirmed that an oxygen-rich layer formed on the surface of the SiN<sub>x</sub> layer and the amount of oxygen vacancy near the interface between SiN<sub>x</sub> and InGaZnO layer was suppressed via pre-implanted oxygen on SiN<sub>x</sub> gate dielectric before deposition of the InGaZnO channel layer. Moreover, the conductance method was employed to directly extract the density of the interface trap ( $D_{it}$ ) in InGaZnO TFT with plasma oxidation exhibited a field-effect mobility of 16.46 cm<sup>2</sup>/V·s, threshold voltage ( $V_{th}$ ) of -0.10 V,  $I_{on}/I_{off}$  over 10<sup>8</sup>, SS of 97 mV/decade, and  $V_{th}$  shift of -0.37 V after NBIS. The plasma oxidation on SiN<sub>x</sub> gate dielectric provides a novel approach for suppressing the interface trap for high-performance InGaZnO TFT.

Keywords: thin-film transistor; InGaZnO; interface traps; plasma oxidation; NBIS

## 1. Introduction

In recent decades, InGaZnO based oxide TFTs have been widely investigated to compete with conventional silicon-based TFTs for active matrix organic light-emitting display (AMOLED) due to its advantages of high field-effect mobility [1], excellent uniformity for large-scaled display panels [2], and high optical transparency in the visible spectrum [3]. Moreover, the InGaZnO shows great penitential for the application of flexible electronic devices owing to its insensitive to intrinsically distorted metal-oxygen-metal chemical bonds [4] and low-temperature fabrication process [5–7]. To investigate the further potential for advanced electronic applications such as high refresh rate display and low power consuming devices, the field-effect mobility, stability, and SS should be critically considered. Among the strategies of boosting the performance of InGaZnO TFTs, the modification of interface between InGaZnO and gate dielectric is one of the effective ways [8–10]. The plasma treatment technique has been widely applied to tailor the surface properties of semiconductors [11,12]. Additionally, the interface between the post-deposited thin film and the former layer could also be affected by plasma treatment. In this work, the plasma oxidation on SiN<sub>x</sub> gate dielectric for InGaZnO TFT with fairly low SS and excellent illumination stability has been reported. The effect of plasma oxidation on the electrical characteristic, interface trap density, and chemical component for InGaZnO have been investigated in detail. The proposed plasma oxidation method on SiN<sub>x</sub> gate dielectric provides a novel approach for achieving the high-performance InGaZnO TFT.



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### 2. Materials and Methods

The InGaZnO TFT was fabricated on the 210 nm-thickness SiN<sub>x</sub> gate dielectric with heavily n-doped (As) Si as a gate electrode. The  $SiN_x$  layer was deposited by low-pressure chemical vapor deposition at the pressure of 160 mTorr from NH<sub>3</sub> and SiCl<sub>2</sub>H<sub>2</sub> precursor with the gas flow of 40 sccm and 175 sccm, respectively. The as-deposit  $SiN_x$  layer was treated in the oxygen plasma for 60 s. The oxygen plasma was generated by the capacity coupling configuration via a radio frequency power supply (Seren, R301) and matching box with a fixed power of 40 W under DC bias about 180 V at a constant pressure of 5 mTorr. The whole substrate was rotated at 5 revolutions per minute to keep the uniformity during the whole plasma oxidation process. Afterwards, a 30 nm thick InGaZnO channel layer was deposited by magnetron sputtering from an InGaZnO target (1:1:1 at%) with a power of 200 W in the same chamber without exposure to the atmosphere. Then, the source/drain electrodes were thermal evaporated Al metal via the shadow mask process with a channel length (L) of 100 µm and width (W) of 1000 µm, respectively. Finally, the InGaZnO TFT with plasma oxidation SiNx gate dielectric (hereinafter referred to as 'POG. TFT') was postannealed at 250 °C in air for 1 h. The reference sample (hereinafter referred to as 'Ref. TFT') was with the same fabrication sequence except for plasma oxidation on SiN<sub>x</sub> dielectric. The process flow diagram and structure of InGaZnO TFTs in this work are shown in Figure 1. The electronic characteristics were evaluated using a source-meter unit (2636B, Keithley, Beaverton, OR, USA) and an LCR meter (IM3536, Hioki, Japan). The chemical status of the thin films was analyzed by XPS (Nexsa, Thermo Scientific, Waltham, MA, USA) with all the XPS data calibrated by C1s BE at 284.8 eV. Surface morphology was performed by the atomic force microscope (AFM, Dimension Icon, Bruker, Billerica, Germany).



Figure 1. Process flow diagram and structure of InGaZnO TFT in this work.

#### 3. Results

Figure 2a shows the transfer characteristics at  $V_{ds} = 10$  V while the  $V_{gs}$  was swept from -5 V to 20 V with a step of 0.125 V for POG. TFT and Ref. TFT.

The field-effect mobility in saturation region is extracted from the following equation:

$$\mu_{FE} = 2L/WC_{ox} \left( d\sqrt{I_{ds}}/dV_{gs} \right)^2 \tag{1}$$

and the SS is calculated by [13]:

$$SS = min(dV_{gs}/dlogI_{ds})$$
<sup>(2)</sup>

where  $C_{ox}$ , *L*, *W*,  $I_{ds}$ , and  $V_{gs}$  are the gate capacitance per unit area, channel length, channel width, current of drain to source, and gate bias voltage, respectively. All the extracted parameters are summarized in Table 1.



**Figure 2.** (a) Transfer characteristic curves for Ref. TFT and POG. TFT. The surface morphology for  $SiN_x$  (b) without plasma oxidation and (c) with plasma oxidation. (d) The atomic ratio for the surface of  $SiN_x$  thin film without/with plasma oxidation.

Table 1. Electrical parameters for InGaZnO TFT with/without SiN<sub>x</sub> surface plasma oxidation.

Device	Mobility (cm <sup>2</sup> /V·s)	$V_{th}$ (V)	SS (mV/Decade)	$I_{on}/I_{off}$
Ref. TFT	10.64	1.95	312	$1.68  imes 10^7$
POG. TFT	16.46	-0.10	97	$3.99  imes 10^8$

Compared with the Ref. TFT, the mobility of POG. TFT increased from 10.64  $\text{cm}^2/\text{V}\cdot\text{s}$ to 16.46 cm<sup>2</sup>/V·s and the  $V_{th}$  slightly shifted from 1.95 V to -0.10 V. The SS has an obvious decrease from 312 mV/decade to 97 mV/decade. Generally, the value of SS is dominated by the density of trap state in semiconductor bulk and interface trap between semiconductor and gate dielectric. The roughness of the gate dielectric could directly influence the interface between the InGaZnO and dielectric [14–16]. Hence, to investigate the condition of the interface, the AFM topography was obtained for the SiN<sub>x</sub> sample with/without plasma oxidation under the identical process condition as described before, as shown in Figure 2b,c. The value of the surface roughness is decreased from 1.23 nm to 0.95 nm after plasma oxidation. The large cluster  $SiN_x$  or absorbed carbon contaminant could be partly peered off from the surface of the  $SiN_x$  by the plasma bombardment which provides a smoother surface for the following sputtering of InGaZnO. Different from using electron cyclotron resonance (ECR) remote plasma to treat the thin film [17], capacitive coupling was used to provide  $O_2$  plasma with a stronger bombardment effect to treat  $SiN_x$  insulators. These strongly bombarded  $O_2$  plasmas would treat the SiN<sub>x</sub> insulators more adequately. To further verify the impact on elements composition after plasma oxidation, the elements composition by XPS for the surface of  $SiN_x$  thin film without/with plasma oxidation is shown in Figure 2d. For the sample of  $SiN_x$  without plasma oxidation, the oxygen atoms are mainly attributed to the surface absorbed oxygen from the environment on the surface of SiN<sub>x</sub>. After plasma oxidation, the O atoms ratio increased from 25.0% to 38.2%, the Si-O bonding would be formed on the surface of  $SiN_x$  thin film. To verify this speculation, the XPS spectra of the Si2p in the surface of SiN<sub>x</sub> thin film were also measured. As shown in Figure 3, the Si2p binding energy on the surface of  $SiN_x$  at 102.5 eV (with plasma oxidation). This binding energy of Si2p is between those of the  $Si_3N_4$  (101.7 eV) and  $SiO_2$  (103.5 eV), which indicate the formation of Si-O bonding on the surface of  $SiN_x$  thin film with plasma

oxidation. Since the  $SiN_x$  thin film was mounted on the anode of the plasma generator in this work, an electric field point to the substrate could form on the  $SiN_x$  surface. As a result, the cations in the plasma such as  $O^{2+}$  or  $O^+$  could sustain surface bombardment, which causes the Si-N bonds to break and oxygen atoms could substitute partly nitrogen atoms to form an oxygen-rich layer on the  $SiN_x$  surface. In addition, the carbon atoms ratio has also been reduced after plasma treatment. Such carbon is mainly induced by the inevitable contamination from the vacuum chamber or transfer process. Since the carbon has been reported as an electron trap in InGaZnO [18], the reduction of carbon on the SiN\_x surface could also increase the mobility and meliorate the SS of the InGaZnO TFT.



Figure 3. Si2p XPS results on the surface  $SiN_x$  film without and with plasma oxidation.

Furthermore, the influence of  $SiN_x$  surface plasma oxidation on the post-deposit InGaZnO layer was evaluated by the O1s XPS profile at the interface between  $SiN_x$  and InGaZnO for the sample of with/without plasma oxidation. Figure 4a,b shows the XPS spectra of the O1s core level in InGaZnO near the interface between SiN<sub>x</sub> and InGaZnO. The O1s peak of XPS spectra is deconvoluted into three peaks with a binding energy of about 530.3 eV, 531.3 eV, and 532.3 eV. The main peak centered at about 530 eV ( $O_L$ ) is related to the lattice oxygen. The peak centered at 531.3 eV (O<sub>M</sub>) and 532.3 eV (O<sub>H</sub>) is related to the oxygen vacancies and -OH hydroxide oxygen [19,20], respectively. The area ratio of  $O_L:O_M:O_H$  for the sample without plasma oxidation and with oxidation is about 1:0.25:0.10 and 1:0.18:0.12, respectively. This result indicates that the amount of oxygen vacancies in a-InGaZnO near the interface between  $SiN_x$  and InGaZnO is decreased after surface plasma oxidation of the  $SiN_x$  layer. This phenomenon could be explained by the following mechanism. After InGaZnO layer deposition, the thermal post-anneal process could cause the oxygen atoms near the interface to diffuse from the InGaZnO layer into the  $SiN_x$  layer, which is driven by the oxygen concentration gradient. Such a diffusion process could be partly restrained by reducing the concentration gradient via pre-implantation oxygen atoms at the SiNx surface leading to a reduction in oxygen vacancies in InGaZnO near the interface between  $SiN_x$  and the InGaZnO layer. Since the oxygen vacancy is considered as the origin of the defects in InGaZnO [21,22], it could be deduced that the density of interface traps in InGaZnO TFTs after O<sub>2</sub> plasma treatment should be decreased. On the other hand, the reduction in oxygen vacancy only near the interface between  $SiN_x$  and the InGaZnO layer would not significantly decrease the carrier concentration in the InGaZnO layer. Hence, the SS should also be decreased and the mobility should be increased, which is consistent with the decrease in the extracted value of SS and the increase in mobility from transfer curves of TFTs in Table 1.



Figure 4. XPS results for surface of  $SiN_x$  thin film (a) without (b) with plasma oxidation.

Since light illumination is inevitable during the display panel working, the NBIS test should be critically considered for InGaZnO TFTs. Furthermore, the result of NBIS could also reflect the interface status in InGaZnO TFT. Therefore, the NBIS tests were performed for both Ref. TFT and POG. TFT under a blue light-emitting diode (LED) illumination with a central wavelength of about 480 nm at full width at half maximum of 10 nm. The LED spectrum was assessed by a spectroradiometer (SpectraScan, PR-655), as shown in Figure 5c. Figure 5a, b represents the NBIS results for Ref. TFT and POG. TFT. The  $V_{ds}$ and  $V_{gs}$  were fixed at 0 V and -10 V, respectively. The threshold voltage shift ( $\Delta V_{th}$ ) after 7200 s NBIS is -4.75 V for Ref. TFT and dramatically decreased to -0.37 V for POG. TFT. During the NBIS test, the holes and electrons are generated by the light illumination, while the oxygen vacancy could act as the hole trap to capture the photoinduced holes which are likely to drift toward the channel/dielectric interface under negative gate bias, resulting in NBIS instability in InGaZnO TFTs [23,24]. Therefore, owing to the effective decrease in the amount of oxygen vacancies near the interface between InGaZnO and  $SiN_x$ by plasma oxidation, the holes trapped by interfacial traps could also be reduced, resulting in a smaller  $\Delta V_{th}$  after NBIS.



**Figure 5.** The curves of transfer characteristic before/after NBIS test for (**a**) Ref. TFT and (**b**) POG. TFT; (**c**) spectrum of blue LED used in NBIS test; (**d**)  $G_p/\omega$  as the function of frequency for Ref. and POG. MOS capacitor.

To directly obtain the  $D_{it}$  between SiN<sub>x</sub> gate dielectric and the InGaZnO layer, the conductance method [25] was employed. This small-signal steady-state method has been widely used to analyze the properties of the interface trap owing to its accuracy and sensitivity in extracting the  $D_{it}$ . The  $D_{it}$  can be calculated from the equivalent parallel conductive ( $G_p$ ) divided by  $\omega$  from the following equation:

$$G_p/\omega = q\omega\tau_{it}D_{it}/\left[1 + (\omega\tau_{it})^2\right]$$
(3)

The  $G_p/\omega$  can be directly calculated from the measured equivalent parallel conductance ( $G_m$ ) and measured capacitance ( $C_m$ ) by the following express:

$$G_p/\omega = \omega G_m C_{ox}^2 / \left[ G_m^2 + \omega^2 (C_{ox} - C_m)^2 \right]$$
(4)

where  $C_{ox}$  is capacitor per unit area. At maximum  $Gp/\omega$ , the  $\omega$  is equal to  $1/\tau it$ , the  $D_{it}$  can be expressed by the measured maximum conductance as:

$$D_{it} = 2/q \left( G_p / \omega \right)_{max} \tag{5}$$

Two metal-oxide-semiconductor (MOS) capacitors have been fabricated with a similar structure except for the plasma oxidation on the SiN<sub>x</sub> surface. The  $G_p/\omega$  as a function of frequency is shown in Figure 5d. The inset is the structure of the MOS capacitor. The extracted  $D_{it}$  is  $3.02 \times 10^{12}$  cm<sup>-2</sup>·eV<sup>-1</sup> and  $1.45 \times 10^{12}$  cm<sup>-2</sup>·eV<sup>-1</sup> for Ref. MOS and POG. MOS capacitors, respectively. This result also proved that the interface traps at SiN<sub>x</sub>/InGaZnO are reduced by the SiN<sub>x</sub> surface plasma oxidation, which is consistent with the aforementioned XPS and NBIS results. Table 2 represents the performance metrics of InGaZnO TFT in this work and other reported SiN<sub>x</sub>-related InGaZnO TFTs. Among all SiN<sub>x</sub>-based InGaZnO TFTs, the TFT from our work exhibits a combination of high  $I_{on}/I_{off}$  and the lowest SS.

**Table 2.** Performance metrics of InGaZnO TFT in this work and other reported SiN<sub>x</sub>-related InGaZnO TFTs.

Reference	Mobility (cm <sup>2</sup> /V·s)	$V_{th}$ (V)	SS (mV/decade)	Ion/Ioff
This work	16.46	-0.10	97	$3.99  imes 10^8$
[26]	10.9	2.0	400	$2 imes 10^8$
[27]	8.79	0.81	160	$3 imes 10^8$
[28]	14.43	-1.25	240	—
[29]	18.1	3.4	137	$1.1 imes10^8$

#### 4. Conclusions

In this work, we demonstrated an a-InGaZnO TFT with plasma oxidation SiN<sub>x</sub> gate dielectric. With plasma oxidation of SiN<sub>x</sub> gate dielectric, the SS and  $\Delta V_{th}$  under NBIS were significantly improved from 312 mV/decade to 97 mV/decade and -4.75 V to -0.37 V, respectively. The plasma oxidation on SiN<sub>x</sub> could provide a smoother surface and form an oxygen-rich layer at the SiN<sub>x</sub>/InGaZnO interface. The XPS result indicates that the amount of oxygen vacancy near the SiN<sub>x</sub>/InGaZnO interface was effectively reduced after plasma oxidation. Furthermore, the interface trap density has been extracted by conductance method, which shows a decrease from  $3.02 \times 10^{12}$  cm<sup>-2</sup>·eV<sup>-1</sup> to  $1.45 \times 10^{12}$  cm<sup>-2</sup>·eV<sup>-1</sup> after plasma oxidation. The plasma oxidation on SiN<sub>x</sub> gate dielectric in this work provides a potential approach for suppressing the interface trap in SiN<sub>x</sub> based InGaZnO TFT for an advanced electronic application.

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# References

- Lee, J.S.; Chang, S.; Koo, S.-M.; Lee, S.Y. High-Performance InGaZnO TFT with ZrO<sub>2</sub> Gate Dielectric Fabricated at Room Temperature. *IEEE Electron Device Lett.* 2010, 31, 225–227. [CrossRef]
- Jariwala, D.; Sangwan, V.K.; Seo, J.-W.T.; Xu, W.C.; Smith, J.; Kim, C.H.; Lauhon, L.J.; Marks, T.J.; Hersam, M.C. Large-Area, Low-Voltage, Antiambipolar Heterojunctions from Solution-Processed Semiconductors. *Nano Lett.* 2015, 15, 416–421. [CrossRef] [PubMed]
- 3. Wang, Y.; Liu, S.W.; Sun, X.W.; Zhao, J.L.; Goh, G.K.L.; Vu, Q.V.; Yu, H.Y. Highly transparent solution processed In-Ga-Zn oxide thin films and thin film transistors. *J. Sol.-Gel. Sci. Technol.* **2010**, *55*, 322–327. [CrossRef]
- 4. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* 2004, 432, 488–492. [CrossRef] [PubMed]
- 5. Yabuta, H.; Sano, M.; Abe, K.; Aiba, T.; Den, T.; Kumomi, H. High-mobility thin-film transistor with amorphous InGaZnO<sub>4</sub> channel fabricated by room temperature rf-magnetron sputtering. *Appl. Phys. Lett.* **2006**, *89*, 112123. [CrossRef]
- Chiu, C.J.; Chang, S.P.; Chang, S.J. High-Performance InGaZnO Thin-Film Transistor Using Ta<sub>2</sub>O<sub>5</sub> Gate Dielectric. *IEEE Electron*. Device Lett. 2010, 31, 1245–1247. [CrossRef]
- Hsu, H.H.; Chang, C.Y.; Cheng, C.H. A Flexible IGZO Thin-Film Transistor with Stacked TiO<sub>2</sub>-Based Dielectrics Fabricated at Room Temperature. *IEEE Electron. Device Lett.* 2013, 34, 768–770. [CrossRef]
- Zheng, L.L.; Qian, S.B.; Wang, Y.H.; Liu, W.J.; Ding, S.J. Mobility and Stability Enhancement of Amorphous In-Ga-Zn-O TFTs with Atomic Layer Deposited Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> Stacked Insulators. *IEEE J. Electron. Device* 2016, 4, 347–352. [CrossRef]
- Abliz, A.; Wang, J.L.; Xu, L.; Wan, D.; Liao, L.; Ye, C.; Liu, C.S.; Jiang, C.Z.; Chen, H.P.; Guo, T.L. Boost up the electrical performance of InGaZnO thin film transistors by inserting an ultrathin InGaZnO:H layer. *Appl. Phys. Lett.* 2016, 108, 213501. [CrossRef]
- 10. Lin, C.I.; Fang, Y.K.; Chang, W.C.; Chiou, M.W.; Chen, C.W. Effect of gate barrier and channel buffer layer on electric properties and transparence of the InGaZnO thin film transistor. *Microelectron. Reliab.* **2014**, *54*, 905–910. [CrossRef]
- 11. Januar, M.; Prakoso, S.P.; Lan, S.Y.; Mahanty, R.K.; Kuo, S.Y.; Liu, K.C. The role of oxygen plasma in the formation of oxygen defects in HfO<sub>x</sub> films deposited at room temperature. *J. Mater. Chem. C* **2015**, *3*, 4104–4114. [CrossRef]
- 12. Pu, H.F.; Zhou, Q.F.; Yue, L.; Zhang, Q. Investigation of oxygen plasma treatment on the device performance of solution-processed InGaZnO thin film transistors. *Appl. Surf. Sci.* 2013, 283, 722–726. [CrossRef]
- 13. Kamiya, T.; Nomura, K.; Hosono, H. Present status of amorphous In–Ga–Zn–O thin-film transistors. *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305. [CrossRef] [PubMed]
- Cho, Y.J.; Shin, J.H.; Bobade, S.M.; Kim, Y.B.; Choi, D.K. Evaluation of Y<sub>2</sub>O<sub>3</sub> gate insulators for InGaZnO thin film transistors. *Thin Solid Film* 2009, 517, 4115–4118. [CrossRef]
- Syamala Rao, M.G.; Sánchez-Martinez, A.; Gutiérrez-Heredia, G.; Quevedo- López, M.A.; Ramírez-Bon, R. Sol-gel derived low temperature HfO<sub>2</sub>-GPTMS hybrid gate dielectric for InGaZnO thin-film transistors (TFTs). *Ceram. Int.* 2018, 44, 16428–16434. [CrossRef]
- Zou, X.; Fang, G.J.; Yuan, L.Y.; Tong, X.S.; Zhao, X.Z. Improved electrical characteristics and reliability of amorphous InGaZnO metal-insulator-semiconductor capacitor with high k HfO<sub>x</sub>N<sub>y</sub> gate dielectric. *Microelectron. Reliab.* 2010, 50, 954–958. [CrossRef]
- 17. Moon, Y.-K.; Lee, S.; Kim, W.-S.; Kang, B.-W.; Jeong, C.-O.; Lee, D.-H.; Park, J.-W. Improvement in the bias stability of amorphous indium gallium zinc oxide thin-film transistors using an O<sub>2</sub> plasma-treated insulator. *Appl. Phys. Lett.* **2009**, *95*, 013507. [CrossRef]
- Yoo, H.; Tak, Y.J.; Kim, W.-G.; Kim, Y.-G.; Kim, H.J. A selectively processible instant glue passivation layer for indium gallium zinc oxide thin-film transistors fabricated at low temperature. *J. Mater. Chem. C* 2018, *6*, 6187–6193. [CrossRef]
- 19. Kang, J.H.; Cho, E.N.; Kim, C.E.; Lee, M.-J.; Lee, S.J.; Myoung, J.-M.; Yun, I. Mobility enhancement in amorphous InGaZnO thin-film transistors by Ar plasma treatment. *Appl. Phys. Lett.* **2013**, *102*, 222103. [CrossRef]

- Zhang, P.P.; Samanta, S.; Fong, X.Y. Physical Insights into the Mobility Enhancement in Amorphous InGaZnO Thin-Film Transistor by SiO<sub>2</sub> Passivation Layer. *IEEE Trans. Electron Device Lett.* 2020, 67, 2352–2357. [CrossRef]
- 21. Korner, W.; Urban, D.F.; Elsasser, C. Origin of subgap states in amorphous In-Ga-Zn-O. J. Appl. Phys. 2013, 114, 163704. [CrossRef]
- Noh, H.-K.; Chang, K.J.; Ryu, B.; Lee, W.-J. Electronic structure of oxygen-vacancy defects in amorphous In-Ga-Zn-O semiconductors. *Phys. Rev. B* 2011, 84, 115205. [CrossRef]
- 23. Ryu, B.; Noh, H.-K.; Choi, E.-A.; Chang, K.J. O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors. *Appl. Phys. Lett.* **2010**, *97*, 022108. [CrossRef]
- Kim, J.H.; Kim, U.K.; Chung, Y.J.; Hwang, C.S. Correlation of the change in transfer characteristics with the interfacial trap densities of amorphous In–Ga–Zn–O thin film transistors under light illumination. *Appl. Phys. Lett.* 2011, *98*, 232102. [CrossRef]
- Nicollian, E.H.; Brews, J.R. *MOS (Metal Oxide Semiconductor) Physics and Technology*; Wiley: New York, NY, USA, 1982.
   Jeong, C.-Y.; Lee, D.; Song, S.-H.; Cho, I.-T.; Lee, J.-H.; Cho, E.-S.; Kwon, H.-I. Border trap characterization in amorphous
- indium-gallium-zinc oxide thin-film transistors with SiO<sub>x</sub> and SiN<sub>x</sub> gate dielectrics. *Appl. Phys. Lett.* 2013, 103, 142104. [CrossRef]
  27. Han, K.-L.; Ok, K.-C.; Cho, H.-S.; Oh, S.; Park, J.-S. Effect of hydrogen on the device performance and stability characteristics of amorphous InGaZnO thin-film transistors with a SiO<sub>2</sub>/SiN<sub>x</sub>/SiO<sub>2</sub> buffer. *Appl. Phys. Lett.* 2017, 111, 063502. [CrossRef]
- 28. Ok, K.-C.; Park, S.H.K.; Hwang, C.-S.; Kim, H.; Shin, H.S.; Bae, J.; Park, J.-S. The effects of buffer layers on the performance and stability of flexible InGaZnO thin film transistors on polyimide substrates. *Appl. Phys. Lett.* **2004**, *104*, 063508. [CrossRef]
- 29. Wang, R.Z.; Wu, S.L.; Jia, D.B.; Wei, Q.; Zhang, J.T. Influence of different conditions on the electrical performance of amorphous InGaZnO thin-film transistors with HfO<sub>2</sub>/SiN<sub>x</sub> stacked dielectrics. *J. Vac. Sci. Technol. B* **2017**, *35*, 051204. [CrossRef]