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Article

Thermal Boundary Conductance of Direct Bonded Aluminum Nitride to Silicon Interfaces

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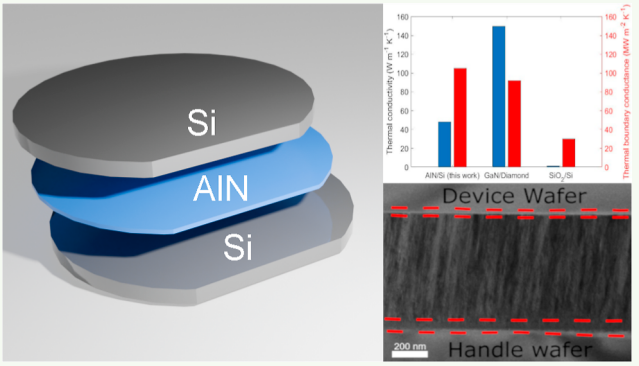
ABSTRACT: Heat accumulation and self-heating have become key issues in microelectronics owing to the ever-decreasing size of components and the move toward three-dimensional structures. A significant challenge for solving these issues is thermally isolating materials, such as silicon dioxide (SiO_2), which are commonly used in microelectronics. The silicon-on-insulator (SOI) structure is a great demonstrator of the limitations of SiO_2 as the low thermal conductivity insulator prevents heat dissipation through the bottom of a device built on a SOI wafer. Replacing SiO_2 with a more thermally conductive material could yield immediate results for improved heat dissipation of SOI structures. However, the introduction of alternate materials creates unknown interfaces, which can have a large impact on the overall thermal conductivity of the structure. In this work, we studied a direct bonded AlN-to-SOI wafer (AlN-SOI) by measuring the thermal conductivity of AlN and the thermal boundary conductance (TBC) of silicon (Si)/AlN and Si/SiO_2/aluminum−oxygen−nitrogen (AlON)/AlN interfaces, the latter of which were formed during plasma-activated bonding. The results show that the AlN-SOI possesses superior thermal properties to those of a traditional SOI wafer, with the thermal conductivity of AlN measured at roughly 40 W m^{-1} K^{-1} and the TBC of both interfaces at roughly 100 MW m^{-2} K^{-1}. These results show that AlN-SOI is a very promising structure for improving heat dissipation in future microelectronics.



KEYWORDS: *silicon-on-insulator, aluminum nitride, thermal boundary conductance, thermal conductivity, time-domain thermoreflectance*

INTRODUCTION

Development of microelectronics toward a three-dimensional (3D) structure and nanometer sizes has made the devices ever more sensitive to the effects of heat accumulation and self-heating. Failure to implement proper thermal management can lead to reduced performance and reliability issues. The silicon-on-insulator (SOI) structure is one of the building blocks of modern microelectronics. One of the major drawbacks of the SOI structure is the dielectric, most commonly silicon dioxide (SiO_2), separating the device wafer from the handle wafer. This prevents heat dissipation through the handle wafer and thus contributes toward self-heating.[1,2] Replacing SiO_2 with a more thermally conductive material is a tempting solution for improving the thermal management of the SOI structure. However, the addition of new materials introduces new interfaces, which can have a significant effect on the thermal properties of the structure.

Aluminum nitride (AlN) is a highly interesting material for this purpose since it has been shown to have a high thermal conductivity through computational[3] and experimental work.[4−8] In addition to having good thermal properties, AlN is a common material in microelectronics with well-known growth methods expediting their integration to new processes. Recently, AlN-based field-effect transistors[9] and p−n diodes[10] have been demonstrated to prove that AlN-based devices have practical appeal beyond the improved thermal properties.

As AIN is an electrical insulator, the thermal conduction in AlN happens exclusively through phonons. Because of this, the thermal conductivity of AlN is closely tied to its crystal quality and has been demonstrated to vary greatly based on the deposition process. Highest thermal conductivities at 300 W m^{-1} K^{-1}[4] have been achieved with AlN grown using metal−organic chemical vapor deposition (MOCVD), while AlN thin films grown using sputtering have had a thermal conductivity of 10−50 W m^{-1} K^{-1},[11] but thermal conductivities above 100 W m^{-1} K^{-1} have been recently reported.[5−8] Moreover,

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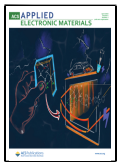

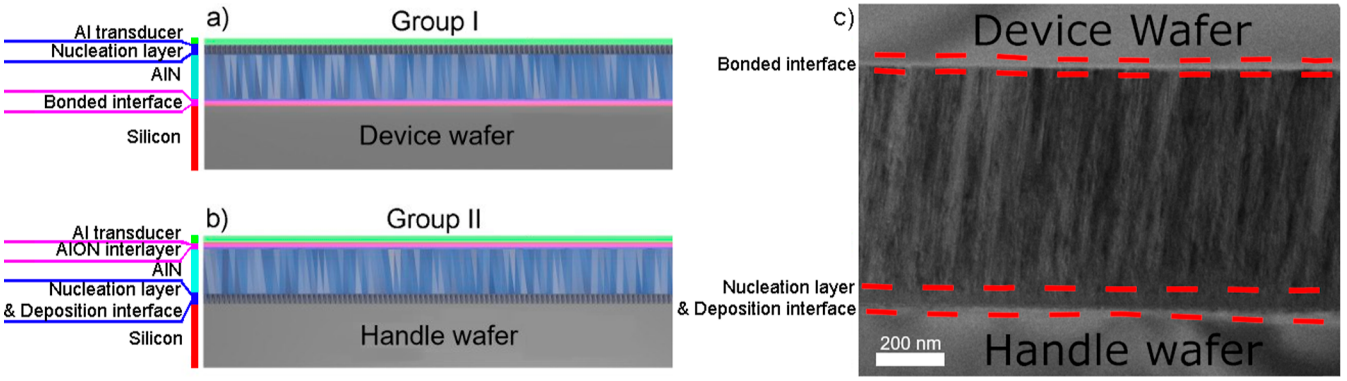

Figure 1. (a,b) Illustrations of samples used in this work. Group I samples prepared by etching the handle wafer of the bonded samples. This exposed the AlN layer and the bonded AlN/Si interface beneath it to allow for $TBC_{AlN/Si,\ bonded}$ to be measured. Conversely, group II samples were prepared by etching the device wafer. This exposed the AlN and the deposition interface between AlN and Si allowing $TBC_{AlN/Si,\ deposition}$ to be measured. (c) STEM DF image of the bonded AlN layer. Important locations are marked in the image.

impurities have been found to significantly decrease the thermal conductivity of AlN by degrading its crystal quality.[3]

Alongside the thermal conductivity of the insulator, the thermal boundary conductance (TBC) between the insulator and the substrate material, usually silicon (Si), plays an important role in determining the heat dissipation capabilities of microelectronic structures. Consequently, thermal interface engineering is an active area of research. Several parameters have been determined to play an important role in defining the TBC of an interface, such as roughness,[12,13] nature of atomic bonding (covalent or van der Waals),[14,15] and existence of intermediate layers.[15−17] Due to the complexity of TBC, it is important to characterize the thermal properties of novel interfaces properly before they can be implemented in actual devices. It has been shown that a poor interface can lead to a significant reduction in TBC.[18,19]

In our previous work,[20] we demonstrated a novel SOI structure, where AlN was used as the insulator (AlN-SOI). To achieve the best bonding yield, Si and AlN surfaces were activated using a combination of SF_6 + O_2 and SF_6 + Ar plasma. This inadvertently created thick, amorphous aluminum−oxygen−nitrogen (AlON) and SiO_2 intermediate layers, with fluorine (F) impurities detected between the AlON and SiO_2 layers. A similar layer has been previously reported by Bao et al.,[21] where they determined that a structure consisting of an AlN-to-AlN bond with an AlON interface in the middle retained good thermal properties. However, as the interlayer was between two AlN films and no values were reported for the TBC of the interface, it is unclear what impact the AlON interlayer would have at an AlN-to-Si interface. As amorphous layers typically exhibit low thermal conductivity, its effect on the TBC requires careful investigation. Similar structures utilizing gallium nitride (GaN) bonded to either diamond or silicon carbide (SiC) have been demonstrated;[18,19,22,23] however, the interfaces studied in these works were considerably thinner, with the exception of ref 18, where the thick interface was found detrimental to the TBC.

In this work, we study the impact of a thick, amorphous AlON-SiO_2 interlayer on the TBC of the AlN/Si interface to determine whether the surface-activated AlN to Si direct bonding method demonstrated in our previous work[20] is a suitable bonding method for achieving a highly thermally conductive SOI structure. Time-domain thermoreflectance (TDTR) was used to characterize the thermal properties of AlN-SOI, which included the thermal conductivity of AlN (Λ_{AlN}), the TBC of the bonded AlN/Si interface (TBC_{bonded}), and the TBC of the AlN/Si deposition interface ($TBC_{deposition}$).

MATERIALS AND METHODS

Sample Preparation. We studied directly bonded structures prepared and reported in our previous work [group "Combined bond (C)" in ref 20. An overview of the fabrication process for the directly bonded samples is given below. The direct bonded samples were prepared by sputtering 720 nm of AlN on top of a 320 μm thick Si(100) wafer (handle wafer), which would then be bonded to a similar Si(100) wafer (device wafer). Before bonding, both the handle and device wafers were cleaned in solvent and surface activated with reactive ion etching (RIE) using SF_6 + O_2 and SF_6 + Ar gases. In addition, the device wafer was cleaned using the RCA-1 cleaning protocol. Next, the wafers were bonded by initially keeping the wafers at ambient pressure and room temperature for 5 h after which the wafers were kept in a vacuum at 80 °C for 3 h. Finally, the wafers were bonded at 300 °C under 1000 N pressure for 4 h. After the bonding, the wafer was annealed in a vacuum at 600 °C for 24 h.

In order to measure the thermal properties of the bonded wafer, it was diced in 5 mm by 5 mm chips using a DISCO DAD3220 dicing saw. To expose the handle/AlN (deposition interface) and device/AlN (bonded interface) interfaces, Si was etched using inductively coupled plasma RIE (ICP-RIE) etching the silicon with Oxford Instruments PlasmaPro Estrelas 100 using 600 W ICP power, 12 sccm O_2 flow, 85 sccm SF_6 flow, −120 °C temperature, and 120 min etching time. The thickness of the AlN layer was measured using a SE-2000 spectroscopic ellipsometer. An aluminum (Al) thin film with a thickness of 80 nm was deposited by e-beam evaporation using a system manufactured by Angstrom Engineering to act as the transducer for the TDTR measurement. Before depositing the Al transducer, the surface of the sample was cleaned using Ar plasma (300 V, 1 A) for 120 s. The thickness of the Al transducer was confirmed by using picosecond acoustic echos produced by pulses reflected from the Al/AlN interface observed in the TDTR measurement.

Inspection of the crystal structure was carried out using transmission electron microscopy (TEM), scanning TEM (STEM), select area electron diffraction using a JEOL JEM-2200FS Cs-corrected microscope and energy-dispersive X-ray spectroscopy (EDS) using a JEOL JEM-2800 microscope, both operating at 200 kV. The TEM lamella process was carried out using a dual-beam (FIB-SEM) JEOL JIB-4700F Multi Beam System using an in situ lift-out process from the molded cross-section.

The samples were divided into two groups: group I and group II. Group I samples were etched from the side of the handle wafer and were used to measure the TBC of the bonded interface ($TBC_{AlN/Si,\ bonded}$). This exposed the AlN, which was then covered

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Table 1. Material Parameters Used in the TDTR Measurement[a]

layer	Λ (W m^{-1} K^{-1})	C (MJ m^{-3} K^{-1})	h (nm)	TBC (MW m^{-1} K^{-1})
Al	170	2.4	80.25	
Al/AlN interface		0.1	0.1	***288 ± 24$_I$/357 ± 33$_{II}$***
AlN	***40 ± 5$_I$/48 ± 5$_{II}$***	3.27	720	***55 ± 6$_I$/66 ± 7$_{II}$***
AlN/Si deposition interface	***0.19 ± 0.03***	0.1	2	***95 ± 19***
AlN/Si bonded interface	***2.1 ± 0.3***	0.1	20	***105 ± 17***
Si	124	1.63	1 × 106	

[a]Values given in ***bold italic*** were obtained during the fitting process with subscripts I and II denoting the sample group. The calculated values are the mean obtained from the measurements and are present with a 95% standard deviation.

Table 2. Measured Values for Reference Samples Used to Verify the Accuracy of the TDTR Measurements[a]

layer	Λ (W m^{-1} K^{-1})	Λ$_{ref}$ (W m^{-1} K^{-1})	TBC with Al (W m^{-2} K^{-1})	TBC with Al (ref) (W m^{-2} K^{-1})
Si	120	115−130[28]	151	120,[26] 120−140[28]
SiO_2	1.3	1.31[29]		
sapphire	30	32.5[27]	227	200[26]

[a]TBC between SiO_2 and Al was not reported as TDTR was not sensitive to that parameter.

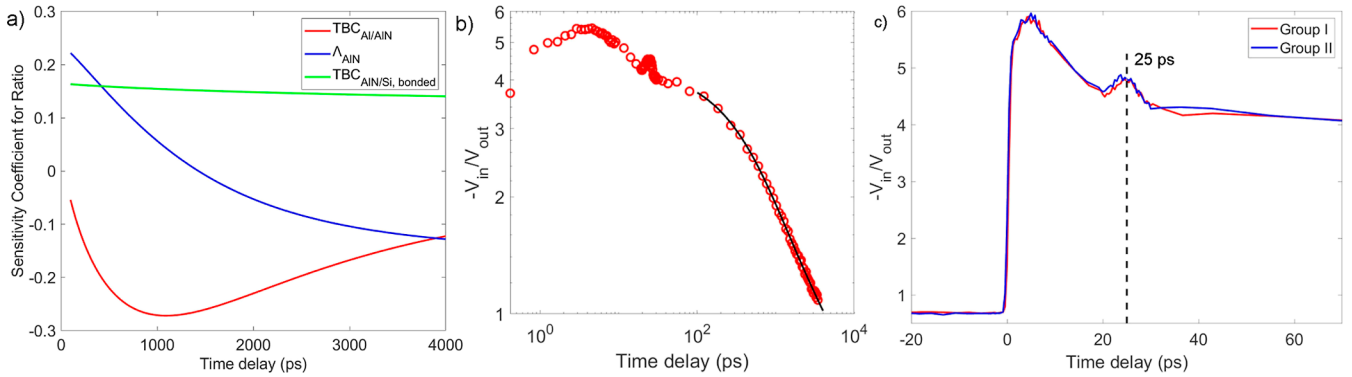

Figure 2. (a) Calculated sensitivities of the unknown parameters for TDTR fitting. These sensitivities describe the impact of the parameter on the ratio at given times. (b) Example TDTR fit. (c) Picosecond pulse observed in TDTR. A small difference in the response can be seen immediately after the pulse; however, the pulse itself is identical for both groups.

with the Al transducer. These samples consist of an Al transducer, an AlN film (nucleation layer toward the Al transducer), a bonded interface containing the AlON/SiO_2 interlayer, and a Si substrate.

Group II samples were etched from the side of the device wafer and were used to measure the TBC of the deposition interface (TBC$_{AlN/Si,\ deposition}$). As illustrated in Figure 1a, the sample consists of layers including the Al transducer, the AlN film (nucleation layer toward the Si substrate), and the deposition interface between AlN/Si and the Si substrate. Illustrations of the samples and a TEM image of the bonded structure before Si etching are shown in Figure 1. The interfaces to be studied were exposed by etching the silicon on the opposing side due to difficulties associated in controlling the silicon etching rate to create a <1 μm thick Si layer after etching 320 μm of Si.

Time-Domain Thermoreflectance and Structure of the Samples. The measurement was conducted on a TDTR setup located at Aalto University. The setup is a two-color setup with a 400 nm pump beam modulated using a 2 MHz sinusoidal wave and an 800 nm probe beam placed on a delay stage, which were focused on a sample using a 10× objective. The laser source used is a MIRA900f Ti/sapphire femtosecond oscillator with a 76 MHz repetition rate pumped by a 532 nm continuous wave laser Millenia Pro by Spectra Physics. The $1/e^2$ radii of pump and probe beams were measured using a CCD camera as 31 and 8 μm, respectively.

Three samples from both groups were measured with three measurement points for each sample for a total of nine measurement points per group. Before measuring each sample, a measurement was performed to determine the amount of coherent pickup. This measurement was done by blocking the pump beam and taking a 50-point measurement, which was then averaged to determine the amount of coherent pickup for the in-phase and out-of-phase components. This value was subtracted from the in-phase and out-of-phase voltages of the measurements to remove the impact of a coherent pickup.

The TDTR data-analysis was performed according to ref 24. The material parameters used in the data analysis are given in Table 1. The thicknesses of Al, AlN, and AlN/Si deposition interface layers were determined by using picosecond acoustic pulses, ellipsometry, and TEM imaging, respectively. The TBC was calculated as TBC = Λ/h.[25]

RESULTS AND DISCUSSION

First, a set of reference samples was measured to establish the accuracy of the TDTR setup. These results are shown in Table 2. The measured values for TBC$_{Al/sapphire}$,[26] Λ$_{sapphire}$,[27] TBC$_{Al/Si}$,[26,28] Λ$_{Si}$,[28] and Λ$_{SiO2}$[29] are in good agreement with previously reported values. Since the measured reference samples correspond well with the previously reported values and the reference values span the range of values that are measured for the AlN samples, the TDTR measurements can be considered accurate.

Calculated sensitivities of the unknown parameters in the TDTR measurements are shown in Figure 2a and were calculated using the following equation: $S_i = \frac{\partial \ln(-V_{in}/V_{out})}{\partial \ln(p_i)}$, where $-V_{in}/V_{out}$ is the ratio measured with TDTR and p_i is the parameter whose sensitivity is calculated. The calculated

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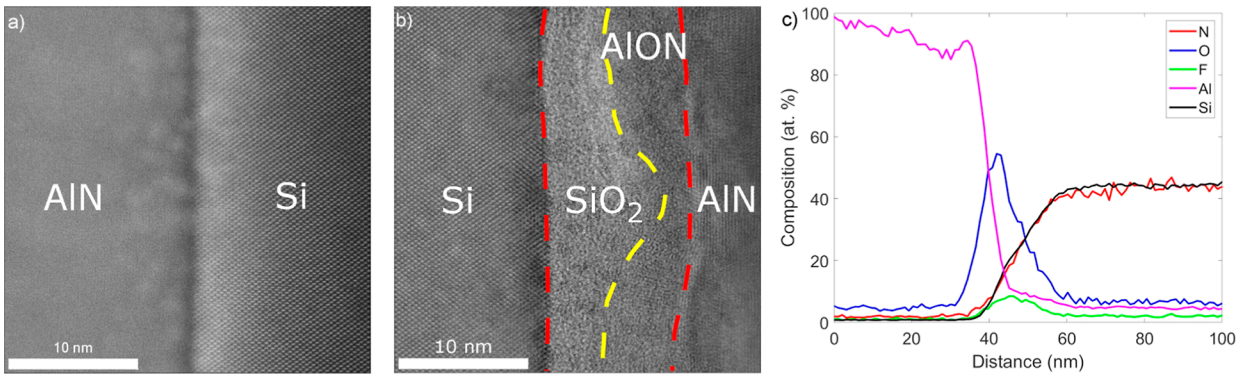

Figure 3. (a) STEM DF image of the deposition interface. The interface does not contain any major impurities and is roughly 2 nm thick. (b) STEM BF image of the bonded interface; different phases are marked in the image. Yellow line in the image describes the location of the bonded interface. It can be seen that the SiO_2 and AlON layers are bonded well and do not contain any visible interface. The total thickness of the interface is roughly 10 nm. (c) EDS linescan of the bonded interface. A fluorine component can be seen in both SiO_2 and AlON interfaces with the peak in between the interfaces, suggesting that it could act as a sort of a bonding agent between the two interfaces.

sensitivities show that the measurement is sensitive to all of the unknown parameters and, thus, can be measured with the used TDTR parameters. An example fit is shown in Figure 2b, which shows an excellent match between the measured values and the theoretical fit.

Results for the thermal conductivity and TBCs of the bonded AlN samples are given in Table 1. $TBC_{Al/AlN}$ measured in this work is considerably higher than that previously reported by Xu et al.[8] and slightly higher than what was reported by Stevens et al.[26] The measured $TBC_{Al/AlN}$ for group II is very close to the TBC calculated using a diffuse mismatch model (DMM);[30] however, $TBC_{Al/AlN}$ measured for group I is roughly 20% lower. This is unexpected since picosecond pulses, shown in Figure 2c, seen from both interfaces are identical, which means that the acoustic impedance of the interfaces is similar. Because of this, it seems probable that the AlON interlayer was removed during the Si etching process and does not contribute to the TBC. A possible explanation for the difference in TBC is the existence of the nucleation layer, which can be seen in Figure 1c. The fact that the Al transducer of the group I samples is deposited on top of the nucleation layer, which has greater disorder than crystalline AlN, the $TBC_{Al/AlN}$ for the group I samples can be excepted to be worse than $TBC_{Al/AlN}$ for group II, where the Al transducer is deposited over crystalline AlN.

Thermal conductivity of sputtered AlN is typically reported in the range of 1−100 W m^{-1} K^{-1}.[11,31−34] The large variation is explained by the crystal quality and degree of crystallinity of AlN, which severely impacts the thermal conductivity, as was demonstrated computationally by Jacquot et al.[34] The thermal conductivity of AlN measured in this work corresponds well to previous experimental results. This suggests that the crystal structure of AlN was not significantly altered during the bonding process, which is expected due to the high thermal stability of the material. This supports the results of our previous work,[20] where the crystallinity of AlN was characterized to be good, with a rocking curve full-width half-maximum (fwhm) for AlN(0002) = 2.3 ± 0.6°. A small difference in the thermal conductivity of the two sample groups was observed, but the source of the difference is unclear.

Having established the accuracy of the TDTR measurements and the quality of AlN after the bonding process, the TBC of the AlN/Si interfaces can now be determined. Results for $TBC_{AlN/Si,\ deposition}$, measured from samples in group II, are presented first. A STEM image of this interface is shown in Figure 3a, from which it can be seen that the interface is between 1 and 2 nm thick. The measured TBC values for the deposition interface are in good agreement to those reported in ref 11 and ref 35 but are noticeably lower than what was achieved by Perez et al.[33] through DMM calculations and experimental measurements. A significant difference between the work done by Perez and this work is that they used Si(111) as the substrate as opposed to Si(100) used in our work. The use of Si(111) could have provided AlN with a more compatible interface to grow on, reducing the lattice mismatch between AlN and Si and leading to a higher TBC.

Inspection of the bonded interface in TEM, shown in Figure 3b, showed that the interface is divided into two regions, which were confirmed to be amorphous SiO_2 and AlON through TEM and EDS (Figure 3b,c). The thickness of the SiO_2 and AlON layers is roughly 10 nm. In addition, a fluorine component can be seen for both layers, with the concentration peaking at the interface between the SiO_2 and AlON layers. When comparing the $TBC_{AlN/Si,\ bonded}$ to $TBC_{AlN/Si,\ deposition}$, no significant difference was observed. This is unexpected due to the vastly different natures of the two interfaces.

It has been shown that the bonding strength of an interface has a large impact on the TBC,[14,15] and as such, several works have reported an increase in the TBC when using intermediate layers[15−17] or even increased surface roughness[13] to increase the bonding strength of an interface. The same phenomena have been demonstrated on bonded GaN samples,[18,22,23] where GaN was bonded to various substrates with the help of different intermediate layers to enhance the bonding between GaN and the substrate. Waller et al.[19] studied the necessity of a SiN interlayer for GaN-on-diamond bonding and discovered that the bond that was created through van der Waals bonding had a seven times lower TBC than bonds using a SiN interlayer to facilitate the creation of strong atomic bonds. Furthermore, Cheng et al. showed that an interlayer can reduce the TBC for a GaN/diamond interface, when a thick Si interlayer exhibited a significantly reduced TBC when compared to a thinner amorphous diamond interlayer.[18]

Based on the work done on bonded GaN samples,[18,22,23] it is evident that a thin amorphous layer formed during a bonding process can achieve a high thermal conductivity, and the results obtained for the SiO_2−AlON interlayer are reasonable.

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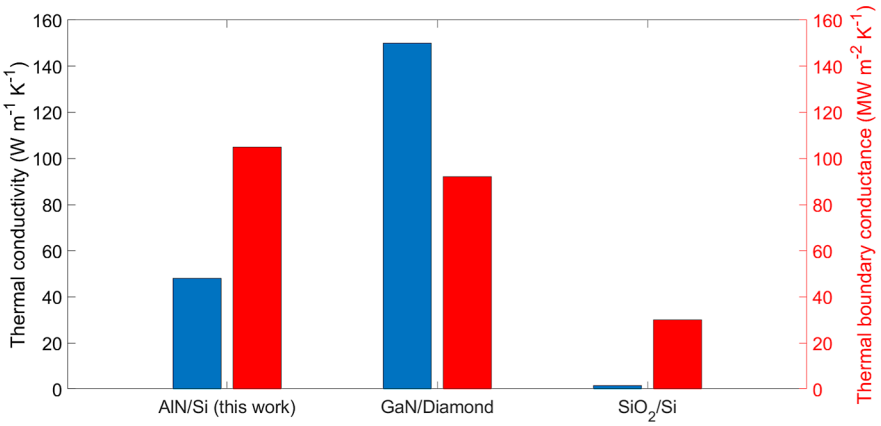

Figure 4. Comparison of previously reported thermal properties for GaN/diamond[18] and SiO_2/Si[36] interfaces to AlN-SOI measured in this work. The thermal conductivity (shown on the left axis and blue bars) represents the thermal conductivity of the dielectric material and the TBC (shown on the right axis and red bars) represents the TBC between the dielectric and the substrate.

However, the exact mechanism of thermal conduction is not clear. A likely explanation is the extremely high-quality bonded interface, where the only distinct interface observed was between Si and SiO_2, which can be seen in Figure 3b. This enables phonon transmission from AlN to Si without significant scattering from the SiO_2−AlON interlayer. Lack of a clear interface inside the interlayer is a major difference between the samples measured in this work and samples measured by Cheng at al.,[18] suggesting that an increase in interlayer thickness does not significantly affect the TBC of the interface if the quality of the interlayer remains good. These results indicate that bonded AlN provides a significant improvement over the thermal conductivity of SiO_2 and has a TBC comparable to that of GaN. Comparison of thermal conductivity and TBC of AlN, SiO_2, and GaN is provided in Figure 4. It should be noted that the AlN used in this work was sputtered AlN rather than MOCVD AlN, which has been demonstrated to have a significantly higher thermal conductivity.[4,11] Replacing sputtered AlN with MOCVD AlN would increase the thermal conductivity of the AlN and lead to improvements in the TBC between AlN and Si by improving the crystal quality of AlN near the interface.

CONCLUSIONS

This work studied the TBC of a directly bonded AlN-SOI structure. A 10 nm thick amorphous SiO_2−AlON interlayer was created in the AlN-SOI inadvertently during the bonding process as a result of AlN and Si surface activation using SF_6 + O_2 and SF_6 + Ar plasma. Thick amorphous layers, such as these, typically have a very low thermal conductivity and thus need to be characterized thoroughly when attempting to fabricate highly thermally conductive structures. The thermal properties of the AlN-SOI were characterized using TDTR, which showed AlN thermal conductivity at 40−48 W m^{-1} K^{-1} and the TBCs between AlN and Si as $TBC_{AlN/Si,\ deposition}$ = 95 MW m^{-2} K^{-1} and $TBC_{AlN/Si,\ bonded}$ = 105 MW m^{-2} K^{-1}. These values for AlN thermal conductivity[11,31,32] and the $TBC_{AlN/Si}$[11,35] are in good agreement with previously reported values. The results show that AlN-to-silicon direct bonding utilizing plasma activation is a viable method for creating highly thermally conductive SOI structures. This work demonstrates the viability of the AlN-SOI structure as a future platform for high thermal conductivity structures. Future work on the topic should be focused on implementing highly thermally conductive AlN in the AlN-SOI structure to further improve its thermal properties. In addition, devices should be fabricated utilizing the AlN-SOI structure to characterize the functional improvements it provides over traditional SOI.

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Notes

The authors declare no competing financial interest.

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