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Se-mediated dry transfer of wafer-scale 2D semiconductors for advanced electronics

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Two-dimensional (2D) semiconductors hold a great promise for next-generation electronics. Yet, achieving a clean and intact transfer of 2D films on device-compatible substrates remains a critical challenge. Here, we report an approach that uses selenium (Se) as the intermediate layer to facilitate the transfer of wafer-scale molybdenum disulfide (MoS_2) monolayers on target substrates with high surface/interface cleanness and structural integrity. Our method enables nearly 100% film intactness of the transferred 2D semiconductors which are free from residues or contaminants. Characterizations reveal that the Se-assisted dry-transfer yields MoS_2 film with superior quality compared to conventional transfer techniques. The fabricated field-effect transistors (FETs) and logic circuits based on these transferred films demonstrate remarkable electrical performance, including on/off current ratios up to 2.7×10^{10} and electron mobility of 71.3 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for individual FETs. Our results underscore the feasibility of this dry-transfer technology for fabricating high-performance 2D electronics that are fully compatible with standard semiconductor processes, paving the way for integrating 2D materials into advanced electronic applications.

Two-dimensional (2D) semiconductors have attracted significant attentions as promising ultrathin channel materials for advanced electronics, such as next-generation integrated circuits (ICs), flexible electronics, sensors, and optoelectronics, owing to their atomic thickness and optical/electrical properties[1–5]. While high-quality, wafer-scale 2D semiconductor films have been successfully achieved via chemical vapor deposition (CVD) technique[6–10], their practical integration into devices remains constrained by the requirement of specific growth substrates (e.g., sapphire) due to the limitation of lattice matching and thermodynamic factors, posing severe challenges for scale batch manufacturing of 2D electronic devices[11–13]. To address this issue, a large-area transfer of 2D semiconductor films from their growth substrates to target substrates is essential in device fabrication process[14–16], while maintaining high integrity of the transferred films and avoiding surface/interface contaminations to the best degree as we could is pivotal to achieve optimal device performances.

In large-scale transfer approaches for 2D materials previously developed, either being wet or dry, a certain of transfer medium are usually employed for carrying these 2D materials transferred from their growth substrates to the target substrates. Yet, some technique bottlenecks remain and hinder the acquisition of high-quality wafer scale 2D films by using existing transfer strategies. For instance, in wet transfer approaches, the delamination of a 2D material from its growth substrate and the removal of the transfer medium (e.g., polymethyl methacrylate, label as PMMA) on the target substrate are usually performed by wet chemical process, which is prone to cause structural damages, incomplete transfer, or surface/interface contaminations[17,18]. In contrast, dry-transfer approaches have shown significant improvements in achieving much cleaner surfaces/interfaces by employing the

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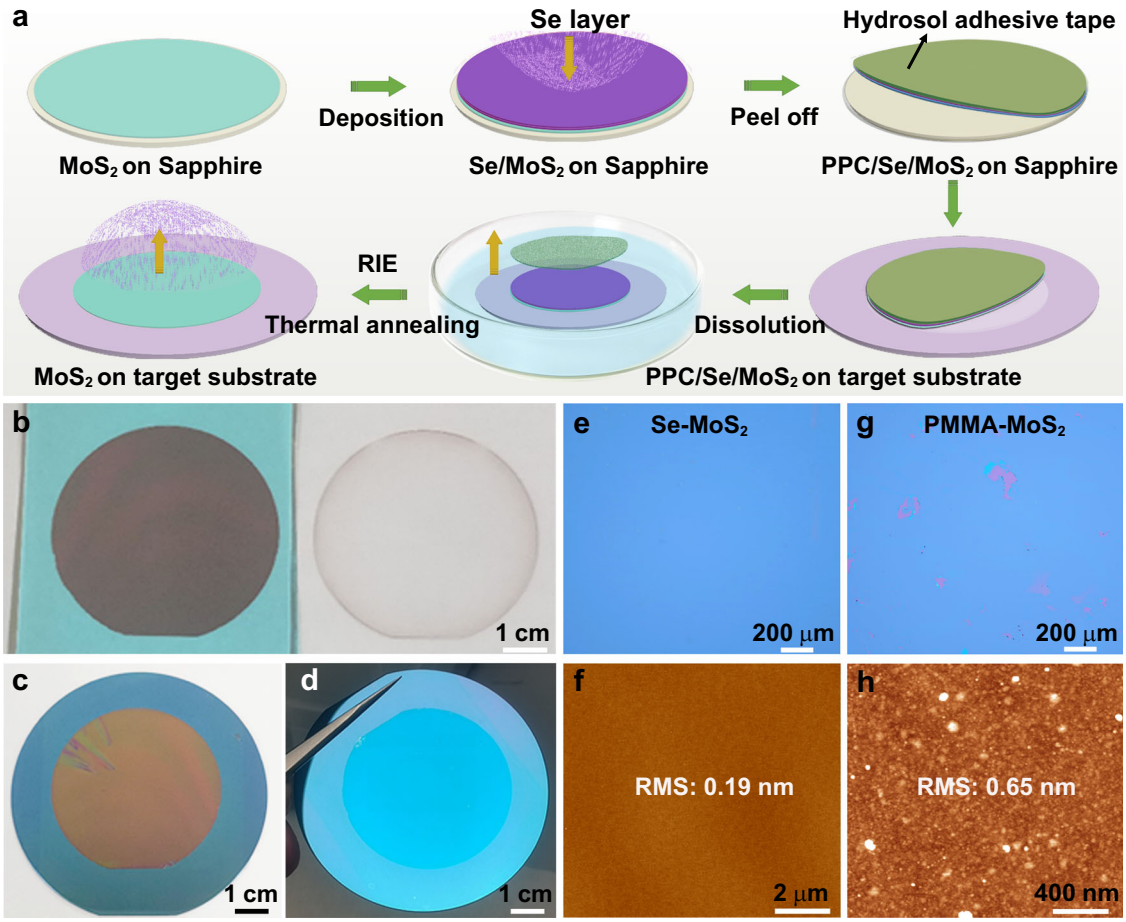

Fig. 1 | Se-mediated dry transfer of wafer-scale 2D MoS_2 film. a Schematic diagram of the transfer process. PPC polycarbonate, RIE reactive ion etching. **b** Photographs of a 2-in. wafer-scale Se/MoS_2 film on hydrosol tape (left) peeled from sapphire substrate (right). Photographs of the as-transferred 2-in. scale MoS_2 film before (**c**) and (**d**) after the removal of PPC/Se layer. Optical (**e**) and AFM (**f**) image of a Se-mediated transfer MoS_2 film on the target substrate. AFM: atomic force microscope, RMS: root-mean-square roughness Optical (**g**) and AFM (**h**) image of a PMMA-transferred 2-in. MoS_2 film for comparison. PMMA: polymethyl methacrylate.

mechanical peeling 2D materials off their growth substrates and releasing them onto the target substrates[19–35]. However, in order to create a stronger adhesive interface between a 2D material and the transfer medium to facilitate the mechanical peeling-off, polymers such as polycarbonate (PPC), thermal release tape (TRT), and UV-tape have been used[21–30], along with metals like Au, Ag, and Ni, acting as the intermediate adhesive layers[31–35]. Consequently, the removal of these polymer and metals on surfaces of 2D materials are usually still assisted by chemical process, and the surface residues are still a concern as the residual contaminations are the main source of the electronic performance degradation.

In this work, we demonstrate a completely dry transfer strategy for wafer-scale 2D semiconductor of monolayer molybdenum disulfide (MoS_2) film epitaxially grown on sapphire. A low melting point metal of Se is utilized as the adhesive intermediate layer which can be finally removed by a physical process, i.e., thermal evaporation, leaving the surface of monolayer MoS_2 ultra-clean. Field-effect transistors (FETs) and logic circuits are fabricated based on the transferred wafer-scale monolayer MoS_2 and corresponding electrical characterizations reveal favorable electrical performances. The as-fabricated FETs exhibit an optimal on/off current ratios (I_{on}/I_{off} ratios) of 2.7×10^{10} and relatively high charge mobility of 71.3 $cm^2 \cdot V^{-1} \cdot s^{-1}$, highlighting the promise of this Se-transfer method for advanced 2D electronics with fabrication process compatible with existing semiconductor fabrication processing lines.

Results

Se-mediated dry-transfer process

Figure 1a illustrates the schematic of Se-mediated transfer process for wafer-scale MoS_2. Starting from a 2-in. wafer-scale monolayer MoS_2 epitaxially grown on sapphire, ~500 nm-thick uniform Se is deposited on the surface of monolayer MoS_2 film. Detailed characterizations, including photographs, optical microscopy, and atomic force microscopy (AFM) images of the MoS_2 surface before and after Se deposition are shown in Supplementary Fig. 1a–f, demonstrating the favorable surface uniformity. A PPC layer is then coated on the Se/MoS_2 stack to serve as a support layer during transfer, enabling the mechanical peeling of the entire PPC/Se/MoS_2 stack from the sapphire substrate with hydrosol tape assistance, as shown in Fig. 1b. Notably, the Se intermediate layer acts as a gentle yet robust adhesive layer can form a strong interfacial interaction with monolayer MoS_2, making it a robust adhesion medium to facilitate the mechanical peeling-off of the MoS_2 monolayers from their growth substrates. The interface between Se and MoS_2 could be accessed from the cross-section HRTEM images as shown in Supplementary Fig. 2 e and f. Additionally, Se is easily evaporated at low temperatures in vacuum due to its low melting point. The PPC/Se/MoS_2 stack is subsequently transferred onto the target substrate, followed by the removal of the hydrosol tape in deionized water (Fig. 1c). Lastly, reactive ion etching (RIE) is employed to remove the PPC residues, while the Se sacrificial layer is thermally evaporated off at 280 °C for 5 h in N_2 atmosphere from the surface of monolayer

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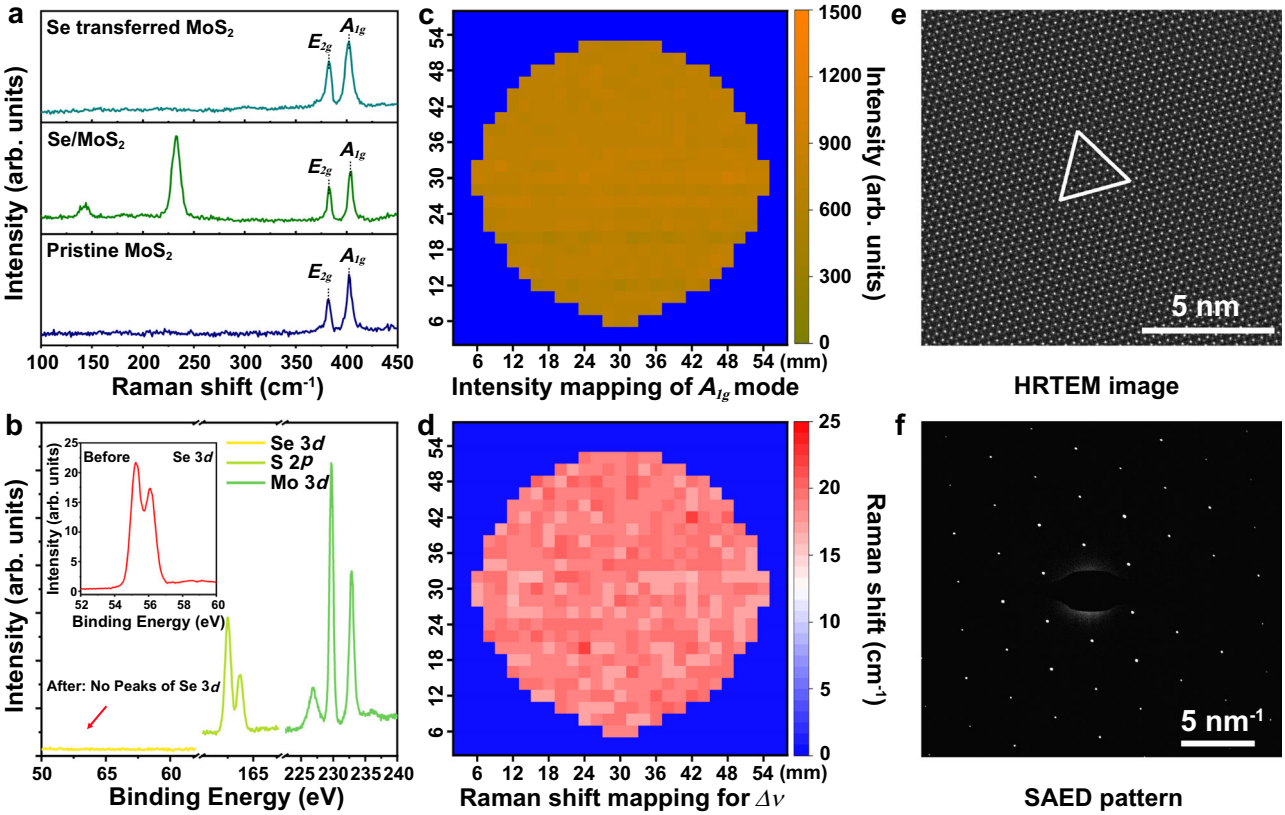

Fig. 2 | Material characterizations for Se-transferred monolayer MoS_2 films. **a** Raman spectra. **b** X-ray photoelectron spectra (*XPS*). Inset: the locally magnified XPS of Se 3d orbitals before annealing treatment. Raman mapping of A_{1g} peak intensity (**c**) and peak distance ($\Delta\nu$) between E_{2g} and A_{1g} vibration modes (**d**). **e** High resolution transmission electron microscope (HRTEM) image. White triangle: the typical orientation of MoS2 domains. **f** Selected area electron diffraction (SAED) pattern.

MoS_2. Note that the melting point of Se is ~ 221 °C, which falls within the evaporation range of PPC[36,37], and see Methods for more experimental details.

Figure 1d shows a typical sample of 2-in. monolayer MoS_2 transferred on Si/SiO_2 substrate with pre-deposited 20-nm thick Al_2O_3 dielectric layer, highlighting the scalability and integrity of the Se-mediated transfer method. Optical images in Fig. 1e and Supplementary Fig. 3 confirm a crack- and wrinkle-free surface over a large scale. Zoom-in AFM images (Fig. 1f, Supplementary Fig. 4a-i) further confirm the surface flatness, cleanness, and uniformity of the transferred MoS_2, with a low root-mean-square (RMS) roughness of ~0.19 nm. In similar control samples of monolayer MoS_2 on the same target substrate fabricated via a conventional PMMA assisted wet-transfer process (Supplementary Fig. 5a, b, corresponding to images before and after removal of PMMA), folds, cracks, wrinkles, and PMMA residues are usually seen. Figure 1g, h show the optical and AFM images, correspondingly. And the measured RMS roughness is much higher, i.e., ~0.65 nm.

Compared to the wet-transfer method, the present Se-mediated dry-transfer method not only avoids the introduction of contaminants from the wet process but also mitigates mechanical stress during the transfer process, reducing the risk of crack formation and maintaining the structural uniformity of the MoS_2 monolayer. The preservation of the film quality and cleanliness could thus play a pivotal role in advancing large-scale 2D semiconductor devices, providing a reliable way toward scalable, high-quality device manufacturing. To further validate the advantages of Se-mediated transfer strategy, we also used PPC as a direct adhesive layer for transferring wafer scale MoS_2 film but failed (supplementary Fig. 6). These results suggest that the binding force between sapphire and MoS_2 is significantly stronger than that between MoS_2 and PPC, making the PPC transfer method unfeasible for transferring large-scale 2D materials grown on sapphire substrates. Additionally, the feasibility of PMMA/Se/MoS2 configuration for transfer MoS2 film was further confirmed. We can see that PMMA/Se layer can be effectively removed by combined RIE and thermal annealing process (Supplementary Fig. 7b). As seen from the optical and AFM images in Supplementary Fig. 7c, d, the transferred MoS2 film exhibits comparable surface cleanliness with a surface roughness approximately 0.196 nm. The results demonstrate the broad applicability of this Se-mediated transfer technique, extending its utility beyond PPC alone.

We attribute the transfer of wafer-scale 2D MoS_2 from the growth substrate to several key aspects: (1) The binding force between Se and MoS_2 is significantly greater than that between MoS_2 and sapphire; (2) The thick Se layer plays a key role for large-area transfer, ensuring the highly integrity of the MoS_2 film during the transfer process. (3) Hydrosol adhesive tape and roller pressing techniques are used to remove air bubbles, ensuring full contact between layers during the transfer process, thereby increasing the success rate of the transfer.

Characterizations of the as-transferred MoS_2 wafer

To confirm the complete removal of Se after thermal evaporation, Raman spectra of raw monolayer MoS_2 film, Se/MoS_2 film, and Se transferred MoS_2 film are compared. As shown in Fig. 2a, the typical two Raman peaks at 382 and 402 cm^{-1} in raw monolayer MoS_2 film can be assigned to the E_{2g} and A_{1g} vibration modes, respectively. A slight blue shift of A_{1g} mode (404 cm^{-1}) of Se/MoS_2 sample is caused by the deposition of Se layer, inducing interface charge transfer at the interface of MoS_2 and Se layer. Note that Raman characteristic peaks of the

Se film locate at 142 and 233 cm^{-1}. For Se-mediated transferred MoS_2 film, the Se-related Raman peaks vanished and only characteristic peaks of MoS_2 existed at 382 and 402 cm^{-1}, indicating complete removal of Se layer after thermal evaporation. The fact of no Se residues is further supported by X-ray photoelectron spectroscopy *(XPS)*, as shown in Fig. 2b, which shows no detectable binding energy signals from the Se 3*d* orbitals post-annealing, thereby confirming the effectiveness of the transfer process in producing a clean MoS_2 film.

The integrity and spatial uniformity of the as-transferred 2-in. monolayer MoS_2 wafer is also accessed via Raman mapping of A_{1g} intensities and the peak distance ($\Delta\nu$) between E_{2g} and A_{1g} across the entire wafer with an adjacent probing interval of 2 mm (Fig. 2c, d, respectively). Note that the $\Delta\nu$ is typically ~20 cm^{-1} for monolayer MoS_2. For more peak position mapping of the A_{1g} and specific Raman spectra at different positions, please refer to Supplementary Fig. 8a, b. It is worth noting that the peak shifts are attributed to strain release or interface effects introduced during the transfer process, evidencing from the fact that Raman mapping of a pristine and the MoS_2 film (after removal of Se layer) shows no obvious difference, as shown in Supplementary Fig. 9e, f. These Raman mapping results confirm the high spatial uniformity across the entire wafer, which is crucial for large-scale integration of 2D semiconductor devices for many practical applications.

The atomic structure of the monolayer MoS_2 transferred via this Se-mediated transfer process is characterized by the atomic-resolution transmission electron microscopy (TEM, Fig. 2e). Nearly perfect lattice structure with no visible Se residues is further confirmed. The selected area electron diffraction (SAED) pattern in Fig. 2f shows a well-defined, undistorted diffraction pattern in the reciprocal space, indicating that the MoS_2 retains its single-crystalline nature after Se-mediated transfer. In addition, energy-dispersive X-ray spectroscopy (EDS) detects no signal corresponding to Se (Supplementary Fig. 10), which is consistent with the above characterization results. These characterizations collectively demonstrate that the Se-mediated transfer strategy enables not only a clean transfer process but also the preservation of the crystallographic integrity of monolayer MoS_2.

FETs based on Se-mediated transferred MoS_2 films

To assess the electrical quality of as-transferred monolayer MoS_2 films, we fabricate MoS_2 FETs on SiO_2/Si substrates (Fig. 3a, b) through a

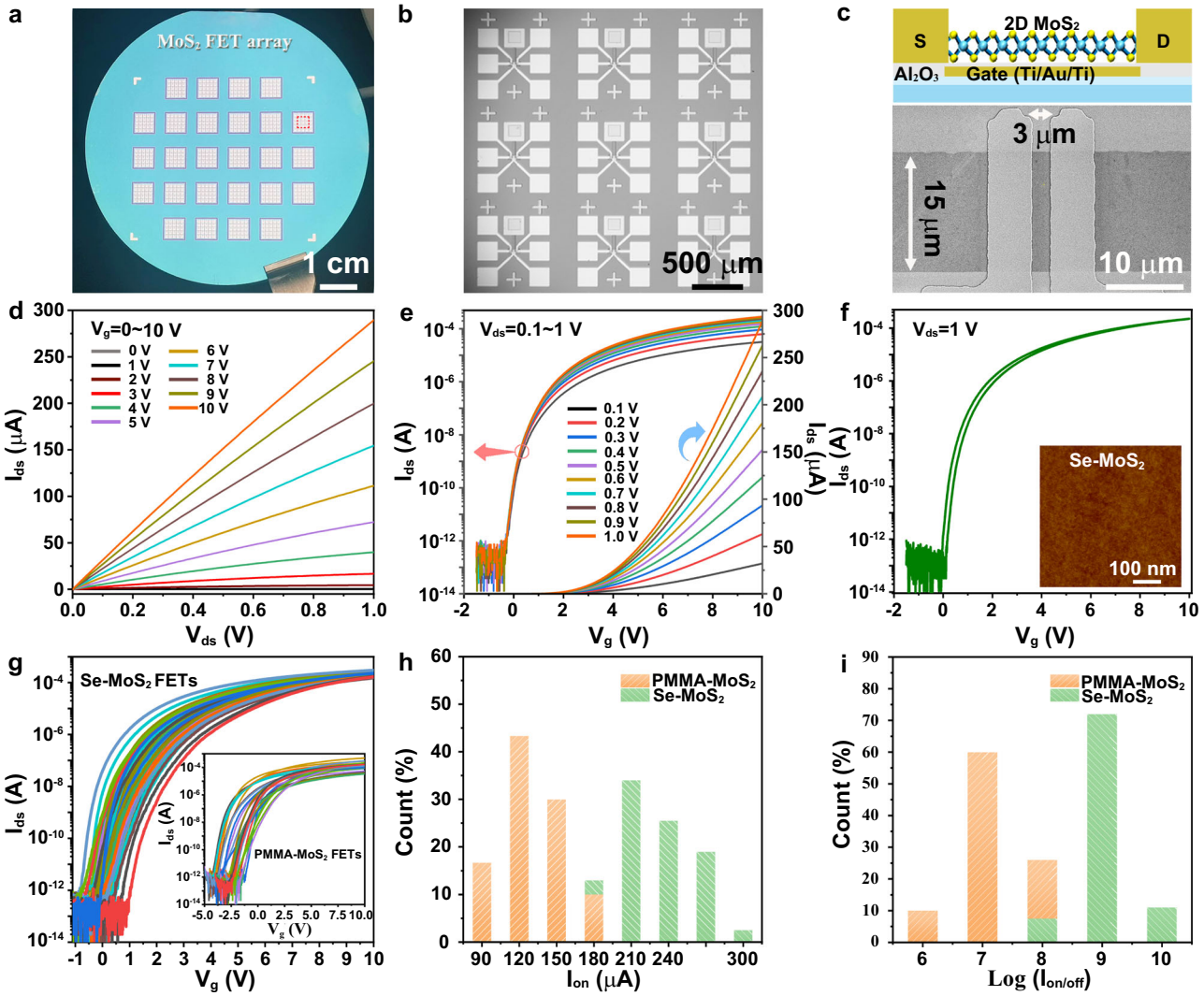

Fig. 3 | Electrical performances of field-effect transistors (FETs) based on Se-transferred MoS_2 films. Photograph (**a**) and optical image (**b**) of an as-fabricated 2-in. monolayer MoS_2 FET array. **c** Device structure and SEM image of an as-fabricated MoS_2 FET. SEM: scanning electron microscope Output (**d**) and (**e**) transfer curves of a typical MoS_2 FET. **f** Transfer curves of a FET upon double-sweeping of V_g, showing small hysteresis. V_g: the back-gate voltage. **g** The transfer characteristics curves from 200 Se-transferred MoS_2 FETs. Inset: the transfer characteristics curves of PMMA- transferred MoS_2 FETs for comparison. Statistical distribution of I_{on} (**h**) and I_{on}/I_{off} ratios (**i**) with both Se-transferred samples and PMMA-transferred samples involved. I_{on}: on-current value, I_{on}/I_{off} ratios: on/off current ratios.

gate-first technology (see Methods). 20-nm Al_2O_3 dielectric layer is involved in these back-gated FETs and the contact metal is gold (Au). Figure 3c shows the schematic device structure, along with the scanning electron microscopy (SEM) image of an individual FET. The corresponding cross-sectional TEM image and elemental mapping via EDS, depicted in Supplementary Fig. 11, confirms the accurate distribution of Mo and S within the FET channel. Typical output and transfer characteristics of a device with channel length/width of 15/3 μm are shown in Fig. 3d, e, respectively. This device exhibits an I_{on}/I_{off} ratios of ~10^9 and a threshold voltage (V_{th}) near 0 V, reflecting the highly intrinsic nature of the monolayer MoS_2 channel. Besides, Fig. 3f shows a relatively low hysteresis only about 0.08 V in typical Se-mediated transferred FET, which may be benefited from the clean surface for Se transferred 2D MoS_2 channel materials (inset of Fig. 3f). In comparison, the data from PMMA-mediated transfer method are shown in Supplementary Fig. 12a. Note that both negligible hysteresis and V_{th} shift are critical for device uniformity at a large scale. The device characterization results underscore the cleanness and integrity of the Se-transfer method, which effectively mitigates charge trapping at the interface or surface.

Electrical performances of 200 randomly selected FETs fabricated from the Se-transfer process are also presented to further validate the scalability and uniformity of them. The transfer curves of these devices are shown in Fig. 3g, in which the electron mobility (μ) and I_{on}/I_{off} ratios can reach 71.3 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 2.7×10^{10}, respectively. The statistical distribution of on-current value (I_{on}) and I_{on}/I_{off} ratios are presented in Fig. 3h, i. Similar FETs fabricated from PMMA-transfer process are also included as control samples. These devices exhibit inferior performance, with a more negative V_{th} offset (inset of Fig. 3g) caused by the presence of doping effect due to surface residues. In comparison, the small distribution of V_{th} for Se-transferred MoS_2 FETs (Supplementary Fig. 12b) indicates that the electrical properties of MoS_2 films are well preserved. As seen from in Fig. 3i, the Se-transferred FETs exhibit an average I_{on}/I_{off} ratios of 2.6×10^9, which is significantly higher than that of PMMA-transferred FETs, e.g., ~8.3×10^7. The reduced performance of PMMA-transferred MoS_2 device is attributed to the contamination and damage introduced during the wet-transfer process. Besides, the contact resistance (R_c) of Se-MoS_2 FETs and PMMA-MoS_2 FETs were measured by transmission line method (TLM) (Supplementary Fig. 13a). At $V_g = 10$ V and $V_{ds} = 1$ V, the extracted R_c and sheet resistance ($R_{\square}$) for Se-MoS_2 FETs are about 0.35 kΩ·μm and 0.92 kΩ, respectively (Supplementary Fig. 13b), significantly lower than those of PMMA-MoS_2 FETs (2.52 kΩ·μm and 1.52 kΩ). The reduction in R_c suggests that the Se-mediated transfer method yields a cleaner contact interface. These results confirm the advantage of the Se-mediated dry-transfer technique in fabricating high-performance 2D FETs.

Large-scale logic circuits

In order to investigate the logic applications of these Se-transferred MoS_2 films, we further fabricated logical units (Fig. 4a), including AND, NAND, NOR, etc. As shown in Fig. 4b, the AND, NAND and NOR logic gates are operated with two input pulses signals of 5 V (V_A and V_B), all demonstrating accurate Boolean output functionality that is consistent with the corresponding truth tables in Fig. 4c. Moreover, as-fabricated inverters (refer to the inset of Fig. 4d and Supplementary Fig. 14a) present typical voltage transfer characteristics (VTC) with V_{dd} varying from 1 to 5 V. Obviously, when V_{in} below the midpoint voltage (V_M), V_{out} reaches a high voltage equal to V_{dd}, and conversely, V_{out} approaches 0 V. Supplementary Fig. 14b further illustrates time-domain VTC curves at $V_{dd} = 5$ V. These results are consistent with the corresponding logical truth tables (inset of Fig. 4d), indicating that the inverter exhibits the inverting logic function as expected. The voltage gain (G) and static power consumption (P) of an inverter are critical parameters for evaluating its electrical performance. Figure 4e illustrates the variation of G with V_{in}, with a relatively high volage gain of ~178.8 V/V observed at $V_{dd} = 5$ V. The static power consumption of the inverter, shown in Fig. 4e, exhibits low values of ~ 4.5 nW at $V_{dd} = 1$ V. In contract, V_M of a typical PMMA-transferred MoS_2 inverter, as depicted in Supplementary Fig. 15a, exhibits a significant negative offset, and its voltage gain, approximately 113 V/V at $V_{dd} = 1$ V, along with its comparatively lower G and gradually increasing static power consumption (inset of Supplementary Fig. 15a, b), which are obviously inferior to those of the Se-transferred MoS_2 inverter.

Large-scale ring oscillators (ROs) consisting of 3-, 5-, and 11-stages are also fabricated, using the Se-transferred monolayer MoS_2. The 11-stage ring oscillator, for instance, comprises 11 cascading inverters to generate frequency oscillations (Supplementary Fig. 16a, b), along with an additional inverter serving as an output buffer. As shown in Fig. 4f, the oscillation frequencies of ROs depend on the number of stages, exhibiting distinct values for the 3-, 5-, and 11-stage configurations. Figure 4g presents the typical frequency output as a function of increasing V_{dd}, revealing an expected trend of decreasing oscillation frequency with increasing stage number (N). The oscillation frequencies reach to 1136 kHz, 711 kHz and 276 kHz for the 3-, 5-, and 11-stage ROs, respectively; and the corresponding delay time per stage (τ) of 0.14 μs, 0.14 μs and 0.16 μs, respectively, calculated by the formula of $\tau = 1/2Nf$, where f is the oscillation frequency. The nearly identical delay times across these MoS_2 ROs with varying stage numbers suggest well uniformity of the Se-transferred MoS_2 film over large areas. As a comparison, similar ROs are also fabricated from the PMMA-transferred MoS_2. As shown in Supplementary Fig. 16c, the highest oscillation frequencies achieved were 660.1 kHz, 390.6 kHz and 152.0 kHz for 3-, 5-, and 11-stage MoS_2 ROs, respectively, with corresponding delay time per stage is about 0.25 μs, 0.25 μs and 0.29 μs. These values of τ are significantly larger than those observed for the Se-transferred ROs. The results highlight the superior performance and potential of Se-assisted dry-transferred MoS_2 films for scalable advanced electronics. Compared with some previously reported about 2D film transfer strategies[21,25,27,28,32], as displayed in Fig. 4h, our Se-mediated dry-transfer route exhibits comprehensive advantages for achieve intact transfer of wafer scale 2D semiconductor MoS_2 film that retains desired cleanliness and superior electrical quality, being more compatible with standard semiconductor processes for batch fabricate 2D semiconductor ICs in future.

Discussion

A Se-mediated dry-transfer route for large-scale 2D semiconductors is developed, yielding near-perfect film integrity without residues and contaminants. The transfer process employs thermal evaporation to remove the Se intermediate layer and is compatible with the existing semiconductor fabrication process. Electrical characterizations of 2D MoS_2 FETs and logic circuits reveal intrinsic performances. This dry transfer approach effectively minimizes the formation of wrinkles and contaminations, providing a reliable solution for the large-scale production of high-performance 2D semiconductor devices.

Methods

Growth of wafer scaled MoS_2 monolayer film

Monolayer MoS_2 film is epitaxially grown on sapphire by a self-built three-temperature zone CVD system[38]. The growth process is carried out by using S (Alfa, 99.9%, 8 g) and MoO_3 (Alfa, 99.999%, 30 mg) powders as reaction sources, which are placed in the temperature zone I and II, respectively. 2-in. sapphire (c-plane) wafers are used as epitaxial substrates and placed in the temperature zone III. During the growth, the temperatures are 130 °C (zone I), 530 °C (zone II), and 930 °C (zone III) for the S, MoO_3 sources and sapphire substrate, respectively. The reactive S and MoO_3 vapors were respectively carried by Ar gas (100 sccm) and Ar (200 sccm)/O_2 (6 sccm) mixed gas, and the

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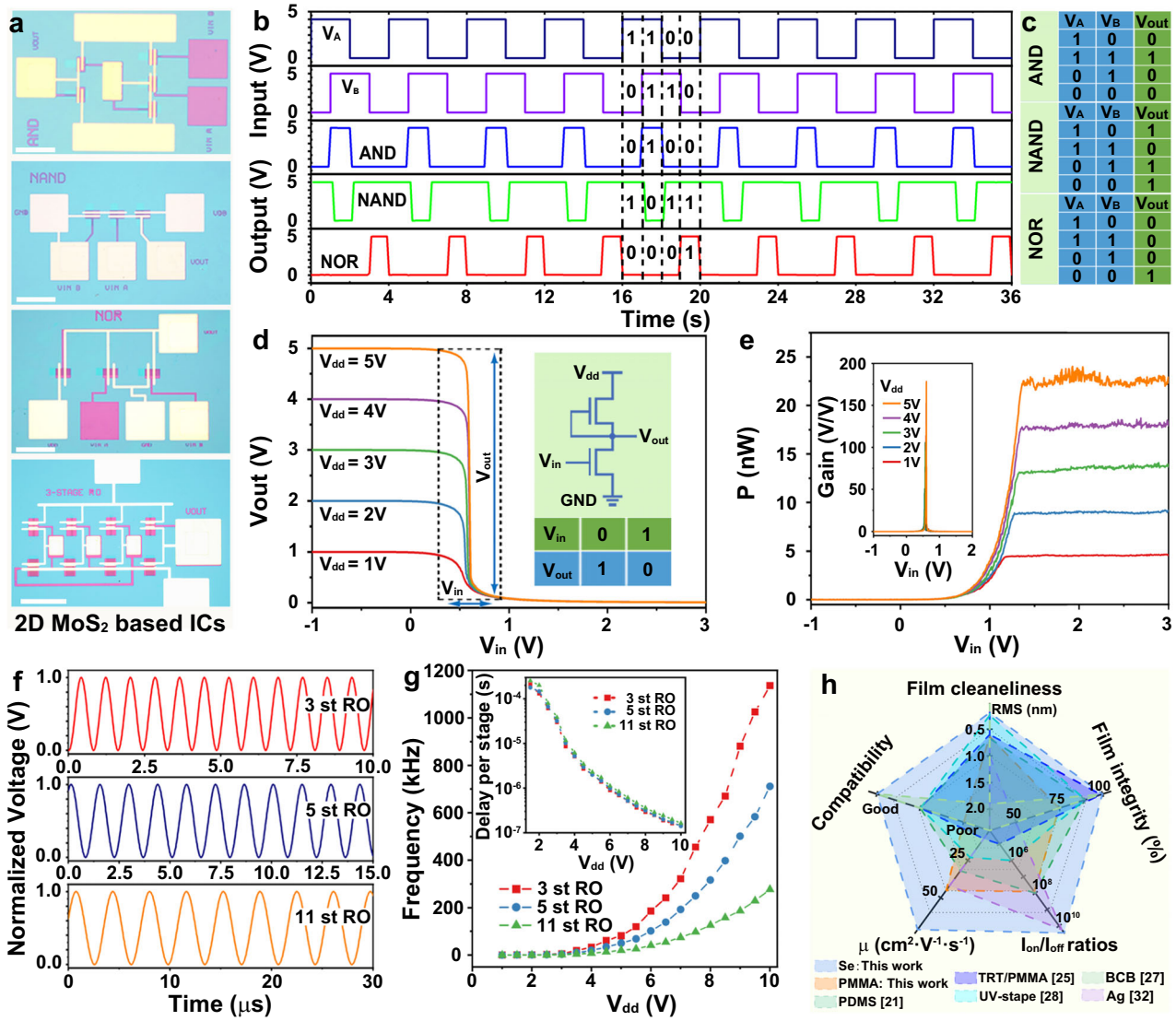

Fig. 4 | Logical circuits based on Se-mediated transferred MoS_2 films. a Optical images of AND, NAND, NOR gates, and ROs. Scale bar, 100 μm. **b** Output characteristics of an AND, NAND, NOR gate as a function of input voltage pulses at V_{dd} = 5 V. **c** The corresponding logic truth tables. **d** VTC for a MoS_2 inverter. VTC: Voltage transfer characteristics, V_{in}: input voltage, V_{out}: output voltage. **e** The static voltage gains and power consumption of a MoS_2 inverter at various V_{dd}. **f** Normalized output signals of 3-, 5-, and 11-stage 2D MoS_2 ROs measured at V_{dd} = 10 V. **g** The output frequency varies with V_{dd} from 1 V to 10 V. Inset: the corresponding delay time per stage (τ). **h** Comprehensive comparison of the Se-mediated 2D transfer strategy with parts of previous reported work. μ: the electron mobility, Compatibility: the potential of 2D films transfer method for large-scale integration based on standard semiconductor processes.

system pressure was maintained at ~1 Torr. The total growth process lasts usually about 50 mins.

Deposition of Se layer on MoS_2 film

Se films were deposited in a home-made tube furnace. High-purity Se powder (99.999%, 29 g) (the evaporation source) was placed in upstream zone (Zone-I, 270 °C) of the tube furnace, while a 2-in. MoS_2 wafer (the substrate) was positioned downstream (Zone-II, RT). The deposition duration is ~40 min, with the chamber pressure is maintained at ~1 Torr. The thickness of the Se layer used in the transfer process is typically around 500 nm. The photographs of as-prepared wafer scale MoS_2 film and that after deposition of Se film are shown in Supplementary Fig. 2, respectively.

Se-mediated transfer process

The high uniformity of Se film is firstly deposited onto MoS_2 wafer. Then, a 5 wt% PPC solution is spin-coated as a buffer layer on the Se/MoS_2/sapphire substrate at 6000 rpm for 60 s and baked at 50 °C to evaporate the solvent. The PPC/Se/MoS_2 stack is mechanically peeled off from the sapphire substrate by using hydrosol adhesive tape and transferred onto a target 3-in. substrate with a 20 nm Al_2O_3 dielectric layer. In the plying-up process of hydrosol adhesive tape to the surface of the PPC/Se/MoS_2 stack, it is important to ensure that no bubbles are trapped between the hydrosol adhesive tape and PPC/Se/MoS_2 stack. Before removing the hydrosol tape by soaking in deionized water, necessary pressure is required to ensure a close contact between the hydrosol tape/PPC/Se/MoS_2 stack and the target substrate with the assistance from an idler wheel. This step minimizes the risk of water infiltration at the edges. After removing the hydrosol tape, the sample should be carefully fished out and air-dried instead of using a nitrogen gun or other tool, which helps prevent wrinkles or breakage for transferred MoS_2 film. Subsequently, the PPC layer is stripped by RIE. Notably, this process does not affect the chemical properties of underlying Se layer or MoS_2 due to the Se layer is thick enough, as shown the cross-section of TEM image in Supplementary Fig. 2c. Finally, the Se sacrificial layer is fully removed by a thermal evaporation

at 280 °C for 5 h in N_2 atmosphere. For comparison, MoS_2 films are also transferred using the PMMA-assisted method. The 2-in. wafer of 2D MoS_2 monolayer on sapphire is first etched in KOH solution, then transferred to a 3-in. substrate with PMMA as a support layer. The PMMA is then removed by acetone.

Device fabrication

The gate electrodes are firstly patterned on SiO_2/Si substrates using UV lithography (MA6, Karl Süss), e-beam evaporation of Ti/Au/Ti (3/8/3 nm), and lifting-off process. Next, a 20-nm Al_2O_3 dielectric layer is grown on the pre-fabricated metal gates using atomic layer deposition at 300 °C. To establish a cascade connection between the lower- and upper-level metal electrodes, rectangular windows are patterned in the Al_2O_3 layer at designated locations by UV lithography, followed by etching with RIE. The 2D MoS_2 film is then transferred onto the metal gates using the Se-assisted transfer method. Subsequently, an Au/Ti/Au (5/3/35 nm) metal layer is deposited by electron beam evaporation for contact electrodes. Finally, the MoS_2 channels are defined by UV lithography and RIE (Plasma Lab 80 Plus, Oxford Instruments).

Material and device performance

The as-transferred 2D MoS_2 film is characterized using AFM (Asylum Research Cypher S) and aberration-corrected TEM (Spectra 300). Raman spectra are obtained with a confocal Raman imaging system (Horiba/LabRam HR-Evolution). XPS (Thermo Fisher ESCALAB XI+) is employed to determine the valence states and elemental composition. Electrical performance measurements are conducted using a probe station (Janis ST-500-1-4CX) equipped with a semiconductor analyzer (Agilent B1500A) and an oscilloscope (Agilent DSOX3054A).

Data availability

Relevant data supporting the key findings of this study are available within the article and the Supplementary Information file. All raw data generated during the current study are available from the corresponding authors upon request.

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Author contributions

G.Z. and N.L. co-supervised this work. X.Z. performed the device fabrications and performance characterizations with the help from T.L., J.Z., and J.L. L. Z., H.Y., S.W., H.D., L.H. and Y.Z. performed the growth of 2-in. wafer scaled monolayer MoS_2 film and Se film. X.Z., N.L., P. C. and H.Y. analyzed data. X.Z., N.L. and G.Z. wrote the manuscript. All authors commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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