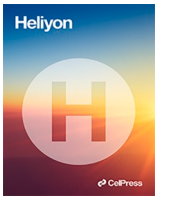
Heliyon 10 (2024) e34134

Contents lists available at ScienceDirect

Heliyon

journal homepage: www.cell.com/heliyon



Research article

Effect of interface defects on electrical characteristics of a-ITGZO TFTs under bottom, top, and dual gatings

Mingu Kang [a], Kyoungah Cho [a,*], Minhyeok Seol [a], Sangsub Kim [b], Sangsig Kim [a,**]

[a] Department of Electrical Engineering, Korea University, Anam-ro 145, Seongbuk-gu, Seoul, 02841, Republic of Korea
[b] Display Research Center, Samsung Display, Samseong-ro 1, Giheung-gu, Yongin-si, Gyeonggi-do, 17113, Republic of Korea

ARTICLE INFO

Keywords:
Amorphous indium-tin-gallium-zinc-oxide
Dual gate thin-film transistor
Bulk accumulation
Interface trap states
TCAD simulation

ABSTRACT

Here, we investigate the effects of interface defects on the electrical characteristics of amorphous indium-tin-gallium-zinc oxide (a-ITGZO) thin-film transistors (TFTs) utilizing bottom, top, and dual gatings. The field-effect mobility (27.3 $cm^2/V•s$) and subthreshold swing (222 mV/decade) under a dual gating is substantially better than those under top (12.6 $cm^2/V•s$, 301 mV/decade) and bottom (11.1 $cm^2/V•s$, 487 mV/decade) gatings. For an a-ITGZO TFT, oxygen deficiencies are more prevalent in the bottom-gate dielectric interface than in the top-gate dielectric interface, and they are less prevalent inside the channel layer than at the interfaces, indicating that the presence of oxygen deficiencies significantly affects the field-effect mobility and subthreshold swing. Moreover, the variation in the electrical characteristics due to the positive bias stress is discussed here.

1. Introduction

Amorphous oxide thin-film transistors (TFTs) have been extensively utilized in display backplanes, and their low-temperature processes allow the freedom of choice for flexible plastic substrates deformed at high temperatures [1–13]. Channel oxide materials have been intensively studied to enhance their electrical characteristics, including field-effect mobilities [14–18]. The properties of the interfaces between the channels and gate dielectric layers and the intrinsic properties of the channel materials determine the electrical characteristics. In particular, field-effect mobilities are closely related to the interface defects generated during fabrication [19–21]. Minimizing the effect of interface defects on the electrical characteristics is important for attaining high-performance oxide TFTs.

The electrical characteristics of the oxide TFTs depend on the gating type. Top, bottom, and dual gatings result in the accumulation of charge carriers near the upper and lower interfaces and bulk accumulation, respectively. Accordingly, the upper and lower interface defects substantially affect the electrical characteristics under top and bottom gatings, respectively. However, these interface defects have a relatively small effect on the electrical characteristics under a dual gating, which enhances the field-effect mobility by forming bulk accumulation [22–24]. Hence, the electrical characteristics of oxide TFTs with top, bottom, and dual gatings were compared to investigate the effects of interface defects. The hysteresis and threshold voltage shift induced by positive bias stress (PBS) under these gatings were examined, and the change in the subgap state distribution was analyzed with technology computer-aided design (TCAD)

* Corresponding author.
** Corresponding author.
E-mail addresses: chochem@korea.ac.kr (K. Cho), sangsig@korea.ac.kr (S. Kim).

https://doi.org/10.1016/j.heliyon.2024.e34134
Received 7 December 2023; Received in revised form 27 February 2024; Accepted 3 July 2024
Available online 4 July 2024

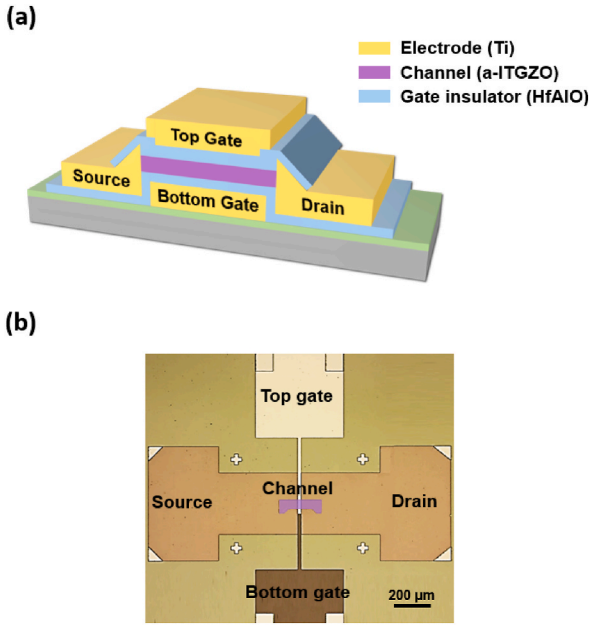


Fig. 1. (a) Schematic and (b) optical microscope image of a-ITGZO TFT with top and bottom gate electrodes.

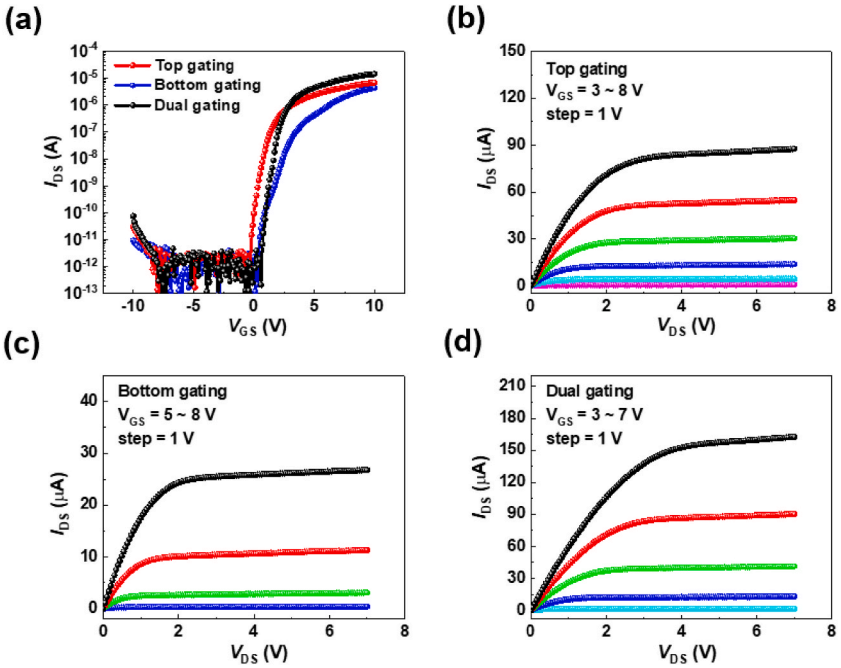


Fig. 2. (a) Transfer characteristics of top, bottom, and dual-gated TFTs. Output characteristics of TFTs under (b) top, (c) bottom, and (d) dual gatings.

simulations.

2. Experiment

We selected amorphous indium tin gallium zinc oxide (a-ITGZO) and hafnium aluminum oxide (HfAlO) as the channel material and gate dielectric, respectively. a-ITGZO TFTs were fabricated on a colorless polyimide substrate with a 15-nm-thick Al_2O_3 buffer layer deposited via atomic layer deposition (ALD) to prevent the penetration of oxygen and moisture. An a-ITGZO channel layer with a

Table 1
Electrical properties of top, bottom, and dual-gated TFTs.

Mode	μ_{FE} (cm^2/V•s)	*SS* (mV/decade)	V_{TH} (V)	I_{ON}/I_{OFF}
Top	12.6 ± 1.8	301 ± 28	1.16 ± 0.23	6.70×10^6
Bottom	11.1 ± 3.3	487 ± 60	2.17 ± 0.41	3.49×10^6
Dual	27.3 ± 6.3	222 ± 62	1.41 ± 0.55	1.97×10^7

M. Kang et al.

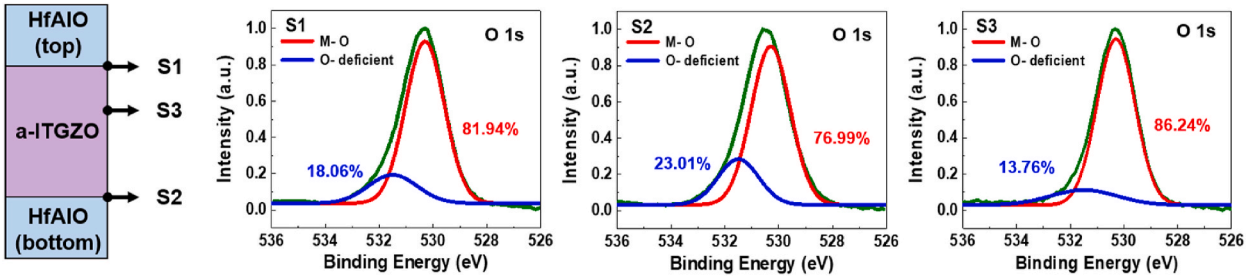


Fig. 3. XPS deconvolution of O 1s spectra at top and bottom interfaces.

thickness of 50 nm was deposited from an ITGZO target utilizing radio frequency (RF) magnetron sputtering under a gas mixture of Ar/O_2 at a working pressure of 1 mTorr and an RF power of 120 W. The length (width) of the channel layer was 20 (50) μm. The source, drain, and gate electrodes were made of Ti by thermal evaporation, and a 25-nm-thick HfAlO gate dielectric layer was deposited by ALD at 150 °C with H_2O as an oxidant and tetrakis (ethylmethylamino) hafnium and trimethylaluminum as precursors of Hf and Al.

The thicknesses of the a-ITGZO and HfAlO layers were measured with X-ray reflectometry (D8 Discover Plus, Bruker), and the oxygen bonding states were examined with X-ray photoelectron spectroscopy (XPS; ESCALAB250, Thermo Scientific). The capacitances of the gate dielectric layers were measured with an LCR meter (HP4285A, Agilent), and the I–V characteristics were examined with a semiconductor parameter analyzer (HP4155C, Agilent) in ambient air and a dark box. As for the PBS condition, a voltage of 5 V was applied to the top and bottom gate electrodes, and a voltage of 0.1 V was applied to the drain electrode. Silvaco Atlas (version 5.0.10. R) was utilized as a TCAD device simulator.

3. Results and discussion

Fig. 1 presents a schematic (a) and an optical microscope image (b) of the a-ITGZO TFT with top and bottom gate electrodes, which can be electrically tied together for a dual gating. Fig. 2 illustrates the transfer curves (a) and output curves (b–d) of the TFT under the top, bottom, and dual gatings; the transfer curves were obtained at a drain-to-source voltage (V_{DS}) of 0.1 V. The field-effect mobility (μ_{FE}) in the linear regime and the subthreshold swing (*SS*) are estimated with the following equations.

$$I_{DS} = \frac{C_{ox}\mu}{2}\frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right] \quad (1)$$

$$SS = \frac{\partial V_{GS}}{\partial(\log I_{DS})} \quad (2)$$

where I_{DS} is the drain-to-source current, C_{ox} (=286 nF/cm^2) is the gate dielectric capacitance per unit area, *W*/*L* (50/20 μm) is the ratio of the channel width to the length, and V_{TH} is the threshold voltage determined as the V_{GS} corresponding to I_{DS} of *W*/*L* × 10 nA. The μ_{FE} values are 12.6, 11.1, and 27.3 cm^2/V•s for the top, bottom, and dual gatings, respectively. The *SS* values are 301, 487, and 222 mV/decade for the top, bottom, and dual gatings, respectively. Table 1 presents the field-effect mobilities, subthreshold swings, threshold voltages, and ON/OFF current ratios (I_{ON}/I_{OFF}). A comparison of these values reveals that the electrical characteristics under a bottom gating are inferior to those under a top gating and that the electrical characteristics under a dual gating are better than those under both top and bottom gatings.

The metal–oxygen (M − O) and oxygen-deficient (O-deficient) bonds of the S1 (S2) interface between the channel and top (bottom) gate dielectric layers and the inner part S3 of the channel were examined by XPS. Fig. 3 illustrates the XPS deconvolution of the O 1s spectra of S1, S2, and S3. An O 1s spectrum can be deconvoluted into an M − O bonding peak at 530.3 eV and an O-deficient peak at 531.5 eV, and the ratios of the O-deficient bonding at S1, S2, and S3 are 18.06, 23.01, and 13.76 %, respectively. Oxygen deficiencies are more prevalent at the interfaces than inside the channel layer, and they are more prevalent at the lower interface than at the upper interface. The surface of the bottom-gate dielectric layer beneath the channel layer is exposed to plasma during channel formation.

The presence of oxygen deficiencies that act as traps degrades the electrical characteristics of a-ITGZO TFT. A comparison between the electrical characteristics under the top, bottom, and dual gatings and the ratios of the O-deficient bonding at S1, S2, and S3 reveals

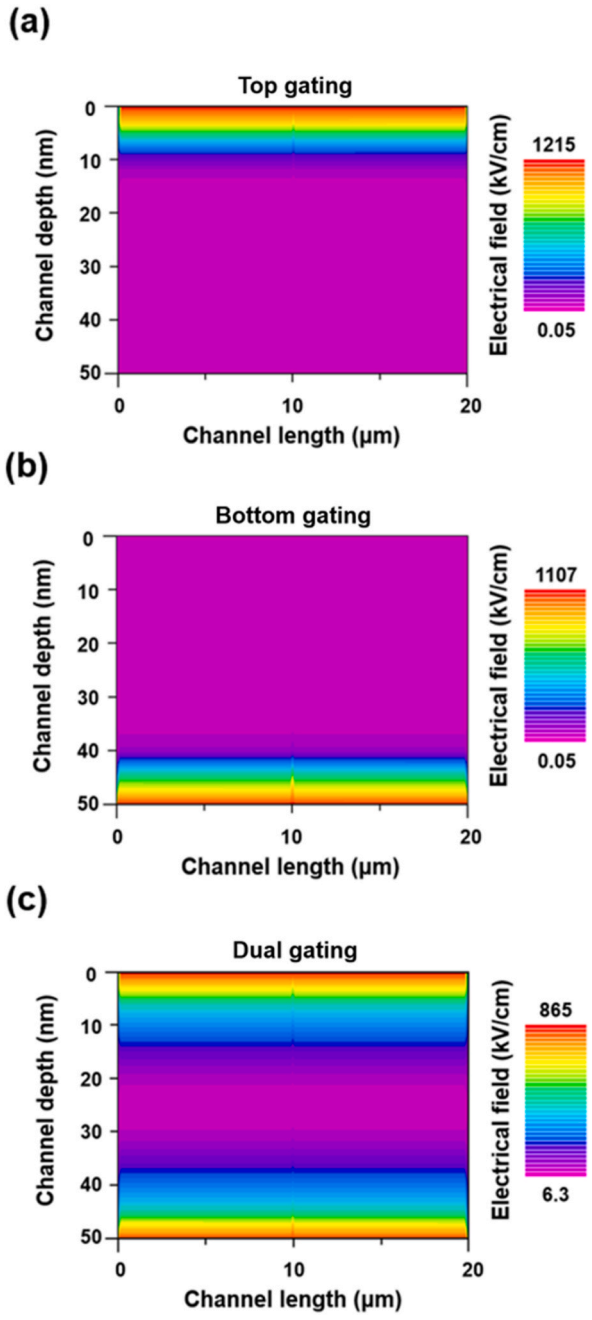


Fig. 4. Vertical electric field in channels of (a) top, (b) bottom, and (c) dual-gated TFTs at gate voltage of 10 V.

that the presence of oxygen deficiencies at the interfaces affects the electrical characteristics under the bottom gating more than those under the top gating. They have relatively less effect on the electrical characteristics under the dual gating than the top and bottom gates.

Fig. 4 illustrates the vertical electric field in the channel under the top (a), bottom (b), and dual (c) gatings at a gate voltage of 10 V. The vertical electric field causes scattering of charge carriers at the interface between the channel and gate dielectric layers, and thereby the vertical electric field affects the μ_{FE} [25–27]. Compared with the top (1215 kVcm^{-1}) and bottom (1107 kVcm^{-1}) gatings, the vertical electric field in the dual-gated (865 kVcm^{-1}) channel is relatively low; hence, the dual-gated TFT has a higher μ_{FE} than the top and bottom gated TFTs. Moreover, the gated region in the channel of the dual-gated TFT was deeper than the sum of the two parallel-gated regions of the top- and bottom-gated TFTs, implying that bulk accumulation occurred in the dual-gated TFT. The bulk accumulation enhances the μ_{FE} and I_{ON}/I_{OFF} of the dual-gated TFT along with the relatively low vertical electrical field. The I_{ON}/I_{OFF}

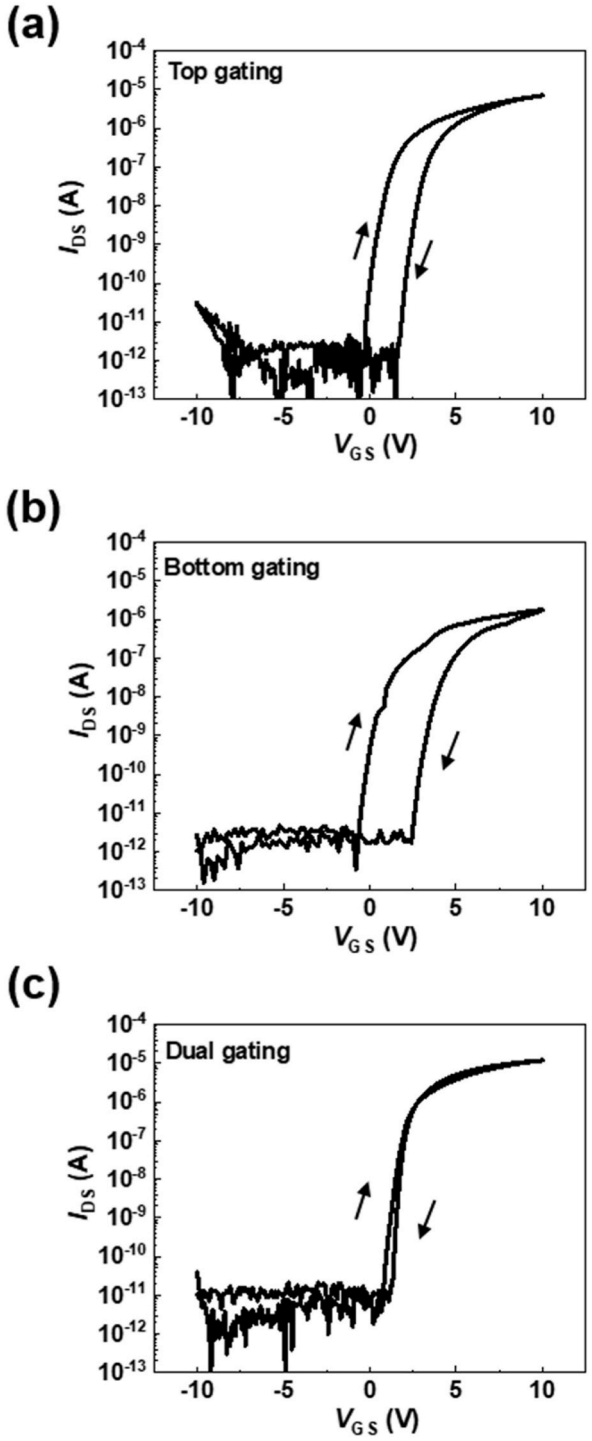


Fig. 5. Hysteresis curves of TFTs under (a) top, (b) bottom, and (c) dual gatings.

values are 6.70×10^6, 3.49×10^6, and 1.97×10^7 for the top, bottom, and dual gatings, respectively.

Hysteresis characteristics reflect the density of interface traps (D_{it}) between the channel and gate dielectric layers [28]. Fig. 5 presents the hysteresis curves under the top (a), bottom (b), and dual (c) gatings, indicating clockwise hysteresis regardless of the gating type. The hysteresis widths are 1.97, 2.99, and 0.20 V for the top, bottom, and dual gatings, respectively. D_{it} was determined with the following equation.

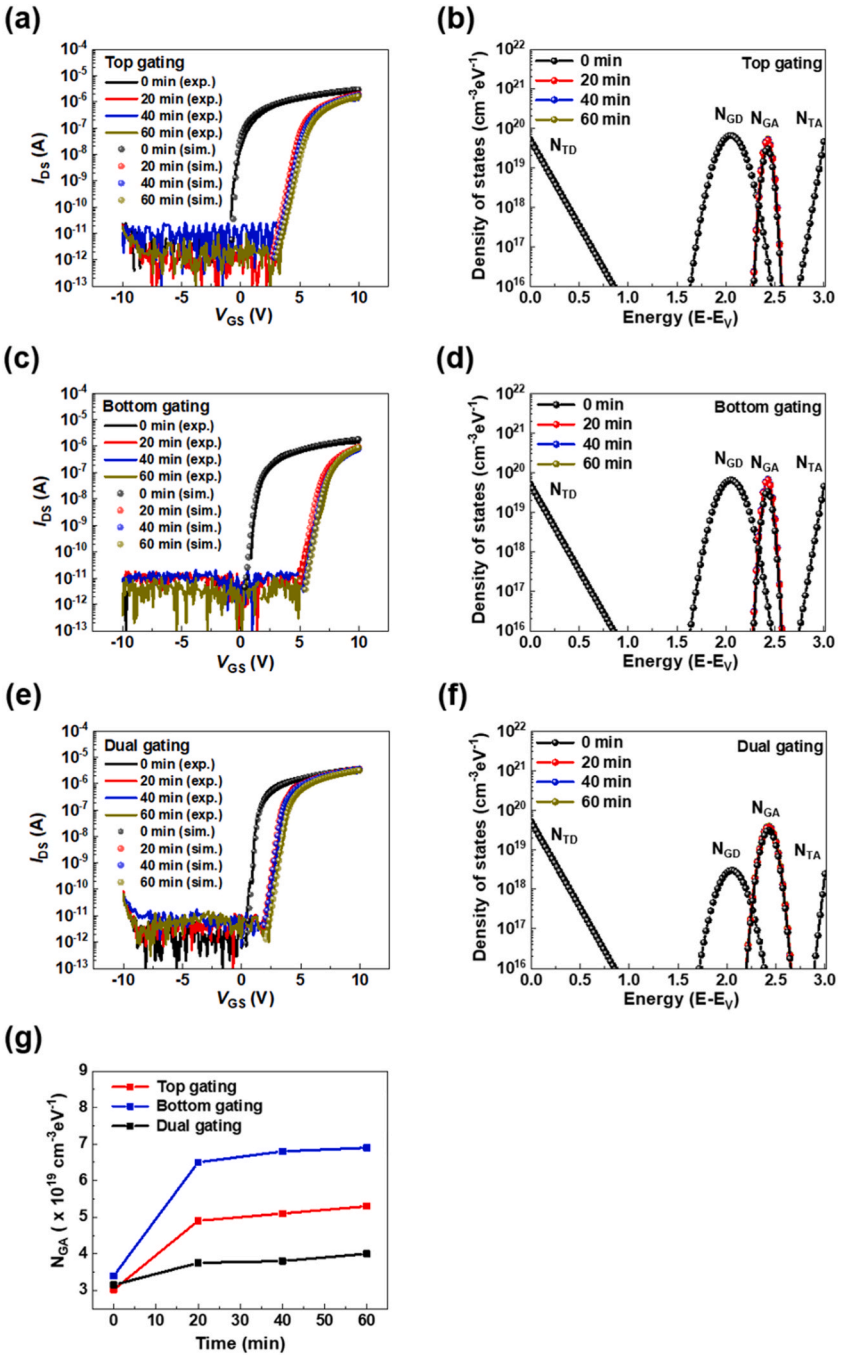


Fig. 6. Transfer curves under PBS and TCAD simulation fitting of (a) top, (c) bottom, and (e) dual-gated TFTs. Density of state of a-ITGZO in (b) top, (d) bottom, and (f) dual-gated TFTs under PBS. (g) N_{GA} of dual, top, and bottom gated TFTs under PBS.

$$D_{it} = \left(\frac{SS}{\frac{k_B T}{q} \ln 10} - 1 \right) \frac{C_{ox}}{q} \tag{3}$$

where k_B is the Boltzmann constant, T is the absolute temperature, and q is the charge quantity [29]. The D_{it} values are calculated to be 6.4×10^{12}, 1.1×10^{13}, and 4.3×10^{12} cm^{-2}eV^{-1} for the top, bottom, and dual gatings, respectively, which is deeply concerned with the hysteresis width.

The hysteresis width and D_{it} values were consistent with the ratios of O-deficient bonding, indicating that they were caused by oxygen deficiencies at the interfaces. The large hysteresis width and high D_{it} value of the bottom-gated TFT were ascribed to oxygen deficiencies at the interface caused by the plasma during the deposition of the a-ITGZO channel. The dual-gated TFT has the same interfaces as those of the top- and bottom-gated TFTs; therefore, the D_{it} values reveal the relationship between the dual-gating effect and the effect of defects on the electrical characteristics. Thus, the performance of the TFT can be improved by a dual gating, even though the TFT has interface defects between the channel and gate dielectric.

The transfer curves of the a-ITGZO TFT under the top (a), bottom (c), and dual (e) gatings were fitted with a TCAD simulation (Fig. 6) to analyze the change in the subgap trap states of the a-ITGZO TFTs during PBS. After the PBS for 60 min, the positive threshold voltage shifts (ΔV_{TH}) are 5.09, 5.69, and 2.50 V for the top, bottom, and dual gatings, respectively. The densities of the states in PBS demonstrate that there are no differences in the distributions of the donor-like tail states (N_{TD}), donor-like Gaussian states (N_{GD}), and acceptor-like tail states (N_{TA}) for the top (b), bottom (d), and dual (f) gatings. However, the density of acceptor-like Gaussian states (N_{GA}) increases with the duration of the PBS, regardless of the gating mode. The positive ΔV_{TH} after the PBS is attributed to electron trapping at the interface [30,31]. The N_{GA} is associated with the neutral oxygen interstitial (O_i) state that traps electrons and generates negatively charged species of oxygen such as O_i^- or O_i^{2-} ($O + e \rightarrow O^-$ or $O + 2e \rightarrow O^{2-}$) [32,33]. Fig. 6 (g) illustrates N_{GA} in PBS. After 60 min, the N_{GA} increased to 75.5 %, 102 %, and 27 % for the top, bottom, and dual gatings, respectively. A larger increase of N_{GA} under the bottom and top gatings induces a significant ΔV_{TH} after the PBS, while a relatively smaller increase of N_{GA} under the dual gating leads to a relatively insignificant ΔV_{TH}. Thus, interface defects lower the performance of TFTs, and a dual gating is an effective way to minimize their effects on electrical characteristics.

4. Conclusion

We examined the effect of interface defects on the electrical characteristics of a-ITGZO TFTs by comparing the electrical characteristics of top, bottom, and dual gatings. The presence of defects at the interfaces affects the electrical characteristics under a bottom gating more than those under a top gating, and they affect the electrical characteristics under a dual gating, which is relatively less than that under top and bottom gatings. Dual gating minimizes the effects of interface defects on electrical characteristics.

CRediT authorship contribution statement

Mingu Kang: Writing – review & editing, Visualization, Validation, Software, Project administration, Methodology, Investigation, Formal analysis, Data curation, Conceptualization, Writing – original draft. **Kyoungah Cho:** Writing – review & editing, Project administration, Methodology, Conceptualization. **Minhyeok Seol:** Writing – review & editing, Software, Investigation, Data curation. **Sangsub Kim:** Writing – review & editing, Resources, Conceptualization. **Sangsig Kim:** Writing – review & editing, Supervision, Project administration, Resources.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

This research was partly supported by Samsung Display Co. Ltd., the Brain Korea 21 Plus Project, the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) (2020R1A2C3004538, 2022M3I7A3046571, RS-2023-00260876), and the Korea University Grant.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.heliyon.2024.e34134.

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors, Nature 432 (2004) 488–492, https://doi.org/10.1038/nature03090.

[2] S.Y. Lee, Comprehensive review on amorphous oxide semiconductor thin film transistor, Trans. Electr. Electron. Mater. 21 (2020) 235–248, https://doi.org/10.1007/s42341-020-00197-w.

[3] T. Kim, C.H. Choi, J.S. Hur, D. Ha, B.J. Kuh, Y. Kim, M.H. Cho, S. Kim, J.K. Jeong, Progress, challenges, and opportunities in oxide semiconductor devices: a key building block for applications ranging from display backplanes to 3D integrated semiconductor chips, Adv. Mater. (2022) 2204663, https://doi.org/10.1002/adma.202204663.

[4] M.M. Hasan, S. Roy, Mohit, E. Tokumitsu, H.-Y. Chu, S.C. Kim, J. Jang, High performance, amorphous InGaZnO thin-film transistors with ferroelectric ZrO_2 gate insulator by one step annealing, Appl. Surf. Sci. 611 (2023) 155533, https://doi.org/10.1016/j.apsusc.2022.155533.

[5] W.-H. Choi, K. Kim, S.-G. Jeong, J.-H. Han, J. Jang, J. Noh, K.-S. Park, J.-J. Kim, S.-Y. Yoon, W. Jeon, J.-S. Park, The significance on structural modulation of buffer and gate insulator for ALD based InGaZnO TFT applications, IEEE Trans. Electron. Dev. 68 (2021) 6147–6153, https://doi.org/10.1109/TED.2021.3117749.

[6] H. Kong, K. Cho, H. Lee, S. Lee, J. Lim, S. Kim, Bias-stress stability of top-gate coplanar a-ITGZO TFTs with HfO_2 and HfAlO gate dielectrics, Mater. Sci. Semicond. Process. 143 (2022) 106527, https://doi.org/10.1016/j.mssp.2022.106527.

[7] J. Sheng, T. Hong, H.-M. Lee, K. Kim, M. Sasase, J. Kim, H. Hosono, J.-S. Park, Amorphous IGZO TFT with high mobility of ~70 cm^2/(V s) via vertical dimension control using PEALD, ACS Appl. Mater. Interfaces 11 (2019) 40300–40309, https://doi.org/10.1021/acsami.9b14310.

[8] W. Xu, G. Zhang, X. Feng, Effects of atomic-layer-deposition temperature on the properties of Al_2O_3 insulators and InAlZnO thin-film-transistors with dual-active-layer structure, Appl. Surf. Sci. 578 (2022) 151987, https://doi.org/10.1016/j.apsusc.2021.151987.

[9] A. Abliz, P. Nurmamat, D. Wan, Rational design of oxide heterostructure InGaZnO/TiO_2 for high-performance thin-film transistors, Appl. Surf. Sci. 609 (2023) 155257, https://doi.org/10.1016/j.apsusc.2022.155257.

[10] P. Wang, H. Yang, J. Li, X. Zhang, L. Wang, J. Xiao, B. Zhao, S. Zhang, L. Lu, Synergistically enhanced performance and reliability of abrupt metal-oxide heterojunction transistor, Adv. Electron. Mater. 9 (2023) 2200807, https://doi.org/10.1002/aelm.202200807.

[11] Y.-S. Shiah, K. Sim, Y. Shi, K. Abe, S. Ueda, M. Sasase, J. Kim, H. Hosono, Mobility–stability trade-off in oxide thin-film transistors, Nat. Electron. 4 (2021) 800–807, https://doi.org/10.1038/s41928-021-00671-0.

[12] H. Lee, K. Cho, D. Kim, S. Kim, Electrical characteristics of bendable a-ITGZO TFTs on colorless polyimide substrates, Semicond. Sci. Technol. 35 (2020) 065014, https://doi.org/10.1088/1361-6641/ab8439.

[13] H. Lee, K. Cho, H. Kong, S. Lee, J. Lim, S. Kim, Electrical characteristics of flexible amorphous indium–tin–gallium–zinc oxide thin-film transistors under repetitive mechanical stress, Jpn. J. Appl. Phys. 60 (2021) 090903, https://doi.org/10.35848/1347-4065/ac1c8d.

[14] K. Liang, Y. Wang, S. Shao, M. Luo, V. Pecunia, L. Shao, J. Zhao, Z. Chen, L. Mo, Z. Cui, High-performance metal-oxide thin-film transistors based on inkjet-printed self-confined bilayer heterojunction channels, J. Mater. Chem. C 7 (2019) 6169–6177, https://doi.org/10.1039/C8TC06596A.

[15] Y.S. Kim, W.B. Lee, H.J. Oh, T. Hong, J.S. Park, Remarkable stability improvement with a high-performance PEALD-IZO/IGZO top-gate thin-film transistor via modulating dual-channel effects, Adv. Mater. Interfac. 9 (2022) 2200501, https://doi.org/10.1002/admi.202200501.

[16] C.-Y. Park, S.-P. Jeon, J.B. Park, H.-B. Park, D.-H. Kim, S.H. Yang, G. Kim, J.-W. Jo, M.S. Oh, M. Kim, Y. H Kim, S.K. Park, High-performance ITO/a-IGZO heterostructure TFTs enabled by thickness-dependent carrier concentration and band alignment manipulation, Ceram. Int. 49 (2023) 5905–5914, https://doi.org/10.1016/j.ceramint.2022.10.098.

[17] A. Olziersky, P. Barquinha, A. Vilà, C. Magana, E. Fortunato, J.R. Morante, R. Martins, Role of Ga_2O_3–In_2O_3–ZnO channel composition on the electrical performance of thin-film transistors, Mater. Chem. Phys. 131 (2011) 512–518, https://doi.org/10.1016/j.matchemphys.2011.10.013.

[18] J.T. Jang, D. Kim, J.H. Baeck, J.U. Bae, J. Noh, S.-W. Lee, K.-S. Park, J.J. Kim, S.Y. Yoon, C. Kim, Y.-S. Kim, S. Oh, D.H. Kim, Cation composition-dependent device performance and positive bias instability of self-aligned oxide semiconductor thin-film transistors: including oxygen and hydrogen effect, ACS Appl. Mater. Interfaces 14 (2022) 1389–1396, https://doi.org/10.1021/acsami.1c18890.

[19] I.M. Choi, M.J. Kim, N. On, A. Song, K.-B. Chung, H. Jeong, J.K. Park, J.K. Jeong, Achieving high mobility and excellent stability in amorphous In–Ga–Zn–Sn–O thin-film transistors, IEEE Trans. Electron. Dev. 67 (2020) 1014–1020, https://doi.org/10.1109/TED.2020.2968592.

[20] J. Lee, C.H. Choi, T. Kim, J. Hur, M.J. Kim, E.H. Kim, J.H. Lim, Y. Kang, J.K. Jeong, Hydrogen-doping-enabled boosting of the carrier mobility and stability in Amorphous IGZTO transistors, ACS Appl. Mater. Interfaces 14 (2022) 57016–57027, https://doi.org/10.1021/acsami.2c18094.

[21] M. Mativenga, S. An, J. Jang, Bulk accumulation a-IGZO TFT for high current and turn-on voltage uniformity, IEEE Electron. Device Lett. 34 (2013) 1533–1535, https://doi.org/10.1109/LED.2013.2284599.

[22] H. Lim, H. Yin, J.-S. Park, I. Song, C. Kim, J. Park, S. Kim, S.-W. Kim, C.B. Lee, Y.C. Kim, Y.S. Park, D. Kang, Double gate GaInZnO thin film transistors, Appl. Phys. Lett. 93 (2008) 063505, https://doi.org/10.1063/1.2967456.

[23] M. Chun, J.G. Um, M.S. Park, M.D.H. Chowdhury, J. Jang, Effect of top gate potential on bias-stress for dual gate amorphous indium-gallium-zinc-oxide thin film transistor, AIP Adv. 6 (2016) 075217, https://doi.org/10.1063/1.4960014.

[24] W.-S. Liu, C.-H. Hsu, Y. Jiang, Y.-C. Lai, H.-C. Kuo, Improving device characteristics of dual-gate IGZO thin-film transistors with Ar–O_2 mixed plasma treatment and rapid thermal annealing, Membranes 12 (2022) 49, https://doi.org/10.3390/membranes12010049.

[25] S.-i. Takagi, A. Toriumi, M. Iwase, H. Tango, On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration, IEEE Trans. Electron. Dev. 41 (1994) 2357–2362, https://doi.org/10.1109/16.337449.

[26] H.M. Nayfeh, C.W. Leitz, A.J. Pitera, E.A. Fitzgerald, J.L. Hoyt, D.A. Antoniadis, Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs, IEEE Electron. Device Lett. 24 (2003) 248–250, https://doi.org/10.1109/LED.2003.810885.

[27] K.-S. Son, J.-S. Jung, K.-H. Lee, T.-S. Kim, J.-S. Park, Y.-H. Choi, K. Park, J.-Y. Kwon, B. Koo, S.-Y. Lee, Characteristics of double-gate Ga–In–Zn–O thin-film transistor, IEEE Electron. Device Lett. 31 (2010) 219–221, https://doi.org/10.1109/LED.2009.2038805.

[28] C. Avis, J. Jang, Understanding the origin of the hysteresis of high-performance solution processed polycrystalline SnO_2 thin-film transistors and applications to circuits, Membranes 12 (2022) 7, https://doi.org/10.3390/membranes12010007.

[29] Y. Guan, Y. Zhang, J. Li, J. Li, Y. Zhang, Z. Wang, Y. Ding, M. Chan, X. Wang, L. Lu, S. Zhang, Ultra-thin top-gate insulator of atomic-layer-deposited HfO_x for amorphous InGaZnO thin-film transistors, Appl. Surf. Sci. 625 (2023) 157177, https://doi.org/10.1016/j.apsusc.2023.157177.

[30] Z. Zhu, W. Cao, X. Huang, Z. Shi, D. Zhou, W. Xu, Analysis of nitrogen-doping effect on sub-gap density of states in a-IGZO TFTs by TCAD simulation, Micromachines 13 (2022) 617, https://doi.org/10.3390/mi13040617.

[31] J.K. Jeong, H. Won Yang, J.H. Jeong, Y.-G. Mo, H.D. Kim, Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors, Appl. Phys. Lett. 93 (2008), https://doi.org/10.1063/1.2990657.

[32] W.-T. Fan, P.-T. Liu, P.-Y. Kuo, C.-M. Chang, I.H. Liu, Y. Kuo, Numerical analysis of oxygen-related defects in amorphous In-WO nanosheet thin-film transistor, Nanomaterials 11 (2021) 3070, https://doi.org/10.3390/nano11113070.

[33] M. Labed, N. Sengouga, A.F. Meftah, Simulation of the effect of deep defects created by hydrogen on the performance of amorphous indium gallium zinc oxide thin film transistor (a-IGZO TFT), Mater. Res. Express 6 (2019) 075904, https://doi.org/10.1088/2053-1591/ab11a5.