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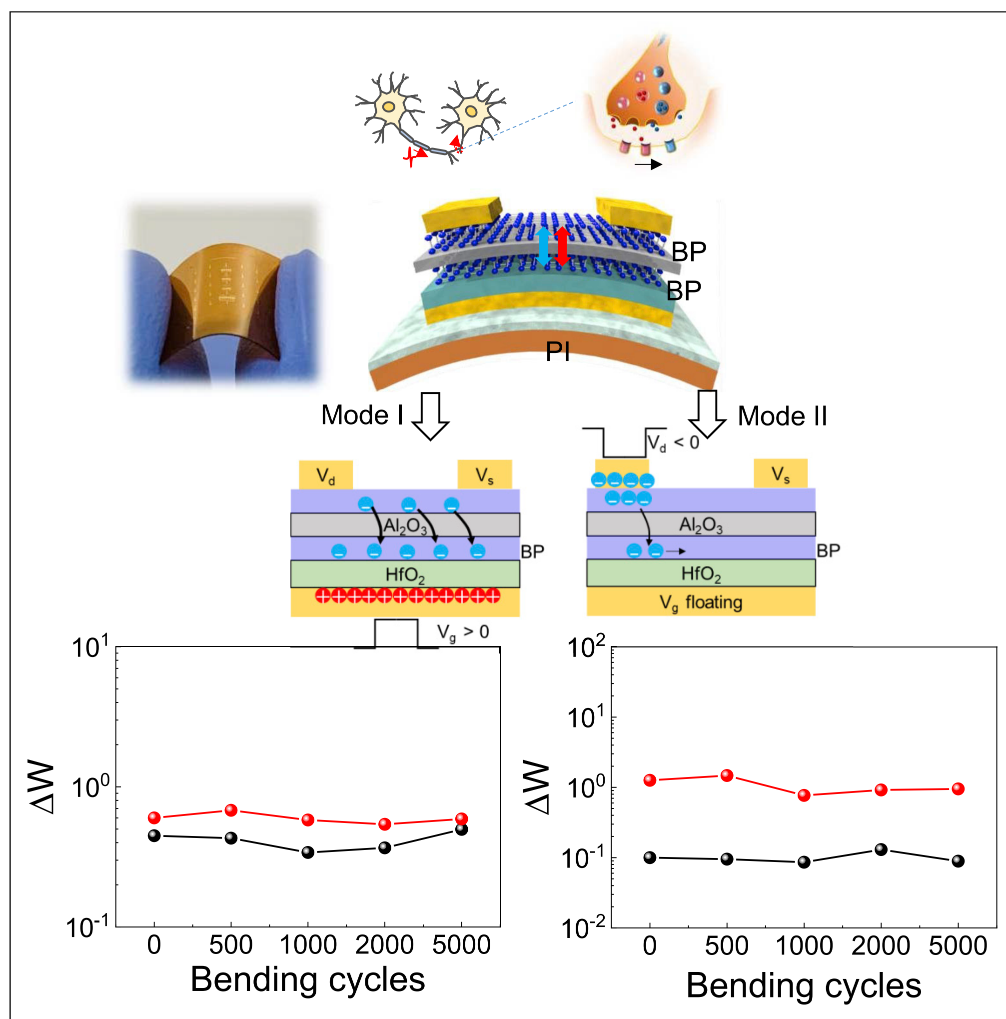


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Highlights

Flexible synaptic transistors based on black phosphorus

Dual electrical modulation for charge trapping in floating gate structure

Nanosecond-level synaptic response and low power consumption

Good endurance against mechanical bending of over thousands of times

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# Flexible synaptic floating gate devices with dual electrical modulation based on ambipolar black phosphorus

Xiong Xiong,[1] Xin Wang,[2] Qianlan Hu,[2] Xuefei Li,[2] and Yanqing Wu[1,2,3,4,*]

## SUMMARY

**Two-dimensional van der Waals materials offer various possibilities for synaptic devices, matching the requirements of intelligent and energy-efficient computation. However, very few studies on robust flexible synaptic transistors have been reported, which hold great potential for soft robotics and wearable applications. Here a floating gate synaptic device based on ambipolar black phosphorus (BP) on a flexible substrate has been demonstrated with two working modes. The three-terminal mode, where the carriers are injected into the floating gate, shows a nonvolatile memory effect, whereas the two-terminal mode shows a quasi-nonvolatile memory effect. Remarkably, the synaptic device working on the three-terminal mode shows an excellent performance in the energy-efficient computation of sub-fJ/spike with a fast gate voltage response down to ∼10 ns. Furthermore, the flexible synaptic device exhibits good endurance under 5,000 bending cycles with a strain of ∼0.63%, suggesting great potential in flexible neuromorphic applications with low energy consumption.**

## INTRODUCTION

The recent rise of interest in neuromorphic computing that mimics the ability of the brain in combining computation and storage with energy efficiency into a compact space focus on new computing architectures that distinguish from traditional von Neumann architectures (Boybat et al., 2018; van de Burgt et al., 2017; von Neumann, 2012; Wang et al., 2017; Zidan et al., 2018). In neuroscience, biological neurons with synapses form a living electrochemical system. The excitatory or inhibitory effect of a biological synapse is determined by the specific neurotransmitter released from the presynaptic neuron to the postsynaptic neuron (Gerstner et al., 2014). As a result, synaptic devices designed by imitating biological synapses play a crucial role in brain-inspired computing architecture. Many kinds of artificial synapses have been demonstrated in the past few decades. Synapses based on complementary metal-oxide-semiconductor transistor (CMOS) circuit are compatible with existing industrial processes but require many transistors to realize one synapse with complex interconnection and high energy consumption (Arthur and Boahen, 2006; Indiveri et al., 2006; Merolla et al., 2014; Qiao et al., 2015). Synaptic functions with a single device can be realized by conventional memristors and transistor-based neuromorphic devices but with unsatisfactory energy consumption when compared with that of the human brain of ∼10 fJ level (Erokhin et al., 2011; Jo et al., 2010; Kuzum et al., 2013; Yang et al., 2017). Two-dimensional (2D) van der Waals heterojunctions offer various possibilities for new classes of functional devices with low power and flexible applications in a compact space because of their multifarious energy band design and ultrathin body (Gao et al., 2019; Geim and Grigorieva, 2013; Gong et al., 2013; Huang et al., 2017; Shim et al., 2016; Xiong et al., 2020a, 2020b). Various heterostructures can be designed and fabricated without considering the lattice constant mismatching by van der Waals forces between different 2D semiconductors (Geim and Grigorieva, 2013; Huang et al., 2017). Synaptic devices based on 2D semiconductors or 2D heterostructures with low energy consumption (Wang et al., 2020) were reported but most of them suffered from a slow operation speed around millisecond-level (Huh et al., 2018; Qin et al., 2017; Sharbati et al., 2018; Tian et al., 2016, 2017a, 2017b; Zhu et al., 2018), preventing the further reduction in power consumption. Moreover, very few studies have been performed on the mechanically bending robustness of flexible synaptic devices. As a result, high performance bendable artificial synaptic devices with low energy consumption and fast operation time are strongly desired and remain to be explored.

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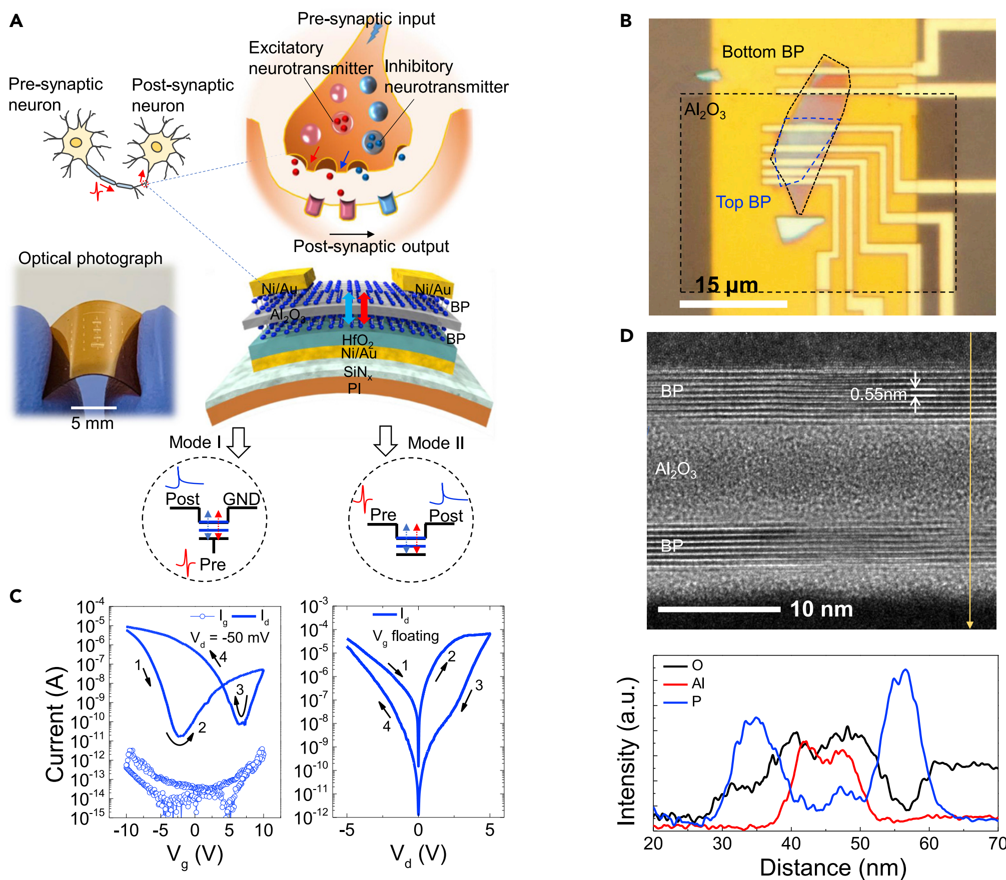


**Figure 1. BP-based floating gate synaptic devices**

(A) Schematic illustration of the concept of using BP based floating gate synaptic devices as synapses between neurons, which shows the optical image (The scale bar is 5 mm) and a schematic diagram of the floating-gate synaptic device based on BP transistors on a flexible polyimide (PI) substrate with two working modes.

(B) The optical image shows the topography geometry of the device on the PI substrate, where the dashed line represents the edge of the two BP films and $Al_2O_3$ layer (The scale bar is 15 μm).

(C) I-V characteristics of the BP synaptic devices working on Mode I which is operated by $V_g$ (left panel) and Mode II operated by $V_d$ (right panel).

(D) Cross section transmission electron microscopy (TEM) image showing the structure of BP/$Al_2O_3$/BP (The scale bar is 10 nm) and the corresponding high-resolution energy-dispersive X-ray spectroscopy (EDX) mappings of the P, Al, and O elements.

In this work, we demonstrate floating-gate synaptic devices based on black phosphorus (BP) transistors working at dual modes with pre-patterned local-gate structures using another BP film as a charge trapping layer on a flexible substrate. As expected, the devices exhibit a significant current hysteresis owing to the superior charge-trapping capacity of the BP floating gate, which is essential for synaptic operation. Different from traditional RRAM devices with abrupt switching (Ge et al., 2018; Zhao et al., 2017), the post-synaptic current (PSC) of the floating gate synaptic devices can be gradually depressed or potentiated by continuous pulse stimulation. It is interesting to note that the two modes correspond to the nonvolatile and the quasi-nonvolatile memory effects by the three-terminal and two-terminal operations, respectively. The devices can be operated using an ultrafast pulse voltage of ~10 ns at three-terminal mode with a low energy consumption of sub-fJ/spike. Furthermore, the bending test for the synaptic functions has been carried out, suggesting a great potential in flexible neuromorphic applications with low energy consumption.

## RESULTS

Figure 1A shows the schematic of a biological synapse connected with the biological neurons. From a biophysical point of view, action potentials are the result of currents passing through different

neurotransmitters. It also shows an optical image and a schematic diagram of the floating-gate synaptic devices based on BP transistors on a flexible polyimide (PI) substrate in Figure 1A. A 200 nm $Si_3N_4$ layer was deposited on PI using plasma-enhanced chemical vapor deposition (PECVD) before patterning 20/50 nm Ni/Au as the local gate by standard electron beam lithography (EBL) process. After depositing 20 nm $HfO_2$ as the blocking oxide, a mechanically exfoliated BP film was transferred within the gate region as the charge trapping layer. Next, the charge tunneling layer of 7 nm $Al_2O_3$ was deposited by atomic layer deposition (ALD), followed by transferring another BP film as the channel layer on the existing structure with careful alignment. Finally, the source/drain metal of the Ni/Au stack was patterned on the top of the channel BP film. Figure 1B shows the optical micrograph of the geometry of a device on a local gate electrode, in which two pieces of BP flakes are separated by an $Al_2O_3$ layer. The corresponding crosssection of the device is characterized by transmission electron microscopy (TEM) as shown in Figure 1D. The exact BP/$Al_2O_3$/BP stacked structure with the highly crystalline layered lattice of BP of the device can be observed. High-resolution energy-dispersive X-ray spectroscopy (EDX) mapping is used to investigate the composition of the corresponding cross-sectional regions, showing the P, O, and Al element profiles. The thickness of the channel BP, $Al_2O_3$, and floating gate BP layers is measured to be around 10, 7, and 12 nm, respectively. The scanning electron microscopy (SEM) image of the device and Raman characterizations of BP is shown in Figure S1. Both excitatory and inhibitory responses can be conducted from presynapse to postsynapse, corresponding to electron and hole trapping or releasing in the floating gate due to the unique ambipolar property of BP. The ambipolar BP channel enables carrier transport and tunneling with both electrons and holes in the charge trapping and detrapping process, resulting in bidirectional threshold voltages shift to realize the memory function. Moreover, the channel layer and floating gate layer of BP films with similar thickness have the same energy band diagram, which does not bring additional barriers for either electron or hole during the carrier injection from channel to floating gate. These factors are helpful to realize large memory windows with fast speed. Besides, the same material used for the channel and floating gate layer may reduce the complexity of integrating different materials in the fabrication process. Floating-gate synaptic devices based on BP can operate in two modes: (I) the gate voltage as presynaptic input and the source/drain as postsynaptic output, and (II) the drain voltage as presynaptic input and the source as postsynaptic output with gate terminal floating, and simplified illustration is shown in Figure 1A. The corresponding current-voltage curves of the device are characterized as shown in Figure 1C. The significant current hysteresis is essential for synaptic devices operation. Obvious hysteresis of drain current could be observed while double sweeping the gate voltage from −10 V to 10 V then back to −10 V at $V_d$ = −0.05 V as shown in the left panel of Figure 1C, configuring in mode I (three-terminal mode). The floating gate BP transistor shows a high on/off ratio of $\sim 10^6$ with a large threshold voltage shift of about 7 V. When a negative gate voltage is applied, the accumulated holes of channel layer BP are trapped and stored in the floating gate via Fowler–Nordheim tunneling through the $Al_2O_3$ layer (Lee et al., 2016). On the other hand, under a large positive gate voltage, the electrons are trapped and stored even after removing the positive gate voltage. The trapped holes or electrons will result in an effective local gate effect and generate a negative or positive shift of the threshold voltage of the devices. Distinguished from being controlled by $V_g$, the charge trapping process in floating gate BP can also be conducted by a large drain voltage. When the device works in mode II (two-terminal mode) with gate terminal floating, the current-voltage curve in the right panel exhibits a memristive-like behavior with hysteresis when applying double swept drain voltage (Vu et al., 2016). The charge can tunnel through the thin $Al_2O_3$ layer into the floating gate by the large potential difference between the drain and the floating gate when a large drain voltage is applied, then the injected charge will spread out through the entire floating gate layer. However, the stored charge cannot tunnel back to the channel by the source terminal because of little potential difference between the source and the floating gate (Figure S2). With the voltage sweeping from −5 to 5 V, the device exhibits a low resistance state (LRS). Then it changes to the high resistance state (HRS) with drain voltage sweeping from five to −5 V. This is because the injected holes in floating gate BP via a large positive $V_d$ can deplete holes in channel BP, resulting in a high resistance state. Similarly, it can turn to the LRS when applying a large negative $V_d$. To verify the explanation, further experiments were performed as presented in Figures S10 and S11.

Excitatory and inhibitory behavior in biological synapses can be realized in this floating gate device. Figure 2A shows the excitatory synaptic responses to positive gate voltage as the presynaptic input of 10 V amplitude with a different pulse width (1 μs, 100 μs, and 10 ms) when the devices work on mode I. The $V_g$ pulse voltage starts at the time of 1 s and otherwise, It is always kept to zero with $V_d$ fixed at −50 mV. Electrons are injected into the floating gate and stored by presynaptic input pulse voltage, causing a higher

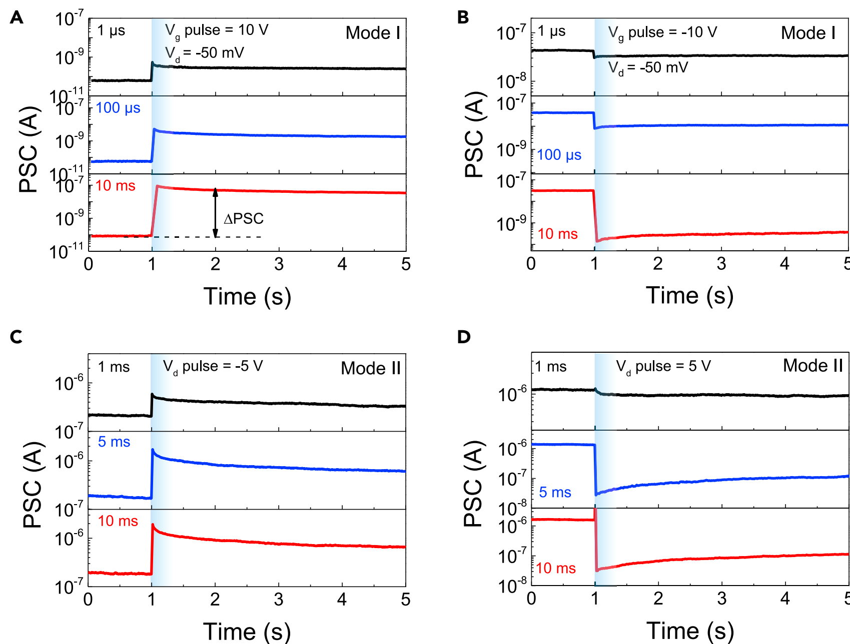


**Figure 2. Excitatory and inhibitory behavior of BP synaptic devices**

(A and B) The excitatory response (A) and inhibitory response (B) at mode I with three different $V_g$ pulse widths (1 μs, 100 μs, and 10 ms). The amplitude of $V_g$ pulse is ±10 V (10 V for the excitatory and −10 V for the inhibitory response) and it happens at 1 s otherwise it stays at 0 V. $V_d$ is always fixed at −50 mV.

(C and D) The excitatory (C) and inhibitory (D) behavior of the device on mode II with three different $V_d$ pulses (1 ms, 5 ms, and 10 ms), respectively. The gate terminal is floating and the read voltage of the drain terminal is 1 V. The $V_d$ pulse happens at 1 s with an amplitude of ±5 V (−5 V for the excitatory and 5 V for the inhibitory response).

postsynaptic current in the BP channel after the gate voltage returns to zero. When the pulse width from 1 μs extends to 10 ms, the device shows a stronger response and a remarkable response that the postsynaptic current from below $10^{-10}$ A switching to over $10^{-8}$ A can be observed. The inhibitory behavior of this device at mode I is demonstrated in Figure 2B after the synaptic device was set at a high current level. A negative gate pulse voltage with −10 V amplitude and different pulse width (1 μs, 100 μs, and 10 ms) is applied as presynaptic input, the holes are injected into the floating gate BP, resulting in a lower PSC with $V_g$ bias return to zero. It can be seen that the current level can be abruptly changed about $10^3$ times by one single pulse with increasing pulse width no matter in excitatory or inhibitory behavior (Figure S9), corresponding to a high dynamic range of synaptic weight change which will be discuss later. Figures 2C and 2D show the excitatory and inhibitory synaptic in Mode II, using the drain pulse voltage as the presynaptic input of ±5 V amplitude with different pulse widths (1 ms, 5 ms, 10 ms) . Excitatory and inhibitory behavior can be successfully emulated in either mode for this floating gate synaptic device.

We further investigate the pulse width dependence on mode I. The excitatory synaptic weight change ($\triangle$W = $\triangle$PSC/initial PSC) under different $V_g$ pulse widths are plotted in Figure 3A. Synaptic weight change exhibits an increasing trend with the longer pulse width because more electrons are injected into the floating gate, enhancing the local gating effect. As far as the weight change in inhibitory behavior, it is a negative number. So $\triangle$W+1 of BP-based synaptic transistors is implemented to show the trend of weight change and the gate pulses width in Figure 3B. On one hand, it can be seen that PSC change of both excitatory and inhibitory behaviors can be achieved about 1,000 times, indicating a wide dynamic range for the neuromorphic application. It is worth emphasizing that the high synaptic weight change is beneficial for neural network applications. On the other hand, an obvious excitatory synaptic response can be still observed even when the pulse width is as short as 10 ns as shown in Figures S3 and S7. It should be noted that the real signal of the pulse amplitude is ~7.36 V with a half peak width of ~13 ns verified by a digital oscilloscope. Fast inhibitory response down to ~20 ns can also be observed. The verified input voltage signal by a digital oscilloscope shows the real signal of the pulse amplitude is −11.2 V with a half peak width of ~19 ns. The distortion of the pulses can be attributed to the inevitable parasitics in

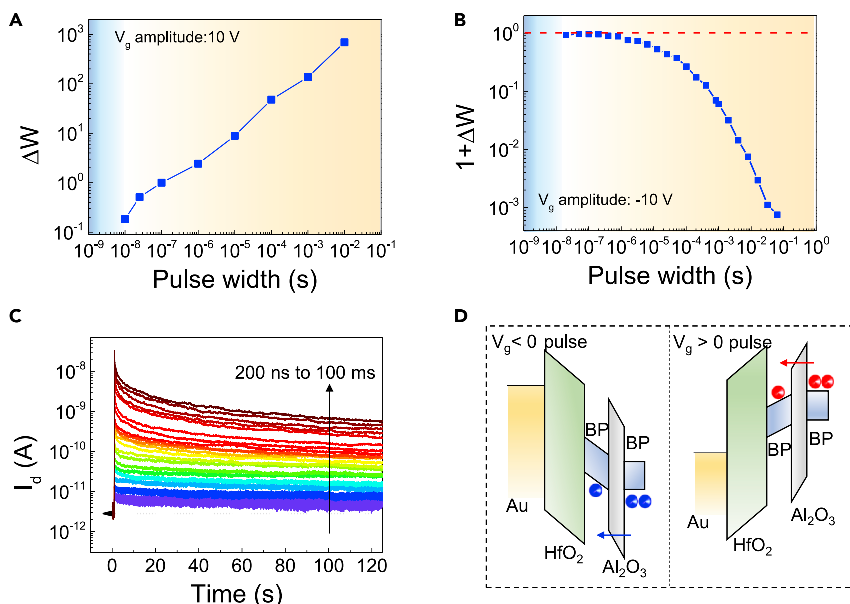


**Figure 3. The pulse width dependence at mode I**

(A and B) The weight change (△W = △PSC/PSC) of excitatory (A) and inhibitory (B) behavior as the function of the operating pulse width. The 1+△W is used in (B) to hold up the changing trend better.

(C) The pulse width dependent (from 200 ns to 100 ms) for the PSC decay to 120 s after applying a positive $V_g$ pulse (10 V).

(D) Schematic band diagrams on this mode under negative $V_g$ bias and positive $V_g$ bias conditions.

the testing setup and the effects on the resulting synaptic measurement are minimal. The ultrahigh-speed operation down to $10^{-8}$ s level of the flash memory-based synaptic device was attributed to the embedded 20 nm $HfO_2$ with a superior gate control capability. The fast response can also break through the bottleneck of reducing energy consumption for flash-based devices (Merrikh-Bayat et al., 2018), which is regarded as one of the most important merits in synaptic devices. A rough estimate of energy consumption can be as low as sub-fJ/spiking when operating with a $V_g$ pulse width of ~10 ns (Figure S4).

Furthermore, pulse width dependence measurements from 200 ns to 100 ms for the PSC decay to 120 s after applying a positive $V_g$ pulse (10 V) are carried out as shown in Figure 3C. The device resets to the same current level to fairly compare the effect of the pulse width. The series of continuous negative $V_g$ pulse train with amplitude of −5 V and pulse width of 500 μs is used to return the PSC to initial level as the reset process (Figure S8). The excitatory postsynaptic current (EPSC) can be enhanced by increasing pulse width and shows the decay trend over time because of some electrons de-trapping from the floating gate layer. However, the EPSC does not decay back to the initial current state after 120 s, suggesting a long-term memory effect of the channel conductance change as well as the ability of multiple state storage. Figure 3D shows the schematic energy band diagrams under excitatory and inhibitory operating to further discuss the mechanism. Applying a negative gate voltage, a strong electric field will be established because of the high-κ dielectric oxide of $HfO_2$. The carriers at channel BP trapping into floating gate BP under the strong static electric field with the same direction make the trapping process more efficient and sensitive, resulting in a fast response.

Because carriers are injected into the floating gate through a different terminal, the synaptic properties of mode II show significant differences compared with mode I. The artificial synapses of mode II can be operated with a single $V_d$ pulse of several millisecond-level pulse widths, which is longer than 10 ns at $V_g$ pulse control mode. This is because the carriers are injected into the floating gate more efficiently by a vertical electric field from the gate. Figures 4A and 4B illustrate the operating schematic diagrams for the $V_g$ pulse and the $V_d$ pulse mode. When a positive gate voltage is applied as the presynaptic input stimulation, the carriers are injected into the floating gate by field-effect coupling with a global back gate capacitor, as shown in Figure 4A. Hence, the entire device channel is under the gate control and the channel conductance could efficiently shift even with short pulse width. On the contrary, as shown in Figure 4B, if the

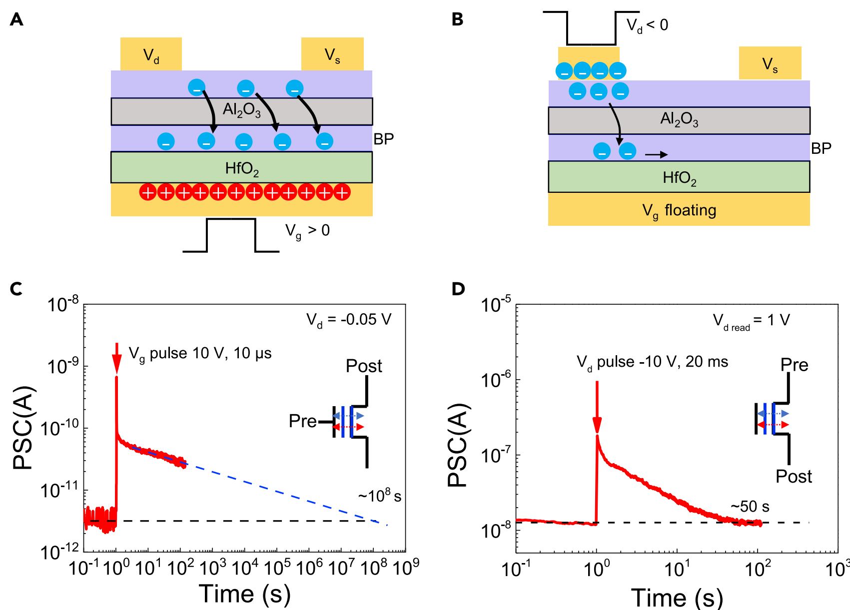


**Figure 4. The synaptic behaviors difference between the two modes**

(A and B) The operating schematic diagrams for the three-terminal synapses (A) and the two-terminal synapses (B).
(C and D) The excitatory postsynaptic current triggered by one presynaptic spike by $V_g$ (C) and $V_d$ (D) versus time shows a long-term and quasi-long-term memory effect.

carriers are injected by a large drain voltage, the trapped carriers are confined to the floating gate area below the drain terminal rather than the entire floating gate area (schematic energy band diagrams in Figure S2). As a result, it needs a much longer pulse width for drain voltage to approach a similar postsynaptic response for gate voltage. Because the large operating current can be effectively restrained with a large amplitude (such as 10 V) and a short pulse width (can be down to 10 ns) for gate voltage but a small conducting source/drain voltage (such as −50 mV), the energy consumption of such a three-terminal design can be extremely low compared with the drain voltage injection mode (often need a large drain voltage to make Fowler–Nordheim tunneling happen with a high operating source-drain current). Meanwhile, it should be noted that a positive gate voltage traps the electrons into the floating gate but a negative drain voltage injects the electrons. Furthermore, typical temporal excitatory responses of the BP floating gate synapses up to 100 s are shown and compared in Figures 4C and 4D. A positive $V_g$ pulse (10 V, 10 μs) and a negative $V_d$ pulse (−10 V, 20 ms) are applied to make sure that the conductance would change the same dozens of times. It can be seen that the PSC of synapses in mode II decays back to the initial current state after 50 s but the time of mode I can be extrapolated to $10^8$ s, suggesting quasi-long-term plasticity (QLTP) for mode II operating by $V_d$ pulse and long-term plasticity (LTP) for mode I operating by $V_g$ pulse. For mode II, the charge can tunnel through the thin $Al_2O_3$ layer into the floating gate by the large potential difference between the drain and floating gate, then the injected charge will be spread out through the entire floating gate layer, which has been reported and proved by previous work with experimental and simulation results (Vu et al., 2016). As a result, compared with the injected charge density of the floating gate layer in mode I, the charge injection efficiency of mode II is much lower than mode I because of the different size of injection area (drain electrode region for mode II and gate electrode region for mode I). The postsynaptic current dynamic behavior originates from the potential modulation of floating gate and bias stress effect because of interface traps. The mode II shows quasi-long-term plasticity with 50 s decay back to the initial current state on account of the lower charge injection efficiency. It is worth noting that the PSC retention time at mode II can be improved by repeated stimulations, mimicking the essential functions of biological synapses for learning and memory, as shown in Figure S5. In addition, the synaptic potentiation and depression can be mimicked by the two modes as shown in Figure S6. The sum of these findings demonstrates that the 2D-synaptic devices based on the floating gate structure modulated by different electric field modes may correspond to different biological synaptic behaviors, which paves the way for achieving complex plasticity in future neuromorphic applications.

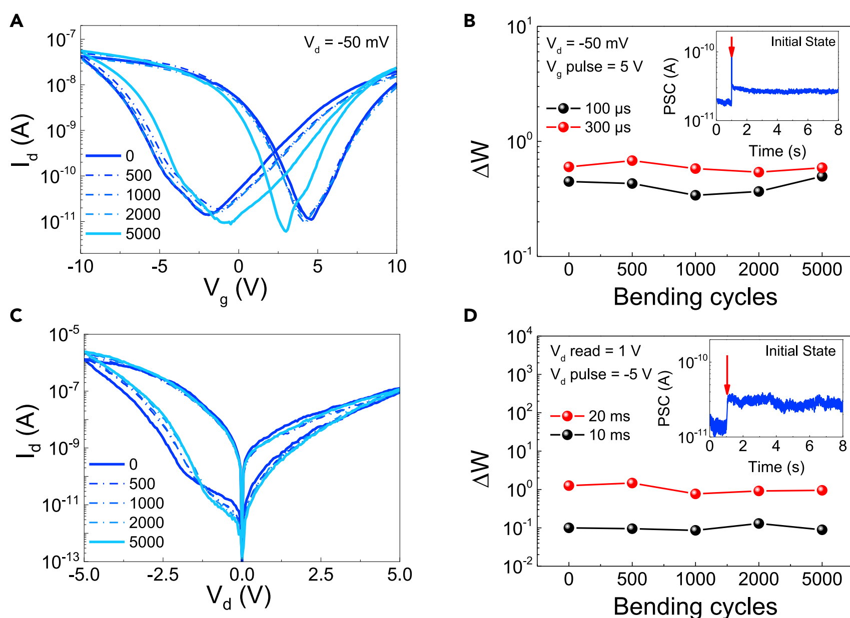


**Figure 5. Synaptic devices with mechanically bending**

(A) I-V curves of the synaptic device at mode I against repeated mechanical bending with a 10 mm radius curvature.

(B) The excitatory weight change by a single $V_g$ pulse in mode I versus mechanical bending times. The inset figure shows the response at the initial state of the device by applying a positive $V_g$ pulse (5 V, 100 µs).

(C) I-V curves of the devices driven by $V_d$ (Mode II) against repeated mechanical bending.

(D) The excitatory weight change by a single $V_d$ pulse in Mode II versus mechanical bending times. The inset figure shows the response at the initial state of the device by applying a negative $V_d$ pulse (−5 V, 20 ms).

The mechanically bending robustness of another typical flexible BP synaptic device is investigated. Layered crystal structure and small thickness of 2D materials on PI substrate make it possible for excellent mechanical flexibility devices. In order to obtain fresh results for the bending test, a new batch of the device is fabricated and measured. The mechanically exfoliated flakes and nonstandard device fabrication techniques lead to device-to-device variability, and more details are presented in Figure S13. Figure 5A shows the $I_d$-$V_g$ curves after different mechanical bending cycles from 0 to 5,000 times with a 10 mm radius curvature, corresponding to a uniaxial strain of ~0.63%. The transfer characteristic curves of the floating gate transistor exhibit good mechanical durability up to 5,000 bending cycles with a slight minimum conduct point shift. The leakage current of the device is also compared and shows little degradation after even bending 5,000 times as shown in Figure S12. Furthermore, the long-term weight change by an excitatory $V_g$ pulse of 5 V amplitude after mechanical bending is investigated as shown in Figure 5B. As shown in the inset figure of Figure 5B, the response at the initial state of the device is excitatory with a positive $V_g$ pulse (5 V, 100 µs). The bending test of mode II operating is demonstrated, as the I-V curves and excitatory weight change under a negative $V_d$ pulse after different bending times are shown in Figures 5C and 5D. The IV curves show little change, resulting in a tiny excitatory weight change. Both mode I and mode II show excellent mechanical durability up to 5,000 bending cycles.

## DISCUSSION

In summary, we have realized the BP-based floating gate synaptic devices with two operating modes in one structure. By using the ambipolar materials BP as the channel layer, both electrons and holes can be injected into the floating gate layer and imitate biological synapses excitatory and inhibitory behaviors. Ultrafast pulse operation of of ~10 ns and ultralow power consumption are demonstrated by $V_g$ driven mode. In addition, the quasi-long-term memory effect for mode II realized by $V_d$ pulses and the long-term memory effect for mode I realized by $V_g$ pulse indicate potential for versatile applications. Finally, the synaptic devices show a good endurance against mechanical bending of over 5,000 times, suggesting possible flexible and ultralow power consumption electronic applications.

### Limitations of the study

The excitatory synaptic response by the gate voltage of the device is at 10-ns level, which is limited by the measurement equipment. Although the flexible synaptic devices based on BP show remarkable performance and diverse operational functions, array demonstration for artificial neural networks based on the BP devices is always a challenge. This is because of the high-quality synthesis of BP materials and nondestructive device fabrication methods have not been solved.

## STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

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- RESOURCE AVAILABILITY
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  - Material availability
  - Data and code availability
- EXPERIMENTAL MODEL AND SUBJECT DETAILS
- METHOD DETAILS
  - Device fabrication
  - TEM images
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- QUANTIFICATION AND STATISTICAL ANALYSIS

## SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.isci.2022.103947.

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## AUTHOR CONTRIBUTIONS

Y.W. conceived the project. X.X. fabricated the devices and performed the electrical measurements. X. W., Q. H., and X. L. assisted with device fabrication and measurements. X.X. and Y.W. analyzed the data and wrote the manuscript. All authors contributed to discussions and commented on the manuscript.

## DECLARATION OF INTERESTS

The authors declare no competing interests.

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# STAR★METHODS

## KEY RESOURCES TABLE

| REAGENT or RESOURCE | SOURCE | IDENTIFIER |
|---|---|---|
| Software and algorithms | | |
| OriginPro 2021b | OriginlLab Corporation | https://www.originlab.com/ |
| Other | | |
| Black phosphorus | HQ graphene | https://www.graphene-info.com/hq-graphene |
| Polyimide substrate | DuPont | https://www.dupont.com/ |
| Polydimethylsiloxane | Metatest Corporation | https://www.metatest.cn/ |
| Atomic layer deposition | Beneq | https://beneq.com/zh/ |
| Electron beam lithography | Raith | http://www.raithchina.com/ |
| Electron beam evaporation | Kurt J. Lesker | https://www.lesker.com/ |
| Scanning electron microscope | Raith | http://www.raithchina.com/ |
| Probe station | Lakeshore | https://www.lakeshore.com/ |
| Semiconductor parameter analyzer | Keysight | https://www.keysight.com/cn/zh/home.html |
| Automatic flexible bending test machine | KangLaiTuo Industrial Equipment Co. LTD | http://www.kanglaituo.com/ |
| Focus ion beam (FIB) system | FEI | https://www.fei.com/ |
| Transmission electron microscopy | Thermofisher | https://www.thermofisher.cn/cn/zh/home.html |

## RESOURCE AVAILABILITY

### Lead contact

Further information and requests for resources should be directed to the lead contact, Yanqing Wu (yqwu@pku.edu.cn).

### Material availability

This study did not generate any new unique reagents.

### Data and code availability

The data and code are available upon reasonable request by contacting the lead contact.

No new code was generated during the course of this study.

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

## EXPERIMENTAL MODEL AND SUBJECT DETAILS

This study does not use experimental models typical in the life sciences.

## METHOD DETAILS

### Device fabrication

Flexible synaptic devices are demonstrated on a polyimide substrate with a thickness of 125 μm. 200 nm $Si_3N_4$ was deposited on PI to smooth the substrate surface using plasma-enhanced chemical vapor deposition (PECVD) at 300°C before patterning 20/50 nm Ni/Au as the local gate by standard electron beam lithography (EBL) process. Few-layer BP flake was firstly mechanically exfoliated from the commercially available bulk BP crystals (Smart elements) and then transferred onto a 20 nm $HfO_2$ by atomic layer deposition. Next, the charge tunneling layer of 7 nm $Al_2O_3$ was deposited on it by atomic layer deposition (ALD).

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The deposition temperature of the ALD chamber is set at 120°C for $HfO_2$ and $Al_2O_3$. Then, another BP flake is deterministically transferred on top of the existing structure with careful alignment on top of the insulating layer. Finally, 20/60 nm Ni/Au metal electrodes are deposited as the ohmic contacts on the top channel. The samples were always kept in the glove box between process steps to minimize the exposure to air, where the oxygen and water contents are always kept below 0.1 ppm.

### TEM images

A cross-sectional specimen of the device was prepared by using a lift-out process in a dual-beam FEI Helios NanoLab G3 focus ion beam (FIB) system. A carbon layer of about 30 nm was first coated onto the samples' surface to increase the electrical conductivity using a Cressington 208carbon coating system. The TEM images of the sample were then obtained using Talos F200S high-resolution transmission electron microscopy.

### Electrical characterizations

During all of the characterization, the device was placed inside a Lakeshore cryogenic probe station in the vacuum. Electrical measurements were carried out using the Keysight B1500A semiconductor parameter analyzer. The pulse voltage is generated by the SPGU module with the 10 ns shortest pulse width. For the waveform verification, the SPGU module was directly connected with a digital oscilloscope with an SPGU cable (SMA to Coaxial), and the target pulse width (minimum value of ~10 ns which is limit by the equipment) is set from the software interface with 8-ns leading and 8-ns trailing time. The devices are bending by an automatic flexible bending test machine (KangLaiTuo Industrial Equipment Co. LTD) with a 10 mm bending radius curvature.

## QUANTIFICATION AND STATISTICAL ANALYSIS

This study does not include statistical analysis or quantification.