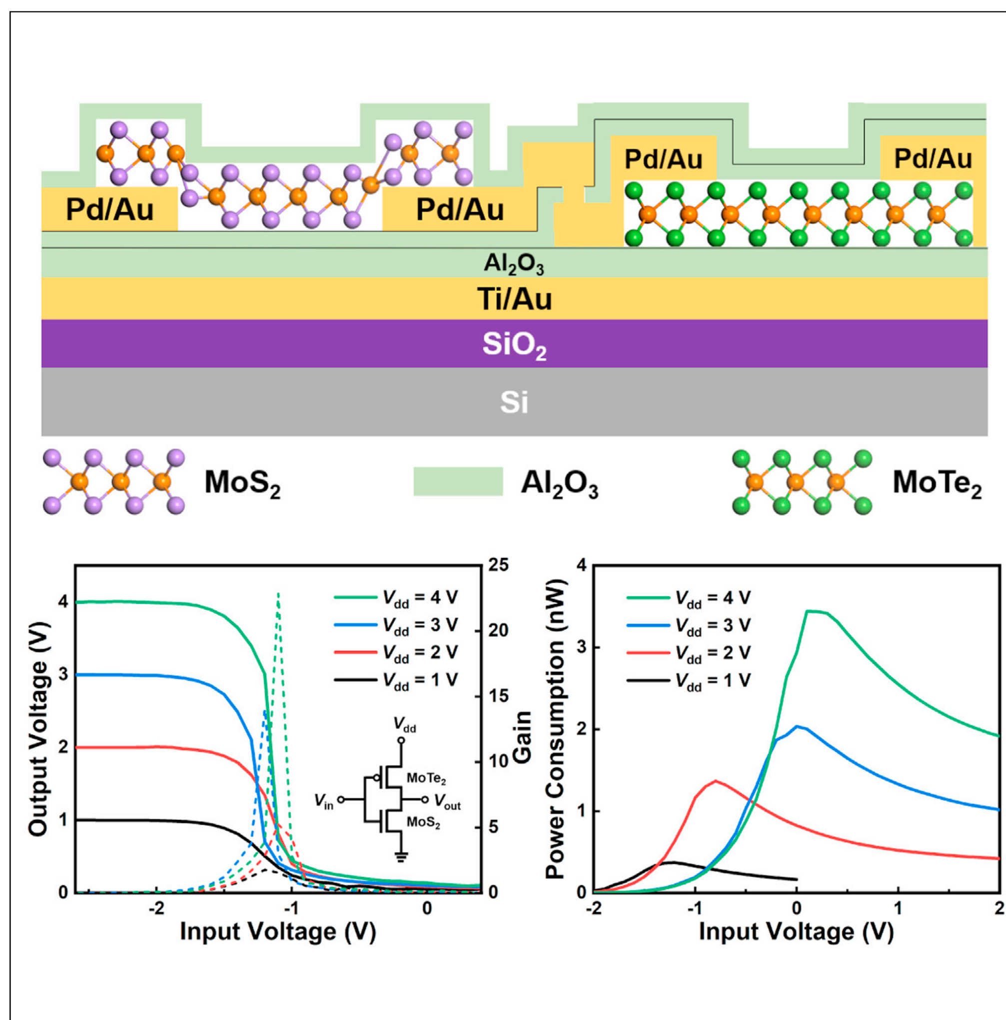
iScience

CellPress
OPEN ACCESS

Article

Low-power-consumption CMOS inverter array based on CVD-grown p-$MoTe_2$ and n-MoS_2



Wanying Du, Xionghui Jia, Zhixuan Cheng, Wanjing Xu, Yanping Li, Lun Dai

lundai@pku.edu.cn

Highlights

A practical approach to fabricate large-scale CMOS inverter arrays is demonstrated

A method to balance the current characteristics of the channel materials is developed

Complete logic swing and clear dynamic switching behavior are observed

Ultra-low power consumption of ~0.37 nW is achieved

Du et al., iScience 24, 103491
December 17, 2021 © 2021
The Author(s).
https://doi.org/10.1016/j.isci.2021.103491

iScience

CellPress
OPEN ACCESS

Article

Low-power-consumption CMOS inverter array based on CVD-grown *p*-$MoTe_2$ and *n*-MoS_2

Wanying Du,[1,2] Xionghui Jia,[1,2] Zhixuan Cheng,[1,2] Wanjing Xu,[1] Yanping Li,[1] and Lun Dai[1,2,3,4,*]

SUMMARY

Two-dimensional (2D) semi-conductive transition metal dichalcogenides (TMDCs) have shown advantages for logic application. Complementary metal-oxide-semiconductor (CMOS) inverter is an important component in integrated circuits in view of low power consumption. So far, the performance of the reported TMDCs-based CMOS inverters is not satisfactory. Besides, most of the inverters were made of mechanically exfoliated materials, which hinders their reproducible production and large-scale integration in practical application. In this study, we demonstrate a practical approach to fabricate CMOS inverter arrays using large-area *p*-$MoTe_2$ and *n*-MoS_2, which are grown via chemical vapor deposition method. The current characteristics of the channel materials are balanced by atomic layer depositing Al_2O_3. Complete logic swing and clear dynamic switching behavior are observed in the inverters. Especially, ultra-low power consumption of ~0.37 nW is achieved. Our work paves the way for the application of 2D TMDCs materials in large-scale low-power-consumption logic circuits.

INTRODUCTION

Over the years, two-dimensional (2D) materials such as graphene and transition metal dichalcogenides (TMDCs) have stimulated great research enthusiasm, owing to their unique electronic and optoelectronic properties and ultrathin geometry (Akinwande et al., 2019; Fiori et al., 2014; Liu et al., 2021). Graphene, with high conductivity and high carrier mobility, has been extensively studied (Castro Neto et al., 2009; Flory et al., 2020; Novoselov et al., 2005; Yu et al., 2013). However, because of its gapless nature, graphene is not a good channel material for field-effect transistor (FET), which requires efficient electrostatic control. Semi-conductive TMDCs, with larger bandgaps, surpass graphene in this aspect. Recently, *n*-channel metal-oxide-semiconductor inverters (Wang et al., 2019) and *p*-channel metal-oxide-semiconductor inverters (Zhang et al., 2019) based on TMDCs have been reported. Complementary metal-oxide-semiconductor (CMOS) inverter, composed of an *n*-channel and a *p*-channel FET, has advantage in reducing power consumption and therefore is an important component in integrated circuits. However, so far, the performance of the reported TMDCs-based CMOS inverters is not satisfactory. They suffered from high power consumption (Liu et al., 2019; Pu et al., 2016) or large leakage current (Lin et al., 2014). Besides, most of the CMOS inverters were made of mechanically exfoliated TMDCs (Cho et al., 2019; Jeon et al., 2015; Pezeshki et al., 2016), which hinders their reproducible production and large-scale integration in practical application. Recently, large-area growth in a cost-effective way has been realized for several TMDCs via chemical vapor deposition (CVD) method (Pu et al., 2016; Wang et al., 2019; Xu et al., 2019a). The as-grown $MoTe_2$ (Xu et al., 2019b) and MoS_2 (Wang et al., 2019) are *p*- and *n*-type, respectively. Moreover, it is demonstrated that atomic layer deposition (ALD) of Al_2O_3 under certain conditions can cause *n*-type doping to 2D materials, including graphene (Zheng et al., 2015), MoS_2 (Li et al., 2017), and $MoTe_2$ (Lim et al., 2017; Park et al., 2019).

In this study, we fabricate CMOS inverter arrays using large-area CVD-grown *p*-$MoTe_2$ and *n*-MoS_2. We have developed a method to balance the current characteristics of the channel materials. Complete logic swing is obtained in our inverters. High voltage gain (~23, much larger than 1) and noise margins close to ideal values are obtained. Especially, ultra-low peak power consumption of ~0.37 nW is achieved, which is among the lowest power consumption values reported so far for TMDCs-based CMOS inverters under similar measurement conditions (Cho et al., 2019; Jeon et al., 2015; Pezeshki et al., 2016). We also investigate the dynamic switching behavior of the CMOS inverters and observe satisfying rising time t_r (several

[1]State Key Lab for Artificial Microstructure & Mesoscopic Physics and Frontiers Science Center for Nano-optoelectronics, School of Physics, Peking University, Beijing 100871, China

[2]Collaborative Innovation Center of Quantum Matter, Beijing 100871, China

[3]Peking University Yangtze Delta Institute of Optoelectronics, Beijing 100871, China

[4]Lead contact

*Correspondence: lundai@pku.edu.cn

https://doi.org/10.1016/j.isci.2021.103491

This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

Figure 1. Optical images that illustrate the fabrication steps of the CMOS inverter array

(A) Arrayed Ti/Au (10/50 nm) electrodes were fabricated on a SiO_2/Si substrate as buried gates for both of $MoTe_2$ and MoS_2 FETs. Then a 20-nm-thick Al_2O_3 dielectric layer was deposited on the substrate via ALD.

(B) A CVD-grown $MoTe_2$ film was transferred onto the Al_2O_3 layer and patterned into rectangular sheets (outlined by the red dashed lines) over the buried gates.

(C) Pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 1 and 2 in (F)) were fabricated on the ends of each $MoTe_2$ sheet. After that, a 3-nm-thick Al_2O_3 layer was deposited on the whole substrate to protect $MoTe_2$ from subsequent steps.

(D) Pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 3 and 4 in (F)) were fabricated on the Al_2O_3 layer. Herein, Electrode 3 and Electrode 2 have an overlapping area in the vertical direction (outlined by the black dashed lines) for measurement purpose.

(E) The MoS_2 channels (outlined by the blue dashed lines) were fabricated by transferring and patterning a CVD-grown MoS_2 film. Finally, a 5-nm-thick Al_2O_3 layer was deposited on the whole substrate, which caused an *n*-type doping effect on MoS_2.

(F) The optical image of a single inverter in the CMOS inverter array. The red, blue, and black dashed lines outline the $MoTe_2$ sheet, the MoS_2 sheet, and the overlapping area of Electrodes 2 and 3, respectively. To construct a complete CMOS circuit, the buried Gate Electrode and Electrode 1 were connected to V_{in} and V_{dd}, respectively. Electrodes 2 and 3 were connected to a digital oscilloscope by a tungsten needle for V_{out} extraction. Electrode 4 was grounded.

(G) The cross-sectional schematic of the device structure depicted in (F).

hundred microseconds) and falling time t_f (several hundred microseconds). Our work paves the way for the application of 2D TMDCs materials in large-scale low-power-consumption logic circuits.

RESULTS AND DISCUSSIONS

Figures 1A–1E are the corresponding optical images after each fabrication step, illustrating the fabrication process of our CMOS inverter array and demonstrating the feasibility of the large-scale fabrication method. First, arrayed Ti/Au (10/50 nm) electrodes were fabricated on a SiO_2 (285 nm)/p^+-Si substrate as buried gates for both of $MoTe_2$ and MoS_2 FETs. Then a 20-nm-thick Al_2O_3 dielectric layer was deposited on the

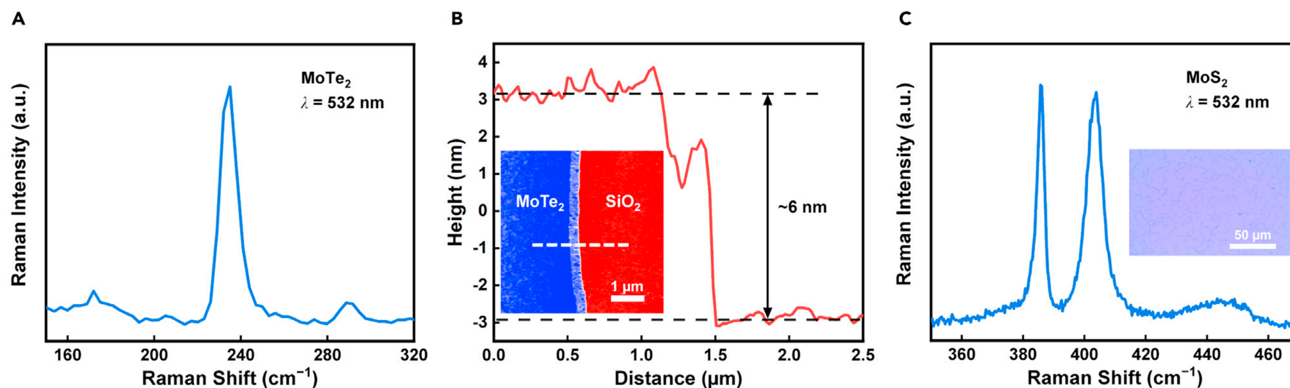


Figure 2. Optical, Raman, and AFM characterizations of the as-grown $MoTe_2$ and MoS_2

(A) The Raman spectrum of the as-grown $MoTe_2$ under 532 nm laser illumination, which is dominated by the Raman characteristic peak of 2H-$MoTe_2$ at $\sim$235 cm^{-1}.

(B) The AFM image of the $MoTe_2$ film and the surface height profile along the white dashed line. The $MoTe_2$ is about 6 nm thick, corresponding to 9-layer $MoTe_2$.

(C) The Raman spectrum of the as-grown MoS_2 under 532 nm laser illumination, which includes the Raman characteristic peaks of MoS_2 at $\sim$386 and $\sim$404 cm^{-1}, with peak distance of $\sim$18 cm^{-1}, indicating the monolayer nature of the MoS_2. Inset: the optical image of the MoS_2 film. The MoS_2 film is formed by single crystal MoS_2 domains.

substrate via ALD method (Figure 1A). Second, a CVD-grown $MoTe_2$ film (see Method details) was transferred onto the Al_2O_3 layer from the growth substrate with the help of polymethyl methacrylate (PMMA) and deionized water, which avoids the common use of hydrofluoric acid (Pu et al., 2016; Xu et al., 2019b). The transferred $MoTe_2$ film was patterned (see Method details) into rectangular sheets (outlined by the red dashed lines) over the buried gates (Figure 1B). Third, pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 1 and 2) were fabricated on the ends of each $MoTe_2$ sheet. After that, a 3-nm-thick Al_2O_3 layer was deposited on the $MoTe_2$ FET array to protect $MoTe_2$ from subsequent steps (Figure 1C). For fabricating the MoS_2 FET array, pairs of Pd/Au (10/50 nm) source and drain electrodes (Electrodes 3 and 4) were fabricated on the Al_2O_3 layer (Figure 1D). Herein, Electrode 3 and Electrode 2 have an overlapping area in the vertical direction (outlined by the black dashed lines) for measurement purpose. Similarly, MoS_2 channels (outlined by the blue dashed lines) were fabricated by transferring and patterning a CVD-grown MoS_2 film (see Method details). Finally, a 5-nm-thick Al_2O_3 layer was deposited on the whole substrate (Figure 1E), which caused an *n*-type doping effect on MoS_2. Figure 1F is the optical image of a single inverter in the CMOS inverter array. To construct a complete CMOS circuit, the buried Gate Electrode and Electrode 1 were connected to the input voltage (V_{in}) and supply voltage (V_{dd}), respectively. Electrodes 2 and 3 were connected to a digital oscilloscope by a tungsten needle for output voltage (V_{out}) extraction. Electrode 4 was grounded. The cross-sectional schematic of the device structure depicted in Figure 1F is shown in Figure 1G. The CMOS circuit diagram is shown in the inset of Figure 3C. Notably, in this work, we fixed the MoS_2 FETs' channel length (15 μm) and changed the $MoTe_2$ FETs' channel lengths to make their current characteristics balanced. The optical image of the CMOS inverter array is presented in Figure S1C.

The $MoTe_2$ films (Figure S1A) used in our devices are formed by seamlessly stitched single crystal $MoTe_2$ domains (Xu et al., 2019a). Figure 2A shows the Raman spectrum of an as-grown $MoTe_2$ film, which presents the Raman characteristic peak of 2H-$MoTe_2$ at $\sim$235 cm^{-1} (Yamamoto et al., 2014). Figure 2B shows the atomic force microscope (AFM) image of the $MoTe_2$ and the surface height profile along the white dashed line. The $MoTe_2$ is about 6 nm thick, corresponding to 9-layer $MoTe_2$ (Lin et al., 2014). The MoS_2 films (Figure S1B) used in our devices are formed by single crystal MoS_2 domains (see the inset of Figure 2C). Figure 2C shows the Raman spectrum of an as-grown MoS_2 film, which presents Raman characteristic peaks of MoS_2 at $\sim$386 and $\sim$404 cm^{-1} (Li et al., 2012). The peak distance is $\sim$18 cm^{-1}, demonstrating the monolayer nature of the MoS_2 (Li et al., 2012).

Figures 3A and 3B show the transfer curves and output curves of the $MoTe_2$ FET (with 15 μm channel length) and MoS_2 FET in an inverter, respectively. The transfer curves are approximately symmetrical about their intersection. Note that the two ALD steps in the device fabrication process balanced the carrier

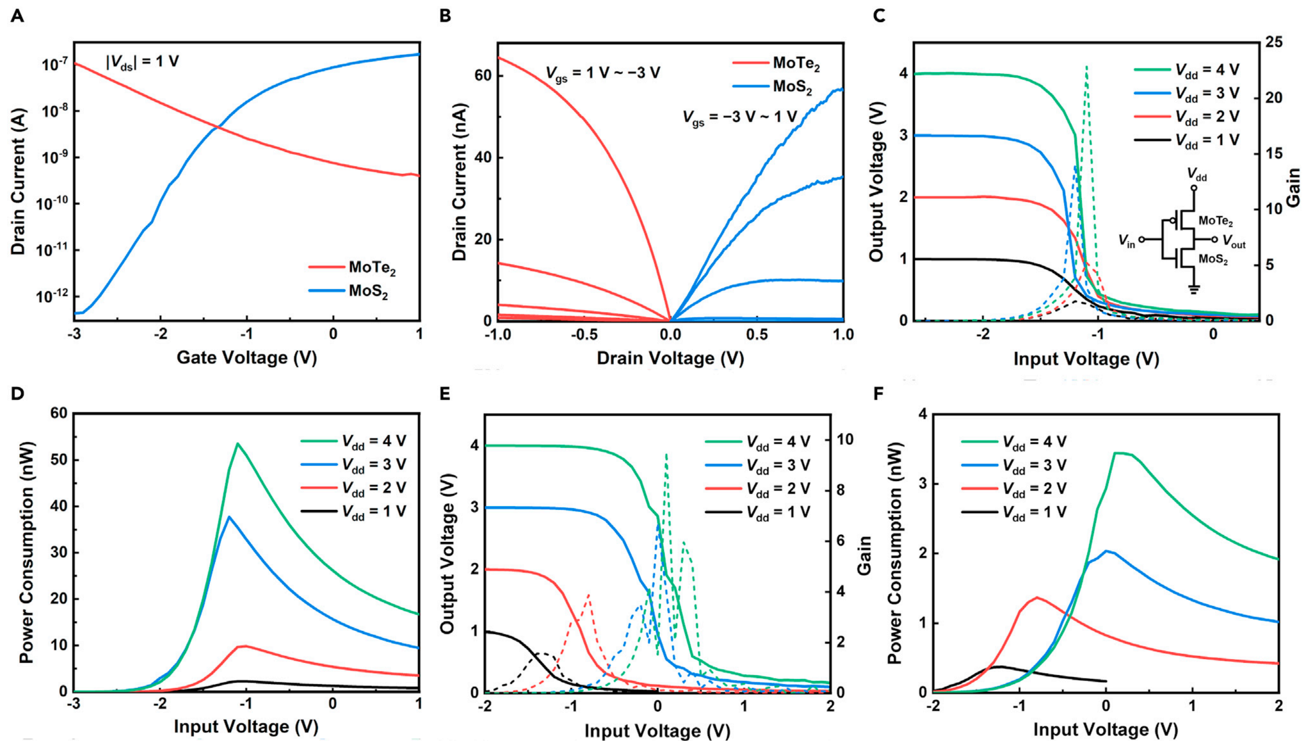


Figure 3. Static operation performance of the inverters (with $MoTe_2$ channel length of 15 μm)

(A) The transfer curves of the $MoTe_2$ and MoS_2 FETs in an inverter at $|V_{ds}|$ = 1 V.

(B) The output curves of the $MoTe_2$ and MoS_2 FETs in the inverter at various V_{gs} with a step of 1 V.

(C) The VTCs and voltage gain ($-dV_{out}/dV_{in}$) plots of the inverter at various V_{dd}. The solid and dashed lines correspond to the output voltage and gain, respectively. Inset: the CMOS circuit diagram. For each V_{dd} applied (from 1 to 4 V), the VTC presents complete logic swing, and the maximum voltage gain is bigger than 1. At V_{dd} of 4 V, a maximum voltage gain of ~23 and good noise margins ($NM_L \approx 0.40\ V_{dd}$, $NM_H \approx 0.44\ V_{dd}$, total noise margin $\approx 0.84\ V_{dd}$) are obtained.

(D) The power consumption ($V_{dd} \times I_{dd}$) characteristics of the inverter at various V_{dd}. At V_{dd} of 1 V, peak power consumption of as low as ~2.3 nW is achieved.

(E) The VTCs and voltage gain plots of another inverter at various V_{dd}. The solid and dashed lines correspond to the output voltage and gain, respectively. For each V_{dd} applied (from 1 to 4 V), the VTC presents complete logic swing. At V_{dd} of 4 V, a maximum voltage gain of ~9.5 and good noise margins ($NM_L \approx 0.36\ V_{dd}$, $NM_H \approx 0.40\ V_{dd}$, total noise margin $\approx 0.76\ V_{dd}$) are obtained.

(F) The power consumption characteristics of the inverter corresponding to (E) at various V_{dd}. At V_{dd} of 1 V, ultra-low peak power consumption of ~0.37 nW is achieved.

concentrations of the $MoTe_2$ and MoS_2, enabling the realization of high-performance CMOS inverters (Figure S2). It is worth noting that, in order to avoid the ALD-caused *n*-type doping effect on the *p*-$MoTe_2$, we also fabricated a CMOS inverter array with another device structure, where the $MoTe_2$ is free from Al_2O_3 coverage (Figure S4). The overall device performance did not improve (Figure S5). Figure 3C shows the voltage transfer characteristics (VTCs) and voltage gain ($-dV_{out}/dV_{in}$) plots of the inverter corresponding to Figures 3A and 3B. The inset is the CMOS circuit diagram. For each V_{dd} applied (from 1 to 4 V), the VTC presents complete logic swing, and the maximum voltage gain is bigger than 1, satisfying the requirement for logic application. At V_{dd} of 4 V, a maximum voltage gain of ~23 and good noise margins ($NM_L \approx 0.40\ V_{dd}$, $NM_H \approx 0.44\ V_{dd}$, total noise margin $\approx 0.84\ V_{dd}$) are obtained, indicating the potential of the CMOS inverter to be integrated into complex circuit systems (Wang et al., 2019). The noise margins for high input voltage (NM_H) and low input voltage (NM_L) are defined as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$. V_{OH} and V_{OL} are the highest and lowest output voltages, respectively. V_{IH} and V_{IL} are, respectively, the higher and lower input voltages, at which the voltage gains of the VTC equal 1. The total noise margin is the sum of NM_H and NM_L. To evaluate the noise margins of our CMOS inverter, the input voltage range of the VTC is shifted to be symmetric with the output voltage range (Das et al., 2014). Figure 3D shows the power consumption ($V_{dd} \times I_{dd}$) characteristics of the inverter. At V_{dd} of 1 V, peak power consumption of as low as ~2.3 nW is achieved. Figures 3E and 3F show the VTCs and power consumption characteristics of another inverter (with $MoTe_2$ channel length of 15 μm). For each V_{dd} applied (from 1 to 4 V), the VTC

Table 1. Power consumption comparison of the CMOS inverters based on TMDCs

Channel materials	V_{dd} (V)	Peak power consumption (nW)	Measurement environment	Reference
CVD p-$MoTe_2$ and n-MoS_2	1	0.37	Dark Ambient	This work
Ex. p-$MoTe_2$ and n-MoS_2	0.25 1	0.4 3–4	Dark Room temperature	Pezeshki et al. (2016)
Ex. p-$MoTe_2$ and n-MoS_2	1	4	Dark Room temperature	Cho et al. (2019)
Ex. p-$MoTe_2$ and n-MoS_2	3	400	Dark Ambient	Seo and Jin (2019)
Ex. p-WSe_2 and n-MoS_2	1 5	0.1–1 1–10	Dark	Jeon et al. (2015)
Ex. p-WSe_2 and n-MoS_2	1	1×10^3	Dark Room temperature	Liu et al. (2019)
CVD p-WSe_2 and n-MoS_2	1	20	N_2 atmosphere Room temperature	Pu et al. (2016)
Ex. p-$MoTe_2$ and n-$MoTe_2$ (n-doped)	1	5	Dark Room temperature	Lim et al. (2017)
Ex. p-WSe_2 and n-MoS_2	1.1	0.2	Under 10^{-5} bar	Wang et al., 2020

Ex., mechanically exfoliated; CVD, CVD-grown.

also presents complete logic swing. At V_{dd} of 4 V, a voltage gain of ~9.5 and good noise margins ($NM_L \approx 0.36\ V_{dd}$, $NM_H \approx 0.40\ V_{dd}$, total noise margin $\approx 0.76\ V_{dd}$) are obtained. Especially, ultra-low peak power consumption of ~0.37 nW is achieved at V_{dd} of 1 V. The statistical gain and power consumption data of the CMOS inverter array are presented in Figures S3A and S3B. It is worth noting that the peak power consumption (0.37–2.3 nW) of our inverters at V_{dd} of 1 V is lower compared with previously reported CMOS inverters based on p-$MoTe_2$ and n-MoS_2 and among the lowest peak power consumption values reported so far for TMDCs-based CMOS inverters (see Table 1). Besides, all the inverters exhibit maximum voltage gains of >1 at each V_{dd} applied.

We also investigated the dynamic switching behavior of the CMOS inverters. Figures 4A–4C show the time-dependent V_{out} of an inverter (with $MoTe_2$ channel length of 10 μm) at V_{dd} of 3 V, driven by square wave V_{in} with various frequencies. The high and low levels of the input square wave were 0 and −6 V, respectively. Logic switching behavior is clear at 100 Hz and remains to be observed at a critical logic switching frequency of 1 kHz. The t_r and t_f are about 340 and 308 μs, respectively, at 1 kHz, calculated at 10% and 90% (marked by the red dashed lines in Figure 4B) of V_{out} amplitude. The RC delays mainly result from the overlap capacitance in the CMOS circuit (Pezeshki et al., 2016; Wang et al., 2019). At 1.4 kHz, the amplitude of V_{out} decreased to half (~1.5 V) of V_{dd}, with t_r (t_f) of about 275 μs (290 μs). The statistical dynamic switching frequency data of the CMOS inverter array are presented in Figure S3C.

Conclusions

We have fabricated CMOS inverter arrays using large-area CVD-grown p-$MoTe_2$ and n-MoS_2. The current characteristics of the channel materials were balanced by atomic layer depositing Al_2O_3 under proper conditions. Complete logic swing and clear dynamic switching behavior are observed in the inverters. The inverters have overall high performance such as maximum voltage gains of >1 at each V_{dd} applied, low and even ultra-low peak power consumption (0.37–2.3 nW), and satisfying t_r (t_f) and working frequencies. Our low-power-consumption CMOS inverters, with the merits of reproducibility and large-scale integration, have promising applications in future 2D microelectronic systems.

Limitation of the study

In order to further improve the device performance, developing new methods to increase the grain size of the monolayer MoS_2 is needed.

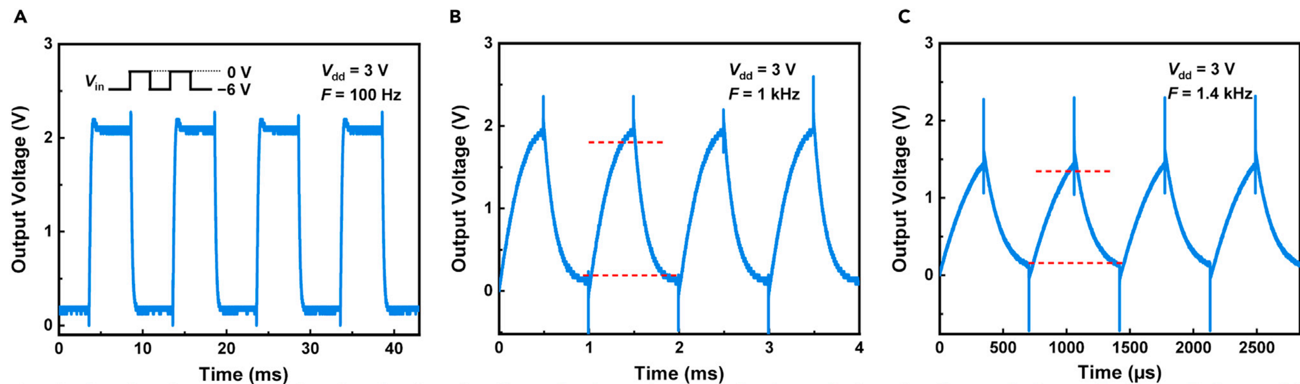


Figure 4. Dynamic switching behavior of an inverter (with $MoTe_2$ channel length of 10 μm)
(A–C) Time-dependent V_{out} at V_{dd} of 3 V driven by square wave V_{in} with various frequencies. The high and low levels of the input square wave were 0 and −6 V, respectively. Logic switching behavior is clear at 100 Hz and remains to be observed at a critical logic switching frequency of 1 kHz. The rising time (t_r) and falling time (t_f) are about 340 and 308 μs, respectively, at 1 kHz, calculated at 10% and 90% (marked by the red dashed lines in (B)) of V_{out} amplitude. At 1.4 kHz, the amplitude of V_{out} decreased to half (~1.5 V) of V_{dd}, with t_r (t_f) of about 275 μs (290 μs).

STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

- KEY RESOURCES TABLE
- RESOURCE AVAILABILITY
  - Lead contact
  - Materials availability
  - Data and code availability
- METHOD DETAILS
  - CVD growth of large-area $MoTe_2$ and MoS_2
  - Fabrication of the CMOS inverter arrays
  - Characterizations

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.isci.2021.103491.

ACKNOWLEDGMENTS

This work was supported by National Natural Science Foundation of China (Nos. 61521004, 61874003, and 62174005).

AUTHOR CONTRIBUTIONS

L.D. and W.Y.D. conceived the project. W.Y.D. grew the MoS_2 and $MoTe_2$ films, fabricated the devices, and conducted the measurement. L.D. and W.Y.D. performed data analysis. X.H.J. helped with the drawing of the cross-sectional schematics of the devices. Z.X.C. and X.H.J. helped with the design of the device structure. W.J.X. prepared the Mo films for $MoTe_2$ growth. Y.P.L. helped with the deposition of the metal electrodes. L.D. supervised this research. W.Y.D. and L.D. wrote the manuscript. All authors contributed to discussions.

DECLARATION OF INTERESTS

The authors declare no competing interests.

Received: August 2, 2021
Revised: October 6, 2021
Accepted: November 19, 2021
Published: December 17, 2021

REFERENCES

Akinwande, D., Huyghebaert, C., Wang, C.H., Serna, M.I., Goossens, S., Li, L.J., Wong, H.S.P., and Koppens, F.H.L. (2019). Graphene and two-dimensional materials for silicon technology. Nature *573*, 507–518. https://doi.org/10.1038/s41586-019-1573-9.

Castro Neto, A.H., Guinea, F., Peres, N.M.R., Novoselov, K.S., and Geim, A.K. (2009). The electronic properties of graphene. Rev. Mod. Phys. *81*, 109–162. https://doi.org/10.1103/RevModPhys.81.109.

Cho, Y., Park, J.H., Kim, M., Jeong, Y., Yu, S., Lim, J.Y., Yi, Y., and Im, S. (2019). Impact of organic molecule-induced charge transfer on operating voltage control of both n-MoS_2 and p-$MoTe_2$ transistors. Nano Lett. *19*, 2456–2463. https://doi.org/10.1021/acs.nanolett.9b00019.

Das, S., Dubey, M., and Roelofs, A. (2014). High gain, low noise, fully complementary logic inverter based on bi-layer WSe_2 field effect transistors. Appl. Phys. Lett. *105*, 083511. https://doi.org/10.1063/1.4894426.

Fiori, G., Bonaccorso, F., Iannaccone, G., Palacios, T., Neumaier, D., Seabaugh, A., Banerjee, S.K., and Colombo, L. (2014). Electronics based on two-dimensional materials. Nat. Nanotechnol. *9*, 768–779. https://doi.org/10.1038/nnano.2014.207.

Flory, N., Ma, P., Salamin, Y., Emboras, A., Taniguchi, T., Watanabe, K., Leuthold, J., and Novotny, L. (2020). Waveguide-integrated van der Waals heterostructure photodetector at telecom wavelengths with high speed and high responsivity. Nat. Nanotechnol. *15*, 118. https://doi.org/10.1038/s41565-019-0602-z.

Jeon, P.J., Kim, J.S., Lim, J.Y., Cho, Y., Pezeshki, A., Lee, H.S., Yu, S., Min, S.-W., and Im, S. (2015). Low power consumption complementary inverters with n-MoS_2 and p-WSe_2 dichalcogenide nanosheets on glass for logic and light-emitting diode circuits. ACS Appl. Mater. Interfaces *7*, 22333–22340. https://doi.org/10.1021/acsami.5b06027.

Kim, J.H., Ko, T.-J., Okogbue, E., Han, S.S., Shawkat, M.S., Kaium, M.G., Oh, K.H., Chung, H.-S., and Jung, Y. (2019). Centimeter-scale green integration of layer-by-layer 2D TMD vdW heterostructures on arbitrary substrates by water-assisted layer transfer. Sci. Rep. *9*, 1641. https://doi.org/10.1038/s41598-018-37219-w.

Li, Y.Z., Li, X.S., Chen, H.Y., Shi, J., Shang, Q.Y., Zhang, S., Qui, X.H., Liu, Z., Zhang, Q., Xu, H.Y., et al. (2017). Controlled gas molecules doping of monolayer MoS_2 via atomic-layer-deposited Al_2O_3 films. ACS Appl. Mater. Interfaces *9*, 27402–27408. https://doi.org/10.1021/acsami.7b08893.

Li, S.L., Miyazaki, H., Song, H., Kuramochi, H., Nakaharai, S., and Tsukagoshi, K. (2012). Quantitative Raman spectrum and reliable thickness identification for atomic layers on insulating substrates. ACS Nano *6*, 7381–7388. https://doi.org/10.1021/nn3025173.

Lim, J.Y., Pezeshki, A., Oh, S., Kim, J.S., Lee, Y.T., Yu, S., Hwang, D.K., Lee, G.-H., Choi, H.J., and Im, S. (2017). Homogeneous 2D $MoTe_2$ p-n junctions and CMOS inverters formed by atomic-layer-deposition-induced doping. Adv. Mater. *29*, 1701798. https://doi.org/10.1002/adma.201701798.

Lin, Y.F., Xu, Y., Wang, S.T., Li, S.L., Yamamoto, M., Aparecido-Ferreira, A., Li, W.W., Sun, H.B., Nakaharai, S., Jian, W.B., et al. (2014). Ambipolar $MoTe_2$ transistors and their applications in logic circuits. Adv. Mater. *26*, 3263. https://doi.org/10.1002/adma.201305845.

Liu, S., Yuan, K., Xu, X.L., Yin, R.Y., Lin, D.Y., Li, Y.P., Watanabe, K., Taniguchi, T., Meng, Y.Q., Dai, L., and Ye, Y. (2019). Hysteresis-free hexagonal boron nitride encapsulated 2D semiconductor transistors, NMOS and CMOS inverters. Adv. Electron. Mater. *5*, 1800419. https://doi.org/10.1002/aelm.201800419.

Liu, Y., Duan, X.D., Shin, H.J., Park, S., Huang, Y., and Duan, X.F. (2021). Promises and prospects of two-dimensional transistors. Nature *591*, 43–53. https://doi.org/10.1038/s41586-021-03339-z.

Novoselov, K.S., Geim, A.K., Morozov, S.V., Jiang, D., Katsnelson, M.I., Grigorieva, I.V., Dubonos, S.V., and Firsov, A.A. (2005). Two-dimensional gas of massless Dirac fermions in graphene. Nature *438*, 197–200. https://doi.org/10.1038/nature04233.

Park, Y.J., Katiyar, A.K., Hoang, A.T., and Ahn, J.H. (2019). Controllable P- and N-type conversion of $MoTe_2$ via oxide interfacial layer for logic circuits. Small *15*, 1901772. https://doi.org/10.1002/smll.201901772.

Pezeshki, A., Shokouh, S.H.H., Jeon, P.J., Shackery, I., Kim, J.S., Oh, I.-K., Jun, S.C., Kim, H., and Im, S. (2016). Static and dynamic performance of complementary inverters based on nanosheet alpha-$MoTe_2$ *p*-channel and MoS_2 *n*-channel transistors. ACS Nano *10*, 1118–1125. https://doi.org/10.1021/acsnano.5b06419.

Pu, J., Funahashi, K., Chen, C.H., Li, M.Y., Li, L.J., and Takenobu, T. (2016). Highly flexible and high-performance complementary inverters of large-area transition metal dichalcogenide monolayers. Adv. Mater. *28*, 4111–4119. https://doi.org/10.1002/adma.201503872.

Seo, S.G., and Jin, S.H. (2019). Photosensitive complementary inverters based on n-channel MoS_2 and p-channel $MoTe_2$ transistors for light-to-frequency conversion circuits. Phys. Status Solidi Rapid Res. Lett. *13*, 1900317. https://doi.org/10.1002/pssr.201900317.

Wang, L., Chen, L., Wong, S.L., Huang, X., Liao, W.G., Zhu, C.X., Lim, Y.F., Li, D.B., Liu, X.K., Chi, D.Z., and Ang, K.W. (2019). Electronic devices and circuits based on wafer-scale polycrystalline monolayer MoS_2 by chemical vapor deposition. Adv. Electron. Mater. *5*, 1900393. https://doi.org/10.1002/aelm.201900393.

Wang, J., Guo, X., Yu, Z., Ma, Z., Liu, Y., Lin, Z., Chan, M., Zhu, Y., Wang, X., and Chai, Y. (2020). Low-power complementary inverter with negative capacitance 2D semiconductor transistors. Adv. Funct. Mater. *30*, 2003859. https://doi.org/10.1002/adfm.202003859.

Xu, X.L., Chen, S.L., Liu, S., Cheng, X., Xu, W.J., Li, P., Wan, Y., Yang, S.G., Gong, W.T., Yuan, K., et al. (2019a). Millimeter-scale single-crystalline semiconducting $MoTe_2$ via solid-to-solid phase transformation. J. Am. Chem. Soc. *141*, 2128–2134. https://doi.org/10.1021/jacs.8b12230.

Xu, X.L., Liu, S., Han, B., Han, Y.M., Yuan, K., Xu, W.J., Yao, X.H., Li, P., Yang, S.Q., Gong, W.T., et al. (2019b). Scaling-up atomically thin coplanar semiconductor-metal circuitry via phase engineered chemical assembly. Nano Lett. *19*, 6845–6852. https://doi.org/10.1021/acs.nanolett.9b02006.

Yamamoto, M., Wang, S.T., Ni, M.Y., Lin, Y.F., Li, S.L., Aikawa, S., Jian, W.B., Ueno, K., Wakabayashi, K., and Tsukagoshi, K. (2014). Strong enhancement of Raman scattering from a bulk-inactive vibrational mode in few-layer $MoTe_2$. ACS Nano *8*, 3895–3903. https://doi.org/10.1021/nn5007607.

Yu, W.J., Liu, Y., Zhou, H.L., Yin, A.X., Li, Z., Huang, Y., and Duan, X.F. (2013). Highly efficient gate-tunable photocurrent generation in vertical heterostructures of layered materials. Nat. Nanotechnol. *8*, 952–958. https://doi.org/10.1038/nnano.2013.219.

Zhang, Q., Wang, X.F., Shen, S.H., Lu, Q., Liu, X.Z., Li, H.Y., Zheng, J.Y., Yu, C.P., Zhong, X.Y., Gu, L., et al. (2019). Simultaneous synthesis and integration of two-dimensional electronic components. Nat. Electron. *2*, 164–170. https://doi.org/10.1038/s41928-019-0233-2.

Zheng, L., Cheng, X.H., Wang, Z.J., Xia, C., Cao, D., Shen, L.Y., Wang, Q., Yu, Y.H., and Shen, D.S. (2015). Reversible n-type doping of graphene by H_2O-based atomic-layer deposition and its doping mechanism. J. Phys. Chem. C *119*, 5995–6000. https://doi.org/10.1021/jp511562t.

STAR★METHODS

KEY RESOURCES TABLE

REAGENT or RESOURCE	SOURCE	IDENTIFIER
Chemicals, peptides, and recombinant proteins		
Tellurium	Zhongnuoxincai	CAS: 13494-80-9
Solid PTAS	2D Semiconductors	N/A
Molybdenum(VI) oxide	Ourchem	CAS: 1313-27-5
Sulfur	Aladdin	CAS: 7704-34-9
PMMA	AllRESIST	CAS: 9011-14-7

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources should be directed to and will be fulfilled by the lead contact, Lun Dai (lundai@pku.edu.cn).

Materials availability

This study did not generate new unique reagents.

Data and code availability

All data reported in this paper will be shared by the lead contact upon request.

This paper does not report original code.

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

METHOD DETAILS

CVD growth of large-area $MoTe_2$ and MoS_2

Large-area $MoTe_2$ and MoS_2 films were grown via CVD method. For $MoTe_2$ growth, Mo films were deposited on SiO_2 (285 nm)/p^+-Si substrates via magnetron sputtering. Then, the substrates were placed in a quartz boat containing Te powder. Molecular sieves were placed in the quartz boat between the substrates and the Te powder. After that, the quartz boat was pushed into the center heating zone of a quartz tube furnace with a tube diameter of 1 inch. After evacuating the quartz tube to an air pressure of less than 1 mTorr, high-purity Ar was let in at the maximum flow rate until the pressure reached atmospheric pressure. Next, the furnace was heated to 650°C in 30 min and kept there for 180 min. High-purity H_2 and Ar were used as carrier gases, whose flow rates were 7 and 5 standard cubic centimeters per minute (sccm), respectively. After the growth, the furnace cooled to room temperature naturally. For MoS_2 growth, SiO_2 (285 nm)/p^+-Si substrates were processed with O_2 plasma. After that, perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) was spin-coated on the substrates as seeding promoter. The substrates were placed in a quartz boat containing MoO_3 powder. Another quartz boat with S power was pushed into the upstream heating zone of a 3-temperature-zone quartz tube furnace with a tube diameter of 2 inch. Then the quartz boat with growth substrates was pushed into the downstream heating zone of the furnace. The growth was performed at atmospheric pressure. High-purity Ar (15 sccm) was used as carrier gas. The upstream and downstream heating zones of the furnace were heated to 200°C and 650°C, respectively, in 40 min, and kept there for 5 min. Finally, the furnace cooled to room temperature naturally.

Fabrication of the CMOS inverter arrays

Both the CVD-grown $MoTe_2$ and MoS_2 films were transferred with the help of PMMA and deionized water (Kim et al., 2019), and patterned into rectangular sheets through ultra-violet (UV) lithography and reactive

ion etching. The Ti/Au and Pd/Au electrodes were fabricated via UV lithography, electron beam evaporation, and lift-off process. The Al_2O_3 layers were deposited using an ALD system (Cambridge NanoTech Inc., Savannah-100). The patterned Al_2O_3 layer (see Figure S4F) was fabricated via UV lithography, ALD, and lift-off process. In the ALD process, trimethylaluminum and deionized water served as precursors and high-purity N_2 served as carrier gas. The reaction temperatures were 200°C for Al_2O_3 films covering the whole substrate and 80°C for the patterned Al_2O_3 layer (because the photoresist could not endure the temperature of 200°C). The Al_2O_3 thickness was controlled by deposition time.

Characterizations

The optical images of the devices were taken by an optical microscope (ZEISS, Axio Imager A2m). The Raman spectra were collected by a micro-zone confocal Raman system (WITec alpha 300R) under 532 nm laser illumination. The thickness of the $MoTe_2$ film was measured by an atomic force microscope (Asylum Research, Cypher S). All the electrical measurement was conducted in the dark with a semiconductor characterization system (Keithley 4200-SCS) that was connected to a probe station. For the dynamic switching performance measurement, a function generator (Tektronix AFG 3102) and a digital oscilloscope (Tektronix DPO 2024) were employed to generate the V_{in} and record the V_{out}, respectively. Both the function generator and the digital oscilloscope had common ground with the semiconductor characterization system, which provided the V_{dd}. All the characterizations were performed in ambient condition.