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A non-volatile cryogenic random-access memory based on the quantum anomalous Hall effect

Shamiul Alam^{1,3}, Md Shafayat Hossain^{2,3} & Ahmedullah Aziz¹✉

The interplay between ferromagnetism and topological properties of electronic band structures leads to a precise quantization of Hall resistance without any external magnetic field. This so-called quantum anomalous Hall effect (QAHE) is born out of topological correlations, and is oblivious of low-sample quality. It was envisioned to lead towards dissipation-less and topologically protected electronics. However, no clear framework of how to design such an electronic device out of it exists. Here we construct an ultra-low power, non-volatile, cryogenic memory architecture leveraging the QAHE phenomenon. Our design promises orders of magnitude lower cell area compared with the state-of-the-art cryogenic memory technologies. We harness the fundamentally quantized Hall resistance levels in moiré graphene heterostructures to store non-volatile binary bits (1, 0). We perform the memory write operation through controlled hysteretic switching between the quantized Hall states, using nano-ampere level currents with opposite polarities. The non-destructive read operation is performed by sensing the polarity of the transverse Hall voltage using a separate pair of terminals. We custom design the memory architecture with a novel sensing mechanism to avoid accidental data corruption, ensure highest memory density and minimize array leakage power. Our design provides a pathway towards realizing topologically protected memory devices.

Electronic bands of non-trivial topology give rise to quantum phenomena at macroscopic scale. Under a strong magnetic field, two-dimensional electron systems exhibit such a quantum state- the quantum Hall effect, i.e. the quantization of Hall resistance¹. Back in 1988, Haldane² predicted that a quantum Hall state can arise even in the absence of an external magnetic field. This new state became known as the quantum anomalous Hall effect (QAHE). However, it took more than two decades for the first experimental realization of QAHE, when it was demonstrated in a magnetic topological insulator [Cr-doped Bi(Sb)₂Te₃]^{3–10}. The experimental fingerprint of QAHE is straightforward: The Hall resistance is quantized to $h/\nu e^2$ (where ν , the so-called Chern number, is an integer that depends on the topological properties of the band structure) at zero magnetic field. Such simple and universal values stem from the current being carried by lossless edge channels which require neither high electron mobility^{11,12} nor external magnetic fields. Moreover, on a given edge, the current flows only in one direction. Thanks to such transport properties which are also immune to sample complexities^{11,12}, QAHE can potentially be useful in spin-filtering¹¹, resistance metrology¹³ and topological quantum computing¹⁴. However, how we can materialize these prospects and come up with a QAHE-based electronic device have remained elusive so far.

Here we bridge the gap between the QAHE physics and device architecture to build the framework of a scalable non-volatile memory. We utilize the quantization of Hall resistance in QAHE to design a memory cell and then construct a 3D cross-point memory array capable of efficient read and write operations.

Design of a QAHE based memory

To design our memory cell, we use the intrinsic QAHE reported in a twisted bilayer graphene (tBLG) on hexagonal boron nitride (hBN) moiré heterostructure, where the quantization of Hall resistance persists at temperatures as high as 6 K¹. This is significantly higher compared to the magnetic topological materials, such as transition metal doped (Bi, Sb)₂Te₃ thin films^{15–18} and MnBi₂Te₄¹⁹. With the ongoing thrust in material discoveries,

¹Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996, USA. ²Department of Electrical Engineering, Princeton University, Princeton, NJ 08544, USA. ³These authors contributed equally: Shamiul Alam and Md Shafayat Hossain. ✉email: aziz@utk.edu

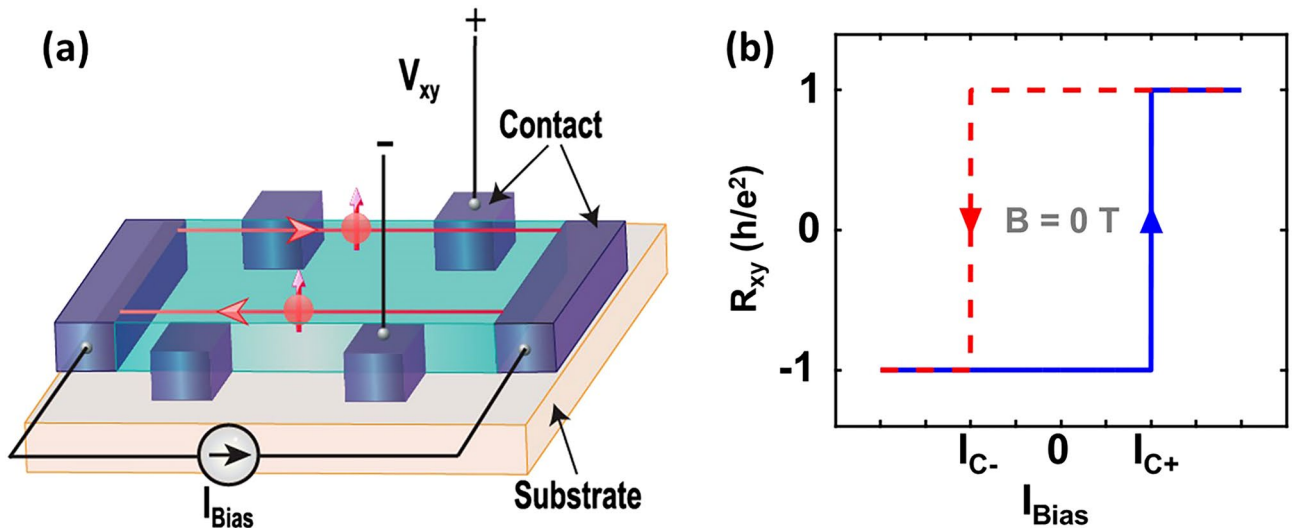


Figure 1. Schematic representation of quantum anomalous Hall effect. (a) Schematic of our device, where the red circles represent the electron and the red arrows show the spin of the electrons. A gate voltage can be applied at the back of the substrate to control the electronic density. V_{xx} and V_{xy} are the longitudinal and transverse (Hall) voltages, respectively, developed in response to the bias current, I_{Bias} . (b) Illustration of the Hall resistance R_{xy} versus the bias current, I_{Bias} at zero external magnetic field. I_{C-} and I_{C+} are two critical values of I_{Bias} which determine the hysteretic switching of R_{xy} between $-h/e^2$ and h/e^2 .

room-temperature applications may become feasible. Very recent works on QAHE in TbMn_6Sn_6 , MnBi_2Te_4 offer such prospects^{20–22}.

We start by delineating the dynamics of a QAHE insulator and how it can be used as a non-volatile memory cell. Figure 1a illustrates the schematic of a QAHE insulator with electric contacts to apply bias current and to measure both longitudinal and transverse (Hall) voltages. The QAHE states occur when an applied gate voltage tunes the bulk carrier density to close to zero. Then, the Hall resistance shows a hysteretic switching with the change of magnetic field. Also, magnetic domains of the ferromagnetic materials (for example, tBLG) strongly interact with the applied electrical current, which provides the electrical control over the polarization of the magnetic domains²³. It has also been shown¹ that the switching of Hall resistance driven by DC bias current is similar to that driven by magnetic field. We leverage this tunability in our design. Broadly, our design can be implemented with any material platform harboring an electrically tunable QAHE. Note that the exact reason behind the electrical switching of QAHE in tBLG awaits a comprehensive understanding. Orientation of the graphene layers as well as the interaction between the electrical current and ferromagnetic domains in tBLG may play a role²². It is also worthwhile to add that electrically tunable QAHE is not unique in tBLG; tri-layer graphene (twisted monolayer-bilayer graphene) also shows similar tunability^{24,25}.

Figure 1b shows a schematic of the hysteretic switching of Hall resistance R_{xy} ($= V_{xy}/I_{\text{Bias}}$) with the bias current at absolutely zero external magnetic field. Here, we mark two critical values of bias current, I_{C-} and I_{C+} , which denote the values of bias current required for the switching of Hall resistance between $\pm h/e^2$.

Figure 2 captures the highlight of our idea to leverage the quantized Hall resistance of a QAHE insulator as a non-volatile memory cell along with the write and read operations. We define the quantized Hall resistances, $-h/e^2$ and $+h/e^2$, as logic ‘0’ and logic ‘1’ respectively. Based on this definition, I_{Bias} can be divided into three regions (Fig. 2a)—(i) $I_{\text{Bias}} \leq I_{C-}$: write ‘0’ region, (ii) $I_{\text{Bias}} \geq I_{C+}$: write ‘1’ region, and (iii) $I_{C-} < I_{\text{Bias}} < I_{C+}$: read region. Figure 2b shows the bias current dependence of the Hall voltage, V_{xy} ($= I_{\text{Bias}} \times R_{xy}$). Importantly, as seen in Fig. 2b, write operations of both logic ‘0’ and ‘1’ entail positive V_{xy} because I_{Bias} and R_{xy} are either both positive (when writing logic ‘1’; Fig. 2c), or both negative (when writing logic ‘0’; Fig. 2d). In sharp contrast, read operations of logic ‘0’ and ‘1’ manifest opposite sign of V_{xy} . For example, if we use a positive bias current ($0 < I_{\text{Bias}} < I_{C+}$), logic ‘1’ and logic ‘0’ correspond to positive and negative V_{xy} , respectively. The clear difference in the sign of the Hall voltage for logic ‘0’ and ‘1’ makes the sensing of the memory states simple and straightforward. Figure 2g summarizes the key idea of a non-volatile memory utilizing the quantization of the Hall resistance in a QAHE insulator, listing I_{Bias} for write and read operations, as well as the state of the Hall resistance and Hall voltage for the two memory states.

Operation of a QAHE based memory

It is worthwhile to analyze the operation of the proposed QAHE based non-volatile memory in a 3D cross-point memory array. Figure 3a schematically shows our memory element: a tBLG moiré heterostructure where tBLG (with interlayer twisted angle of 1.1°) is encapsulated between flakes of hBN¹⁴. We have developed a Verilog A based phenomenological model for the QAHE in tBLG moiré heterostructure to use in our analysis of the heterostructure as a memory cell. The model can also be calibrated for other QAHE insulators using the values of bias currents (I_{C-} and I_{C+}) and the Chern number (ν). A behavioral representation of our model is shown in Fig. 3b. Figure 3c shows R_{xy} as a function of I_{Bias} at zero external magnetic field and at $T = 4$ K which is obtained

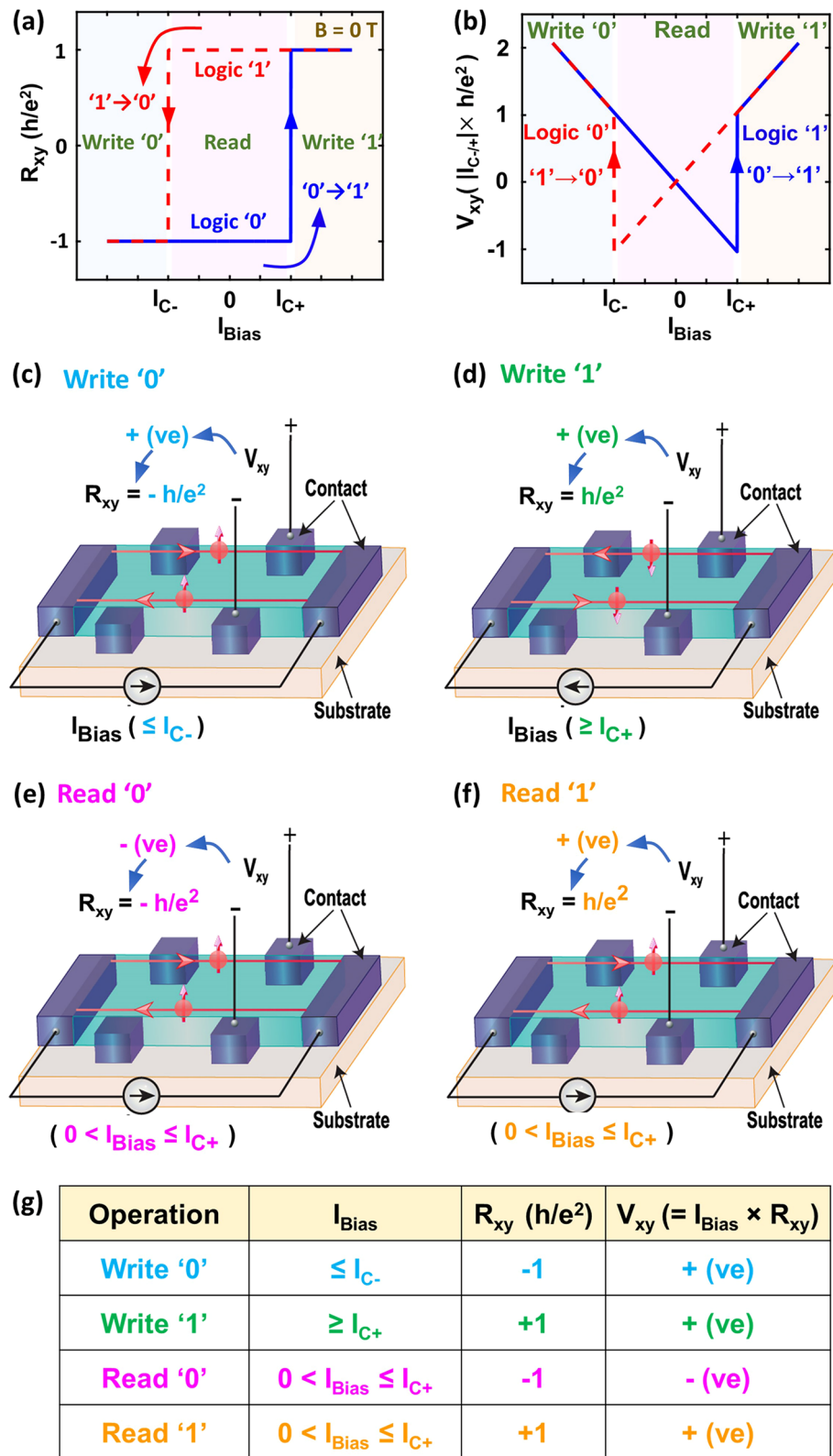


Figure 2. Illustration of the quantum anomalous Hall effect based memory operation. (a) R_{xy} vs. I_{Bias} at zero external magnetic field. Hall resistance values of $-h/e^2$ and $+h/e^2$ are defined as logic '0' and logic '1' respectively. Three regions: (i) $I_{Bias} \leq I_{C-}$, (ii) $I_{Bias} \geq I_{C+}$, and (iii) $I_{C-} < I_{Bias} < I_{C+}$ are marked as write '0', write '1' and read region, respectively. We use this division to choose the required I_{Bias} for different memory operations. (b) Hall voltage, V_{xy} , plotted as a function of I_{Bias} . (c), (d), (e), & (f) The procedures of write '0', write '1', read '0', and read '1' operations, respectively, along with the state of electron spins (red arrows). (g) Summary of the key idea for the QAHE based memory. The table enlists the required ranges of I_{Bias} corresponding to all memory operations, along with the corresponding Hall resistance and Hall voltage levels.

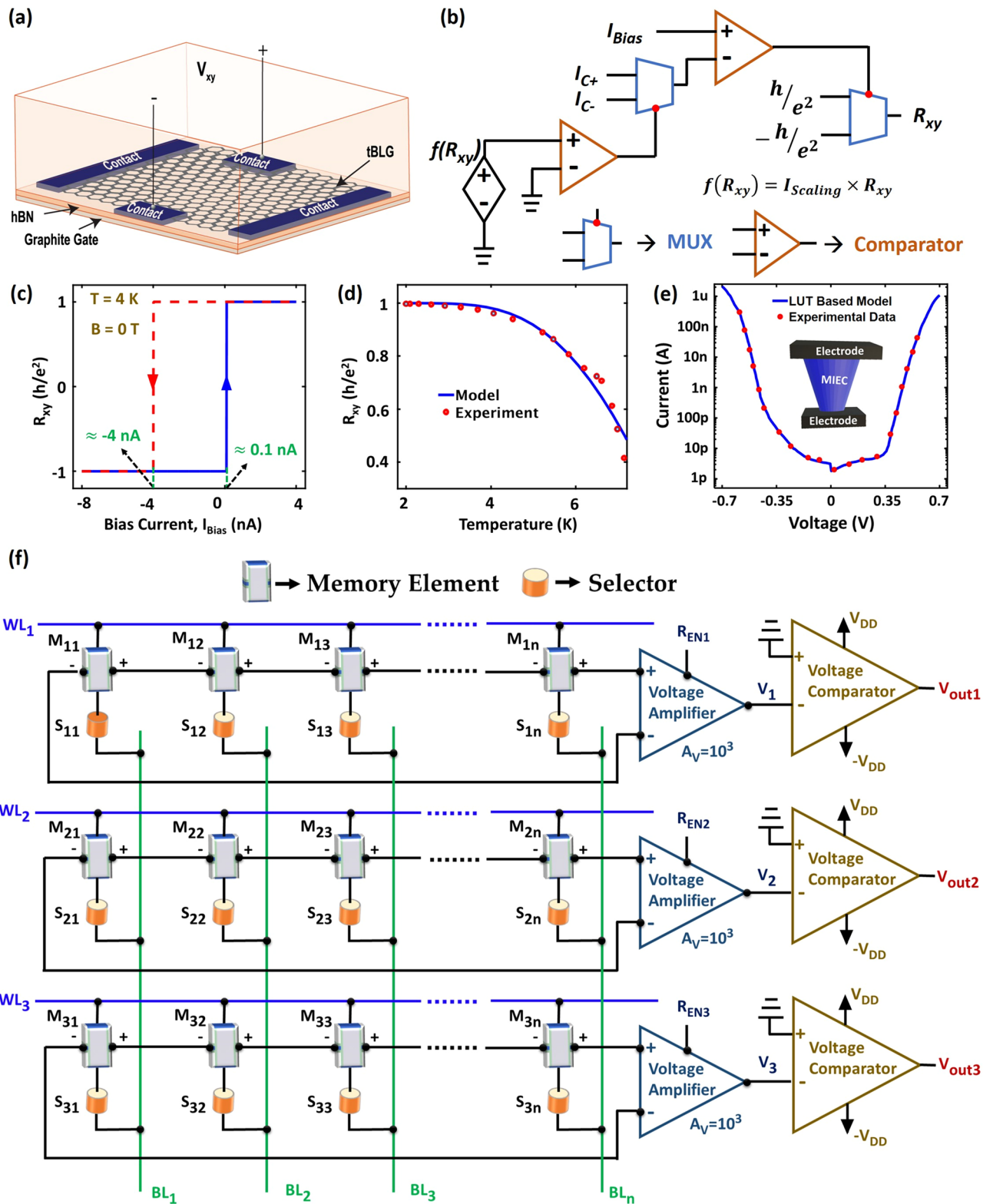


Figure 3. Design of the 3D cross-point memory array structure using a tBLG moiré heterostructure as a memory element and mixed-ionic-electronic-conduction based access device as selector. (a) Schematic of a tBLG moiré heterostructure where tBLG is encapsulated between flakes of hBN and a flake of few-layer graphite is used as gate. (b) Behavioral representation of our phenomenological model of the observed QAHE in the tBLG moiré heterostructure. (c) R_{xy} data, plotted as a function of I_{Bias} at $T = 4$ K and $B = 0$ T, exhibit current driven hysteretic switching. (d) Temperature dependence of R_{xy} with an experimental matching. (e) I - V characteristics obtained from a look-up table (LUT) based model of the mixed-ionic-electronic-conduction (MIEC) based selector device. (f) Illustration of the overall memory array structure, custom-designed for the QAHE based memory devices.

from the model shown in Fig. 3b. As seen from Fig. 3c, we can deduce the values of I_{C-} and I_{C+} for the tBLG heterostructure (approximately -4 nA and 100 pA, respectively) which are crucial for the memory operation. In our phenomenological model, we also account for the temperature dependence of Hall resistance using the following Eq. ¹:

$$R_{xy} = \frac{h}{e^2} - R_1 e^{-\frac{\Delta}{T}}, \quad (1)$$

where R_1 is a fitting constant, Δ ($= 26 \pm 4$ K) is the energy required to create and separate an excitation of particle-antiparticle of the QAH state and T is the temperature. Figure 3d, which shows the temperature dependence of the Hall resistance obtained from our model, agrees reasonably with the measured values reported in Ref. ¹.

Design of a cross-point array. To evaluate the practicality of a memory device, it is crucial to consider an array level scenario. The unique properties of our QAHE based memory device necessitate a custom designed memory array. To ensure the highest storage density, we adopt the cross-point memory architecture²⁶ with slight modification in the inter-cell connection pattern. A major component of the cross-point array is a two-terminal selector device²⁷ that allows access to a specific cell for read/write operation and suppresses current flow through the other cells. The selector devices are connected in series with the memory elements in every cell. A multitude of selector devices exist^{28–33} with diverse selectivity (ON/OFF ratio) and switching thresholds. For our QAHE based memory, the Cu-containing mixed-ionic-electronic-conduction (MIEC) material will be a perfect selector, due to its high selectivity ($\sim 10^6$), and ultra-low leakage (< 10 pA)^{34–36}. We have developed a look-up-table based phenomenological model (in Verilog-A) for this selector and calibrated the model (Fig. 3e) with the measured current–voltage (I – V) characteristics reported in Refs.^{34–36}.

Figure 3f shows the schematic view of our proposed array architecture. Every memory cell (QAHE device + selector) is sandwiched between orthogonally running metal lines, namely word line (WL) and bit line (BL). The WLs and the BLs are shared along the rows and columns of the array, respectively. The difference between the DC voltages applied on the WL and BL of a particular a memory cell essentially dictates the effective voltage across the cell (V_{Cell}). Note, the substrate terminal of every cell is biased with a constant voltage to maintain an appropriate electron density [not illustrated in the figures for simplicity]. Conveniently, we need only one control input, V_{Cell} , to read from or write into the QAHE devices. We utilize three different levels of V_{Cell} (with appropriate polarity) to write logic ‘1/0’ and to read the stored data.

Our architecture entails accessing one cell per row at a time. The Hall-voltage terminals of the neighboring cells in the same row are electrically connected in series with each other (Fig. 3f). Importantly, the resultant voltage across the end terminals of the series connected cells in a row (V_{hr}) bears the signature of the stored data in the accessed memory cell, along with some residual contributions from the other cells in the same row. For example, consider that every row holds n cells, and the k th cell of the i th row is being accessed. The resultant terminal voltage for this row can be expressed as:

$$V_{hr-i} = \sum_{j=1}^n V_{xy-ij} - 2n \times V_{loss} = I_{Bias-ik} \times R_{xy-ik} + \sum_{j=1, j \neq k}^n I_{Bias-ij} \times R_{xy-ij} - 2n \times V_{loss} \quad (2)$$

here V_{loss} denotes the average loss component per contact, indicating the inherent non-ideality. The specialized biasing scheme of the memory array (discussed later) ensures that the losses and residual components are negligible (quantified in the Sect. 3 of the Supplementary Materials) compared with the Hall voltage of the accessed cell. As a result, the polarity of V_{hr} is dictated by the R_{xy} of the accessed cell. For the tBLG moiré heterostructure based QAHE device, we need to amplify the V_{hr} from a few tens of microvolts to tens of millivolts using cryogenic amplifiers. A suitable candidate for such an amplifier can be one of the cryogenic low-noise amplifiers reported in Refs.^{37–39}. After the amplification, the millivolt level Hall voltage is used to determine the memory state of the accessed cell. Recall, during read operation, logic ‘0’ and ‘1’ memory states correspond to opposite polarity of Hall voltage (Fig. 2b). Therefore, we feed the amplified V_{hr} to a cryogenic voltage comparator⁴⁰ to sense the memory state of the accessed cell.

Read/write operations. In Fig. 4, we present the simulated memory operations (read/write) in our proposed QAHE based cross-point array. Figure 4a illustrates four types of memory cells in a block of cross-point array. We utilize a standard biasing scheme for cross-pint arrays, commonly known as the $V/2$ biasing³³. Different levels of access voltage (V_{ACC}) are applied to read from or write into a specific cell. The row (column) that holds the accessed cell is called the half-accessed row (column), because the inactive cells in this row (column) receive half of the access voltage ($V_{ACC}/2$). All the other unaccessed cells ideally have zero voltage across them. Without any loss of generality, we assume M_{11} (Fig. 3f) to be the accessed cell and examine its read/write dynamics. Figure 4b shows the cell current levels through the accessed, half-accessed, and unaccessed cells during $1 \rightarrow 0$ memory write operation. Only the accessed cell exhibits a transition ($+h/e^2 \rightarrow -h/e^2$) in the Hall resistance (R_{xy}) (Fig. 4c), indicating a successful write operation in the accessed cell without disturbing the other cells. Figure 4d,e show similar time dynamics for the $0 \rightarrow 1$ write operation. Note, the cell current level for the $0 \rightarrow 1$ operation is of the opposite polarity compared to the $1 \rightarrow 0$ operation (Fig. 4d). The repeated write operations ($0 \rightarrow 0$ and $1 \rightarrow 1$) have also been tested and are presented in supplementary Fig. S2.

Next, we examine the read dynamics (Fig. 4f–j) of the proposed memory cell. The current flow direction for the read operation is the same as the $1 \rightarrow 0$ write operation (Fig. 4f). However, the magnitude of the read current is about one-third of the critical current of transition (I_{C-}), which alleviates the possibility of accidental $1 \rightarrow 0$ data

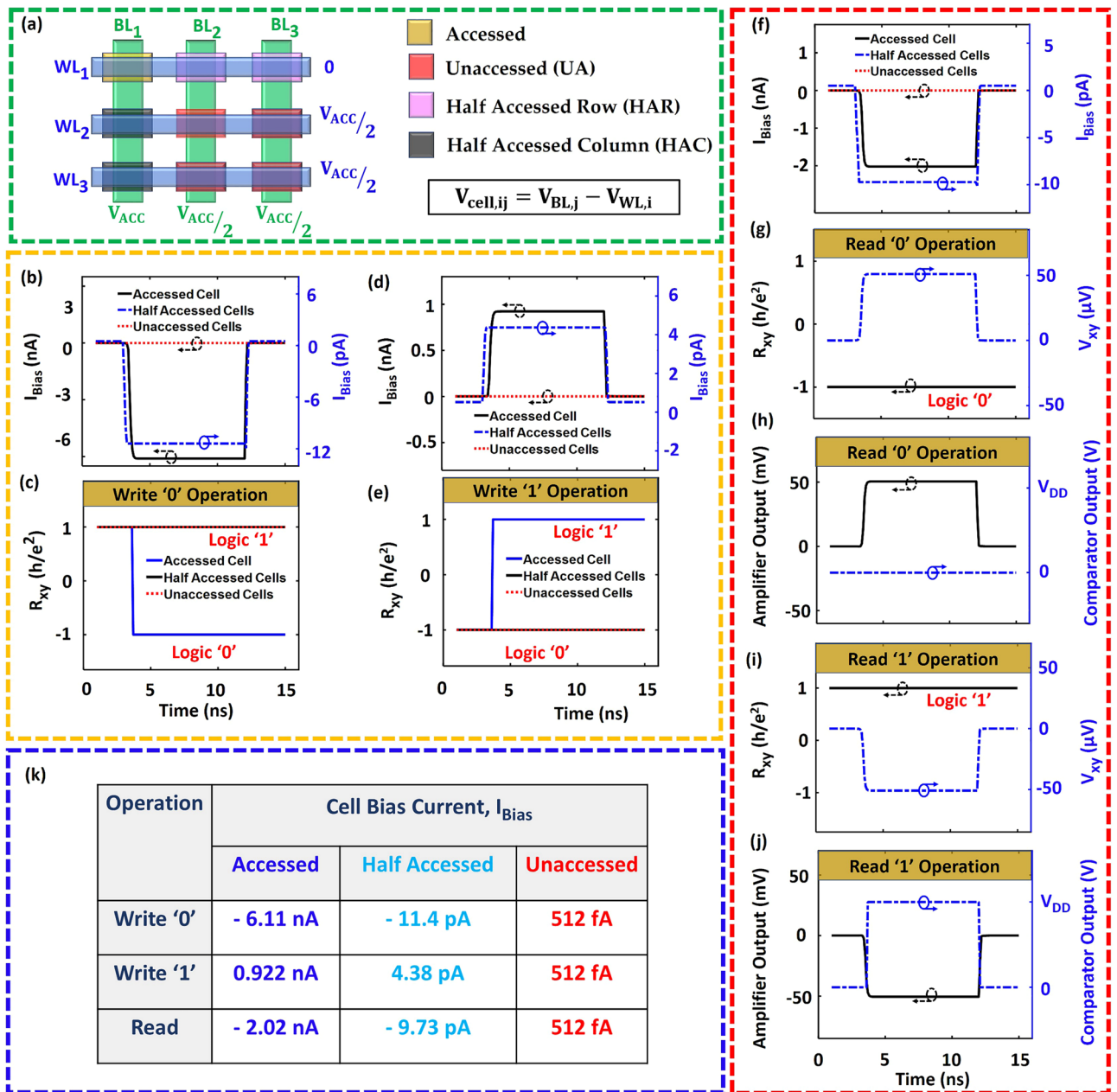


Figure 4. Compilation of the simulation results for the memory array. (a) Arrangement and types of memory cells in a conventional cross-point memory array under the $V/2$ biasing scheme. *Write '0' operation:* (b) Cell Bias currents (I_{Bias}) through different memory cells generated by applying appropriate V_{ACC} . (c) The time dynamics of the Hall resistance (R_{xy}) illustrating state transition only in the accessed cell. *Write '1' operation:* (d) I_{Bias} with different magnitude and opposite polarity (compared with the write '0' case) flowing through different memory cells (e) Corresponding transition in R_{xy} . *Read operation:* (f) The I_{Bias} is of the same polarity as the write '0' operation, but has $\sim 3X$ lower magnitude. The peripheral circuits (amplifier and comparator) are enabled only during this period. The comparator output is always initialized at zero voltage. (g) If the memory cell holds binary '0', the Hall voltage (V_{xy}) exhibits a positive polarity during the read operation. R_{xy} remains unchanged throughout the process. (h) The amplified V_{xy} is fed into a comparator which produces a digital output. While reading '0', the comparator output remains unchanged at its initial value (0 V). (i) Read '1' operation produces the opposite polarity in V_{xy} , and R_{xy} remains unchanged. (j) The amplified V_{xy} triggers a $0 \rightarrow V_{DD}$ transition in the comparator output, which remains stable throughout the read operation.

flip. In addition, the chosen polarity of the read current nullifies the possibility of accidental $0 \rightarrow 1$ transition. The read current through the QAHE device generates a Hall voltage (V_{xy}), whose polarity is dictated by the previously set Hall resistance ($+h/e^2$ or $-h/e^2$). In our design, positive/negative polarity of V_{xy} corresponds to

logic 0/1, respectively (Fig. 4g,i). It is worth noting, the read operation utilizes different pair of terminals than the write operation, allowing independent optimization of read/write peripheral circuits. Furthermore, the amplifier-comparator pairs are enabled only during the read operation to minimize peripheral power demand. The comparator in our design also provides digital outputs corresponding to the stored data in the accessed cell (Fig. 4h,j). Note, the resistance of the MIEC exponential selector drastically increases for lower voltage range (< 0.35 V), as shown in supplementary Fig. S5. The array biasing scheme is designed to enforce high resistance mode of the selector in every memory cell but the accessed cell. This design technique ensures that the half-accessed and unaccessed cells encounter orders of magnitude less current compared with the accessed cell. The MIEC selector takes an overwhelming share of any voltage applied across the cell, averting the chances of a breakdown in the QAHE device. The bias currents that flow through the cells during different memory operations are shown in Fig. 4k which clearly demonstrate that the memory states of the half-accessed and unaccessed cells will not be disturbed during write or read operation in the accessed cell. Thus, our architecture lays out a device-to-array design pathway for the QAHE based unique memory devices.

Outlook and discussion

Our cryogenic memory framework is transferable to the material structures that exhibit current-controlled switching of QAH states (e.g., tri-layer graphene^{24,25}). Some of these material structures will necessitate an initialization step to first create a magnetic moment in the system. The additional analog components required for this purpose will be parts of the array peripherals. The underlying transition mechanisms of the QAHE devices may determine their endurance and reliable life span.

We close by discussing the broad impact of our work. This manuscript makes the first mark to construct a working electronic device using topological properties of materials. Here we leverage QAHE, that does not require an external magnetic field, and design an elegant memory device that can be built with topological quantum materials. The proposed non-volatile memory architecture is a strong candidate for the cryogenic memory system, thanks to its ultra-low temperature compatibility. Note, the cryogenic memory block is a crucial component of quantum computing systems based on superconducting qubits⁴¹. Our proposed QAHE-based memory device offers a significant reduction in the cell area and 1000 times reduction in the cell read/write power compared with the state-of-the-art cryogenic memory devices^{42–49} (see supplementary Table S1 for detailed comparison). Our proposed memory device is a potential game-changer for scalable quantum computing systems⁴¹ and space cryogenics⁵⁰.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

Received: 25 November 2020; Accepted: 22 March 2021

Published online: 12 April 2021

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Author contributions

S.A. and M.S.H conceived the idea. S.A. performed the simulations and array design. M.S.H. and A.A. analyzed the results. A.A. supervised the project. All authors commented on the results and wrote the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary Information The online version contains supplementary material available at <https://doi.org/10.1038/s41598-021-87056-7>.

Correspondence and requests for materials should be addressed to A.A.

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