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Optimizing pentacene thin-film transistor performance: Temperature and surface condition induced layer growth modification

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Abstract

In this work we present *in situ* electrical and surface analytical, as well as *ex situ* atomic force microscopy (AFM) studies on temperature and surface condition induced pentacene layer growth modifications, leading to the selection of optimized deposition conditions and entailing performance improvements. We prepared p⁺⁺-silicon/silicon dioxide bottom-gate, gold bottom-contact transistor samples and evaluated the pentacene layer growth for three different surface conditions (sputtered, sputtered + carbon and unspattered + carbon) at sample temperatures during deposition of 200 K, 300 K and 350 K. The AFM investigations focused on the gold contacts, the silicon dioxide channel region and the highly critical transition area. Evaluations of coverage dependent saturation mobilities, threshold voltages and corresponding AFM analysis were able to confirm that the first 3–4 full monolayers contribute to the majority of charge transport within the channel region. At high temperatures and on sputtered surfaces uniform layer formation in the contact–channel transition area is limited by dewetting, leading to the formation of trenches and the partial development of double layer islands within the channel region instead of full wetting layers. By combining the advantages of an initial high temperature deposition (well-ordered islands in the channel) and a subsequent low temperature deposition (continuous film formation for low contact resistance) we were able to prepare very thin (8 ML) pentacene transistors of comparably high mobility.

Keywords

Organic thin-film transistor; Pentacene; Carrier mobility; Atomic force microscopy; Diffusion; Dewetting

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Author contributions

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1. Introduction

Organic electronics, the extensive field of employing the electronic properties found in polymers and small organic molecules, is already far beyond being a primarily research specific term. It is frequently used in today's marketing strategies for electronic devices, symbolizing high quality, cutting-edge technology [1,2]. The organic systems inherent advantage of room temperature processing and patterning, enables a completely new class of temperature critical substrates and materials, with associated qualities such as low-cost, flexibility and bio-degradability [3,4]. With the first systems achieving commercial status, scientific focus expands from the hands-on creation of organic thin film transistor (OTFT) devices towards more and more fundamental research. Indeed, device features of critical interest, such as transistor performance and organic semiconductor growth, are to the present date not fully understood and controllable in satisfactory detail [5–8].

Being part of organic field effect transistor research and development for almost 25 years [9,10], the polycyclic aromatic hydrocarbon pentacene ($C_{22}H_{14}$) has earned its reputation as a working horse material in OTFT fabrication. This is for the most part attributable to the attainable high charge carrier mobilities and can be related to the materials tendency to form well-ordered layers of standing molecules with excellent long axis alignment of the five linearly connected benzene rings, which form the molecules structure [11]. To gain conclusive insight into thin-film growth and the connected electrical properties recently several groups turned their attention to *in situ* measurements under vacuum conditions, in an effort to improve reproducibility and reduce atmosphere induced contamination and degradation [12–20]. These groups were able to show that ultra-high vacuum (UHV) chamber deposition in combination with *in situ* surface analytical and electrical characterization methods are able to accurately connect active layer growth and morphology with the resulting electrical transistor properties, based on specific, well-controlled surface alterations [21,22].

One distinguished point of interest is the number of closed monolayers (ML) at which the rise in mobility with increasing coverage saturates and therefore indicates the maximum effective Debye length in the film [23,24]. This was subject-matter of a number of articles [14,15,19,20,23–27] and was also discussed to some extent in our previous publication [28]. In this work we reported a saturation of the mobility at a layer thickness of about 4 monolayers (approximately 6.4 nm) for low temperature (200 K) layers. For room temperature deposition a significant additional mobility increase up to 50 nm layer thickness was observed. This was attributed to a decrease of the access resistance due to better, continuous film formation in the silicon dioxide–gold electrode transition region [28].

The complementary measurements described in this contribution address and expand the aforementioned reports for pentacene growth. Pentacene layers have been deposited on carbon contaminated as well as sputter cleaned SiO_2 for sample temperatures up to 350 K. This allowed us to gain further insight into the optimal processing temperatures for pentacene deposition for a range of semiconductor thicknesses. Based on the gained information we were able to prepare mixed layer systems, featuring different sample temperatures during deposition, which showed improved transistor behavior.

2. Experimental

2.1. Film preparation and surface analytical characterization

Our experimental setup enables full control over the semiconductor deposition process through precise deposition temperature and rate adjustment, as well as exact sample surface temperature control and variation between 120 K and 800 K, during and subsequent to the deposition itself. The sample surface and deposited layers can be modified by argon ion sputtering and analyzed by Auger electron spectroscopy (AES) as well as thermal desorption spectroscopy (TDS). Electrical characterization was performed via a self-designed LabVIEW[®] processing software. *Ex situ* AFM was used to characterize the morphology of the films. A detailed description of the sample preparation, vacuum equipment and experimental methods at our disposal can be found in our previous publication [28].

2.2. Electrical characterization

While not always applicable to its full extent [23,29], the formalism developed for silicon based field effect transistors has proven to be the most efficient and intuitive way to compare the performance characteristics between samples and with results from other research groups. By setting either the drain-source voltage (U_{DS}) and sweeping the gate-source voltage (U_{GS}) or vice versa and measuring the resulting source-drain current (I_{DS}), transfer and output characteristics can be generated, which in turn contain the necessary information to extract the parameters of relevance for organic transistor characterization, in our case the charge carrier mobility (μ) and the threshold voltage (U_T) [30]. For our investigations the saturation mobility (μ_{Sat}) as a function of coverage was the main point of interest, extracted from the well-known formula:

$$I_{DSSat} = C_G \mu_{Sat} \frac{W}{2L} [U_{GS} - U_T]^2 \text{ for } |U_{DS}| > |U_{GS} - U_T| > 0 \quad (1)$$

(saturation regime)

with the aforementioned parameters for the saturation condition, as well as the gate capacitance of SiO₂ C_G (23 nF/cm²), the channel width W (4 mm) and length L (25 μ m) [28].

2.3. Preparation condition matrix

The main intention of this work was to reach a comprehensive understanding of the influence of film preparation parameters on the transistor properties. For this purpose, we deposited pentacene films on a SiO₂ bottom-gate, gold bottom-contact configuration at three different temperatures (200 K, 300 K, 350 K). Following our preceding investigations [28] on substrates, which had been sputter cleaned before creating a carbon saturation layer (labeled as Sputtered + C), we expanded our investigations to the contrasting surface conditions of unsputtered and subsequently carbon covered (labeled Unsputtered + C) as well as sputter cleaned samples (labeled Sputtered). The carbon saturation layer was established by repeated adsorption/desorption cycles of pentacene layers, as described in more detail in our previous paper [28]. For all of the samples (3 temperatures, 3 surface conditions) we have performed full *in situ* electrical characterization via output and transfer curves and subsequently investigated the film morphology by *ex situ* AFM in the SiO₂

channel region, the gold contact region and in the very important SiO₂–Au transition region. This resulted in a (3 × 3 × 3) information matrix. Additionally, our systems unique possibility of repeated pentacene deposition and removal allowed us to perform the depicted coverage dependency measurements on a single silicon wafer sample for each parameter set and therefore ensured optimal reproducibility for the displayed results. The obtained values for the mobilities and threshold voltages showed excellent agreement with our previous measurements for similar parameter sets. This comparability of measurements performed over a timespan of more than a year and over 50 samples is proof of the reliability and reproducibility provided by our experimental setup.

3. Results and discussion

3.1. Coverage dependent mobility on Unspattered + C samples

A series of pentacene transistors have been prepared on the Unspattered + C sample surface at 200 K, 300 K and 350 K. The corresponding output and transfer curves have been recorded for parameter extraction, in particular the mobility and threshold voltage as a function of coverage. Characteristic output and transfer curves for the three temperature regimes are shown in Figs. 1–3. The non-linearity for low drain-source voltages (U_{DS}) in Figs. 2 and 3 can be related to contact resistance effects [30]. The mobility evolution with increasing pentacene layer thickness for these temperatures in a coverage range of 0–150 nm, as well as an inset depicting the formation of the first percolation layer for electrical conductivity at low coverage are shown in Fig. 4.

3.1.1. Pentacene deposition at 200 K and 300 K—An immediately observable feature in the electrical evaluations is the excellent reproducibility within error margins when it comes to the extracted mobility values for the two 300 K measurements on the Unspattered + C surface. The first source-drain currents and therefore mobilities larger than zero can be observed at around 1.2–1.5 nm nominal pentacene coverage for the 200 K and 300 K layers (see inset in Fig. 4), equivalent to a layer thickness of approximately 0.75 monolayers, which in turn shows good agreement with the postulated percolation threshold of about 0.7 monolayers reported by other groups [31–33]. The maximum recorded saturation mobilities for both temperatures on the Unspattered + C surface are roughly a factor of 10 lower than the previously published results on the Sputtered + C samples [28], indicating a strong influence of the surface preparation. The 200 K growth shows mobility saturation at the completion of 3–4 monolayers, corresponding to approximately 5–7 nm of nominal pentacene coverage. This saturation indicates the complete filling of all the charge contributing semiconducting layers in the channel region within the Debye length [19,23,24]. AFM investigations on 1.5 ML (equivalent to 2.4 nm) of pentacene in the channel and in the gold contact region, as well as 7.5 ML (12 nm) in the transition between those two, reveal the underlying layer growth responsible for the electrical results (see Fig. 5). At the comparably low process temperature of 200 K the pentacene molecules impinge on the surface and stick within a comparably short timeframe, without having the possibility to diffuse over a large area in order to occupy an energetically more favorable site, such as the accommodation at an existing island edge [34]. This leads to the formation and growth of a high number of small, sub 250 nm diameter grains on the silicon dioxide (see Fig. 5(a))

(The very large mean layer thickness suggested by the cross section is caused by the numerous high and pointy islands and a resulting overestimation and feature broadening by the AFM tip). On gold (see Fig. 5(b)) the low temperature also significantly influences the layer growth of the pentacene islands, leading to a distribution of small islands composed of lying molecules as described by Käfer et al. [35]. In Fig. 5(c) an AFM analysis on 7.5 ML of pentacene in the transition from the gold contact area (top left) to the channel region is shown. The small grains forming at 200 K substrate temperature cover the whole transition region uniformly, as can be observed in the cross section.

In Fig. 6 AFM images of 1.5 ML (equivalent to 2.4 nm) of pentacene in the channel and in the gold contact region, as well as 7.5 ML (12 nm) in the transition region, all deposited at 300 K, are depicted. For the room temperature deposition on SiO₂ a Stranski–Krastanov like growth mode is observable [36] (see Fig. 6(a)), characterized by the full development of the first monolayer of standing molecules before transitioning into a more island-like layer form, again featuring the characteristic step heights of approximately 1.6 nm, equivalent to the long pentacene axis. The excellent calibration of our deposition system for low coverages and the accompanying small margin of error for actual layer thickness evaluations become evident by the congruence of the second layer area in Fig. 6(a) with the nominally deposited layer thickness of 1.5 full monolayers. This allows us to draw clear conclusions from the differences in the onset of transistor behavior for different growth regimes. At this elevated temperature impinging molecules can diffuse over a larger area than at 200 K and overcome diffusion and Ehrlich–Schwoebel barriers more easily [37,38]. This leads to a decrease in the total number of islands and the preferable accommodation of molecules at the energetically favorable edges of existing islands, which are now accessible by diffusion and up and down-hopping between island layers [39].

For growth on gold at 300 K distinguished high island structures composed of flat-lying molecules (see Fig. 6(b)) are now observable and follow the growth patterns reported by Käfer et al. [35]. The very different island structure on SiO₂, consisting of strongly cascaded islands with monomolecular steps of standing pentacene molecules, plays a significant role for island growth in the channel–contact transition region (Fig. 6(c)). With the increased diffusion at 300 K, compared to 200 K deposition, more pentacene molecules are able to escape the energetically unfavorable transition region. The molecules then tend to incorporate into the existing structures on either the gold or the silicon dioxide, inhibiting the smooth layer formation in the transition region observed at 200 K. Following the formation of one full wetting layer between the two gold contacts, characterized by the onset of transistor behavior at about one monolayer (see inset Fig. 4), a further closing of layers in the transition region with increasing coverage is delayed. This leads to an ongoing rise in the virtual charge carrier mobility up to coverages of over 50 nm.

3.1.2. Pentacene deposition at 350 K—For coverage dependent mobility measurements on the Unspattered + C surface at 350 K sample temperature the recorded mobility values are still more than a factor 10 below those of the layers of comparable thickness on the Sputtered + C system in our previous investigations [28]. The form of the coverage dependent mobility curve now shows a very pronounced double saturation behavior (Fig. 4). The 350 K layer reaches a very early and strongly pronounced first

mobility saturation around a pentacene coverage of 6–8 nm, indicating 4–5 fully closed layers within the Debye length in the channel region [23]. This is attributed to the increase in molecular mobility with increasing temperature [11], usually facilitating a more layer by layer like growth of the pentacene in the channel region and the formation of larger, well-ordered crystals, entailing a lower number of grain boundaries. In Fig. 7(a) an AFM image for a film of 7.5 ML pentacene, deposited onto the SiO₂ channel region at 350 K, is displayed. While the 200 K layers show a very high number of small grains (Fig. 5(a)) and the 300 K film features the characteristic and often reported cascaded, pyramid-like island growth (Fig. 6(a)), the 350 K film displays very large, well-ordered islands with little cascading and associated islanding and a large number of fully closed layers underneath the visible islands, as can be seen in the corresponding cross section (Fig. 7(a)). The higher coverage of 7.5 ML, compared to the 1.5 ML depicted for 200 K and 300 K, has been selected to display the uniformity in layer formation for a wide coverage range. On the gold contacts (Fig. 7(b)) large island structures form on top of closed layers, both composed of flat lying pentacene molecules [35].

The transition region from the channel area onto the gold contacts shows the well-ordered layer formation on the SiO₂, as well as rather smooth layers with a few very high islands on the gold contacts (Fig. 7(c)). One would generally expect an increase in charge carrier mobility in a 350 K film compared to the same layer thickness deposited at 200 K and 300 K through the superior layer structure and the general temperature dependence of the mobility [28]. However, the SiO₂–Au transition region seems to be an energetically very unfavorable region for pentacene growth in this sample configuration and the deciding factor for the maximum attainable mobility for elevated temperature deposition. The formation of distinct trenches takes place at the edge of the channel–contact transition, as can be seen in the corresponding cross section below Fig. 7(c). Apparently, the increased temperature allows the molecules not only to diffuse over larger distances, but also to overcome Ehrlich–Schwoebel barriers for up-hopping onto existing islands and the partial formation of double layers [39]. This results in a delay in the onset of transistor behavior to around 2.5 nm of pentacene coverage, almost twice the coverage necessary for percolation at 200 K and 300 K (see inset in Fig. 4). At higher coverages this dewetting in the transition region counteracts the superior conductivity of the inner channel structure within the Debye length. Thus, the advantage of well-ordered pentacene films in the channel region due to high temperature deposition can only be utilized to its full extent once the gold contact is sufficiently connected to the active semiconducting layer. Therefore, a pentacene coverage of approximately 120 nm is necessary for the 350 K layer to fully overtake the 300 K layer in performance.

3.2. Coverage dependent mobility on sputtered samples at 200 K, 300 K and 350 K

Following the measurements on the Unspattered + C surface, the same sample was then used for investigations on pentacene growth and electrical performance on sputtered SiO₂ and gold. Fig. 8 shows the output and transfer curves for the highest recorded mobility measured for a 96 nm thick pentacene layer deposited at 350 K onto the sputtered surface. The mobility evolution as a function of pentacene coverage on the sputtered sample surface for all three temperature regimes and an inset depicting the onset of the transistor behavior

are displayed in Fig. 9. Sputtering is generally assumed to increase surface roughness and therefore decrease the diffusion of particles on the surface [40]. On the other hand, depending on the material system, the removal of contaminations can lead to an increase in diffusion. As no significant surface roughening of the very smooth SiO₂ surface through sputtering could be registered with our AFM setup, an increase of diffusion probability can be assumed.

As expected from the previous discussions, the increase in diffusion led to a trend of an even more delayed onset of transistor functionality for the sputtered samples. Only the 200 K experiment demonstrated no change in onset behavior from the sputtering process, once more showing first percolation at approximately 1.5 nm of pentacene coverage.

The coverage necessary for the first percolation increases from approximately 1.2 nm to 2 nm of pentacene coverage for the 300 K deposition and from about 2.5 to 3 nm for the 350 K measurement in comparison to the unsputtered samples. The reason for this behavior is the above described tendency to form double layers instead of monomolecular wetting layers by up-hopping when the diffusion probability is sufficiently high [39]. In Fig. 10(a) a detailed AFM analysis of this region for the critical transition coverage of 2.5 ML just below the percolation threshold for the sputtered 350 K configuration is depicted. From the absence of transistor functionality at this coverage and the corresponding cross section we can conclude that the darkest area in Fig. 10(a) close to the gold electrode indeed has to be the silicon dioxide surface, since the deposited amount of material wouldn't suffice to form a third underlying layer. Thus, virtually no contact between the pentacene layer and the gold contact area exists. In Fig. 10(b) an analysis of a similarly prepared film with a coverage of 7.5 ML (sputtered sample, 350 K temperature) in the mid-channel region also shows the described up-hopping behavior, leading to the preferred formation of double layers for the lowest observable plane even for thicker layers, as depicted by the measured step height of two standing pentacene molecules (3.2 nm) for the lowest layer in the corresponding cross section.

As described in Section 3.1.2, an increase in maximum attainable charge carrier mobility from the reduction of the total number of grain boundaries is expected for all preparation temperatures on the sputtered samples. The analysis of the electrical data proves this claim and indicates a rise of the saturation mobility by factors of 5–10 for all temperature settings (mind the difference of one order of magnitude in the mobility axis scaling between Figs. 4 and 9). Nonetheless, the dewetting processes in the channel–contact transition region are so strongly developed for those samples, that no complete saturation in mobility with increasing coverage takes place up to pentacene layer thicknesses of 96 nm for all three processing temperatures.

3.3. Coverage dependent threshold voltages

Next to the mobility, the threshold voltage (U_T) is a transistor parameter of very high interest. Defined as the voltage for 'appreciable' source-drain current flow [22], U_T has to be extracted in order to employ our selected method of saturation mobility calculation. In this form the threshold voltage is sometimes seen as a mere fit parameter [41], nonetheless, important information on the charge carrier transport in the channel region can be gained. As

displayed in Fig. 11, the threshold voltage generally displays rather early saturation behavior with increasing coverage, especially compared to some of the connected results for delayed mobility saturation. This can be explained with the aforementioned 3–4 full monolayers of pentacene channel coverage being responsible for the vast majority of the charge transport between the electrodes. Once a sufficient level of gate voltage is reached, the channel fully opens and all accessible charge carrier transport sites within the Debye length can contribute to the transport. For layer configurations featuring a very uniform growth and therefore low access resistance towards the gold electrodes, the threshold voltage and the mobility saturate at a coverage representing approximately 4 fully closed monolayers, as can be observed for the measurements at 200 K sample temperature (see Figs. 4 and 9).

For samples with a delayed formation of closed layers in the gold electrode–SiO₂ channel transition region a significant influence of the contact resistance is observable (see S-shape of the output curves in Fig. 8(a)) [30]. Layers on the SiO₂ inside the channel still fully close, leading to a saturation of the threshold voltage at the aforementioned coverage of 3–4 monolayers, representing the Debye length. A further, ‘virtual’ increase of mobility with pentacene coverage, as observable for all measurements at 300 K and 350 K (see Figs. 4 and 9), is then attributable to the closing of layers in the SiO₂–Au transition region.

The general threshold voltage curve shape as a function of pentacene coverage is governed by the density of trap states in the layer. Deep hole trap states related to the semiconductor–dielectric interface influence the starting point for conduction and are responsible for the lowest values of U_T to be found at low coverage, since a more negative gate voltage is necessary in order to attract enough charge carriers to the dielectric surface to fill the traps and allow conduction between source and drain. According to Fiebig et al. [20] and as seen in our previous evaluations [28], the rise in threshold voltage with increasing coverage can be attributed to the formation of electron traps in the pentacene film and especially on its surface. These traps lead to a negative charging of the film and counteract the deep-hole traps. This effect levels off at higher coverage, where the surface shape related traps have no direct influence on the electrically conducting layers at the bottom of the film, which are closest to the gate electrode. Therefore, above sufficient pentacene coverage, the threshold voltage should remain nearly constant with increasing coverage. This saturation behavior is most obvious for the 300 K and 350 K layers on the Unspattered + C sample and for both 200 K films. For the sputtered sample at 300 K and 350 K an ongoing slight increase in threshold voltage with pentacene coverage is observable, attributed to the introduction of new traps states through the Ar⁺-ion bombardment.

Nonetheless, the major sputter influence is a uniform threshold voltage decrease compared to the Unspattered + C sample. In our opinion this is caused by a shift in the electrostatic potential due to the incorporation of Ar⁺-ions in the channel area. This leads to a screening of the gate potential, requiring stronger negative gate voltages in order to achieve the same charge attracting field and therefore shifts of the threshold into the negative direction. By heating the sample to temperatures above 650 K, Ar⁺-ions that had been implanted in the surface near region can be degassed prior to pentacene deposition, as shown by thermal desorption spectroscopy. Indeed, this led to an upward shift in the threshold voltage. This opens up the possibility of influencing the threshold voltage in a controlled way via argon

implantation and therefore the adjustment of the threshold voltage to specific application needs. Specifically designed experiments performed in our system have shown stable and reversible shifts of the threshold voltage through argon sputtering and annealing processes. Since the focus of this work lies on the layer formation and morphology as a function of coverage and growth conditions this special feature will not be discussed in further detail here.

3.4. Optimized pentacene growth and experimental conclusion

In the previous sections, the pentacene layer growth within the channel and in the SiO₂-Au transition region, as a function of deposition temperature and sputter controlled carbon surface contamination, has turned out to be the major area of interest for optimizing the semiconductor growth in our system. The demonstration of the sample temperature dependent layer growth mode on the Unspattered + C samples in Figs. 5–7 depicts the entire transition from the uniform growth of small islands at 200 K (Fig. 5(c)), through the strongly cascaded growth at 300 K (Fig. 6(c)), up to the formation of the largest and most well-ordered islands with the detrimental SiO₂-Au transition region dewetting at 350 K (Fig. 7 (c)). A corresponding representation of the sputter influence on the layer growth mode and island density is depicted in Fig. 12.

The sample temperature of 300 K has been chosen to be the most representative one, based on the pronounced sputter influence on layer growth mode in Fig. 9 and the corresponding largest shift in mobility onset. The AFM evaluations show excellent agreement with our investigations on diffusion dominated layer growth. From the largest, most well-ordered and cascaded islands on the Sputtered sample in Fig. 12(a), a clear transition to higher island density on the Unspattered + C sample is observable (Fig. 12(c)). The Sputtered + C sample, as analyzed in our previous report [28], depicts a film morphology in between those two configurations (Fig. 12(b)).

With this gathered information we can now return to the question of optimized layer growth for our pentacene transistors. Most research groups employ various forms of surface cleaning and elevated surface temperatures to improve the pentacene layer growth [11]. One factor of importance is the often comparably high total pentacene layer thickness deposited. This puts the system into the high temperature–high coverage regime, where we also achieved our best performance results (see Fig. 9). On the other hand, this neglects the influence of the highly critical SiO₂-Au transition region for the bottom-contact configuration, which might be the dominant factor for the large variation in saturation mobility values as a function of coverage reported in literature, ranging from 3.2 nm to over 150 nm [15,19,20,25–27]. Therefore the layer thickness is of fundamental interest when it comes to the selection of the optimal processing temperatures. As it often is the case in semiconductor physics, the tendency to make layers as thin as possible is a major factor in device design and fabrication. The charge transport takes place in only the first few monolayers within the Debye length [23,24]. For thinner layers this implies that, through an improved contact to the electrodes, the low surface temperature growth regime, in spite of the inferior layer quality in the channel, can result in an increase in performance compared to higher temperature layers, featuring the originally better inner layer structure. Following

our investigations on sputtered and unsputtered systems we propose a mixed layer system on a sputtered substrate, consisting of a thin 350 K film to form a well-ordered conducting layer in the channel region, covered by a thin 200 K film. This ensures a low number of grain boundaries for high mobility in the channel and a uniform coverage and electrode connection in the SiO₂–Au transition region. The result of this experiment, compared to non-mixed layers of equivalent coverage, is shown in Fig. 13.

The combination of 4 ML (6.4 nm) of pentacene deposited at 350 K (i) and covered with another 4 ML at 200 K (ii) displays the expected qualities. While a 8 ML (12.8 nm) film deposited at 350 K gives a mobility of about 0.004 cm²/Vs, the deposition of 4 ML at 350 K and additional 4 ML at 200 K results in a mobility increase by a factor of 4 to approximately 0.016 cm²/vs. The mixed layer configuration is stable at room temperature and the 200 K layer shows no dewetting over time in this temperature range. Additional 4.5 ML deposited at 300 K sample temperature then only increased the mobility in the range expected from previous 300 K investigations.

4. Summary and conclusions

In extension of our previous work on *in situ* fabrication and characterization of silicon/silicon dioxide bottom-gate, gold bottom-contact pentacene transistors we prepared and analyzed devices on carbon covered and sputter-cleaned samples at three different surface temperatures during deposition of 200 K, 300 K and 350 K. Our unique sample setup allowed precise temperature control, as well as the repeated desorption of pentacene off the sample surface, enabling all of the coverage dependent mobility evaluations to be performed on only a single sample, ensuring maximum comparability of the obtained results. We were able to achieve conclusive insight into the primary parameters affecting the pentacene layer growth, namely the growth temperature during layer formation and the surface contamination through carbon residues. The newly acquired data supports the model of a gradual transition in growth mode and related transistor performance from 200 K to 350 K as well as from growth on carbon covered to sputter-cleaned samples. Electrical evaluations showed a rise in the maximum attainable mobility and an increase of the required layer thickness for the first percolation through sputtering for all temperatures, attributed to an increase in surface diffusion.

In combination with extensive AFM and threshold voltage analysis, we were able to show that in our setup the formation of the active layer and electrode contact is mainly governed by a surface temperature and treatment induced variation in the prevalent diffusion probability during the semiconductor deposition process. While a high diffusion probability increases the conductivity in the channel, due to a reduced number of grain boundaries and a better molecular ordering in the grains, increased dewetting in the contact–channel transition region counteracts this benefit.

With the acquired knowledge we designed a particular deposition sequence on a sputtered sample, featuring 4 ML of pentacene deposited at 350 K as the conducting layer within the channel with the most optimal charge transport properties, followed by a 4 ML capping layer deposited at 200 K sample temperature, ensuring optimal connection of the active

layer to the gold electrodes. The mixed layer configuration is stable at room temperature and the 200 K layer shows no dewetting in this temperature range. With this preparation method we were able to achieve a considerable increase in charge carrier mobility compared to all other single deposition temperature processes on sputtered samples.

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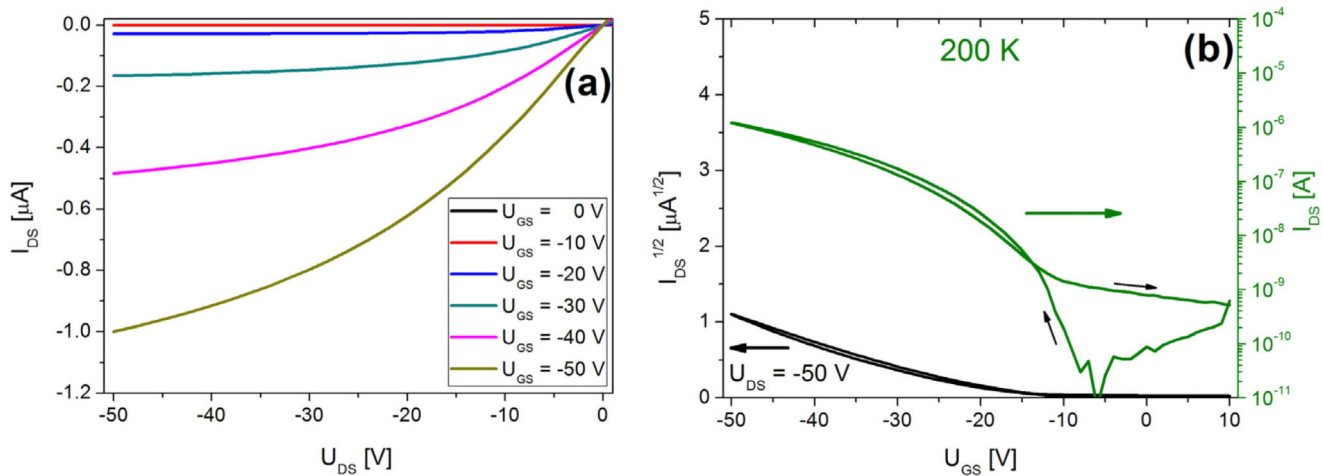


Fig. 1. Output (a) and transfer characteristics (b) of an 80 nm thick pentacene film on an Unspattered + C surface, deposited at 200 K and measured at 300 K sample temperature. Channel width and length are 4 mm and 25 μm , respectively.

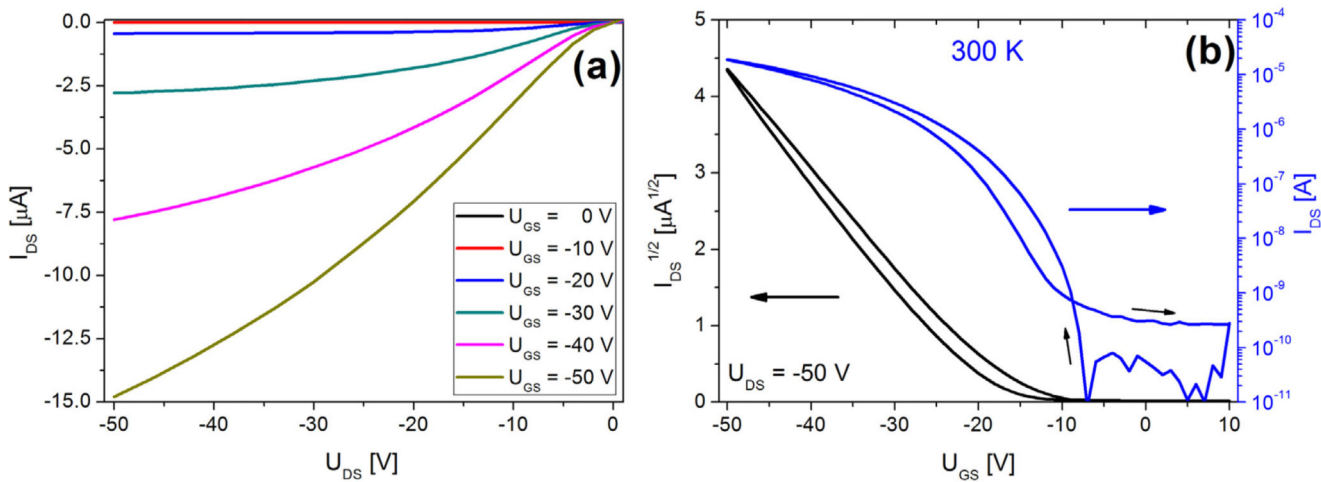


Fig. 2. Output (a) and transfer characteristics (b) of an 80 nm thick pentacene film on an Unspattered + C surface, deposited and measured at 300 K sample temperature. Channel width and length are 4 mm and 25 μm , respectively.

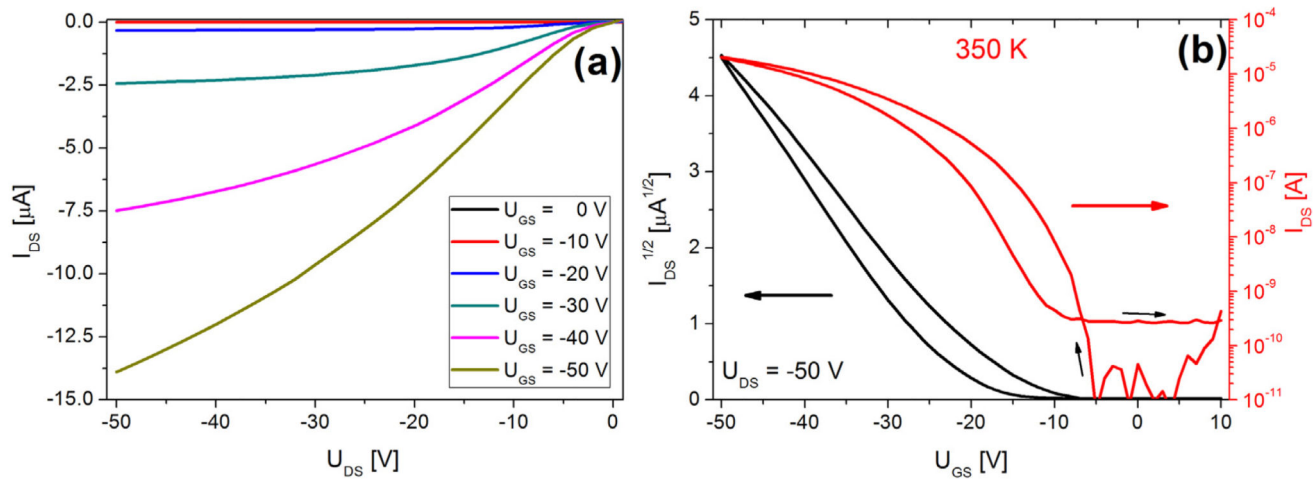


Fig. 3.

Output (a) and transfer characteristics (b) of a 144 nm thick pentacene film on an Unspattered + C surface, deposited at 350 K and measured at 300 K. Channel width and length are 4 mm and 25 μm , respectively.

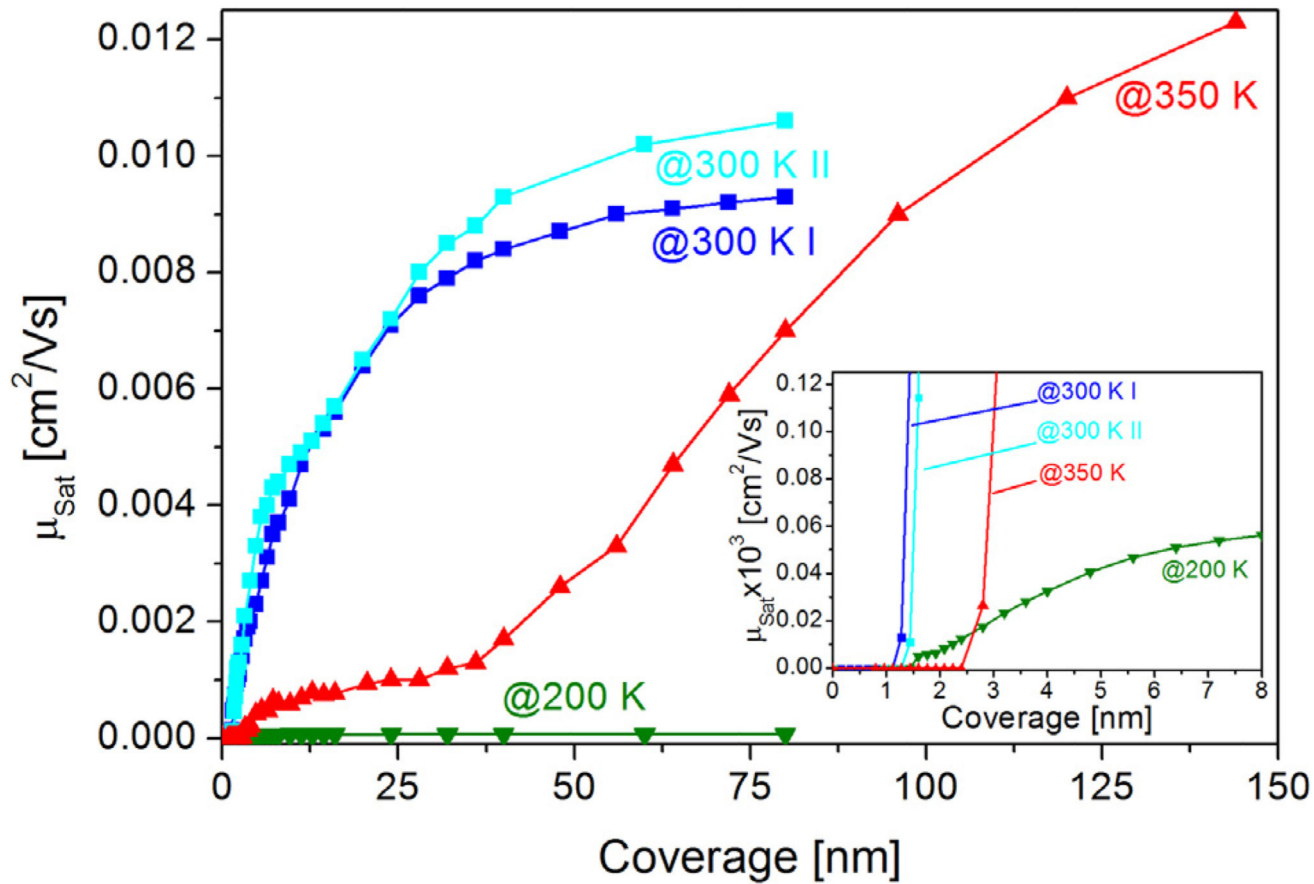


Fig. 4. Saturation mobility μ_{Sat} as a function of coverage for pentacene films on the Unspattered + C SiO_2 surface, prepared and measured at 200 K, 300 K and 350 K, respectively. The inset shows the onset of transistor behavior in the very low coverage regime.

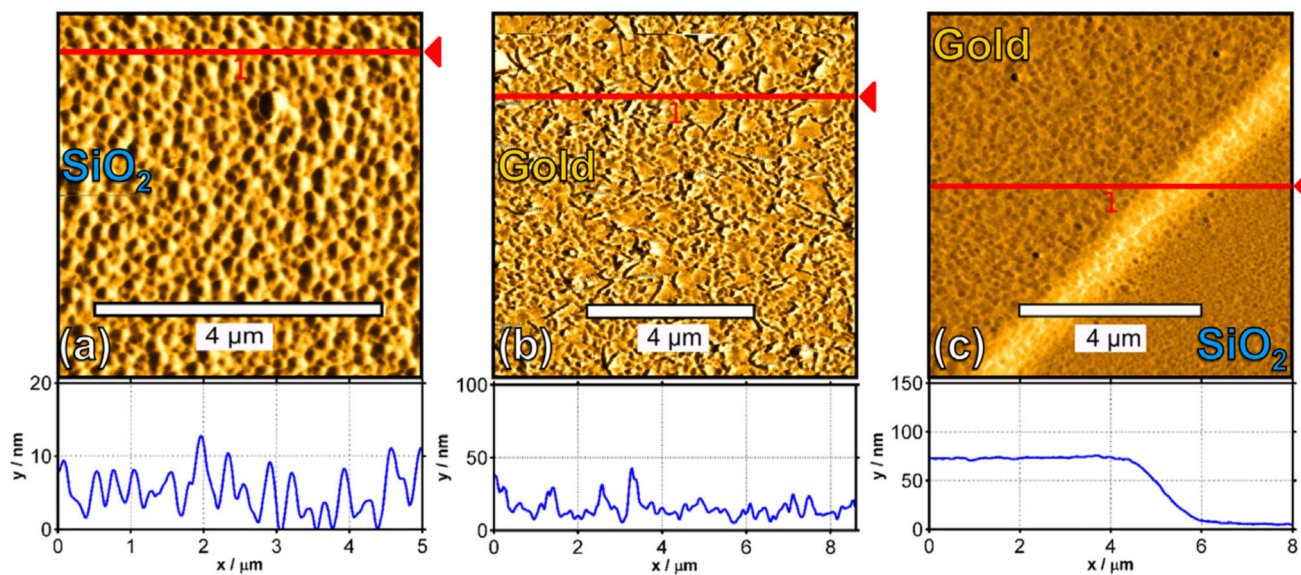


Fig. 5.

Pentacene deposited at 200 K: 1.5 monolayers on SiO₂ (a) and gold (b), as well as 7.5 monolayers on the gold contact–channel transition region (c). The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

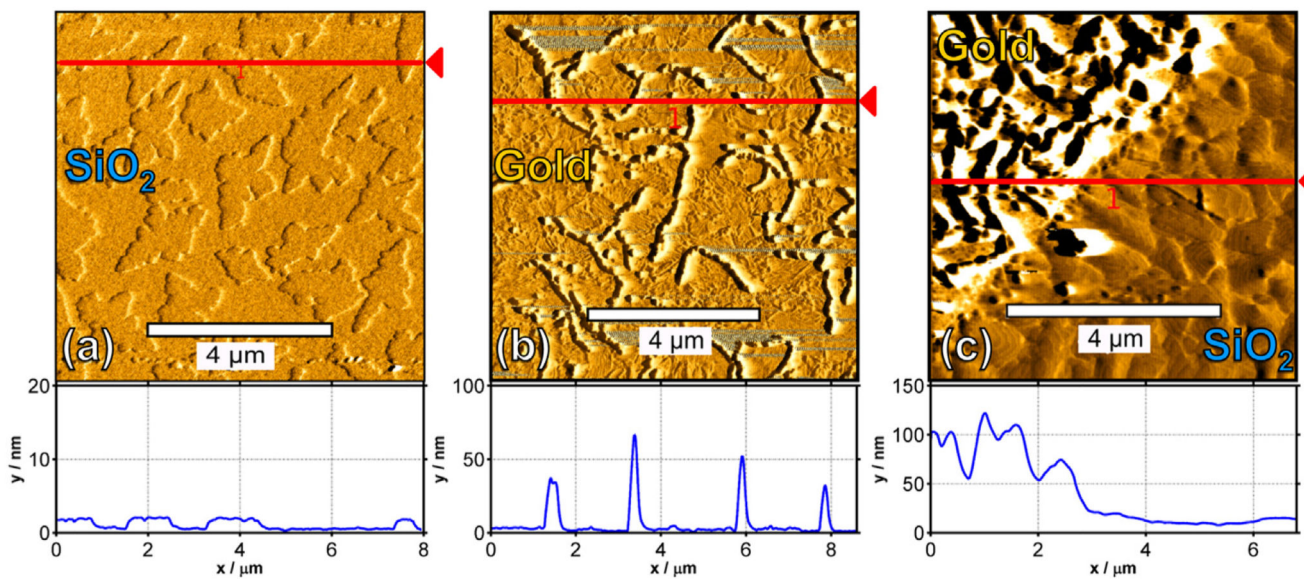


Fig. 6. Pentacene deposited at 300 K: 1.5 monolayers on SiO_2 (a) and gold (b), as well as 7.5 monolayers on the gold contact–channel transition region (c). The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

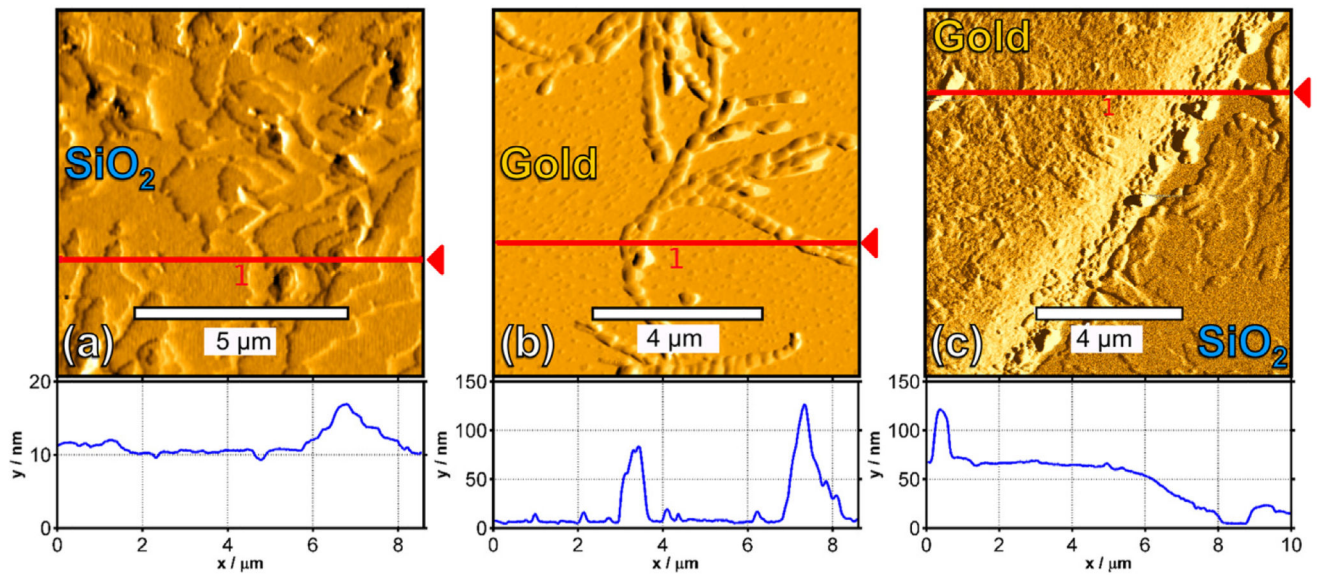
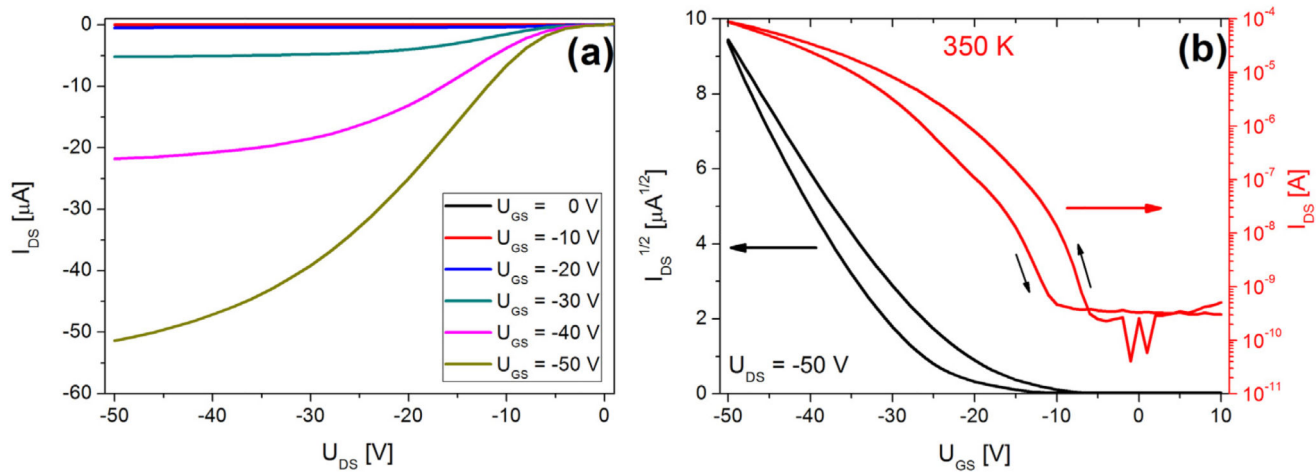


Fig. 7. Pentacene deposited at 350 K: 7.5 monolayers on SiO₂ (a), gold (b) and on the gold contact-channel transition region (c). The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

**Fig. 8.**

Output (a) and transfer characteristics (b) of a 96 nm thick pentacene film on a sputtered surface, deposited at 350 K and measured at 300 K sample temperature. Channel width and length are 4 mm and 25 μm , respectively.

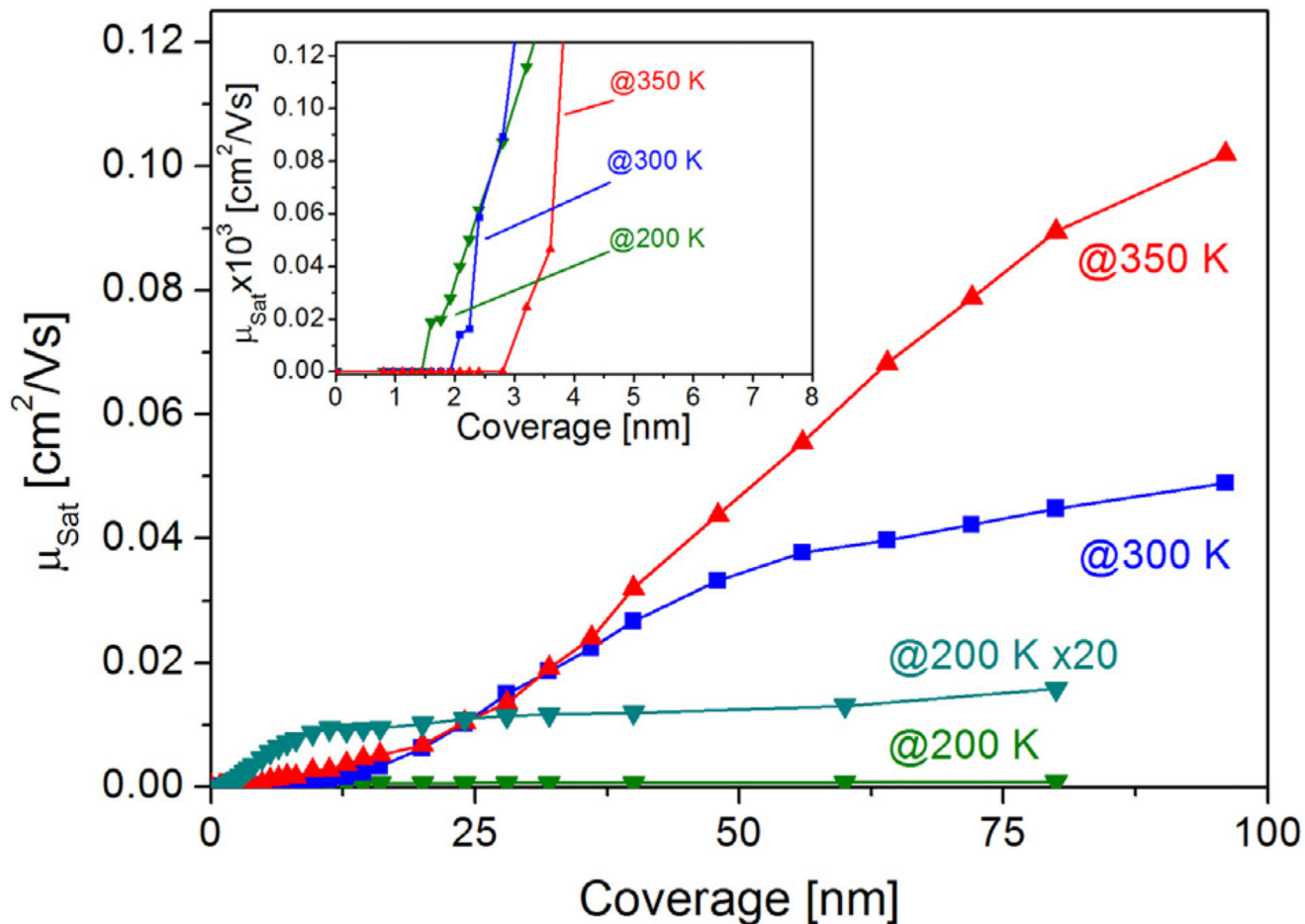


Fig. 9. Saturation mobility μ_{Sat} as function of coverage for pentacene films on a sputtered SiO_2 surface prepared and measured at 200 K (including 20 \times magnification), 300 K and 350 K, respectively. The inset shows the onset of transistor behavior in the very low coverage regime.

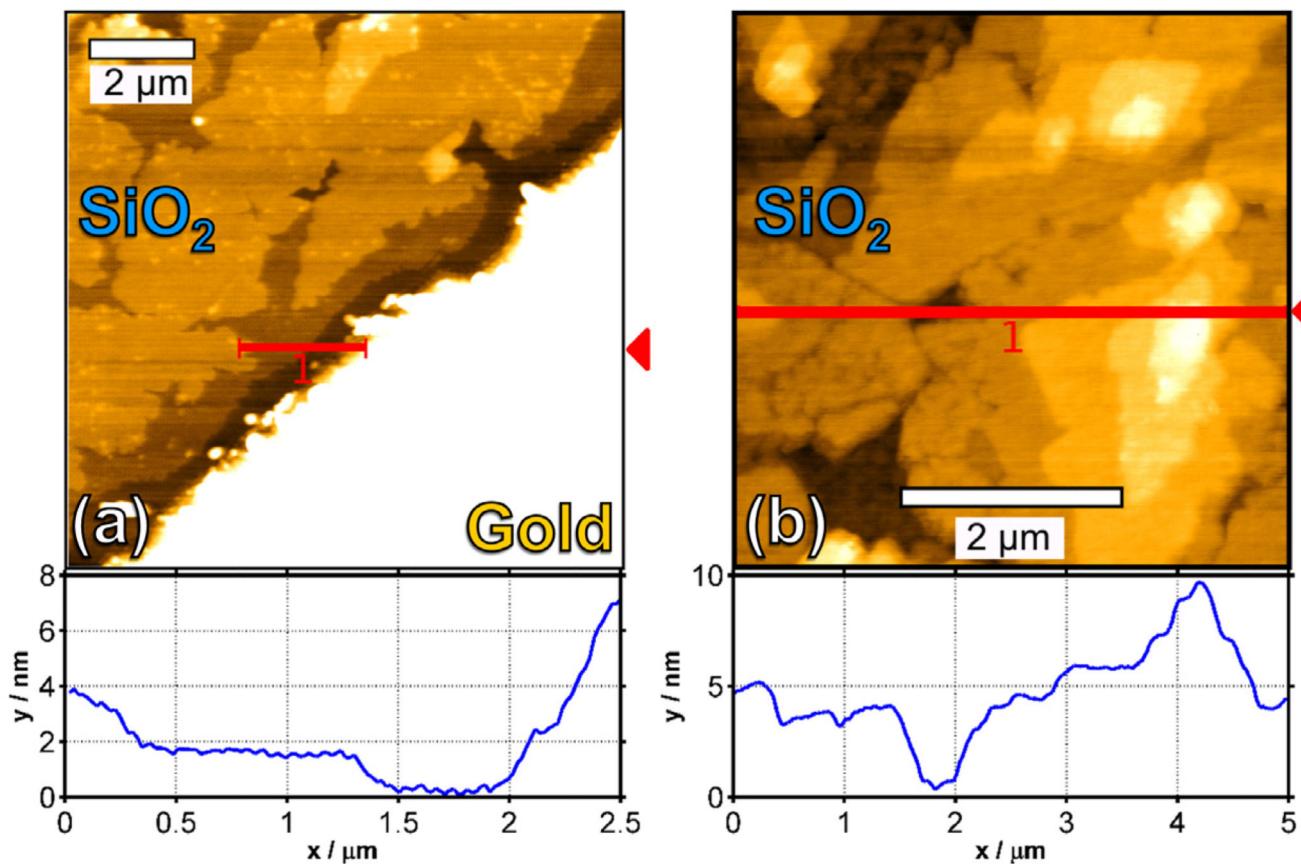


Fig. 10. 2.5 monolayers of pentacene on the gold contact–silicon dioxide channel transition region (a) and 7.5 monolayers of pentacene on SiO₂ (b), both deposited onto sputtered surfaces at a sample temperature of 350 K. The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

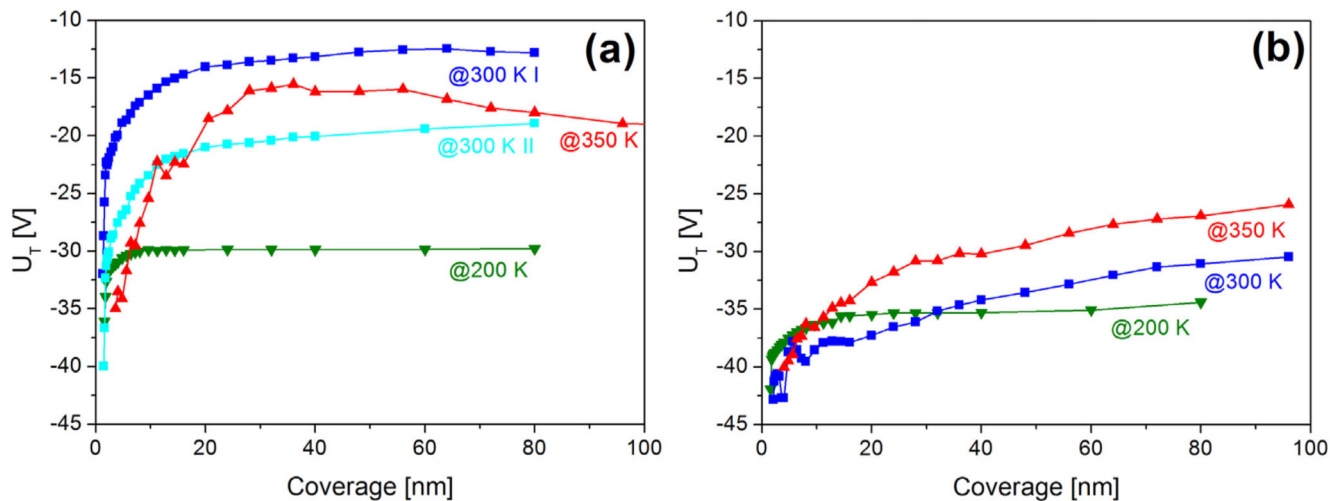


Fig. 11. Threshold voltage U_T as function of coverage for pentacene films on an Unspun + C (a) and a Sputtered (b) SiO_2 surface, prepared and measured at 200 K, 300 K and 350 K, respectively.

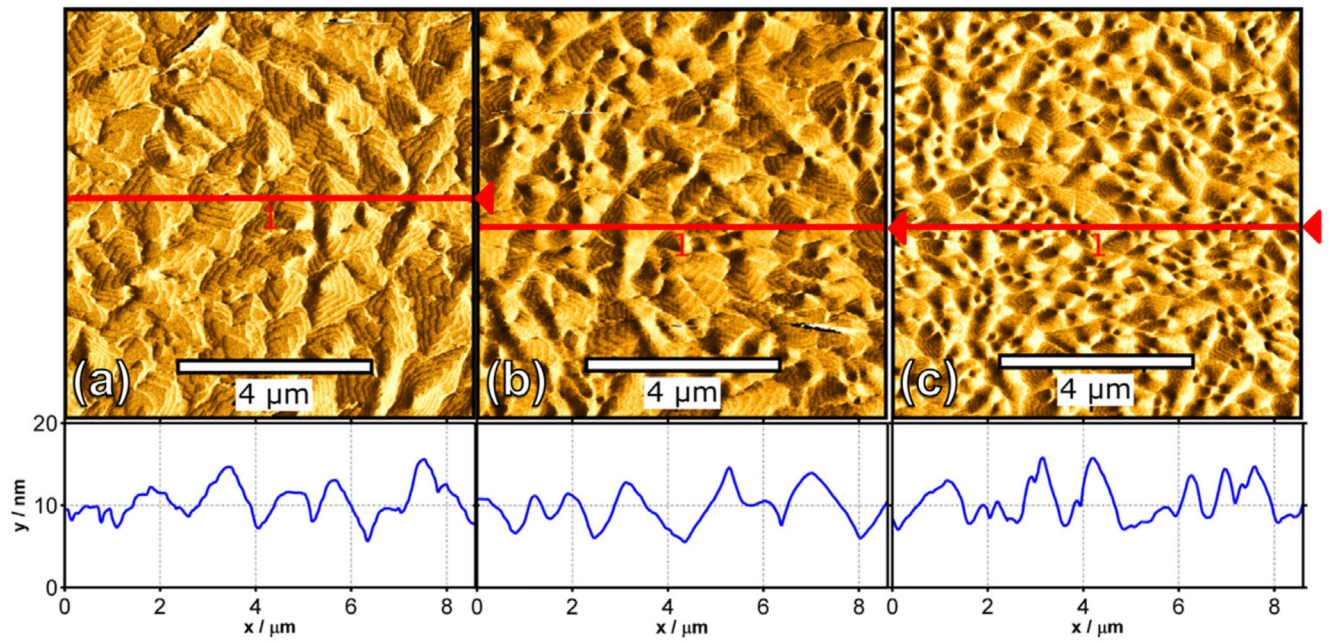


Fig. 12.
7.5 monolayers of pentacene on a sputtered (a), Sputtered + C (b) and Unspattered + C (c) SiO₂ sample, all deposited at 300 K surface temperature.

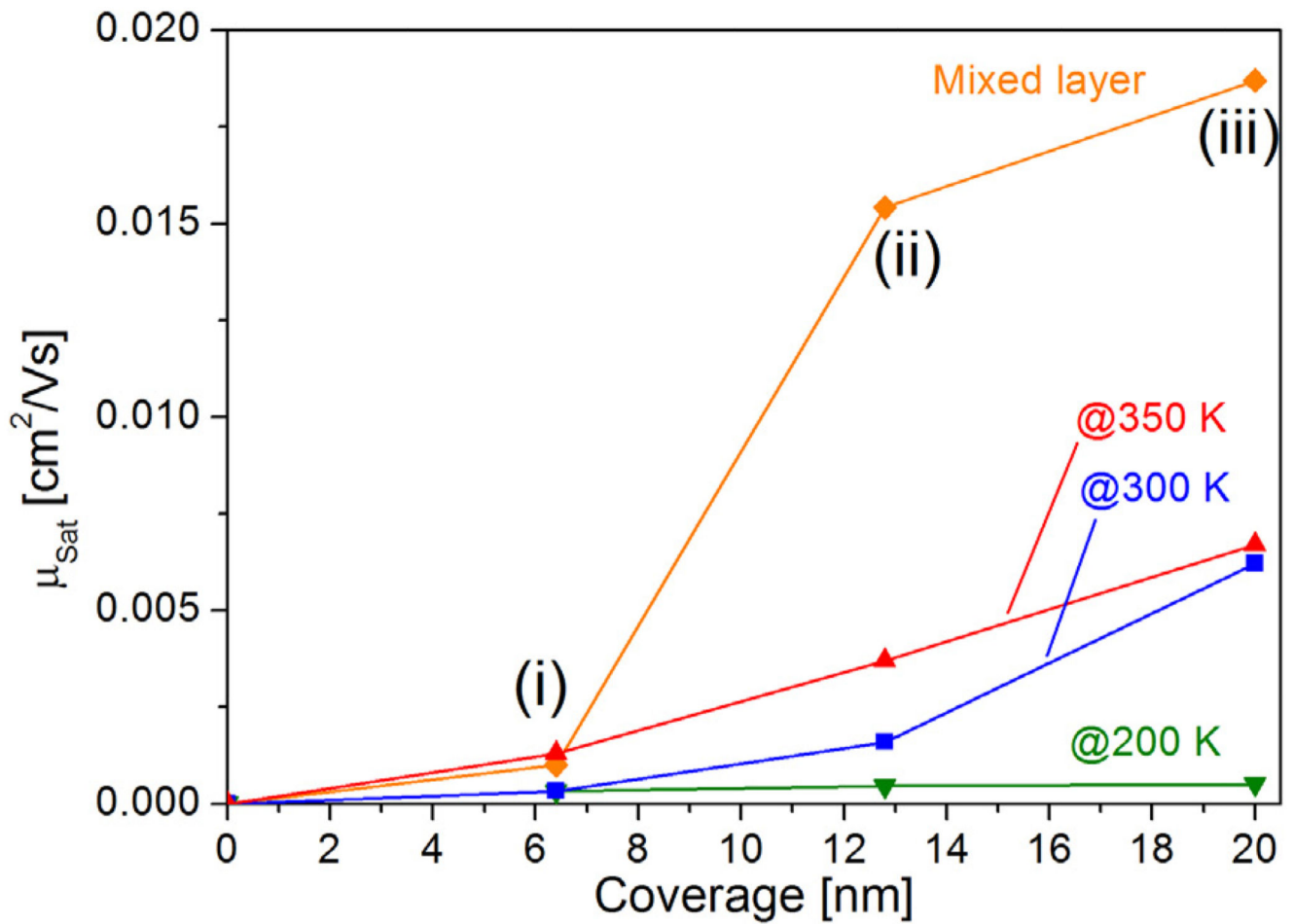


Fig. 13. Coverage dependent saturation mobility μ_{Sat} for 200 K, 300 K, 350 K and mixed temperature layers on a sputtered sample. The mixed layer represents 4 monolayers (6.4 nm) at 350 K (i), additional 4 monolayers at 200 K (ii) and finally 4.5 additional monolayers at 300 K (iii).