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Use of Ambipolar Dual-Gate Carbon Nanotube Field-Effect Transistor to Configure Exclusive-OR Gate

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Cite This: *ACS Omega* 2022, 7, 8819–8823

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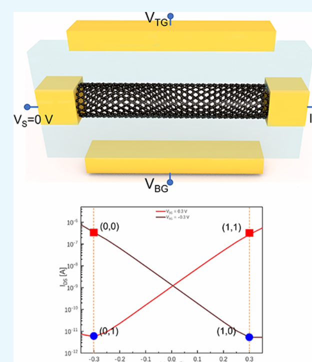
ABSTRACT: As the physical scaling limit of silicon-based integrated circuits is approached, new materials and device structures become necessary. The exclusive-OR (XOR) gate is a basic logic gate performed as a building block for digital adder and encrypted circuits. Here, we suggest that using the ambipolar property of carbon nanotubes and the threshold modulation ability of dual-gate field-effect transistors, an XOR gate can be constructed in only one transistor. For a traditional XOR gate, 4 to 6 transistors are needed, and this low-footprint topology could be employed in the future for hyperscaling and three-dimensional logic and memory transistor integration.



INTRODUCTION

It becomes increasingly difficult to overcome the physical limitations of traditional silicon-based transistors due to the so-called short channel effect,[1] which causes drain-induced barrier lowering, threshold voltage roll off, and charge sharing between the gate and drain as the transistor scales down. Aside from silicon channel materials, quicker top-of-the-barrier injection velocities and greater intrinsic carrier mobilities are required.[2] Carbon nanotubes (CNTs) are a promising candidate for the next generation of channel material in field-effect transistors (FETs) due to their faster performance, small transistor footprint,[3] and lower power consumption compared to that of Si.[4] A CNT field-effect transistor (CNTFET) is an ambipolar transistor because the major charge carrier can be switched between holes and electrons.[5] However, the ambipolar characteristic is frequently suppressed in current CNTFET-based designs for classic complementary metal-oxide-semiconductor (CMOS) design considerations.[6,7] The ambipolar feature of CNTFETs was given less concern for the design aspect. The exclusive-OR (XOR) gate is widely used in digital encryption[8] and is a basic building block of adders.[9,10] In a typical XOR circuit based on traditional FETs, there should be at least 4 or 6 FETs for various design purposes.[11] To create an XOR gate using a neural network, more than two layers are required.[12]

We show in this study that a two-input XOR gate can be implemented in just one dual-gate transistor using the ambipolar feature of CNTFETs. By applying a negative (positive) bias to the back gate, the threshold voltage of the top-gate FET shifts to the right (left), and the device's on/off state is transferred. Using the CNTFET's ambipolar characteristic, an XOR gate can be created.

RESULTS AND DISCUSSION

The ambipolar CNTFET can be understood by the band diagram structure. As schematically illustrated in Figure 1c,d, the negative (Figure 1c) and positive (Figure 1d) back-gate voltage biases, respectively, cause holes and electrons to accumulate in the channel.[5] Electric field programming can selectively and arbitrarily vary the major charge carriers in the CNT between holes and electrons.[5] Figure 1a,b shows the band diagrams of a back-gate CNTFET in negative back-gate bias and positive back-gate bias, respectively. As shown in Figure 1b, a Schottky barrier (SB) can be built in the source and drain connections. The energy difference between the Fermi level of the metal electrode and the position of the valence (p-type) or conduction (n-type) band edge of the CNT determines the SB height, which can be reduced by carefully selecting a metal with a suitable work function, such as scandium (Sc) for p-type and palladium (Pd) for n-type,[13] or by configuring bonding and wetting preparation.[14] Figure 1a

Received: December 15, 2021
Accepted: February 21, 2022
Published: March 2, 2022

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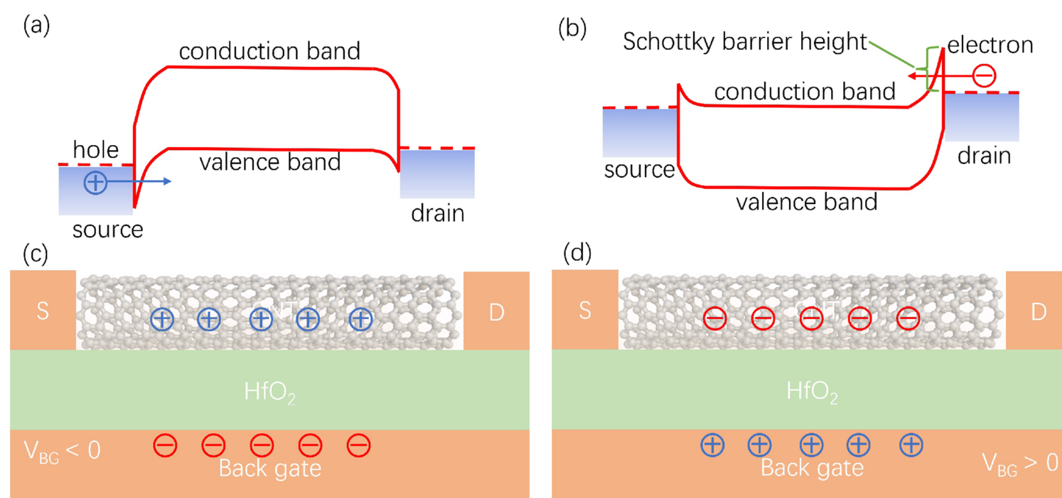

Figure 1. (a,b) Band diagrams of a back-gate CNTFET in negative back-gate bias and positive back-gate bias, respectively. (c,d) Illustration of the charge accumulation in the CNT channel induced by negative and positive back-gate bias, respectively.

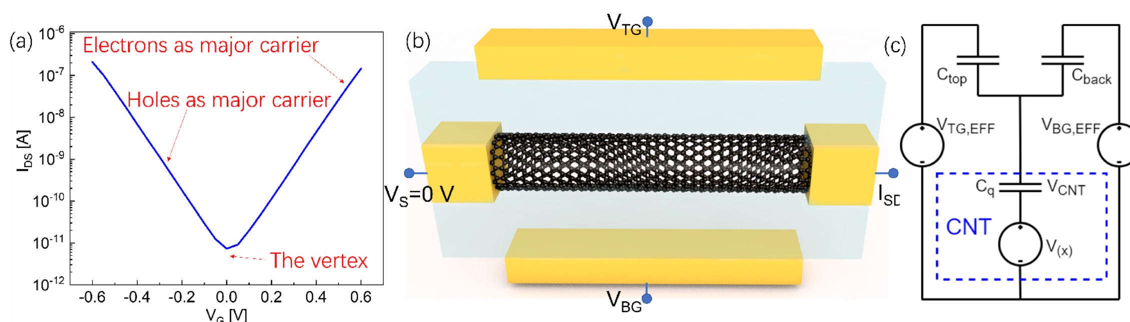

Figure 2. (a) Typical transfer curve of the ambipolar transistor. To the left of the vertex, the holes are the major carriers, and to the right of the vertex, the electrons are the major carrier. (b) Dual-gate CNTFET. From bottom to top are the back gate (bottom yellow block), the back-gate dielectric (bottom light blue block), the source/drain (left/right yellow block), the CNT channel, the top-gate dielectric (top light blue block), and the top gate (top yellow block). (c) Equivalent capacitive circuit of the dual-gate CNTFET.

shows how the conductance band and valence band of the CNT lifts for a negative back-gate bias, allowing holes to pass through the valence band of the CNT from the source to the drain. A positive back-gate bias lowers the conduction band and valence band of the CNT channel, as illustrated in Figure 1b, allowing electrons to travel from the drain to the source through the conduction band.

Figure 2a depicts the corresponding transfer curve, source–drain current (I_{DS}) against gate voltage (V_G), of the back-gate CNTFET, which has a distinct parabolic shape. The negative gate voltage induces holes in the CNT channel as the major carrier, corresponding to the left part of the curve. The lower the gate voltage, the higher the current, and at a particular gate voltage, the current is saturated. Similarly, a positive gate voltage induces electrons as the major carrier, as shown in the right part of the curve of Figure 2a.

For a dual-gate construction, as illustrated in Figure 2b, using a single CNT as the channel, the top gate is on the directly opposite side of the back gate. Because the n- or p-type behavior is determined by the back-gate bias, the dual-gate CNTFET allows for reconfiguration.[15] This indicates that the n- or p-type CNTFET can be obtained using a possible back gate and drain bias.

Channel Voltage. Figure 2c depicts an equivalent capacitive circuit[16,17] based on the dual-gate CNTFET, as illustrated in Figure 2b. C_{back} and C_{top} represent the capacitance of the back dielectric and the top-gate dielectric, respectively. The quantum capacitance (C_q) of the CNT channel must be considered as a series connection of the dielectric capacitance as the density of state (DOS) of the CNT channel is limited.[18] The corresponding low voltage in the CNT channel causes a variation in the Fermi level,[16] which is denoted by V_{CNT}. $V_{(x)}$ represents the channel's potential variation due to source–drain bias (V_{DS}), and it ranges from zero on the source side to V_{DS} on the drain side. $V_{BG,EFF}$ is the effective back-gate voltage, which takes into account any possible charged interface states at the CNT/dielectric interfaces, as well as deliberate or unintentional CNT doping, to determine the potential requirements for carrier densities in the CNT channel.[18] $V_{BG,EFF}$ can be calculated with the following equation:

$$V_{BG,EFF} = V_{BG} - V_{BG0} \quad (1)$$

where V_{BG0} is the back-gate voltage when the carrier density of the CNT is minimum for zero applied top-gate and drain–source voltages.[18] The same consideration can be used to determine the effect top-gate voltage, $V_{TG,EFF} = V_{TG} - V_{TG0}$. For the equivalent circuit depicted in Figure 2c, the following equation may be used to obtain Kirchhoff's relation:[18]

https://doi.org/10.1021/acsomega.1c07088
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$$V_{CNT} = [V_{TG,EFF} - V(x)]\frac{C_{top}}{C_{top} + C_{back} + \frac{1}{2}C_q} + [V_{BG,EFF} - V(x)]\frac{C_{back}}{C_{top} + C_{back} + \frac{1}{2}C_q} \quad (2)$$

The coefficient of 1/2 is because of C_q's unique reliance on V_{CNT}. We can suppose $C_{top} = C_{back} =$ Cto simplify the equation and produce a more symmetrical vertex shift, and then we have

$$V_{CNT} = \frac{[V_{TG,EFF} + V_{BG,EFF} - 2V_{(x)}]C}{2C + \frac{1}{2}C_q} = \frac{[V_{TG} + V_{BG} - 2V_{(x)} - V_{TG0} - V_{BG0}]C}{2C + \frac{1}{2}C_q} \quad (3)$$

We can infer that, when V_{BG} is increased by 1 V for the same V_{CNT}, V_{TG} should decrease by 1 V in response, and vice versa.

Source–Drain Current. The source–drain current equation can be derived by the Landauer formula:

$$I_{DS} = \frac{4e}{h}\int dE\cdot T(E)[f(E - E_{FS}) - f(E - E_{FD})] \quad (4)$$

which denotes the ideal contact ballistic transmission.[19] $T(E)$ is the source–drain transmission,[20] which can be deduced by the Schrödinger equation using the non-equilibrium Green's function.[21] The first term represents the electrons coming from the source (E_{FS}) filling up the $+k$ states, and the second term represents the electrons coming from the drain (E_{FD}) filling up the $-k$ states.[19] The source–drain bias (V_{DS}) is what causes the difference between E_{FS} (Fermi energy of the source) and E_{FD} (Fermi energy of the drain). After integrating all of the energy sub-bands, the I_{DS} can be written as[22]

$$I_{DS} = \frac{4ek_BT}{h}\sum_{p=1}^{+\infty}\left[\ln\left(1 + \exp\frac{-\Delta_p + V_{CNT}}{k_BT}\right) - \ln\left(1 + \exp\frac{-V_{DS} - \Delta_p + V_{CNT}}{k_BT}\right)\right] \quad (5)$$

where e is the electron's charge, k_B is the Boltzmann constant, h is the Planck constant, Δ_p is the pth energy sub-band, and T is the temperature.

We may deduce from the expressions of V_{CNT} (eq 3) and I_{DS} (eq 5) that when a given amount of back-gate bias is applied, the top gate must be applied in the opposite direction to produce the same kind of magnitude I_{DS}. This means the back-gate bias causes the contrary shift of the top-gate voltage for the same I_{DS}. A negative back voltage causes positive charges to be induced in the CNT channel adjacent to the back-gate dielectric, followed by negative charges being induced in the CNT channel adjacent to the top-gate dielectric. As a result, greater V_{TG} values are required for achieving channel charge inversion, leading to a positive shift of top-gate voltage in the vertex.

Simulation Results. The as-expounded top-gate voltage vertex shift caused by the back-gate bias phenomenon is then simulation by the CNTFET Lab[23] in the nanoHUB platform. A single carbon nanotube, with a (13,0) chirality and a 10 nm length, was chosen as the channel material for the dual-gate CNTFET with both top- and back-gate dielectrics of 10 nm thickness and with 20 F/m dielectric constants. A Newman boundary condition was used, which means that the contact is MOS-like. The source–drain voltage was fixed at 0.1 V. Figure 3a illustrates the source–drain current simulation results for

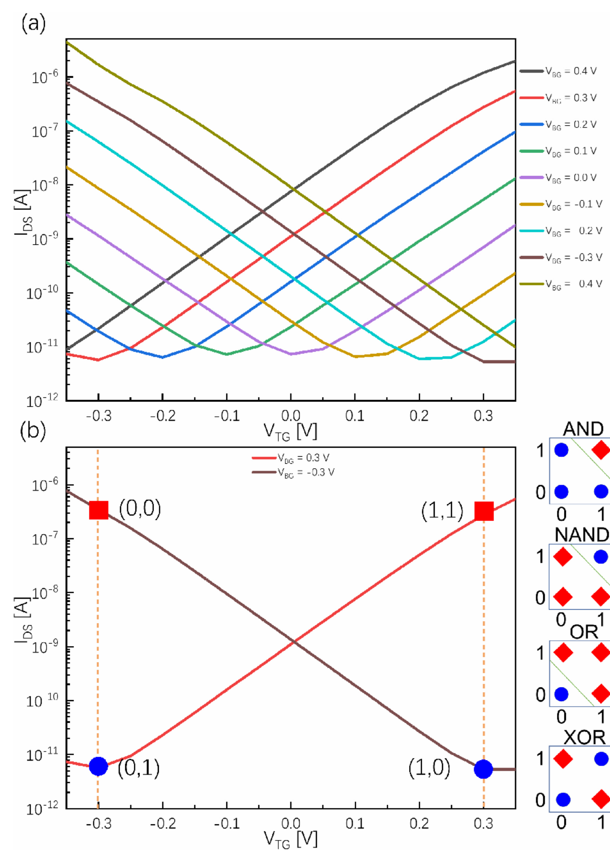
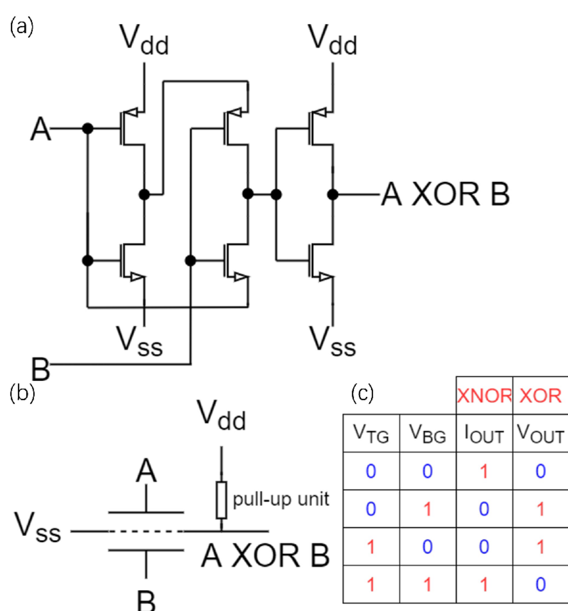


Figure 3. (a) Transfer curve of the top-gate device of the dual-gate CNTFET, showing the vertex of the curves' right shift with the decrease of the back-gate bias. (b) As-selected two transfer curves at the V_{BG} equal 0.3 and −0.3 V. The two blue circles and the two red squares represent the four selected XNOR gate work points.

top-gate voltage sweeps from −0.35 to 0.35 V in 0.5 V steps, with the back-gate bias shifting from −0.4 to 0.4 V in 0.1 V steps. When the back-gate bias is set to V_{BG} = 0 V, the vertex of the curve occurs around V_{TG} = 0 V. The vertex of the curve right shifts when negative back-gate bias (−0.4 to 0 V) is applied, and the more negative the bias, the righter the shifts occur. Similarly, by applying a positive back-gate bias, the vertex of the curve shifts left, and the higher positive the bias, the more left shifts occur. These simulation results are identified with the analysis above and from the results published by other authors.[24−26]

When the curves at the back-gate bias of V_{BG} = 0.3 V and V_{BG} = −0.3 V are selected, as shown in Figure 3b, an X-shaped structure is achieved. The top-gate voltage and back-gate voltage are set as the input single and the drain current as the output single. We define 0.3 and −0.3 V as the "1" and "0" for both the back gate and the top gate, as illustrated by the dashed line in Figure 3b. The output of the logic gate is false only when exactly one of its inputs is true, performing a typical XNOR gate property (Figure 4c). In real-world applications, the output current should be converted to voltage using a pull-up unit,[27] thus the XNOR gate is converted to an XOR gate (Figure 4c). The I_D–V_G curve of a dual-gate CNTFET can be moved considerably in practical applications by applying a specified source voltage V_S or appropriate doping to make the

https://doi.org/10.1021/acsomega.1c07088
ACS Omega 2022, 7, 8819−8823



		XNOR	XOR
V_{TG}	V_{BG}	I_{OUT}	V_{OUT}
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

Figure 4. (a) Traditional XOR gate constructed by six transistors (three PMOSs and three NMOSs). (b) Ambipolar dual-gate CNTFET using top-gate and back-gate voltage as inputs and drain voltage as output to construct XOR gate. (c) Truth table of (b).

output voltage capable of becoming the input of the logic gate in the following step. The XOR gate is then configured by just one dual-gate CNTFET. As depicted in the inset in Figure 3, different from AND, NAND, and OR gates whose output can be separated by a single line, the XOR gate cannot be divided by a single line,[28] and this property causes the first artificial intelligence (AI) winter.[29] Figure 4a depicts a traditional XOR gate constructed by three n-channel MOS (NMSO) transistors and three p-channel MOS (PMOS) transistors.[11] Figure 4b,c shows the XOR gate constructed by our ambipolar dual-gate CNTFET and the corresponding truth table, respectively. This low footprint structure may be used in the era of hyperscaling in the future[2] and for the three-dimensional (3D) integration of logic and memory transistors.[30] This device may have great utilization potentiality in encrypted circuits. In addition, this strategy can be used not only in CNTFET but also in all of the ambipolar transistors consisting of ambipolar channels (e.g., graphene, black phosphorus, WSe_2, $MoTe_2$) and even ambipolar tunneling FET (TFET).

In summary, we have shown the analysis and simulation results of the construction of a single transistor XOR gate using ambipolar dual-gate CNTFET. Using traditional FETs requires 4 to 6 transistors to build an XOR gate. We propose that an XOR gate can be built in only one transistor using the ambipolar property of carbon nanotubes and the threshold modulation ability of dual-gate field-effect transistors. In the encrypted circuit, this device may hold a lot of promise. Hyperscaling and 3D logic and memory transistor integration could also benefit from this low-footprint design in the future.

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https://pubs.acs.org/10.1021/acsomega.1c07088

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work was supported by the National Key Research and Development Program of China under Grant No.

https://doi.org/10.1021/acsomega.1c07088
ACS Omega 2022, 7, 8819−8823

2016YFA0201903, Research and Development Project in Key Fields of Guangdong Province under Grant No. 2020B010171001, as well as the Opening Project of Key Laboratory of Microelectronic Devices & Integrated Technology Institute of Microelectronics Chinese Academy of Sciences.

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