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Inverted Pyramid Morphology Control by Acid Modification and Application for PERC Solar Cells

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ABSTRACT: Silicon inverted pyramid (IP) structures, with lower reflectance and increased surface recombination, are one of the best choices for light-trapping structures of high-efficiency silicon solar cells. The solution process of IP generally goes through three main steps: porous silicon etched by metal-assisted chemical etching, acid etching, and alkali anisotropic etching. In this paper, the role that acid modification plays in IP preparation and the application of our optimized texture for passivated emitter and rear solar cells (PERC) were investigated. Experimental results show that acid plays a decisive role in optimizing and modifying the morphology of porous silicon; thus, the morphology of porous silicon has no direct influence on the morphology of IP. In addition, the opening size of IP is mainly determined by the size of silicon micron holes modified by the acid process. PC1D simulation results manifest that IPs can increase the short-circuit current density (J_{sc}) of devices by 1.04 mA/cm^2 and power conversion efficiency by 0.55%; hence, our optimized IP-based PERC achieve the highest simulative conversion efficiency of 23.21%. This is an effective and important way to manipulate the structure of IP, which points out the direction of fabrication and application of high-efficiency IP textures.
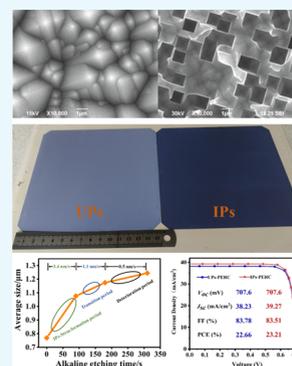
1. INTRODUCTION

Reducing cost and improving efficiency are still the goals of the photovoltaic industry. It is an effective way to develop novel micro-/nanostructured textures with excellent optical and electrical properties and compatible technology with the existing production lines.[1−8] Inverted pyramid (IP) texture, as a novel light-trapping structure, has attracted extensive research interest. Compared with the traditional upright pyramid (UP) texture, this novel structure can reduce the surface reflectivity of silicon wafers without increasing the surface recombination and thus has better photoelectric property.[6,9−15]

Back in 1999, Professor Green's group[16] fabricated IP structures (IP-Strus) by photolithography and applied them to passivated emitter with rear locally diffused cells, eventually achieving 25% power conversion efficiency (PCE) on an area of 4 cm^2. The relative complexity of lithography, however, is bad news for mass production. Recently, many researchers have reported an all-solution IP preparation process based on metal-assisted chemical etching (MACE). For example, Zhang et al.[17] have fabricated a 20.19% efficient 1 μm sized IP-textured device with a large area. Huang et al.[19] repared highly uniform IP-Strus on the front surface of industry-sized (156 × 156 mm^2) silicon wafers, and a passivated emitter-and-rear cell-based IPs-Strus with a conversion efficiency of 22.09% was obtained by Sunsolve software simulation. By optimizing the opening size (the side of IP opening square) of IP-Strus, Gao

et al.[19]inally prepared the IP-based passivated emitter and rear cells (PERCs) with a PCE of 21.4%. In these processes, the preparation methods of IP-Strus generally experienced the following three main steps: porous silicon etching, acid etching, and alkali anisotropic etching. Alkali anisotropic etching is considered to be the key step of forming IP-Strus, but the role of "acid" in the IP-Strus preparation process is not very clear, and there is also no article for detailed research.

In this paper, the role of acid process in the IP texture prepared by an all-solution process based on MACE and the influence of acid on the morphology of porous silicon and subsequent IP fabrication were studied. Subsequently, IP morphology was controlled by acid modification, and the application of our optimized texture for PERC solar cells was investigated by PC1D simulation software. The main conclusions are as follows: acid process plays a decisive role in optimizing and modifying the morphology of porous silicon, and the morphology of porous silicon has no direct influence on the morphology of IP; in the case of good uniformity and density of IP-Strus, the corresponding opening size is
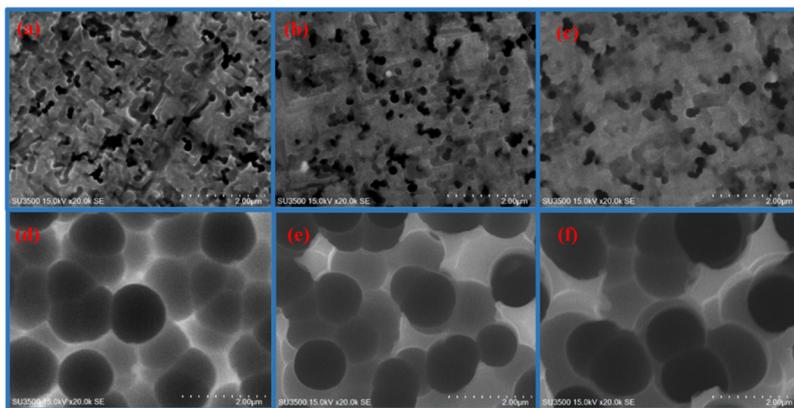
Figure 1. Porous silicon structures prepared by the MACE method for (a) 3 min; (b) 5 min; (c) 7 min; and silicon micron holes of (d) a, (e) b, and (f) c after HNO_3/HF etching for 2 min, respectively.

determined by the size of the silicon micron holes modified by the acid process. We have finally obtained optimized IP-Strus with relatively good uniformity and opening size of 1.076 μm. Subsequent PC1D simulation results show that PERC solar cells based on our optimized IPs (IP-PERC) exhibit 0.55% PCE higher than the PERC solar cell based on UPs from the production line (UP-PERC) due to the increase of short-circuit current density from 38.23 to 39.27 mA/cm^2, which is attributed to the light-trapping advantage of the optimized IP texture.

2. RESULTS AND DISCUSSION

2.1. Morphology Control. Figure 1 shows the porous silicon structures with different morphologies prepared by Ag-assisted chemical etching and their micron hole structures formed by acid modification. As can be seen from the diagram, the size, shape, density, and distribution of the holes in three groups of porous silicon structures in Figure 1a−c are completely different. Specifically, in Figure 1a, the circular holes with 100−200 nm in diameter and linear holes with a length of 300−500 nm dominated. In Figure 1b, circular holes with a diameter of 200−400 nm or overlapping circular holes are the main ones, and the density of the holes is also relatively high, while Figure 1c is covered by wormlike nanoholes of 300−500 nm in length, with lower density and more chaotic distribution. To our surprise, when these different porous silicon structures were etched by the HNO_3/HF mixed solution for 2 min, micron hole structures with a diameter of 0.769 μm and a relatively uniform distribution were obtained, which arises from the isotropic etching effect of the HNO_3/HF mixed solution on monocrystalline silicon. First, HNO_3, as an oxidizing agent, reacts with nanoporous silicon with a larger surface area to form SiO_2 and then HF as a complexing agent reacts with SiO_2 to form soluble $SiHF_6$. As the reaction progresses, some of the tiny nanostructures are completely corroded, and the nanoporous silicon gradually grows into micron structures. By controlling the reaction time, we can obtain the microhole structure with uniform size distribution. This shows how acid "modifies" nanoporous silicon.

2.2. Size Control. Figure 2 shows the SEM images of the silicon hole structure prepared by acid treatment for 1 min 35 s and IP-Strus fabricated by alkali etching for three different times, 1 min 30 s/3 min/5 min 10 s. The morphology in Figure 2b is our optimized IP texture. According to our statistical analysis, the average opening size of silicon holes is
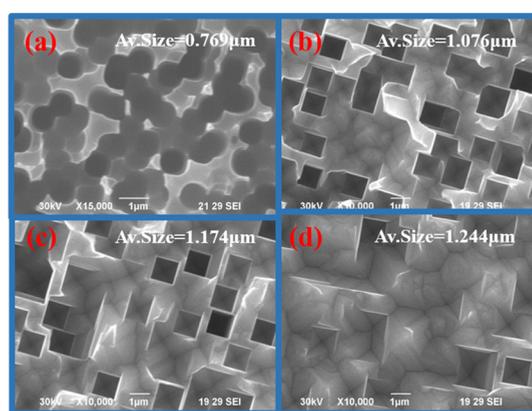
Figure 2. (a) SEM image of a typical silicon microhole structure obtained by acid modification of porous silicon and IP-Strus formed after alkali etching of silicon micron holes for three different periods of (b) 1 min 30 s; (c) 3 min; and (d) 5 min 10 s.

0.769 μm, while the average open size of IP after alkali etching for 1 min 30 s, 3 min, and 5 min 10 s is 1.076, 1.174, and 1.244 μm, respectively. Figure 3 shows the change curve of the
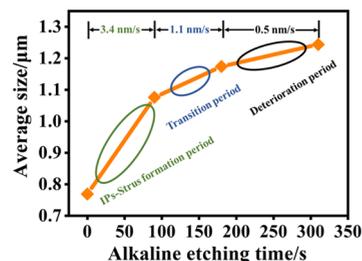
**Figure 3.** Average opening size of IP as a function of alkali etching time.

average opening size of silicon holes and IP-Strus with the alkali etching time. It can be seen from the above two figures that on the one hand, the opening rate was very fast, with the average opening rate reaching 3.4 nm/s in the early 90 s of the reaction. The opening size of the nanostructure grew from 0.769 to 1.076 μm. This period is considered as the "IP-Strus formation period". From 1 min 30 s to 3 min, the opening rate slows down, the average opening rate decreases to 1.1 nm/s, the opening size of IP-Strus increases from 1.076 to 1.174 μm,

and the etching process changes from the "IP-Strus formation period" to the "transition period". However, from 3 min to 5 min 10 s, the etching becomes slow, the average opening rate further reduces to 0.5 nm/s, and the IP opening size only increases by 70 nm. In this stage, the IP-Strus collapses and overlaps in a large area, UPs begin to appear, and the etching process enters the "deterioration period". On the other hand, during the IP-Strus formation period, the silicon holes become uniform and orderly IP-Strus under the action of anisotropic etching of the alkali. When the etching process reaches the "transition period", the size of the IP continues to increase slowly, but remains around 1.1 μm, which is the optimal size of the IP corresponding to the size of our silicon hole, and the density and uniformity do not change significantly. When the "deterioration period" is reached, the IP-Strus collapsed and overlapped, and the uniformity and density also deteriorated sharply. The above two phenomena indicate that the change of the opening size of IP-Strus mainly takes place in the "IP-Strus formation period", while the change of density and uniformity mainly takes place in the "deterioration period"; so, the "transition period" is the best period to obtain uniform and orderly IP-Strus.

Based on the morphology analysis, we know that once the micron holes are prepared, the subsequent alkali (IP) etching time will be determined if we want to obtain IP-Strus with good uniformity and density. When the alkali (IP) etching time is short, the IP-Strus will not be fully formed on the surface of the Si wafer; while the alkali etching time is long, the micron holes will be overetched, and the as-prepared IP-Strus start to collapse. This means that we can control the silicon hole size through optimizing the acid modification process to obtain IP-Strus with different target opening sizes and excellent uniformity and density, which shows that the acid process plays an important role in the IP texture preparation by the all-solution process based on metal-assisted chemical etching, and it is an effective and important IP-Strus size control measure. This points out the direction of high-performance IP texture preparation technology, and it injects new vitality into the development of high-efficiency solar cells.

2.3. Application in Devices. Figure 4a shows the appearance of the silicon UP on the production line and our optimized IP-based monocrystalline silicon wafers. The photo shows that the IP texture is darker than the upright one, so it will have a better light-trapping performance. Figure 4d shows the broad-band reflectance and further confirms the point, we can see from the diagram, that the reflectivity of the IP texture is lower than the normal pyramid suede, almost in the range of 300−1100 nm. Figure 4b,c shows the SEM microstructure of both; the opening size of the optimized IP was 1.1 μm, and the size of the UP was about 3 μm. The optical properties of devices with IP texture can be predicted in a more excellent way, which will eventually bring the improvement of the device short-circuit current and PCE.

In order to demonstrate the application potential of our optimized IP texture in solar cell devices, PC1D software was used to simulate the device output performance of IP-PERC solar cells and make a comparison with the traditional UP-PERC. In the simulation process, the front external reflectance of IP/UP is obtained from the experiment, wherein the reflectance spectra of IP-PERC were measured from our optimizing IP texture (Figure 4c) and UP texture (Figure 4b) from the production line. The surface recombination rates of IP/UP are calculated, respectively, according to our previous
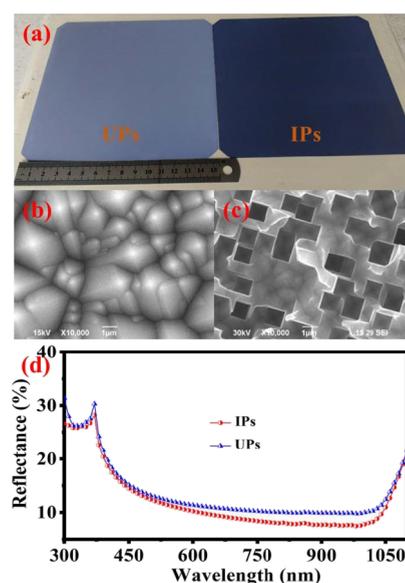

Figure 4. (a) Images of UP- (left) and IP- (right) based silicon wafer; (b) SEM images of UP texture; (c) SEM images of IP texture; (d) reflection of UP texture and IP texture at 300−1100 nm bands.

study results.[18] Some other input parameters are set based on the existing level of the PERC production line, and detailed simulation parameter settings are listed in Table 1.

Table 1. Parameter Settings of IP-PERC/UP-PERC by PC1D Software

parameters setting	value
front external reflectance	obtained from experiments
device area	244.33 cm^2
surface texture	UPs/IPs
base contact	1.5×10^{-6} Ω
internal conductor	3×10^{-5} S
internal diode	3×10^{-12} A
internal diode	3×10^{-8} A
rear-surface Al$_2$O$_3$	2 nm
rear-surface SiN$_x$	125 nm
device thickness	180 μm
P-type background doping	1×10^{16} cm^{-3}
emitter doping level	8.192×10^{18} cm^{-3}
front diffusion depth	0.5 μm
bulk recombination	1200 μs
front-surface recombination	475 cm/s(UPs), 561 cm/s(IPs)
rear-surface recombination	10 cm/s

The light J−V curves, other performance output parameters, external quantum efficiency (EQE) curves, and the reflectance spectra of IP-PERC and UP-PERC are shown in Figure 5. Note that the reflectance spectrum here is that we obtained from the experiment. We can see that the UP-PERC exhibits low values of short-circuit current density (J_{sc}) (38.23 mA/cm^2) and open-circuit voltage (V_{oc}) (707.6 mV); hence, a relatively low PCE of 22.66%. If we replace the UPs with IPs, J_{sc} is improved significantly, from 38.23 to 39.27 mA/cm^2, while V_{oc} and fill factor (FF) are almost not affected, which finally contributes to the improvement of PCE (from 22.66 to 23.21%). A significant increase of J_{sc} can be attributed to the optimization of our optimized IP-Strus with better light-trapping performance compared to UP-Strus; meanwhile, the
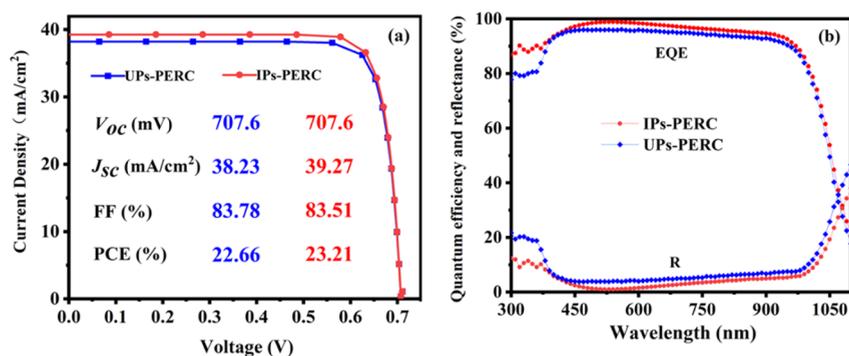
Figure 5. (a) Comparison of the device output performance based on IP texture and traditional UP texture: $I-V$ curve and output parameters; (b) reflectance and external quantum efficiency.

IP texture can convert optical gain into electrical advantage because, as previously reported by Huang,[18] it has almost the same surface area (1.74 times that of a planar sample) as the UP texture, and thus, both have identical level carrier recombination loss.[18] At the same time, as shown in Figure 5b, the EQE of IP-PERC has been significantly improved thanks to the lower reflectance of the IP texture in the wavelength range of 300−1100 nm. These indicate that our IP texture is a novel light-trapping structure with excellent photoelectric properties, and our research results point out a clear direction for the size and shape control of IPs, making the IP texture a closer step from the laboratory to industrialization.

4. CONCLUSIONS

This paper has experimentally investigated the role of acid in the IP texture prepared by solution process based on MACE and IP morphology optimization by acid modification, as well as the application of our optimized texture for PERC solar cells by PC1D modeling. Experimental results show that acid has a modification effect on the morphology of porous silicon and can transform the disordered porous silicon structure into silicon holes with uniform size and distribution, which widens the process window of MACE and is conducive to the preparation of high-quality IP-Strus. At the same time, the size of silicon holes modified by the acid process determines the opening size of the IP-Strus in the IP texture with optimal density and uniformity. For the optimization of the opening size of the IP-Strus, we should start with the acid. In addition, IP-PERC with an efficiency of up to simulative 23.21% has been achieved in PC1D with the application of optimized IP due to its optical advantage, which is superior to 22.66% of UP-PERC. This work points out the direction for the optimization of the IP preparation process and injects new vitality into the development of high-efficiency solar cells.

EXPERIMENTAL SECTION

Commercial 180 μm thick 156 mm × 156 mm (100)-oriented monocrystalline silicon, boron-doped (1−3 Ω·cm) p-type wafers were used as substrates. After the standard cleaning process, IP textures were prepared on the surface of Si wafers as follows: ①The cleaned Si wafers were immersed in the mixed solutions of $AgNO_3$(0.0001 M)/HF (4 M)/H_2O_2 (1 M) for 300 s, resulting in porous Si. ②Si wafers with porous Si were etched in an HNO_3/H_2O = 1:1 (volume) solution for 600 s to remove the residual Ag nanoparticles. ③The wafers with porous Si were modified in an $HNO_3/H_2O/HF$ = 4:2:1 (volume) solution to prepare silicon holes. ④IP texture was

fabricated on the surface of Si wafer by anisotropic etching of 80 °C−NaOH solutions.

The morphologies and structures of the samples were characterized with a JEOL JSM-6390LA scanning electron microscope. The reflectance spectrum was measured on the platform of quantum efficiency measurement (Crown Tech IVTest Station 1000ADX).

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Notes

The authors declare no competing financial interest.

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