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Research Article

Edge-Contact MoS_2 Transistors Fabricated Using Thermal Scanning Probe Lithography

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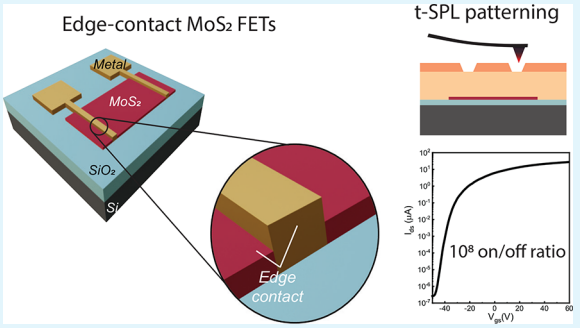
ABSTRACT: The science and engineering of two-dimensional materials (2DMs), in particular, of 2D semiconductors, is advancing at a thriving pace. It is well known that these delicate few-atoms thick materials can be damaged during the processing toward their integration into final devices. Thermal scanning probe lithography (t-SPL) is a gentle alternative to the typically used electron beam lithography to fabricate these devices avoiding the use of electrons, which are well known to deteriorate the 2DMs' properties. Here, t-SPL is used for the fabrication of MoS_2-based field effect transistors (FETs). In particular, the use of t-SPL is demonstrated for the first time for the fabrication of edge-contact MoS_2 FETs, combining the hot-tip patterning and Ar^+ milling to etch the 2DM. To avoid contamination of the contact interface by atmospheric gas molecules, etching and metal deposition are performed without breaking the vacuum conditions in between. With this process, edge-contact MoS_2 FETs are successfully fabricated and characterized. On/off ratios up to 10^8 and 10^9 are obtained at room temperature in air and vacuum, respectively, i.e., comparable with the best values reported in the literature.



KEYWORDS: *2D materials, TMDCs, MoS_2, FET, edge contact, lithography, thermal scanning probe*

INTRODUCTION

Two-dimensional materials (2DMs) have emerged as potential candidates for future electronic and optoelectronic devices. Not only their ultrathin nature but also the possibility of tuning their properties by, for example, modifying the dimensionality[1,2] or by applying strain,[3,4] have put 2DMs in the spotlight. As compared to silicon technologies, transition metal dichalcogenides (TMDCs) overcome short-channel effects even in multilayered devices[5] which makes them good candidates for miniaturization of low-power electronics. However, 2DMs are also extremely delicate, and their properties can be significantly affected by chemical and physical fabrication processes. Conventional lithography methods like UV photolithography and electron beam lithography (EBL) have been shown to produce detrimental effects in 2DM devices.[6,7] In particular, it has been reported that UV radiation can affect the interface between graphene and SiO_2, induce hysteresis in the electronic characteristics, and reduce the charge carriers' mobility.[7] Electron and ion radiation can result in local band-gap modification, nanoscale domain formation, and vacancy creation.[6,8] The exposure to ion beams, even for short times at relatively low energies, can cause serious alterations to 2DMs that are reflected as a decreased photoluminescence.[8] Besides, it has been reported that both PMMA and photoresist leave residues that also deteriorate the device performance.[9,10] It is clear that this effect is more relevant in the case of top-contact devices. However, when EBL is used, the incoming electrons interact along their path, resulting in forward scattering and secondary electrons. This results in an interaction volume that goes beyond the desired aperture, causing the well-known proximity effects of EBL. For the same reason, the scattered electrons and secondary electrons generated could affect the 2DM located close to the patterned areas (with an extension of a few nanometers). Hence, for miniaturized devices, not only the contacts but also a significant part of the channel could be affected.

Another recurring challenge in the fabrication of 2DM devices is their contact to metals. The characteristic Schottky barrier appearing at the junction between 2DMs and metallic contacts remains a limiting factor in the performance of 2DM-based electronic devices.[11−13] There are two main configurations to contact metallic electrodes to 2DMs (Figure 1a): top contact, in which the metal is deposited on top of the 2DM uppermost layer (basal plane), and edge contact, when the metal contacts every layer of the 2DM through the side (edge plane). When 2DMs are exposed to air, molecules such as

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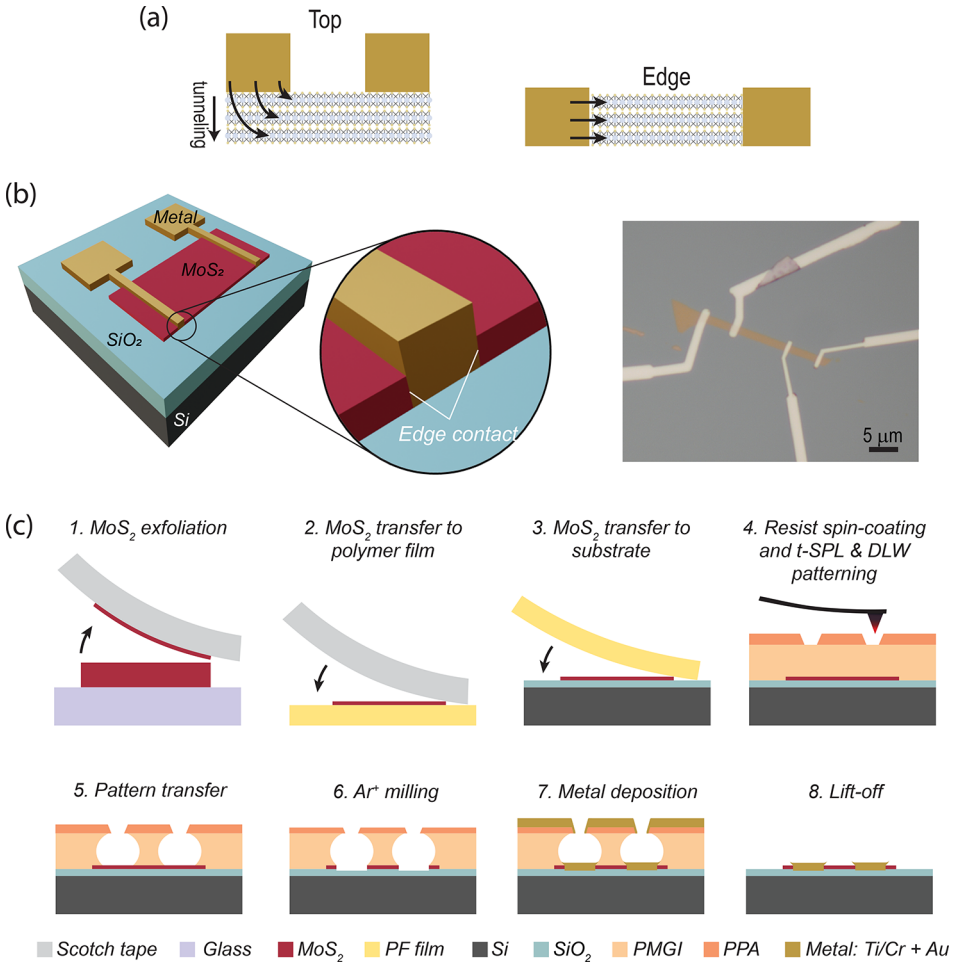

Figure 1. (a) Schematic illustration of current injection in metal–MoS_2 structure. (i) In the top-contact mode, the electrode only contacts the topmost layer of the MoS_2 channel and the current has to tunnel to reach deeper layers. (ii) In the edge-contact mode, the current can be injected directly from the metal electrode to all layers of the MoS_2 channel. (b) Illustration of an edge-contact device (left), and optical microscope image of a fabricated device (right). (c) Process flow for the fabrication of edge-contact FET: (1) bulk MoS_2 is exfoliated using scotch tape, (2) exfoliated MoS_2 is transferred to polymer films and inspected under the optical microscope to look for thin flakes, (3) desired flakes are transferred to the Si–SiO_2 substrate, (4) bilayer stack of PPA and PMGI is spin coated and t-SPL and DLW are used to pattern the device, (5) diluted TMAH is used to transfer the pattern to the substrate, (6) Ar^+ milling is used to etch the MoS_2, (7) metal for the electrodes is deposited using electron beam-induced PVD, (8) lift-off is performed using Remover 1165.

water or hydrocarbons adhere to the surface, forming layers with a thickness that can be of the same order of the 2DM itself.[14] As a consequence, in the case of top-contact devices, these molecules directly affect the 2D semiconductor–metal interface and could result in Fermi level pinning and increased contact resistance.[11] Besides, 2DMs have a large conductivity anisotropy between the in- and out-of-plane directions. This means that, in multilayer devices, when a top-contact configuration is used, each interface between two layers acts as a tunneling barrier,[15] decreasing the final performance of top-contacted devices, while in the case of edge contact, every single layer is contacted. The lack of reactivity of the basal planes in 2DMs also complicates an efficient bonding to the metal electrode in top-contact configuration. Density functional theory (DFT) calculations for graphene have shown that the shorter bonding distance in edge-contacted devices reduces significantly the contact resistance.[16] Although top contacts are easier to fabricate, the current flow on these devices depends on the contact area. Hence, for the miniaturization of the devices to length scales where Si suffers from short-channel effects, edge contacts would be beneficial.[14]

Many studies have focused on TMDCs[17] and, in particular, on MoS_2, a 2DM with a direct band gap for a monolayer and decent charge-carrier mobility, mechanical flexibility, and optical transparency, making it a good candidate for flexible devices,[18] low-power electronics,[19] photodetectors,[20] and gas sensing.[21] Here, we report on the fabrication of edge-contacted MoS_2 field effect transistors (FETs) where the lithography is performed by a combination of thermal scanning probe lithography (t-SPL) and direct laser writing (DLW) to avoid the exposure of the 2DM channel to energetic charged particles (ions and electrons) and UV radiation (see Supporting Information, section S1). As already proven in earlier work,[4,22] t-SPL is well suited for these delicate materials: free from UV radiation or electrons, t-SPL uses a heated tip to locally create patterns reaching a resolution better than 10 nm.[23] Typically, polyphthalaldehyde (PPA) is used as resist, as it thermally decomposes into volatile monomers above 150 °C.[24] A direct laser write add-on incorporated within the t-SPL tool allows for a seamless combination of both micro- and nanopatterning processes to increase the patterning throughput. This method overcomes the problems of the other

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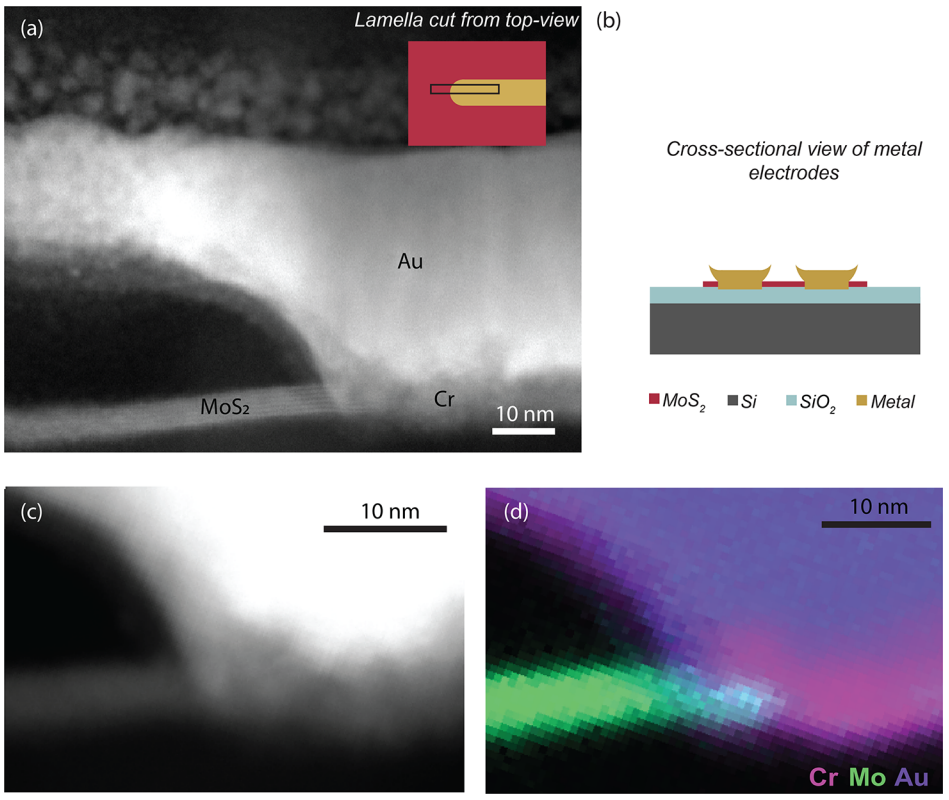

Figure 2. (a) TEM cross-sectional view of an edge contact with the inset showing a sketch of the lamella cut. (b) Cross-sectional scheme of the metal electrodes after metal deposition and lift-off illustrating the "ears" that are formed due to the angled evaporation. (c) STEM HAADF imaging and (d) EDX map from the contact region imaged in c showing the edge contact.

approaches by substituting electrons, ions, and photons for patterning with a hot tip where only the upper part of the resist is exposed to heat[9] and using the laser for the large pads located far away from the 2DM. Moreover, to avoid possible atmospheric contamination of the contacts, the etching of the 2DM and deposition of metallic contacts are performed in the same process chamber without breaking the vacuum.

Following this approach, we demonstrate the fabrication of top- and edge-contact MoS_2 FETs with a global silicon back gate (Figure 1b) and study systematically the performance of 29 devices. We show that the best performance is achieved with edge-contacted few-layer (FL) MoS_2 FETs, reaching a mobility of 38 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 1×10^8 (air)/1×10^9 (vacuum), while for monolayer (1L) devices, the highest achieved mobility is 7 $cm^2\ V^{-1}\ s^{-1}$ and the best on/off ratio is 7×10^7, also with edge-contact configuration. Besides, thanks to the freshly created edge surfaces on MoS_2, edge-contact FETs, both 1L and FL devices, show, in general, better electrical performance (higher mobility, higher on-state current, and lower contact resistance) than similar top-contacted devices.

RESULTS AND DISCUSSION

Fabrication Process. In the following, the fabrication process of edge-contact MoS_2 shown in Figure 1c will be discussed (see Experimental Section for further information). MoS_2 flakes were exfoliated onto polymer films (X4 PF films, Gel-Pak). Upon inspection under an optical microscope, flakes of different thicknesses, ranging from monolayer to 8 nm, were chosen and transferred to the substrate consisting of 500 μm thick doped Si with a 200 nm thick layer of thermally grown SiO_2. The 2DM thickness was confirmed by Raman spectroscopy and/or atomic force microscopy (AFM).

For the fabrication of the contacts, a bilayer stack of 90 nm of polydimethylglutarimide (PMGI) and 30 nm of PPA was used. Contacts were patterned by a mix-and-match approach combining t-SPL for the small features on top of the semiconductor channel and DLW for larger features far away from the 2DM.[25] Prior to patterning, the surface of the sample was imaged using the thermal-based readout of the t-SPL tool to find the area of interest. Then, the surface was scanned setting a target patterning depth equal to the thickness of PPA, creating the desired patterns with a markerless overlay accuracy of around 20 nm. Thanks to the closed-loop algorithm linking the thermal lithography and the reading, the system adjusts the voltage to correct for deviations in the target depth, which is required for successful lift-off processes as any residual PPA would prevent the opening of the PMGI in the following step. For the pads and other large features, the DLW system was adopted. In this case, a 405 nm laser was used, resulting also in the direct sublimation of PPA. Then, wet etching in diluted TMAH for 2 min was used to open the PMGI, controlling the undercut for the subsequent lift-off. TMAH can fully remove PMGI without deteriorating the 2DM, as reported in previous studies.[9,26]

Previous studies have shown that even though MoS_2 is chemically very inert on its basal planes, the edges are much more reactive and can adsorb molecules when exposed to air.[14] In particular, Ar milling was used to create Mo and S vacancies in MoS_2[27] and to fully etch the 2DM.[8] In both cases, the newly created sites were much more reactive to molecules such as O_2. It has also been shown that edge-contact configurations can

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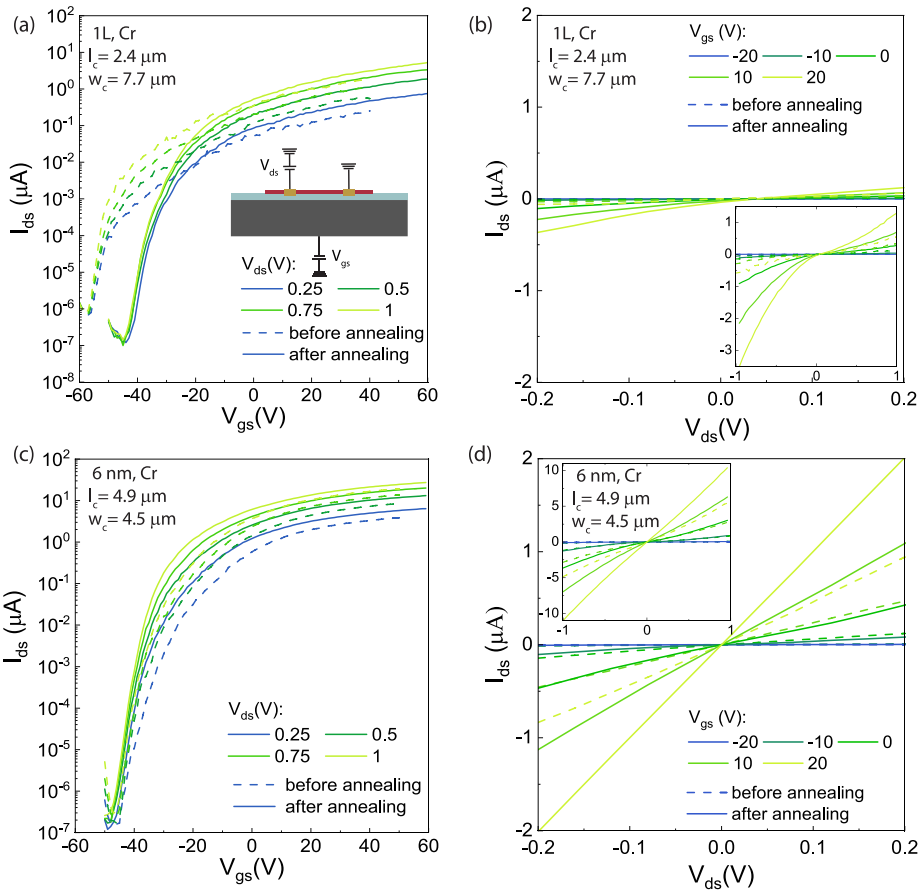

Figure 3. Electrical characteristics of edge-contact MoS_2 FETs measured before (dashed lines) and after (solid lines) thermal annealing. (a, c) Drain current I_{ds} as a function of the gate voltage V_{gs} at varying drain-to-source bias voltages V_{ds} for 1L (a) and FL (c) devices. (b, d) I_{ds} as a function of V_{ds} at varying V_{gs} for 1L (b) and FL (d) devices. (Inset in a) Schematic cross-section with the electrical connections of the device.

improve the contact to metals such as In, Au, Pd, and Ti by lowering tunnel barriers and strengthening the orbital overlaps.[28] Hence, to create the contact through the edge, the flakes were milled using an Ar^+ ion source in the same vacuum chamber in which the contacts were subsequently deposited, resulting in a complete etch of the MoS_2 in the patterned area without destroying the undercut needed in the resist for the subsequent lift-off. In this way, the dangling bonds from the just created edge can efficiently bond to the metal contacts. It has been previously reported that 2DM can be affected by chemical changes or kinetic energy transfer during metal deposition.[11,29] For top contact, the evaporated materials would directly impinge the contact area affecting the contact area,[29,30] whereas in the case of edge contact, the 2DM is presumably less affected due to the lower energy involved in the lateral diffusion of the deposited atoms to the 2DM edge.

The ion source milling process is 5 min long for all devices, meaning that for thinner ones there will be more etching of the SiO_2 underneath but always ensuring complete removal of the 2DM. To check the milling step, the same process was done without the metal evaporation step and the samples were characterized using optical microscopy, AFM, and Raman spectroscopy. All techniques showed that even the thicker parts of MoS_2 (>15 nm, thicker than those used for devices) were completely etched away (Supporting Information, Figure S2).

Regarding the selection of the contact electrode material, previous studies showed that Cr results in a shorter bonding length, lower potential barrier, and higher density of states at the Fermi level in top-contact FETs than other alternative metals for MoS_2.[31] For this reason, we opted for Cr as the electrode material for our initial devices. Given the fact that the ion-milling time is always the same and that our devices vary in thickness from 1L to FL devices of up to 8 nm, 20 nm of Cr were deposited by electron beam-induced physical vapor deposition (PVD) to ensure the edge contact is defined only through the Cr (only the sample used for TEM inspection has a thinner Cr layer, but it is not part of the devices analyzed within this paper). Then, a Au layer was deposited to protect the Cr from oxidation. However, the deposition of a 20 nm thick layer of Cr caused cracks in the film due to stress, inducing leakage of metal through the cracks that resulted in short circuits in some of the devices (Supporting Information, Figure S3). For this reason, Ti/Au was used in a second set of devices, showing a better fabrication yield but lower device performance (see Supporting Information, Table S1).

TEM Characterization. Cross-sectional scanning transmission electron microscopy (STEM) studies were carried out to have a closer insight into the nature of the 2DM−metal contact in one of our preliminary devices. For this experiment, a 6L MoS_2 flake was chosen. In this case, 5 nm of Cr and 25 nm of Au were used in the metallic side of the contact (note that all devices characterized in the rest of the manuscript are consistent in metal thickness with 20 nm of Cr or Ti and 5 nm of Au). Figure 2 shows a STEM image and the corresponding EDX map of an edge contact. In our PVD setup, the angle

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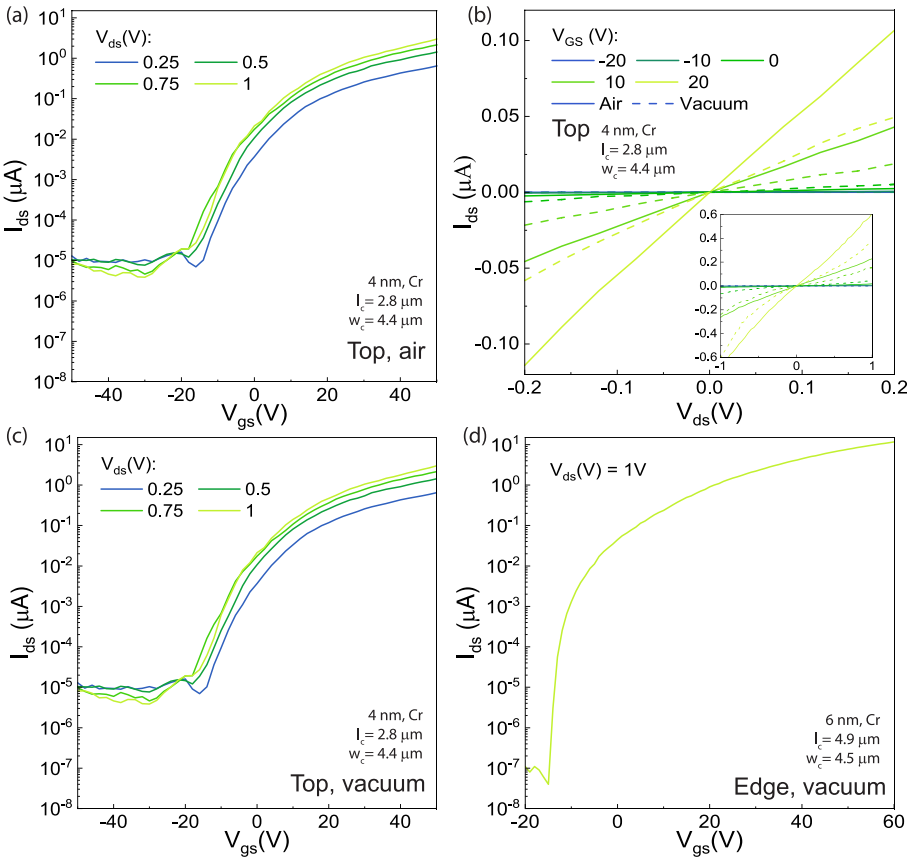

Figure 4. (a–c) Electrical characteristics of top-contact few-layer MoS_2 FET. (a) I_{ds} as a function of V_{gs} at varying V_{ds} in air. (b) I_{ds} as a function of V_{ds} for varying V_{gs}. (c) I_{ds} as a function of V_{gs} at varying V_{ds} in vacuum. (d) I_{ds} as a function of V_{gs} at V_{ds} = 1 V in vacuum for the edge-contact device characterized also in air (see Figure 3c and 3d).

between the samples and the evaporation source is around 7°; for this reason, some material is deposited laterally, resulting in "ears" that appear after lift-off (Figure 2a and 2b). This overhanging metal part appearing after lift-off from the lateral deposition of metals in the PMGI cavity protected the edge contact from the carbon deposited for the lamella preparation, allowing us to see the 6 layers of the MoS_2 flake. This overhanging metal part does not affect the performance of the device as this part is not contacted to the 2DM. EDX experiments (Figure 2c and 2d and Figure S4) show the complete milling of the flake by the ion source. However, it is difficult to say if there is an oxidation of the MoS_2 as the Cr-L line is superimposed on the O-K_α line. It is worth noting that previous publications reported the need for tilted evaporation both for the ion source milling (to expose pristine MoS_2) and for the metal deposition (to achieve a successful contact).[32] However, due to the inherent angle between the metal source and the sample in our setup, we found that the contact is successful without specifically adding more tilting.

Electrical Performance of MoS_2 Transistors. Previous reports show that for top contact, the performance of the devices, in particular, the mobility, is highly dependent on the number of layers.[5,33,34] In top-contact configuration, the metal is in direct contact only with the topmost layer of the 2DM flake, and hence, the charge carriers need to overcome tunneling gaps to reach lower layers. Scattering from the MoS_2–SiO_2 interface will affect the bottom layers of the device, and thinner flakes will be more affected by the substrate interface than thicker ones, where this effect will be partially screened.[5] In the case of edge contact, we expect the influence of the substrate to have the same effect but with the benefit of having a contact to each single layer of the flake and, in turn, direct access for the current to be injected.

A set of 29 MoS_2 devices with different channel thicknesses, lengths, and widths have been fabricated. For the sake of comparison, both edge- and top-contact configurations have been implemented. The fabrication process for both configurations is the same except that the ion source milling step (see Figure 1c, step 6) is not done in the case of top-contact devices. Table S1 in the Supporting Information shows the list of devices fabricated within this study, including Cr/Au and Ti/Au contacts and top- and edge-contact configurations. Here, we have chosen 3 representative devices to analyze them in more detail.

Figure 3 shows the transfer characteristics before and after thermal annealing (dashed and solid lines, respectively) for two edge-contact transistors using Cr as the contact metal: 1L MoS_2 (Figure 3a and 3b, w_c = 7.7 μm; l_c = 2.4 μm) and FL MoS_2 (Figure 3c and 3d, w_c = 4.5 μm; l_c = 4.9 μm, t_c = 6 nm), where w_c, l_c, and t_c are the width, length, and thickness of the transistor channel, respectively. Figure 3a and 3c shows the drain current (I_{ds}) as a function of the back-gate voltage (V_{gs}) for various drain voltages (V_{ds}) measured in ambient conditions. As shown, the as-fabricated edge-contact FETs exhibit electron conduction behavior (n-type transport) and on/off ratios of about 3×10^6 (1L) and 6×10^7 (FL) with on-state currents of 2 and 19 μA, respectively, at V_{ds} = 1 V. The electron field effect mobility can be extracted from the linear

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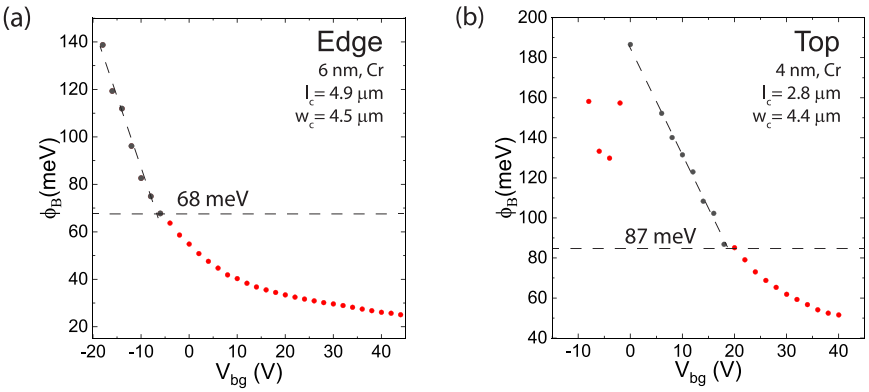

Figure 5. Schottky barrier height for (a) the FL edge-contact device shown in Figure 3 and for (b) the FL top-contact device shown in Figure 4. From a reasonable variation of the extraction region, the extracted value of SBH can change by about ±20%.

dependence of $I_{ds}(V_{gs})$ in the strong inversion regime (see Supporting Information, section S5).[34] As a result, mobilities of 1 and 20 $cm^2\ V^{-1}\ s^{-1}$ are calculated for the 1L and FL FET, respectively. For the sake of comparison, the mobility has also been estimated with the Y-function method (see Supporting Information, section S5).[32,35] In this case, we obtain electron mobilities of 0.2 and 36 $cm^2\ V^{-1}\ s^{-1}$ for the 1L and FL devices, respectively. For the monolayer, $I_{ds}(V_{ds})$ shows a nonlinear response (see Figure 3b) that could originate from the Schottky barrier between the metal and the semiconductor. The asymmetry in these curves is a sign of different Schottky barrier heights (SBHs) in the two electrodes.

Previous studies have shown that annealing the devices in an inert atmosphere or vacuum can induce atomic rearrangement and improve bonding. As a result, annealing can reduce the contact resistance, increase mobility, and reduce hysteresis.[10,32,34] Hence, we measured the electrical characteristics of the same devices before and after annealing at 250 °C for 3 h in N_2 atmosphere. We observe an increase in the mobility (μ_{slope}/μ_Y), reaching values of 2/1 and 31/38 $cm^2\ V^{-1}\ s^{-1}$ for the 1L and FL FETs, respectively. The on-state currents and the on/off ratio also increased, reaching I_{on} = 6 (1L) and 28 (FL) μA (at V_{ds} = 1 V) and $I_{on}/I_{off} = 4 \times 10^7$ (1L) and 1×10^8 (FL).

Figure 4a–c shows the FL top-contact transistor (w_c = 4.4 μm, l_c = 2.8 μm, t_c= 4 nm, Cr contacts) having the best performance among the fabricated ones. Figure 4a and 4c shows the corresponding $I_{ds}(V_{gs})$ characteristics measured in air and vacuum, respectively. From the data in vacuum, at V_{ds} = 1 V, mobility values of 9 and 3 $cm^2\ V^{-1}\ s^{-1}$ were extracted with the slope and Y-function methods, respectively. The on/off ratio in this case was 1×10^6 and I_{on} = 4 μA. The $I_{ds}(V_{gs})$ curve at V_{ds} = 1 V for the FL edge-contact device shown in Figure 3c and 3d is plotted in Figure 4d for the sake of comparison. It is worth noting that the $I_{ds}(V_{ds})$ characteristics present a linear response in the range between −1 and 1 V in vacuum, which was not the case for the response in air (see Figure 4b). This cannot be attributed to the SBH as we should not observe a variation between air and vacuum. As compared to the edge-contact FL device, the performance of the top-contact is worse, presumably due to the tunneling barriers from layer to layer and the possible contamination of the 2DM surface where the electrode is fabricated, as discussed also in previous works.[15,36,37]

The Y-function method was also used to obtain the contact resistance, R_c (see Supporting Information, section S5). The results of a representative set of samples are displayed in the Supporting Information in Table S1. In the case of Cr/Au contacts, a clear trend shows that top-contact devices present the highest contact resistance independently of the number of layers, which is most likely due to contamination between the electrode metal and the 2DM. Edge-contact devices show clear differences between 1L and FL, where the contact resistance of the later is at least one order of magnitude lower. In the case of Ti/Au, determining a clear trend is less obvious and the contact resistance is, in general, higher than that of Cr/Au contacts.

To determine the effect of temperature in the electrical response of the devices, additional $I_{ds}(V_{ds})$ and $I_{ds}(V_{gs})$ measurements were carried out with temperatures starting from 80 K until room temperature (see Supporting Information, section S6). For low temperatures, the response is less linear and I_{ds} is slightly lower, in accordance with previous studies.[13,38] The variation in the electrical performance is more noticeable for devices where the performance is lower, which we attribute to a worse contact between the 2DM and the metallic electrode. This set of measurements was also used to obtain the SBH in the thermionic regime, leading to values of 68 and 87 meV for the edge- and top-contact FL devices, respectively (see Figure 5).

2DM devices are typically characterized by their variability due to the quality of the exfoliated flakes themselves, defects introduced during the fabrication process, and effects of the environment. In this paper, we present 29 devices, which helps to see some trends but underlines also the large variability among nominally similar devices. The fabricated devices are compared in terms of mobility, contact resistance, on/off ratio, and on-state current (Figure S10, Supporting Information). According to previous studies,[34] mobility should be higher for 1L MoS_2 FETs than for that 2L or 3L devices. Despite a broad variation in the measured values, mobility clearly tends to increase with thickness, which was also reported in the past by different groups.[5,33] This effect is most probably due to the molecules adsorbed on the channel upon exposure to air, which Lembke and co-workers avoided by doing the measurements in high vacuum and annealing the samples in situ to have a clean semiconductor channel. This effect is clearly more important for 1L FETs. Besides, the effect of the substrate has also an important contribution. It has been reported that the contribution of the scattering from the interface between SiO_2 and MoS_2 is critical for the degradation of mobility in monolayer devices, which is reduced with an

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increasing number of layers.[5] The contact resistance is reduced with an increasing number of layers for edge-contact devices, as expected from the fact that this configuration enables a direct injection of current into every single layer. The dispersion of the measured on/off current values is very high (10^4–10^7 for 1L edge contact, 10^4–10^8 for FL edge contact, and 10^3–10^5 for top contact). In some devices, we see an increase in the current for large negative gate voltages (for example, Figure 3c) that has been also observed and discussed in previous studies.[14,39,40] In the case of 1L devices, it is clear that mobility, on-state current, and contact resistance are better for the edge-contact configuration than that for the top-contact configuration. The performance of our top-contact devices is worse than those reported previously in terms of mobility[11] and on/off ratio,[9] which we attribute to the contamination of the surface of our devices. This demonstrates how delicate the fabrication process of these devices is and reinforces the benefits of edge-contact devices, where our results are comparable to previous studies without encapsulation (see Table S2 in Supporting Information).

It is also worth noting the difference between the contacts made of Ti and Cr. Even though Cr induced problems in terms of fabrication due to the formation of cracks, Cr electrodes show higher on currents, higher mobilities, lower contact resistance, and better on/off ratios (Table S1 and Figure S10 in the Supporting Information).

Given the high variability of performance from device to device, all 29 devices were measured multiple times and on different days. In the measurements of a device within the same day, we observe that the on-state current of the first measurement is sometimes lower than that for the following measurements, but afterward, we see a stabilization of the electrical performance which we attribute to a mechanism of self-annealing through current (see Figure S11 in the Supporting Information). However, from day to day, there are variations in the device. We measured the $I_d(V_d)$ characteristics of some of our devices several months after their fabrication, and we observed that in most cases the performance decreased (Supporting Information, Figure S12). Some of them, especially monolayer devices, were no longer measurable after some months exposed to air. Encapsulating MoS_2 FETs with hBN[11,32] or a top layer deposited by ALD[41] to protect the channel has been reported in several studies. Hence, adding an encapsulation step to our process might be also effective in preserving the performance of the FETs.

Finally, the devices were electrically characterized in vacuum and compared to the measurements performed in air. We observe that in all cases, the hysteresis is reduced and the mobility and on current tend to be improved when measured in vacuum (see Supporting Information, Figure S13). This is in agreement with previous reports[34,42] and attributed to the adsorbed molecules in the MoS_2 surface (and water in particular), which are partially removed in the vacuum chamber. In vacuum, we achieved a maximum on/off ratio of 10^9.

CONCLUSION

In this work, we demonstrate a combination of t-SPL and DLW to fabricate edge-contact MoS_2 FETs in a gentle and clean manner. Neither energetic electrons nor UV photons are used near the semiconductor channel during lithography, avoiding the risk of deteriorating the properties of MoS_2. In addition, the edge-dangling bonds created by Ar^+ milling are kept in vacuum until the PVD deposition of the contact is performed. This fabrication method resulted in edge-contact FETs comparable to the state-of-the-art and with better performance than top-contact devices of similar characteristics fabricated following an analog approach. This is attributed to the cleaner interface between the 2DM and the metal. Both Ti and Cr were studied as possible contact metals. In spite of the cracks induced in Cr due to stress, this type of contact seems to result in lower contact resistance, higher performance, and less variability. For implementation in devices, FL FETs seem more promising than 1L devices as they present higher mobility, higher on-state currents, lower contact resistance, and less degradation.

EXPERIMENTAL SECTION

Preparation of MoS_2 Flakes. MoS_2 flakes were exfoliated from MoS_2 bulk (HQ Graphene) onto PF films (Gel-Pack) glued on a glass slide and then transferred to the substrate consisting of 500 μm thick doped Si with a 200 nm thick layer of SiO_2.

Fabrication of Edge-Contact MoS_2 Transistors. The process flow for the fabrication of edge-contact MoS_2 transistors is shown in Figure 1c. The $MoS_2/SiO_2/Si$ samples were dehydrated for 5 min at 190 °C in air. Then, PMGI SF2S (Microchem) was spin coated at 1000 rpm, followed by a bake of 3 min at 190 °C. A 1.3% solution of polyphthalaldehyde (PPA, Allresist) in anisole (abcr GmbH) was prepared and spin coated at 2000 rpm with a subsequent soft bake at 90 °C for 3 min. A commercial t-SPL system (Nanofrazor, Heidelberg Instruments) was used to pattern the contacts. A combination of t-SPL and DLW was used for smaller and bigger features, respectively. For t-SPL, the heater temperature was set to 950 °C and the step size and depth were fixed to 30 nm. For DLW, the step size was 50–100 nm, the pixel time was 70 μs, and the power was varied from 150 to 300 mW. Then, the pattern was transferred to the substrate by dipping the sample in AZ 726 MIF (2.38% TMAH in H_2O) for 120 s and then rinsing in DI water and isopropanol. For the milling of the flakes and the metal deposition, LAB600H (Leybold Optics) was used. The milling was performed using an end-Hall ion source (Kaufmann Robinson, Inc., KRI EH1000 equipped with a hollow cathode electron source KRI SHC-1000) for 300 s, and in the same chamber, the metals for the contacts were evaporated. A voltage of 160 V and a current of 3.5 A were used, resulting in a current density of around 0.5 mA/cm^2. Finally, lift off was performed in Remover 1165, followed by soft ultrasounds when needed.

Fabrication of Top-Contact MoS_2 Transistors. The $MoS_2/SiO_2/Si$ samples were dehydrated for 5 min at 190 °C in air. Then, PMGI SF2S (Microchem) was spin coated at 1000 rpm, followed by a bake for 3 min at 190 °C. A 1.3% solution of polyphthalaldehyde (PPA, Allresist) in anisole (abcr GmbH) was prepared and spin coated at 2000 rpm with a subsequent soft bake at 90 °C for 3 min. A commercial t-SPL system (Nanofrazor, Heidelberg Instruments) was used to pattern the contacts. A combination of t-SPL and direct laser writing was used for smaller and bigger features, respectively. For t-SPL, the heater temperature was set to 950 °C and the step size and depth were fixed to 30 nm. For DLW, the step size was 50–100 nm, the pixel time was 70 μs, and the power was varied from 150 to 300 mW. The pattern was transferred to the substrate by dipping the sample in AZ 726 MIF (2.38% TMAH in H_2O) for 120 s and then rinsing in DI water and isopropanol. For the metal deposition of the electrodes, LAB600H (Leybold Optics) was used and the process finished with a lift off using Remover 1165, followed by soft ultrasounds when needed.

Lamella Preparation and Cross-Sectional STEM. A carbon layer was deposited on the sample to protect it from the focused ion beam (FIB). First, electron beam-assisted deposition at 5 kV was used to protect MoS_2 from ion implantation and surface damage. Then, a second carbon layer of around 1.3 μm was deposited using ion beam-assisted deposition at 30 kV and 150 pA. A lamella was cut perpendicular to one of the contacts to observe the interface between

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the edge of MoS_2 and the contact. A Thermo Fisher Tecnai Osiris transmission electron microscope was used to study the interface between the electrode and the 2DM. The HAADF STEM detector was used to image the contact, and EDX was performed to analyze the material composition of the interface.

Electrical Measurements. Electrical measurements of all devices were performed at room temperature and ambient conditions. Some devices were also characterized in vacuum (4×10^{-6} mbar). For the Schottky barrier height extraction, some of the best devices were measured for a set of temperatures ranging from 80 to 300 K, also in vacuum. The standard DC measurements were performed using a HP4156A Semiconductor Parameter Analyzer and a Cascade Summit probe station.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.2c10150.

> Thermal scanning probe, Ar^+ milling, cracks in the Cr layer, TEM characterization, fabricated devices, low-temperature measurements, effect of thickness, configuration and electrode material in the performance of the device, reproducibility of the measurements, stability of the devices over time, and effect of ambient atmosphere in the device performance (PDF)

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Notes

The authors declare no competing financial interest.

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