



Article

Amorphization Optimization of Ge₂Sb₂Te₅ Media for Electrical Probe Memory Applications

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Abstract: Electrical probe memory using Ge₂Sb₂Te₅ media has been considered a promising candidate in the future archival storage market due to its potential for ultra-high density and long data retention time. However, most current research efforts have been devoted to the writing of crystalline bits using electrical probe memory while ignoring the viability of writing amorphous bits. Therefore, this paper proposes a physical, realistic, full three-dimensional model to optimize the practicable media stack by spatially and temporally calculating temperature distributions inside the active media during the writing of amorphous bits. It demonstrates the feasibility of using an optimized device that follows a Silicon/Titanium Nitride/Ge₂Sb₂Te₅/Diamond-Like Carbon design with appropriate electro-thermal properties and thickness to achieve ultra-high density, low energy consumption, and a high data rate without inducing excessive temperature. The ability to realize multi-bit recording and rewritability using the designed device is also proven, making it attractive and suitable for practicable applications.

Keywords: Ge₂Sb₂Te₅; amorphization; probe; optimization; model

1. Introduction

Data storage devices play a crucial role in citizens' daily life as a result of the proliferation of computerized data triggered by the global digitalization storm. Accordingly, global digital data has increased at an unprecedented rate, much higher than that of conventional data storage devices such as the magnetic hard disk, magnetic tape, and optical disc. Under such circumstances, research has focused on the development of innovative memory devices that can satisfy the current storage requirements from either industry or consumers. Recently, electrical probe memory has been considered as one of the most promising storage devices for the future archival storage application due to its superior recording and replay performances when compared to its predecessors [1]. Electrical probe memory usually comprises a conductive probe tip that serves as the top electrode, a storage stack that consists of a Chalcogenide alloy (e.g., Ge₂Sb₂Te₅ media) surrounded by a protective capping layer and a bottom electrode, both of which are deposited into the silicon (Si) wafer. The recording process of electrical probe memory is achieved by raising the temperature inside the Chalcogenide layer through Joule heating, by means of an appropriate electric stimulus applied either to the crystallization temperature to induce the crystalline mark embedded inside the amorphous background or to the melting temperature, followed by fast cooling and quenching of the molten materials to generate amorphous marks surrounded by crystalline background. The replay process is accomplished by applying a low readout voltage through the conductive tip to the storage stack and, subsequently, sensing the readout current variations caused by the large resistance contrast between crystalline/amorphous marks and their respective background. These variations can be further adjusted by reversing the bias voltages which are linked to the solid-state electrolytic behavior [2].

The principles of the recording and replay processes of the electrical probe memory are schematically shown in Figure 1.

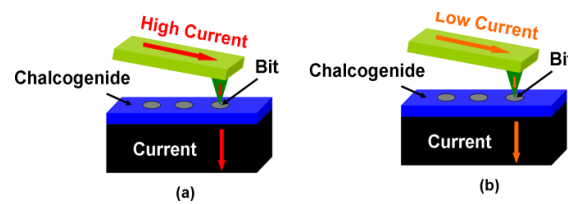


Figure 1. The electrical probe memory using Chalcogenide media when operated in (a) write mode and (b) readout mode.

The advantageous features of the electrical probe memory derive from the use of the nanoscale probe tip, leading to the possibility of securing ultra-high recording density; additionally, the Chalcogenide alloy acts as storage media to provide super-fast phase transition, long data retention, low energy consumption, excellent scalability, and high On/Off resistance contrast [3,4]. Given its performance superiorities over conventional storage devices, the electrical probe memory has recently received considerable attentions from worldwide researchers in the aspects of the experimental fabrication [2–7] and the theoretical simulation [8–10]. It should be noted that the majority of previous research concentrated on the phase transition from amorphous to crystalline phases while ignoring the writing of amorphous marks from the crystalline background. Undoubtedly, the writing of crystalline marks from an amorphous background typically costs less energy than its counterpart and thus exempts high temperatures from appearing inside the capping layer. However, this writing mechanism severely deteriorates its rewritability, as erasing the previously written crystalline mark partially crystallizes the neighbouring amorphous region. Consequently, this results in a peculiar crystalline ‘halo’ which encompasses the erased region, thereby degrading both the readout signal and the achievable recording density [8]. In this case, the recording of the electrical probe memory based on the crystalline-to-amorphous transformation (i.e., amorphization) is more desirable than the amorphous-to-crystalline transition (i.e., crystallization) in terms of its rewritability and, accordingly, worth particular investigation. Notably, the GeTe-Sb₂Te₃-based superlattice material has recently become a hot spot as a result of its potentially lower switching energy and faster switching speed [11,12]. However, as a result of increased knowledge regarding the electro-thermal and mechanical properties of the Ge₂Sb₂Te₅ media since its debut for storage applications, the active media of the electrical probe memory studied here is focused on the Ge₂Sb₂Te₅ layer.

2. Modeling

Prior to the study of the amorphization of the electrical probe memory, a physical-realistic model is required to provide insight into temporally and spatially resolved kinetics of writing current, device temperature, and phase transition for the required amorphized process. As amorphization closely pertains to temperature and cooling rate inside the storage layer, the designed model, similar to the previous crystallization case [9], includes several equations, comprising the Laplace equation and the heat transfer equation to compute temperature and cooling rate inside the Chalcogenide layer (i.e., Ge₂Sb₂Te₅ in this paper), given by

$$\nabla \cdot (\sigma \cdot \nabla V) = 0, \quad (1)$$

$$\rho C_p \frac{\partial T}{\partial t} - k \cdot \nabla^2 T = \sigma |E|^2, \quad (2)$$

where σ is the electrical conductivity; V is the electric potential; ρ is the density; C_p is the specific heat; T is the temperature; k is the thermal conductivity; E is the electric field.

The Laplace equation is solved to provide the electric field and current density distributions inside the Ge₂Sb₂Te₅ layer, which are simultaneously implemented as the heat source for the heat transfer equation, performing the calculations of temperature and cooling rate distributions inside the Ge₂Sb₂Te₅ layer. In our simulation, the crystalline Ge₂Sb₂Te₅ turned into its amorphous state in the region where the temperature exceeded the melting point (i.e., 620 °C) [8], and the cooling rate was greater than 37 °C/ns [8]. In this case, the electrical conductivity of the Ge₂Sb₂Te₅ alloy was defined by:

$$\sigma_{\text{GST}} = \sigma_{\text{am}} \cdot (T \geq 620 \text{ }^\circ\text{C}) \cdot (T_t \geq 37 \text{ }^\circ\text{C/ns}) + \sigma_{\text{cryst}} \cdot ((T < 620 \text{ }^\circ\text{C}) \parallel (T_t < 37 \text{ }^\circ\text{C/ns})), \quad (3)$$

where T_t is the cooling rate, and σ_{am} and σ_{cryst} are the electrical conductivity of the Ge₂Sb₂Te₅ alloy in its amorphous and crystalline phases respectively, given by [6]:

$$\sigma_{\text{am}} = \sigma_{0\text{am}} \times \exp(-\Delta\xi_{\text{am}}/k_{\text{B}}T) \times \exp(E/E_0), \quad (4)$$

$$\sigma_{\text{cryst}} = \sigma_{0\text{cryst}} \times \exp(-\Delta\xi_{\text{cryst}}/k_{\text{B}}T), \quad (5)$$

where $\sigma_{0\text{am}}$ and $\sigma_{0\text{cryst}}$ are prefactors for amorphization and crystallization with a value of $1.88 \times 10^4 \text{ } \Omega^{-1} \cdot \text{m}^{-1}$ and $1.5 \times 10^4 \text{ } \Omega^{-1} \cdot \text{m}^{-1}$, respectively; $\Delta\xi_{\text{am}}$ and $\Delta\xi_{\text{cryst}}$ are the activation energies for the temperature dependence of amorphous σ_{GST} and crystalline σ_{GST} with a value of 0.32 eV and 0.04 eV, respectively; E_0 is the critical electric field with a value of $5 \times 10^7 \text{ V} \cdot \text{m}^{-1}$ and k_{B} is the Boltzmann Constant. The thermal conductivity of the Ge₂Sb₂Te₅ alloy is described in a similar manner to its electrical conductivity, given by:

$$k_{\text{GST}} = k_{\text{am}} \cdot (T \geq 620 \text{ }^\circ\text{C}) \cdot (T_t \leq -37 \text{ }^\circ\text{C/ns}) + k_{\text{cryst}} \cdot ((T < 620 \text{ }^\circ\text{C}) \parallel (T_t > -37 \text{ }^\circ\text{C/ns})), \quad (6)$$

where k_{am} and k_{cryst} are the thermal conductivities of amorphous and crystalline Ge₂Sb₂Te₅ with a value of $0.2 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ and $0.58 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$, respectively. To more closely mimic the practical setup, all simulations in this paper were performed in fully three-dimensional (3D) environments. Previous literature has reported that amorphization of the Ge₂Sb₂Te₅ media can be induced using the conductive probe by directly contacting the probe tip with the phase-change layer [2]. However, if the phase-change layer were exposed directly to the air, it would be easily prone to oxidation and wear and, therefore, is not practicable for the real design. In this case, it was important to overcoat phase-change layer with a capping layer which met the electrical requirements for successful writing and reading while providing oxidation protection and wear resistance. Accordingly, a typical electrical probe memory consists of a conductive probe and a trilayer stack, which is made up of a Ge₂Sb₂Te₅ layer sandwiched by a diamond-like carbon (DLC) layer and a titanium nitride (TiN) bottom electrode, as illustrated in Figure 2. Such an architecture has been previously used to optimize the writing of crystalline bits [9,10]. A commercial software package based on the finite-element method, i.e., Comsol MultiphysicsTM, was deployed to imitate the electrical, thermal, and phase-transformation kinetics which occurred inside the device. The write or readout pulse was applied to the conductive probe while the bottom TiN electrode was grounded. These two boundaries were also maintained at room temperature, whereas all others were assumed to be electrically and thermally insulated. The values of characteristic parameters used in the model are given in Table 1.

Table 1. Characteristic parameters used in the model.

Parameter	TipDLC	DLC	GST	TiN	Si
Thickness (nm)	10	2–5	10	40	1000
ρ (Kg·m ⁻³)	12,400	2800	6150	5400	2330
C_p (J·Kg ⁻¹ ·m ⁻³)	250	540	210	400	720
K (W·m ⁻¹ ·K ⁻¹)	25	0.5–2	Equation (3)	3 or 12	149
σ ($\Omega^{-1} \cdot \text{m}^{-1}$)	3.3×10^{-6}	10–200	Equation (4)	1×10^6 – 1×10^7	N/A

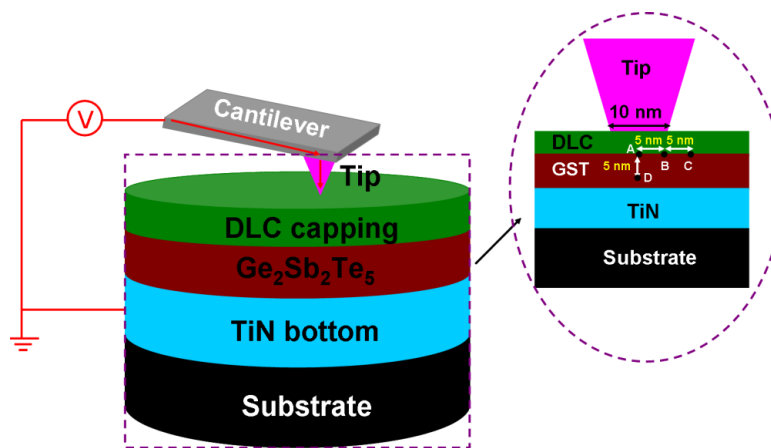


Figure 2. The 3D modeling geometry of the electric probe memory and its cross section (inset) where GST represents $\text{Ge}_2\text{Sb}_2\text{Te}_5$.

3. Results

Several design requirements needed to be fulfilled to successfully optimize the amorphization without incurring any adverse effects on device. To achieve multi-Terabits/ in^2 density, a small diameter of the probe tip was required, as it determined the conductive region through which current could flow, and thus strongly affect the bit size [13]. In our simulation, the diameter of the tip was restricted to 10 nm to provide ~ 10 Tbit/ in^2 , which corresponded to a bit diameter of ~ 10 nm. Such writing should also be accomplished without inducing excessive temperature inside the device (predominantly the thin DLC capping layer); the resulting thermal cross-talk that can overwrite the adjacent written bit must be strongly suppressed. These requirements have been used to define a set of maximum and minimum temperatures that should be realized at various locations in the storage media during the amorphization process.

To write amorphous bits with ~ 10 Tbit/ in^2 , the temperatures in the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer at points A (at the top of the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer and under the tip), B (at the top of the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer and at the tip edge being 5 nm away from A), and D (in the middle of the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer, being 5 nm away from A) needed to reach a minimum of 620 °C so as to satisfy one of the two indispensable conditions for amorphization. Additionally, because the maximum temperature of the device took place approximately at A, the temperature at A was required to be less than 1000 °C to maintain the thermal stability of the DLC capping [14]. Finally, the temperature at point C, where the edge of the adjacent written bit was located, could not exceed 200 °C so as not to weaken the resulting thermal cross-talk [15]. Therefore, it was necessary to optimize the prototype of the electrical probe memory shown in Figure 1 so as to simultaneously meet the aforementioned maximum and minimum temperature requirements.

The electrical conductivity and the thickness of the DLC capping layer have previously been found to play a critical role in determining the crystallization extent of the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer, as it serves as a conductive bridge for write current to flow into the active media. The optimum values of these parameters for the writing of crystalline bits fall within the range of $10 \Omega^{-1}\cdot\text{m}^{-1}$ to $100 \Omega^{-1}\cdot\text{m}^{-1}$ (electrical conductivity), and 2 nm to 4 nm (thickness) [9]. Therefore, the minimum and maximum temperatures at locations A, B, C, and D, were calculated by varying the electrical conductivity and the thickness of the DLC capping from $10 \Omega^{-1}\cdot\text{m}^{-1}$ to $200 \Omega^{-1}\cdot\text{m}^{-1}$, and from 2 nm to 5 nm to cover the range of possible values reported previously [9,16]. The tip voltage was set at a 4 V pulse of 120 ns, with 100 ns rising and 20 ns trailing edge (such a voltage was chosen to induce sufficiently high temperature for amorphization while achieving the appropriate cooling rate), resulting in Figure 3a. As can be seen from Figure 3a, the temperature inside the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer continuously increased by either reducing the capping layer thickness or enhancing the electrical conductivity of the DLC

capping. This was expected, as both strategies could lower the whole device resistance and thus induce more Joule heating inside the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer for a given pulse. However, notably, a thin capping layer with a very high electrical conductivity was not anticipated, as this would have caused excessively high temperatures in the capping layer ($>1000^\circ\text{C}$) and the adjacent written bit ($>200^\circ\text{C}$), thereby adversely affecting the device performances. In this case, the optimum values for the electrical conductivity and the thickness of the DLC capping that can fulfill the aforementioned maximum and minimum temperature requirements were mainly concentrated on the two gray regions highlighted in Figure 3a. As indicated in Figure 3a, the optimum values for electrical conductivity and thickness of DLC capping within the left gray region ranged from $100\ \Omega^{-1}\cdot\text{m}^{-1}$ to $150\ \Omega^{-1}\cdot\text{m}^{-1}$, and from 2 nm to 3.5 nm. In contrast, for the right gray region, these optimum parameters varied from $140\ \Omega^{-1}\cdot\text{m}^{-1}$ to $160\ \Omega^{-1}\cdot\text{m}^{-1}$, and from 4.5 nm to 5 nm. Undoubtedly, to design a practicable device, the values of these characteristic parameters are pertinent to the inherent properties of materials which suggest that a thicker DLC layer usually exhibits a higher electrical conductivity [17]. Additionally, recent literature has reported that the electrical conductivity of a 5 nm DLC capping layer, when subjected to Joule heating, can sharply increase to $140\ \Omega^{-1}\cdot\text{m}^{-1}$ [18,19]; in contrast, a DLC capping layer with an electrical conductivity of $140\ \Omega^{-1}\cdot\text{m}^{-1}$ and a thickness of 5 nm appears to be a satisfying configuration that can simultaneously meet the temperature requirements for amorphization as well as the practicable measurements.

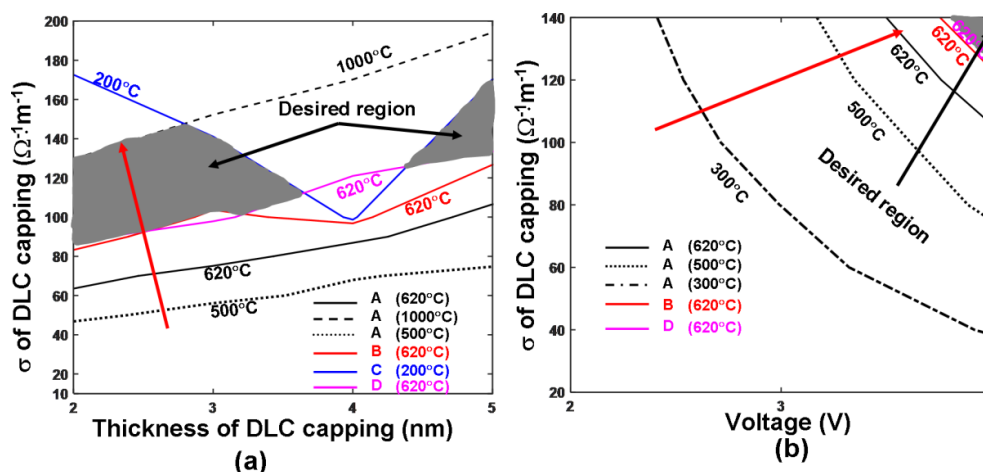


Figure 3. Temperature contours at points A, B, C, D as a function of (a) electrical conductivities and thickness of the DLC capping layer; and (b) electrical conductivities and tip voltages. For both simulations, the thermal conductivities of the capping and under layer remained at $0.5\ \text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$ and $12\ \text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$, while other modeling parameters are given in Table 1. Note that for (b) maximum temperature contours of 1000°C at A and 200°C at C are outside this figure and, therefore, are not visible. The red arrow indicates the direction along which the temperature at A increased.

Apart from the target for ultra-high density, the write pulse for amorphization must be carefully determined so that the write power and energy of a real device can be minimized. To investigate this, the minimum and maximum temperatures at locations A, B, C, and D were recalculated by both varying the electrical conductivities of the DLC capping from $20\ \Omega^{-1}\cdot\text{m}^{-1}$ to $140\ \Omega^{-1}\cdot\text{m}^{-1}$ to cover the previously designed optimum values and adjusting the pulse magnitudes from 2 V to 4 V, as depicted in Figure 3b. Notably, the 200°C and 1000°C contours were outside the plot (i.e., they only occurred for voltage beyond 4 V). Clearly, the write pulses of either 2 V or 3 V were incapable of generating the required amorphization temperature within the electrical conductivity range investigated in Figure 3b; the above temperature requirements could only be satisfied by implementing a write pulse of 4 V and a DLC capping with an electrical conductivity between $130\ \Omega^{-1}\cdot\text{m}^{-1}$ and $140\ \Omega^{-1}\cdot\text{m}^{-1}$. As a result,

the use of a 4 V pulse of 120 ns and a DLC capping with an electrical conductivity of $140 \Omega^{-1} \cdot \text{m}^{-1}$ and a thickness of 5 nm is an optimum choice for writing amorphous bits inside the electrical probe memory.

In addition to electrical conductivity, thermal conductivity of the DLC capping was previously found to play a critical role in determining the temperature distribution inside the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer during its crystallization process [9]. Accordingly, we assessed the influence of the thermal conductivity of the DLC capping on the aforementioned maximum and minimum temperature requirements by changing its thermal conductivity and thickness from $0.5 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ and 2 nm to $2 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ and 5 nm from to cover the possible reported values [20,21], leading to Figure 4. The results shown in Figure 4 clearly suggest that increasing the thermal conductivity of DLC capping reduces the temperature in the detected locations for a given write pulse, as this reinforces the heat spreading effect, and inversely prevents the original transformed region from acquiring sufficient heat. As a result, a higher write pulse is required to achieve essential temperatures for amorphization when using a DLC capping with a large thermal conductivity. According to Figure 4, the optimum values of the thermal conductivities also lie in the two gray regions. The left region exhibits a thermal conductivity from $0.5 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ to $0.8 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ and a thickness from 2 nm to 3.5 nm, whereas the thermal conductivity and the thickness inside the right region ranges from $0.5 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ to $0.75 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ and from 4.5 nm to 5 nm. To match above optimization findings for electronic parameters of the DLC capping (i.e., $140 \Omega^{-1} \cdot \text{m}^{-1}$ and 5 nm) as well as practicable measurements, $0.5 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ was selected as the optimized thermal conductivity of the DLC capping.

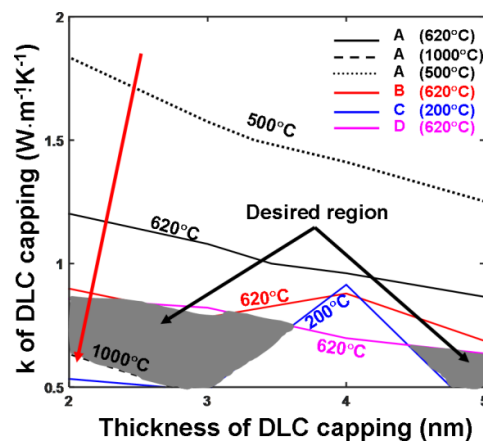


Figure 4. Temperature contours at points A, B, C, D as a function of thermal conductivities and thickness of the DLC capping layer. For both simulations, the electrical conductivities of the capping and under layer remained at $0.5 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ and $12 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$, while other modeling parameters are given in Table 1. The write pulses for all simulations were maintained as 4 V of 120 ns. The red arrow indicates the direction along which the temperature at A increased.

Notably, the electro-thermal properties of the TiN bottom layer also needed to be carefully determined, as they predominantly function as a bottom electrode where the write current is collected and, accordingly, may affect the resulting Joule heating. To investigate this, the minimum and maximum temperatures at aforementioned locations were recomputed by altering the electrical conductivity of the TiN layer from $1 \times 10^6 \Omega^{-1} \cdot \text{m}^{-1}$ to $1 \times 10^7 \Omega^{-1} \cdot \text{m}^{-1}$, with a thermal conductivity of either $3 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ or $12 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ to include the experimentally reported values [22], as illustrated in Figure 5. Notably, for the TiN layer with a thermal conductivity of $12 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$, T_c was below $200 \text{ }^\circ\text{C}$, and is therefore not visible in Figure 5. On the one hand, it was determined that the electrical conductivity of the TiN bottom electrode had a negligible impact on the resulting temperatures at these points (and, accordingly, not shown in Figure 5), which arose from the fact that the electrical conductivity of the TiN layer was much higher than those of the DLC capping and the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer. As a result, any variation in its electrical conductivity rarely affected the whole device

resistance and the write current. On the other hand, using a TiN bottom layer with lower thermal conductivity ($3 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$) induced higher temperatures at detected locations than the larger thermal conductivity case ($12 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$). This was expected, because the bottom electrode with larger thermal conductivity allowed Joule heat to flow more readily towards the Si substrate which acted as a heat sink as opposed to staying inside the active media, thereby resulting in a lower temperature inside these locations. Further observations in Figure 5 reveal that the temperature requirements for points A, B, and D could be satisfied by the TiN layer with either $3 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$ or $12 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$, whereas the $3 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$ case exhibited a temperature of $350 \text{ }^\circ\text{C}$ at point C that clearly exceeded the defined safety range. For this reason, the electrical conductivity and the thermal conductivity of the TiN bottom electrode were chosen to be $1 \times 10^7 \text{ }\Omega^{-1}\cdot\text{m}^{-1}$ and $12 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$, respectively.

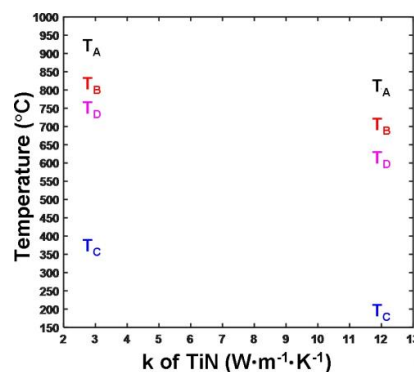


Figure 5. Calculated temperature at points A, B, C, D as a function of thermal conductivities of the TiN bottom electrode (i.e., $3 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$ and $12 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$). During simulations, the thickness, electrical conductivity, and thermal conductivity of the capping layer were set to be 5 nm, $140 \text{ }\Omega^{-1}\cdot\text{m}^{-1}$, and $0.5 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$, respectively, while other modeling parameters are given in Table 1. The write pulses for all simulations were maintained as 4 V of 120 ns.

4. Discussion

According to the results, to optimize the writing of amorphous bits in the crystalline starting phase, a design of an electrical probe memory structure is proposed here that comprises the following (as seen in Figure 6): a conductive probe with a diameter of $\sim 10 \text{ nm}$ as well as a storage media stack consisting of a 10 nm $\text{Ge}_2\text{Sb}_2\text{Te}_5$ layer sandwiched by a 5 nm DLC capping layer with electrical and thermal conductivities of $140 \text{ }\Omega^{-1}\cdot\text{m}^{-1}$ and $0.5 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$, respectively, in addition to a 40 nm TiN layer with electrical and thermal conductivities of $1 \times 10^7 \text{ }\Omega^{-1}\cdot\text{m}^{-1}$ and $12 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$, respectively. As can be seen from Figure 6a, integrating the aforementioned optimized device design with a 4 V pulse of 120 ns enables a formation of an amorphous bit with a diameter of 10 nm, corresponding to multi-Terabits/ in^2 recording density. Notably, as illustrated in the inset of Figure 6a, the written amorphous bit did not have to extend through the whole thickness of the active media which contrasts with the writing of crystalline bits in which it is preferred to extend through the whole thickness. This is because the resistance of the amorphous bits is much higher than its surrounding crystalline background; as a result, the readout current induced when the tip is on top of the amorphous bit is still much lower than the case with the tip on top of the crystalline surrounding, thus easily distinguishing the recording bit from its background. Accordingly, it is not necessary to amorphize the entire region underneath the tip, which allows for lower writing energy and results in a writing energy per bit of $\sim 2 \text{ pJ}$ that suggests for 0.2 nJ and 2 nJ for using 100 and 1000 tips in parallel. Furthermore, the use of pulse duration of 120 ns readily enables a data rate per tip of 1 Mbit/s, which can be even dramatically boomed for parallel probe recording.

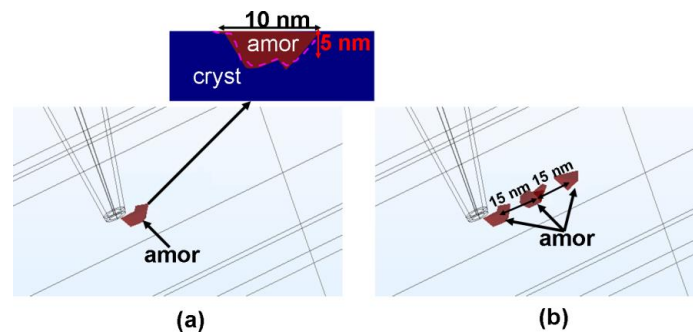


Figure 6. The writing of an isolated amorphous bit (a) and multiple amorphous bits (b) based on the optimized device architecture and a 4 V pulse of 120 ns. The inset shows the cross-section image of the written isolated amorphous bit bounded by the purple dash.

To more closely model the real environment, the main functions of the electrical probe device, such as multi-bit recording and rewritability, which functioned as the adopted scenarios in practice, needed to be reflected in the developed 3D model. To simulate the writing of multiple bits, the conductive probe was first brought to the position where amorphization was expected to occur; the write pulse was subsequently applied to the conductive probe to perform the recording, after which the probe was moved to the next data point. It was found in Figure 6b that three consecutive amorphous bits, with a 10 nm diameter and a center-to-center distance of 15 nm, were formed by means of the above optimized device architecture, further demonstrating its attractive potential for ultra-high density. Additionally, observations that the contiguous region between two adjacent amorphous bits remained crystalline indicated an effective inhibition of the resulting thermal cross-talk phenomenon which frequently arises during the writing of crystalline bits. This result ensured the reliability of the device. In addition to multi-bit recording, the erasure of a previously written amorphous bit (i.e., recrystallization) was also simulated, leading to Figure 7. Clearly, such an erasing process involves crystallization kinetics which can be accurately modelled by simultaneously solving a set of coupled equations, including the Laplace equation, the heat conduction equation, and the crystallization rate equation, all of which have been previously proposed for the optimization in the writing of crystalline bits [10] and, consequently, have not been repeated here. According to Figure 7, by choosing the appropriate erasing pulse (4 V of 100 ns here), the previously written amorphous bit could be completely recrystallized without adversely re-amorphizing the surrounding crystalline background (i.e., the temperature inside the surrounding crystalline region did not exceed the melting point). This simulation result suggests that re-writable probe storage should be feasible by first writing amorphous bits into a crystalline starting phase, followed by erasure by re-crystallization.

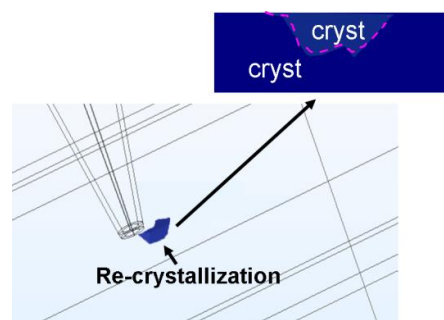


Figure 7. The erasing (re-crystallization) of the previously written amorphous bit in Figure 6a by a 4 V pulse of 100 ns. The inset shows the cross-section image of the re-crystallized bit bounded by the purple dash.

5. Conclusions

A full 3D theoretical model that involves the electrical, thermal, and amorphization processes of the Ge₂Sb₂Te₅ media for probe storage applications was developed to optimize the architecture of the electrical probe memory by spatially and temporally calculating temperature distributions inside the active media during the writing of amorphous bits. The feasibility of using the optimized device that follows a Si/TiN/Ge₂Sb₂Te₅/DLC design with appropriate electro-thermal properties and thickness to achieve ultra-high density, low energy consumption, and high data rate without inducing excessive temperature in the device was demonstrated. The ability to realize multi-bit recording and rewritability using the designed device as also proven, making it attractive and suitable for practicable applications.

Author Contributions: L.W. and B.X. conceived and designed the simulation scenario; L.W. and C.Y. performed the amorphization simulations; J.W. performed the multi-bit recording simulations for amorphization; C.Y. performed the erasing simulations; L.W. and C.Y. analyzed the data; L.W. and B.X. wrote the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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