Heliyon xxx (xxxx) xxx

Contents lists available at ScienceDirect

Heliyon

journal homepage: www.cell.com/heliyon

Research article

A design TCADAS tool for semiconductor devices and case study of 65 nm conventional floating-gate MOS transistor

Thinh Dang Cong [a,b], Trang Hoang [a,b,*]

[a] Department of Electronics Engineering, Ho Chi Minh City University of Technology (HCMUT), Ho Chi Minh City, 72506, Viet Nam
[b] Vietnam National University, Ho Chi Minh City, 71308, Viet Nam

ARTICLE INFO

Dataset link: https://github.com/Steve-Dang459/tcadas.git

Dataset link: https://github.com/hoangtranghcmut/tcadas

Keywords:
TCAD Silvaco tool
Semiconductor device
Floating-gate MOS transistor
Device characterization

ABSTRACT

An automatic programming tool has become an essential component in virtual fabrication in recent years. This paper aims to propose a methodology of virtual fabrication for semiconductor devices and design a tool called Technology Computer-Aided Design Automatic Simulation (TCADAS) which can perform a completely virtual fabrication, device simulation, process variation, and output extraction. Especially, the TCADAS tool eliminates drudgery when studying semiconductor devices such as complexity in setting inputs, substantial manual work, and long run time of simulations. This work investigates the completed flow for a 65 nm conventional Floating-gate MOS transistor as a case study, which is widely considered a vital determinant of the non-volatile memory field. A detailed automatic process from the entry to a completed three-dimension structure, device characterization, extract important output parameters such as memory window, I_{ON}/I_{OFF}, Gate Coupling Ratio (GCR), and speed operations are presented. The TCADAS tool was designed by Python language and the utilities of TCAD Silvaco tools including Athena, Atlas, and DevEdit3D.

1. Introduction

Over the past decades, the semiconductor device has been developed to serve the needs of the memory, artificial intelligence, neural network, and internet of things fields [1]. In the meantime, the industry has been demanding high density, low power, rapid speed products, etc. Therefore, the semiconductor device fabrication has been becoming more complex to obtain the requirements for the performance of the device in different applications.

In order to archive the performance requirements of the device in the fabrication phase, the virtual fabrication and simulation are entirely studied by using the Technology Computer-Aided Design (TCAD) tools, which refer to the use of computer simulations to develop and optimize the semiconductor devices. For almost applications such as the Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOSFET), Fin Shaped Field Effect transistor (FinFET), power devices, image sensors, solar cells, Analog/RF devices, interconnect modeling and extraction, and providing critical parasitic information for optimizing device performance, the TCAD tools has become highly essential component as it is [2,3]. There are two main types of TCAD tools which are TCAD Silvaco tools including Antenna, Atlas, and DevEdit3D, etc. [4,5] and Sentaurus tools of Synopsys [6,7].

* Corresponding author at: Department of Electronics Engineering, Ho Chi Minh City University of Technology (HCMUT), Ho Chi Minh City, 72506, Viet Nam.
E-mail address: hoangtrang@hcmut.edu.vn (T. Hoang).

https://doi.org/10.1016/j.heliyon.2024.e26496
Received 9 April 2023; Received in revised form 24 November 2023; Accepted 14 February 2024

Available online 21 February 2024

In fact, in the very early design phase of new technology, the test structures on silicon might not be available or not be successfully designed. Thus, the simulated fabrication is considered a "robust design" in that situation. Making the simulated fabrication possible only relies on the TCAD simulations [7,8]. As a result of the vital role of the tools, the innovative technologies have improved and enhanced the performance of semiconductor devices like MOSFET (Metal Oxide Semiconductor Field Effect transistor), SOI (Silicon on Insulator), HEMT (High Electron Mobility transistor) structures, to a remarkable degree [9–14].

Regarding related work, in 2019, work [9] proposed a promising tool named Impulse TCAD, which provided an automatic solution for investigating the transient behavior of the negative-capacitance field-effect transistor (NC FET). The Impulse TCAD tool uses Python language, some specified libraries, and the nonlinear finite volume algorithm for development. Besides, the tool is flexible when allowing modification of the device parameters and simulated formulas from the users. For the quality of the Impulse TCAD, while it provides the reasonable transient characteristics of the NC FET, the tool helps investigate the relation between the Ginzburg term in the Ginzburg-Landau-Devonshire (GLD) model and the radius r_c factor. Although that paper used the emerging approach which uses the Python language and some necessary libraries, that work did not provide the detailed flow and methodology for researchers to adopt and improve further. Moreover, the use of a nonlinear finite volume algorithm does not provide better results of the transient characteristics of the device.

Furthermore, work [10] published an RD50 tool for studying the radiation damage on silicon detectors. On top of the TCAD tools like TCAD Silvaco or Synopsys Sentaurus, the RD50 tool obtains the radiation damage with an expected precision for the acceptor removal effects on the Low Gain Avalanche Detectors (LGAD) device. However, one of the main drawbacks of the tool is that the RD50 cannot adapt to other semiconductor devices and can be obtained only for the LGAD device. As a result, a particular defect model and significantly upgraded version are needed for each device when using the RD50 tool.

Regarding the process variation of the semiconductor devices, a proposed algorithm called MINO ANN was presented in work [11]. The new method showed that the computation cost could be reduced six times compared to the well-known process variation tool, the 3-D stochastic TCAD simulator. The ultra-scaled Gate-All-Around (GAA) Vertical FET (VFET) device was virtual fabricated by the Sentaurus tool and investigated in that work as a case study. However, the performance of the GAA device was not compared to other studies to prove the quality of the proposed algorithm of that work. In addition, the flexibility when applying to other semiconductor devices is not mentioned in the paper [11].

In 2020, work [12] used an upgraded Impulse TCAD tool version in the study [9] and proposed a finite volume method for transporting phonons along with electrons and holes in semiconductor devices. The method considers the total phonon dispersion, transmission, and reflection at boundaries. Hence, relying on the tool and new method, the paper proved the importance of phonon transportation in estimating the thermal behavior of semiconductor devices. Interestingly, that work was successfully applied to a thin silicon-on-insulator (SOI) device. On the other hand, the detailed process and input information were not completely given for user investigation.

Besides, an open-source tool named Nano-Electronic Software Simulator (NESS) was given in work [13]. The purpose of the tool is that it can incorporate a wide range of semiconductor device structures and operating conditions. The tool is flexible and customizable with different architectures by using many modules such as gate tunnel leakage, quantum transport solver, kinetic Monte Carlo, etc. In 2021, work [14] proposed a new approach to solve the partial differential equation (PDE) named element edge based (EEB) finite volume method (FVM). The method was implemented and developed in the DEVSIM device simulator. As a results, this study resolved the polarization effect of the ferroelectric devices which are a 3D ferro capacitor and a 2D ferroelectric FET. In spite of the contribution of the work [13] and [14], the algorithm was not present clearly which is one of the key factors of these tools.

Hence, based on the works mentioned above [9–14], in order to enhance the performance of the semiconductor devices, and make the simulation work automatic, a combination of the traditional TCAD tools and Python has been becoming a promising approach in recent years. However, one of the most disadvantages of the studies is that they did not provide a detailed flow, process, and all the input parameters needed for the study, especially the proposed methodology. Therefore, this paper aims to present all the detailed information such as detailed fabrication flow, how to configure the huge input parameters, and emphasizes the proposed method which is appropriate for many semiconductor devices such as Metal Oxide Semiconductor Field Effect transistor (MOSFET), Silicon on Insulator (SOI), High Electron Mobility transistor (HEMT), and the floating-gate MOS transistor including nanocrystal and conventional structures. Furthermore, the TCADAS tool will help the researchers study and improve the semiconductor devices further by eliminating drudgery in designing a device from the beginning with many complexity inputs needed or manual simulations.

Regarding the conventional Floating-gate MOS transistor, the MOS is the heart of non-volatile memories [15–19]. Besides, the transistor has been applied in analog mixed-signal, artificial intelligence, and neural network fields [20–22] as a potential component. Hence, in state-of-the-art applications, the MOS must be fabricated perfectly to obtain high performance such as low power, high speed operation, and good scalability [23]. However, one of the most disadvantages of the studies is that they did not provide a detailed flow, process, and all the input parameters needed for the study, especially the proposed methodology. Therefore, this paper aims to present all the detailed information such as detailed fabrication flow, how to configure the huge input parameters, and emphasizes the proposed method which is appropriate for many semiconductor devices such as Metal Oxide Semiconductor Field Effect transistor (MOSFET), Silicon on Insulator (SOI), High Electron Mobility transistor (HEMT), and the floating-gate MOS transistor including nanocrystal and conventional structures. Furthermore, the TCADAS tool will help the researchers study and improve the semiconductor devices further by eliminating drudgery in designing a device from the beginning with many complexity inputs needed or manual simulations.

Therefore, in this paper, we proposed a methodology to enhance the virtual fabrication process for semiconductor devices and a tool named TCADAS (Technology Computer-Aided Design Automatic Simulation) by applying that methodology. The TCADAS tool

was designed by Python language and the utilities of the TCAD Silvaco. In addition, this work applied the methodology and TCADAS tool for the conventional Floating-gate MOS transistor as a case study. The case study solved the central problem of developing a tool for researching the conventional Floating-gate MOS transistor in the 65 nm process. The proposed TCADAS consists of two main stages. While the detailed flow was designed to perform the virtual fabrication automatically in the first part, the provided equations were imported to calculate and extract the output device parameters in the second part. With regard to the performance of the conventional Floating-gate MOS transistor that was designed in this paper, the TCADAS tool carries out the high performance of the MOS transistor such as a large memory window of 4 V, a competitive I_{ON}/I_{OFF} ratio of 293.466, a high value of GCR parameter of 0.645, and the Write/Erase speed of 50 ms/70 ms with the low control gate voltages of 6/-6 V and the thin of the tunnel oxide layer of 9 nm.

The remainder of this work is organized as follows: A proposed methodology for designing semiconductor devices is presented in section 2. Next, section 3 illustrates a case study of the TCADAS tool for a 65 nm conventional Floating-gate MOS transistor. A completed virtual fabrication and device characterization, a comparison of the quality of the Floating-gate MOS transistor which was fabricated by TCADAS tool to the published works are given in that section. Finally, the conclusion is presented in section 4.

2. TCADAS methodology - a proposed algorithm

In this section, a proposed methodology for the fabricated semiconductor device fields was presented. Based on that methodology, the TCADAS tool was designed and developed to help researchers solve the problems mentioned earlier in section 1, and further improve semiconductor devices.

There are five main steps of the proposed methodology. First, step 1 imported the essential parameters for the virtual fabrication process and formulas in characterization. Second, step 2 focused on the mesh designing which are two-dimensional and three-dimensional meshes. The mesh is one of the most important components in simulated fabrication since it directly affects the quality of results. Hence, the compare statement was provided to validate the quality of the designed meshes. Third, a virtual fabrication process was conducted, and the industrial standard Athena tool, which is proven in commercial when realized physical device, was used in that step. The verification at each sub-step was given to ensure that the performance of the device would be as expected. Fourth, the step plotted the designed two-dimensional and three-dimensional structures for virtual verification. Finally, the characterize analysis for simulating the device behavior was provided, and the output results were generated in a *csv file. The proposed algorithm of the TCADAS tool is presented below.

Algorithm 1 The proposed TCADAS algorithm.

Input: Datain consists of sub-set parameters (x_1, x_2,..., x_n)
Input: Datain essential formulas of semiconductor device for characteristic analysis (f_1, f_2,..., f_m)
while(1)
    $Mesh_{TMP}$ = Create Mesh (2D → 3D)
    if $Mesh_{TMP} \geq Mesh_{Target}$ **then**
        Mesh ← $Mesh_{TMP}$
    end if
end while
for $x_i = 1 \rightarrow n$
    fabricate $step_i$ using Athena
    if Verify($step_i$) ≥ Verify($step_{Target}$) **then**
        i = i + 1
    end if
end for
Output: Dataout structure (2D → 3D)
Characterize analysis: **export** $y_i = f_{1\rightarrow m}(x_{1\rightarrow n})$
print *.in file (all inputs) and *.csv file (all outputs)

Where:

- $x \in \{1,...,n\}$ are the fabrication variables of the device. The $x_{1\rightarrow n}$ variables are stored in a file named *.in. For instance, x_i is a set of the input parameters for each fabricated step such as the substrate creation, Nwell doping, tunnel oxide growth, gate deposition, width, length creation, etc., of the semiconductor device.
- Functions $f_j() \ \forall j \in \{1,...,m\}$ are the mathematical functions used to characterize the semiconductor device.
- $y_i = f_{1\rightarrow m}(x_{1\rightarrow n})$ are output of the characterization process. The *.csv file will be generated for all the values of y_i storage. At the same time, y_i indicates the output values like the threshold voltage, I_{ON}/I_{OFF} ratio, GCR, etc. of the device.

Regarding the imported parameters process, the parameters of a semiconductor device are defined explicitly by the researchers such as a mesh, substrate material, Nwell, tunnel oxide layer, floating gate layer, control gate layer, source/drain region values, etc. Then, the TCADAS tool classifies and presents all the input parameters in the format of the conventional TCAD tools. Finally, the TCADAS generates the *.in file used for the virtual fabrication process. Fig. 1 shows an example of the import data flow for a fabricated semiconductor device.

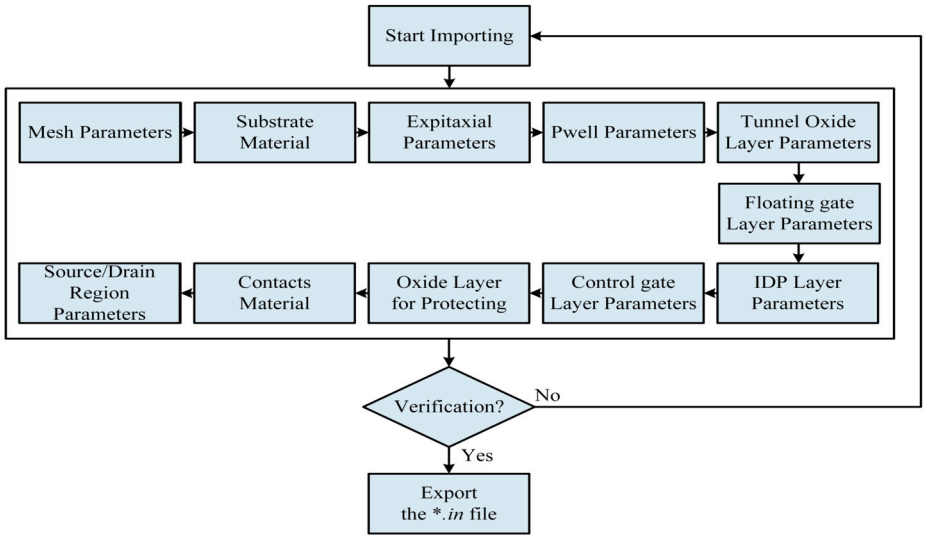

Fig. 1. The import data flow.

3. Case study for a 65 NM conventional floating-gate MOS transistor: virtual fabrication & characterization

In order to validate the TCADAS tool in a particular semiconductor device, this work proposed to study a 65 nm conventional Floating-gate MOS transistor as a case study. There are a few compelling reasons why the MOS was chosen. Firstly, as mentioned in section I, the conventional Floating-gate MOS transistor lies at the heart of the non-volatile memories, which has excellent features for non-volatile purposes [15–19]. Furthermore, the MOS has been applying other fields such as analog mixed-signals, neural networks, internet of things, etc. [20–22].

This paper presents the application of TCADAS in detail from virtual fabrication in sub-section 3.1 to complete the conventional Floating-gate MOS transistor structures, followed by output generation and extraction in sub-section 3.2, and device characterization in sub-section 3.3. This work showed that not only the TCADAS provided the automatic flow in the virtual fabrication and characterization but also the quality of the conventional Floating-gate MOS transistor is competitive. The details of this section are given as follows.

3.1. Virtual fabrication

This sub-section gives the virtual fabrication for the 65 nm conventional Floating-gate MOS transistor. The established steps for fabricating MOS transistor consist of ten steps, which are illustrated in Fig. 2. The parameters for fabricating the conventional Floating-gate MOS transistor were applied from the import process. First, we have to design an efficient mesh, which trades off between the accuracy and the simulation time. Next, the substrate creation step was implemented by using substrate doping with a fit dopant dose. Following the substrate creation, an epitaxial layer was fabricated to reduce the latch-up effect for the conventional Floating-gate MOS transistor. Subsequently, the Pwell was designed by doping the group IIIA elements in the periodic table, such as B, Al, In, at a correct temperature and duration time.

Following that, the tunnel oxide layer was designed by the dry or wet oxidation process to archive the expected thickness. That plays an essential step in the fabrication process because the thickness of the tunnel oxide layer affects significantly the performance of the device such as the memory window, the Write/Erase speeds, and the GCR. After that, this work deposited a floating gate layer for charge storage purposes. Next, the TCADAS tool created the inter-poly dielectric layer, which consists of a below-oxide layer, a middle nitride layer, and an above-oxide layer. Then, the oxidation phenomena commence forming a thick oxide layer for protecting the device. After the protective oxide layer was formed, the source/drain regions were created with the Fermi method by doping the group IIIA elements in the periodic table (such as B, Al, In) at an appropriate temperature, energy, and duration time. At the end of the design process, the Aluminum contacts were deposited on the source/drain regions.

After all the steps are completed, the TCADAS tool extracts the values of the device structure such as the tunnel oxide thickness, the IPD layer thickness, the control gate layer thickness, the channel length, the width of the device, etc. Then, we verified the values of a device structure with the design rules of the technology process. After that, the variables were implicitly created, which are used to calculate and illustrate the performances of the conventional Floating-gate MOS transistor. The diagram for the virtual fabricated conventional Floating-gate MOS transistor is given in Fig. 2. The following sub-section shows the output export process of the TCADAS tool.

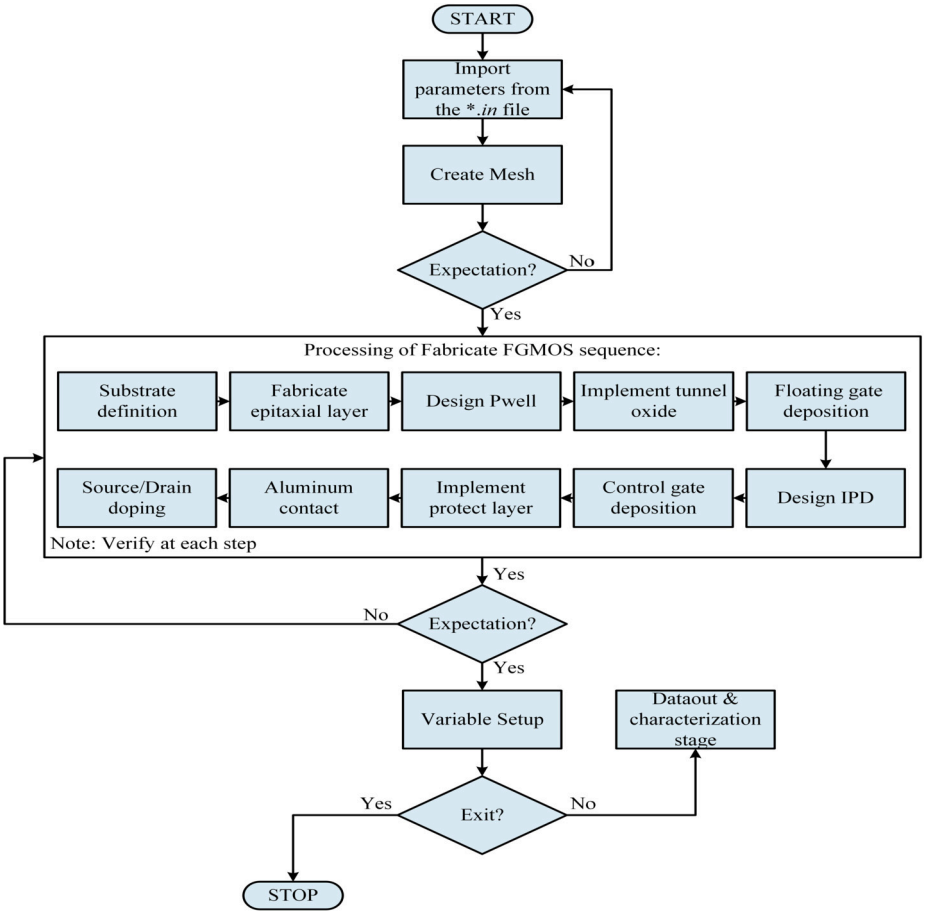

Fig. 2. The simulated fabrication process.

3.2. Output parameters generation and extraction

With regards to the output export process, the flow is divided into three stages which are the before-programming simulation, the after-programming simulation, and the erasing simulation stages. Especially, the results of each stage were formed in the *.csv file. The *.csv file is used to accurately verify and compare to the targeted specifications, and input for the next stage in the industry flow. The block diagram of the results extraction is shown in Fig. 3. The results are calculated by leveraging the equations demonstrated in [24].

Firstly, after all the input variables including the control gate voltage are established, the before-programming simulation was commenced. In this simulation, the threshold voltage and GCR of the conventional Floating-gate MOS transistor were measured. In 65 nm technology requirements for Floating-gate MOS transistor, the GCR ranges from 0.6 to 0.7. In the second stage, the after-programming simulation was launched to determine the memory window and write speed. The memory window is characterized by the threshold voltage shift during the write operation time. In the write operation, the charge is injected from the substrate to the floating gate layer. Thus, the write operation time is defined as the write speed of the conventional Floating-gate MOS transistor [24]. Finally, the erasing simulation was experimented to extract the erase speed. In contrast with the write operation, the memory window drops to zero because the charge is rejected from the floating gate layer to the substrate.

Regarding the TCADAS tool usage, at the beginning, the researchers import the parameters by using a graphic user interface. The graphic user interface consists of an Add Parameters tab, an Import Input Data tab, a Run Simulations tab, and an Export Output Data tab, which is shown in Fig. 4.

First, the Add Parameters tab is used to create parameters for the conventional Floating-gate MOS transistor fabrication. The Import Input Data tab imports these parameters of the fabrication process into the source code of the TCAD tool that is named as the *.in file, which is on the right of the Add Parameters tab. When designing a semiconductor device for a particular process, the researcher can input a value for Length (L) in the Graphic user interface (GUI) of the TCADAS tool. Besides the Import Input Data tab, the Run Simulation tab will conduct the two-dimensional structure, three-dimensional structure, and performance simulations of the conventional Floating-gate MOS transistor with the input data. When the Run Simulation tab is clicked, the virtual fabrication process is initialized by using the parameters. Then, the two-dimensional and three-dimensional structures with the mesh of the

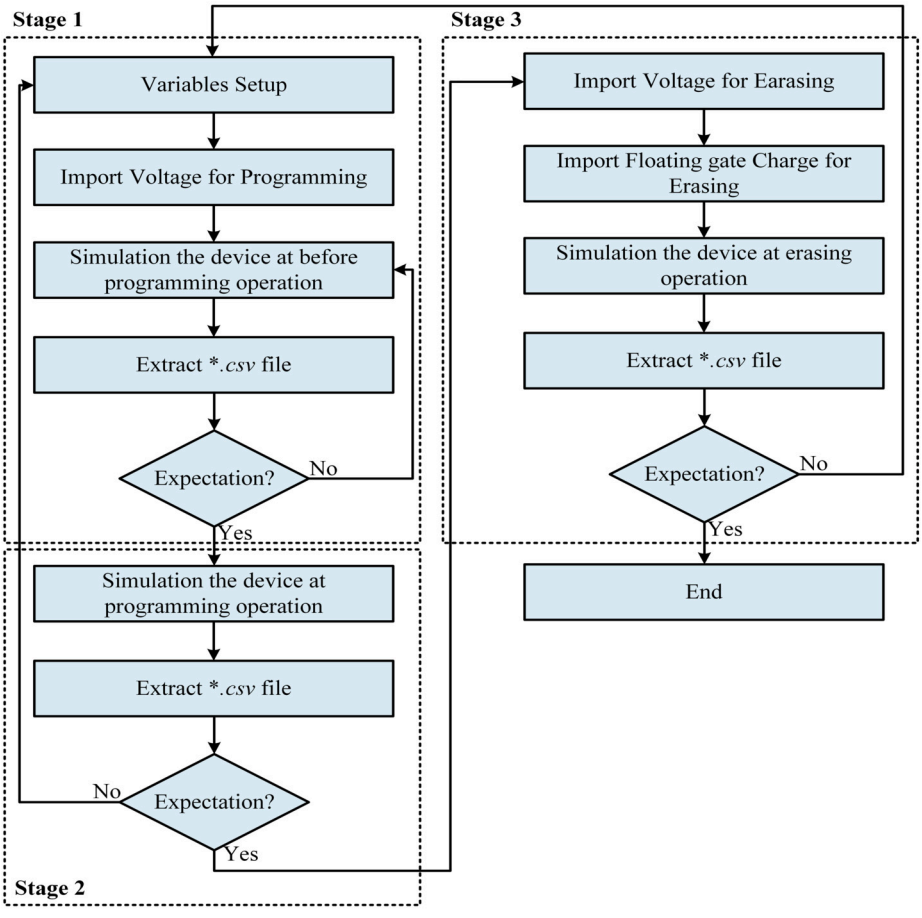

Fig. 3. The export data results flow.

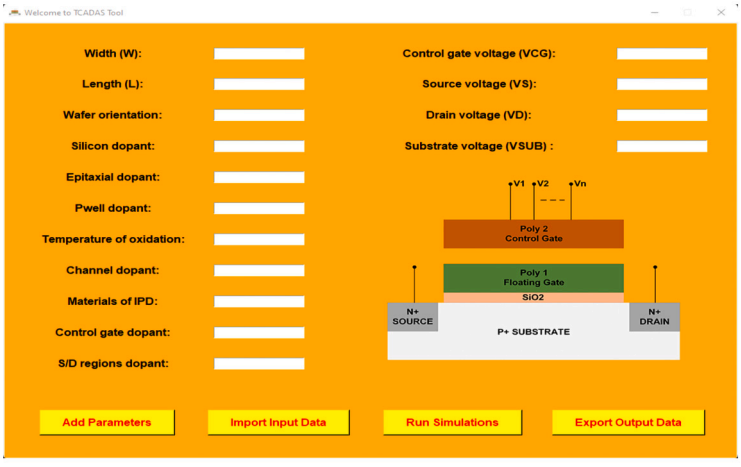

Fig. 4. Graphic user interface of TCADAS tool.

conventional Floating-gate MOS transistor in our experiment are shown in Fig. 5a and 5b, respectively. Finally, the characterization of MOS transistor is executed. However, in the conventional TCAD tool, the output of the performance simulation process is discrete data. Thus, in the proposed TCADAS tool, the Export Output Data tab was designed to collect and sort the output of the process into the *.csv file.

Fig. 5. The structure of the simulated Floating-gate MOS transistor. a. Two-dimensional mesh, b. Three-dimensional mesh.

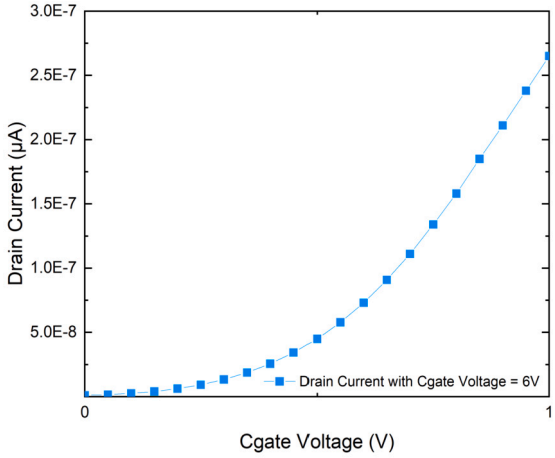

Fig. 6. I_{ON}/I_{OFF} ratio extraction.

Table 1
The value of input voltages for characterization the Floating-gate MOS transistor.

Device Performance	V_{CG} (V)	V_{Drain} (V)	V_{Source} (V)	$V_{Substrate}$ (V)	Period Time (s)	Frequency (MHz)
OFF-state current (I_{OFF})	0	1	0	0	X	X
ON-state current (I_{ON})	1	1	0	0	X	X
Before Programming	6	1	0	0	X	X
Gate Coupling Ratio	0 ÷ 18	1	0	0	X	1
In Programming	6	1	0	0	5×10^{-2}	X
After Programming	6	1	0	0	X	X
Erasing	−6	1	0	0	7×10^{-2}	X

*X was not given.

3.3. Characterization

After the detailed parameters have been imported, the virtual fabrication flow is executed. The virtual fabrication is completed, and the two-dimensional and three-dimensional structures of the conventional Floating-gate MOS transistor are shown in Fig. 5a and 5b, respectively. Then, the values of the Control Gate voltage (V_{CG}), the Drain voltage (V_{Drain}), the Source voltage (V_{Source}), and the Substrate voltage ($V_{Substrate}$) are defined and used to commence characterizing the proposed conventional Floating-gate MOS transistor.

The values of voltages are listed in Table 1. The results of our experiment on device performance are presented in the following sub-sections. In this part, I_{ON}/I_{OFF} ratio, the threshold voltage before-programming, the charge in programming, the threshold voltage after-programming, the charge in erasing operation, and GCR were extracted.

3.3.1. I_{ON}/I_{OFF} ratio

Firstly, the on-state current (I_{ON}) and off-state current (I_{OFF}) measurement for the conventional Floating-gate MOS transistor was conducted in the before-programming simulation, which is calculated from the *.csv file. Table 1 lists the conditions for the extraction of the I_{OFF} and I_{ON}. Consequently, in the Fig. 6, we can calculate the I_{OFF}, I_{ON}, and ratio as the three equations (1), (2), and (3) below.

$$I_{OFF} = 9.03 \times 10^{-10} A \tag{1}$$

$$I_{ON} = 2.65 \times 10^{-7} A \tag{2}$$

Therefore, the I_{ON}/I_{OFF} ratio is calculated by:

$$\frac{I_{ON}}{I_{OFF}} = \frac{2.65 \times 10^{-7}}{9.03 \times 10^{-10}} = 293.466 \tag{3}$$

3.3.2. The threshold voltage before-programming

Next, Fig. 7a illustrates the drain current versus the control gate voltage of the device before-programming simulation which is exported in the *.csv file. It is clear that the change in the control voltage results in a considerable change in the drain current, when the control voltage changes from 0 V to 6 V, the current witnesses a drastic increase from 9.03×10^{-10} A to 1.375×10^{-6} A, respectively. Especially, based on the graph in Fig. 7a, the value of 0.2 V is determined as the threshold voltage value of the convention Floating-gate MOS as the threshold voltage is unchanged when the control voltage continues to increase as shown in Fig. 7a.

3.3.3. The charge in the programming operation

In the simulation for programming operation, the charges are injected from the substrate to the floating gate layer. In our experiments, the charge increases from 0 C to -1×10^{-16} C during a period time of 50 ms, which was described in Fig. 7a. In Fig. 7a, the charges remain constant until 10^{-5} s and rise rapidly in the rest of the period.

3.3.4. The threshold voltage after-programming

In the next result, because of the charge movement in the programming operation, the threshold voltage of the conventional Floating-gate MOS transistor is changed. The threshold voltage shift is considered as the memory window of the MOS transistor, which is indicated in Fig. 8a. In our investigation, when the control voltage varies from 0 V to 5 V, the current observes a significant rise from 9.03×10^{-10} A to 4×10^{-7} A, respectively. Especially, based on the graph in Fig. 8b, the value of 4.2 V is determined as the threshold voltage value of the conventional Floating-gate MOS transistor after programming. Thus, the threshold voltage shift is 4 V or our memory window is 4 V.

3.3.5. The charge in the erasing operation

In the erasing operation, the Fowler-Nordheim tunneling mechanism was used for the simulation because it could provide less power consumption and tunneling efficiency of charge carriers. The results of the transient simulation are given in Fig. 7b. The charges change from -1×10^{-16} C to 0 C, which results in the threshold voltage changes from 4.2 V to 0.2 V. Moreover, the erasing speed can be determined with the value of 70 ms.

3.3.6. Gate coupling ratio measurement

Finally, the GCR extraction for the conventional Floating-gate MOS transistor is measured before-programming simulation. In order to calculate the GCR, the values of the parasitic capacitances are defined including the C_{CG-FG} is the capacitance between the control gate and floating gate, $C_{FG-Source}$ is the capacitance between the floating gate and source region, $C_{FG-Substrate}$ is the capacitance between the floating gate and substrate, $C_{FG-Drain}$ is the capacitance between the floating gate and drain region. Our tool extracted these parameters and calculated GCR by simulated results, which were stored in the *.csv file. Table 1 lists the conditions for the extraction.

We extracted the capacitances of the conventional Floating gate MOS transistor from the capacitance versus voltage characteristics which are shown in Fig. 9a. The GCR is calculated by the below equation:

$$GCR = \frac{C_{CG-FG}}{C_{CG-FG} + C_{FG-Source} + C_{FG-Substrate} + C_{FG-Drain}} \tag{4}$$

As the results of our experiments, the effect of control gate voltage on the GCR was investigated, which is illustrated in Fig. 9b. The GCR changes from 0.649 to 0.541 when the control gate voltage varies from 0 V to 18 V.

3.3.7. Fabrication experiment results

Moreover, there are data from the real fabrication of a floating gate which is the result of this TCADAS tool for drain current versus control gate voltage and drain current versus drain voltage with the dimensions of the device W/L = 0.12 um/0.1 um. Fig. 10 and Fig. 11 give the relation between the drain current versus control gate voltage in linear and log. When the control gate voltage varies from 0 V to 4 V, the drain current increases and the gap between the results of TCADAS and fabrication is reasonable even if there is a few mismatch. Besides, the relation between drain current and drain voltage is presented in Fig. 12. It is clear that the gap

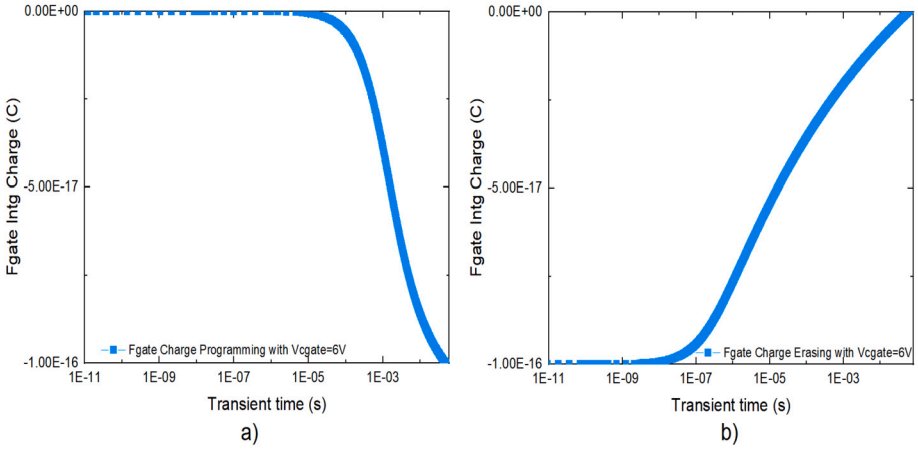

Fig. 7. The simulation results of the device in. a. programming, b. erasing.

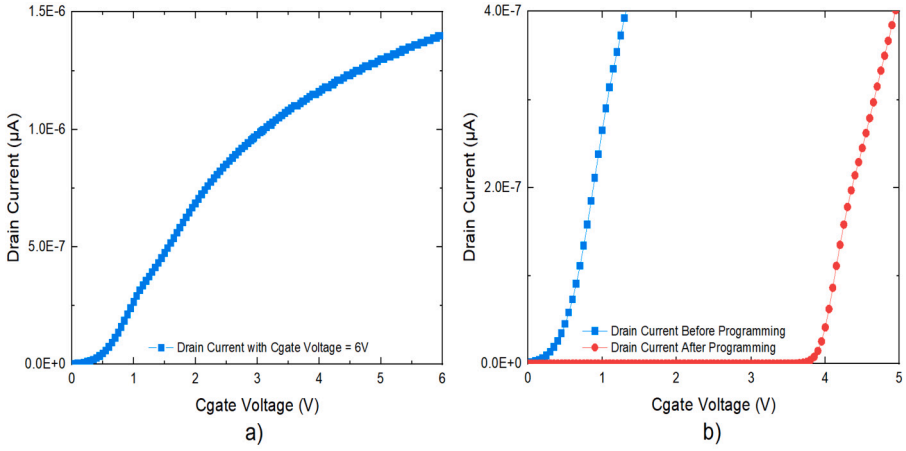

Fig. 8. The simulation results of the device in. a. before programming, b. after programming.

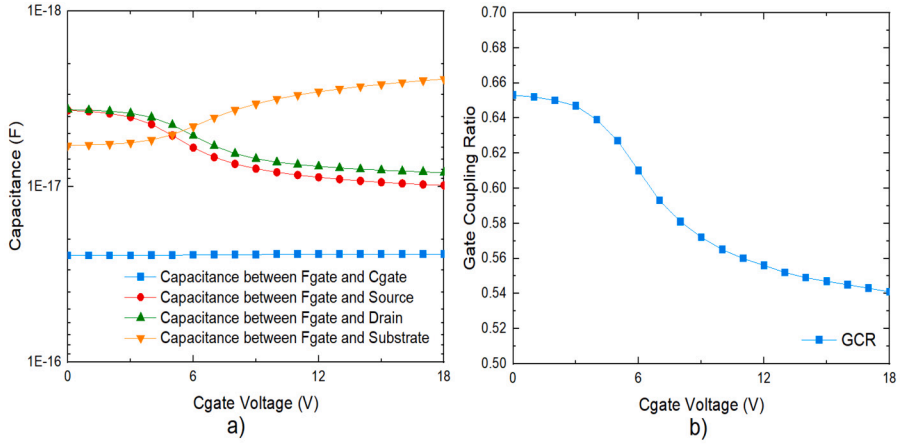

Fig. 9. The gate coupling ratio extraction.

Table 2
Performance comparison between related works.

	Unit	[16]	[17]	[19]	This work			
Device structure								
Structure	X	Conventional FG	Conventional FG	Conventional FG	Conventional FG			
Tunnel layer thickness	nm	9.75	10	7.5	9			
Tunnel layer material	X	SiO_2	SiO_2	X	SiO_2			
Storage layer thickness	nm	70	X	X	5			
Storage layer material	X	Polysilicon	X	X	Polysilicon			
IPD layer thickness	nm	13	13	X	15			
IPD layer material	X	SiO_2-Si_3N_4-SiO_2	X	X	SiO_2-Si_3N_4-SiO_2			
Device performance								
W/E Voltage	V	9.5/-5	9.5/-9.5	18/-18	9.5/-5	9.5/-9.5	18/-18	18/-18
Memory Window	V	2	9	4.3	3.3	3.3	5.9	8.3
GCR	X	X	X	X	0.645	0.645	0.645	0.645
Transient performance								
Write Speed	s	1×10^{-5}	1×10^{-5}	1×10^{-2}	5.6×10^{-4}	5.6×10^{-4}	5.6×10^{-4}	9×10^{-4}
Erase Speed	s	5×10^{-2}	5×10^{-2}	1×10^{-2}	4.09×10^{-2}	5.83×10^{-7}	1.68×10^{-10}	2×10^{-10}

*X was not given

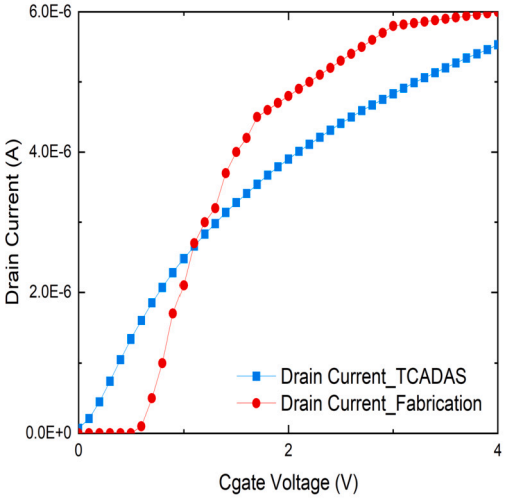

Fig. 10. The simulation results of the device in. a. TCADAS tool, b. Fabrication.

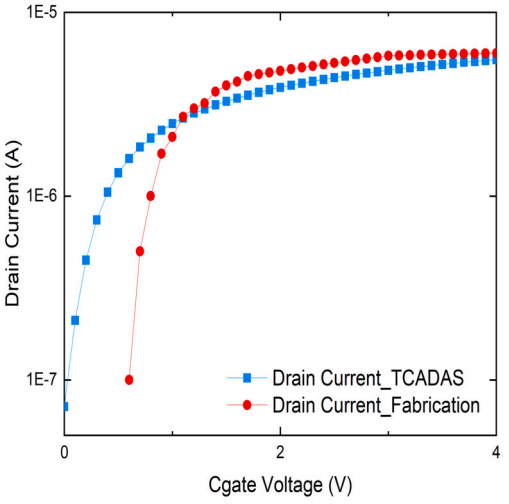

Fig. 11. The simulation results of the device in. a. TCADAS tool, b. Fabrication.

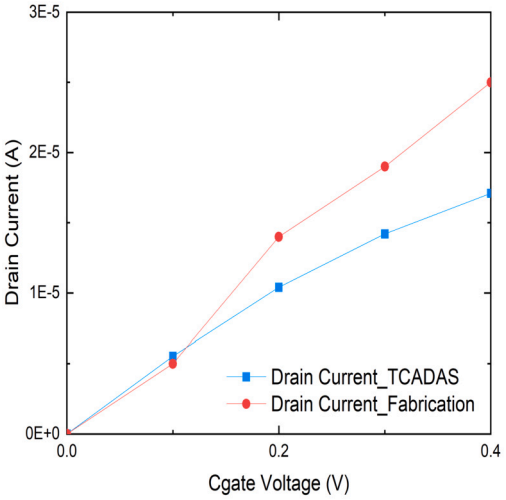

Fig. 12. The simulation results of the device in. a. TCADAS tool, b. Fabrication.

is small when the drain voltage is lesser than 0.2 V and negligible when the drain voltage is greater than 0.2 V. To sum up, although there is a gap between TCADAS results and fabricated results, the results show that the virtual nature of the work can be realized physically when it is necessary.

3.3.8. Performance comparison with related works

In this sub-section, Table 2 compares the performance of the Floating-gate MOS transistor, which was simulated from the TCADAS, with the three previously published works [16,17,19].

In [16], the authors proposed a method to improve the quality of the tunnel oxide layer process in the real fabricated condition. The study proposed the use of an additional sacrificial oxide layer growth which carries out the uniformity for the layer and reduced the interface traps during the programming and erasing operations of the device. However, when compared with the device designed by the TCADAS tool, the performance of the device in this work is much better compared to the study [16]. Especially, for the most important value of the floating gate device is the memory window, the value of this work is 3.3 V whereas the value of the work [16] is only 2 V with the same input voltages of 9.5/-5 V. Regarding the speeds, as in the manuscript, the compatible results of write and erase speeds are presented.

In [17], the floating-gate MOS transistor was fully fabricated with a good memory window of 9 V when the input voltages are 9.5/-9.5 V. However, when comparing the tunnel oxide layer thickness, it is 10 nm while our study can obtain 9 nm. Whereas the compatible write speed is between 10^{-5} s and 5.6×10^{-4} s, the huge differences in erase speeds were given in Table 2. In [17], the erase speed is only 5×10^{-2} s and our work is extraordinary with a value of 5.83×10^{-7} s. The reason why the work [17] has a large memory window and low erasing speed is because the post-metallization anneal (PMA) was taken into account in the fabrication process. The PMA will induce the water-related trapped near the SiO2 interface which reduces the electric field of the erasing. Moreover, the erase time is increased when the programming and erasing cycles increase. Therefore, the author in [17] also suggested skipping the PMA process since its drawbacks.

In [19], the arch-active structure was fabricated which can solve the industry demains such as small on-cell current, low writing speed, and current fluctuation. However, compared to the floating-gate MOS structure from the TCADAS tool, the performances of our study are much better in terms of memory window and speeds. When it comes to the memory window, while our structure can obtain a very large value of 8.3 V, the study [19] only archives 4.3 V. Regarding the speeds, the extraordinary write and erase speeds of this work are 9×10^{-4} s and 2×10^{-10} s, respectively. In work [19], the speeds are 10^{-2} s for both speeds only.

4. Conclusion

This paper successfully proposed a methodology of virtual fabrication for semiconductor devices and designed a tool called TCADAS (Technology Computer-Aided Design Automatic Simulation). The TCADAS tool can perform an entirely virtual fabrication, device simulation, process variation, and output extraction. Moreover, the TCADAS provided a solution for automatic simulation to reduce the effort in massive manual work and simulation time. In addition, a design of the 65 nm conventional Floating-gate MOS transistor was performed by applying the TCADAS tool. This work showed that not only the TCADAS archived the automatic flow in the virtual fabrication and characterization, but also the quality of the conventional Floating-gate MOS transistor is competitive with the published studies. The memory window, I_{ON}/I_{OFF} ratio, GCR, and Write/Erase speeds are 4 V, 293.466, 0.645, 50 ms/70 ms with the default input settings, respectively. Besides, the input control gate voltages are low, with the 6/-6 V values, and the thin tunnel oxide layer is 9 nm. Regarding future works, the TCADAS tool will be upgraded in order to adopt the new structure of semiconductor devices such as Fin Field-Effect transistor (FinFET) and Gate-All Around Field-Effect transistor

(GAAFET). Furthermore, data from the TCADAS tool was uploaded to Github as an open-source tool for studying and investigating the semiconductor devices further by users and researchers with the links: https://github.com/Steve-Dang459/tcadas.git or https://github.com/hoangtranghcmut/tcadas.

CRediT authorship contribution statement

Thinh Dang Cong: Formal analysis, Investigation, Methodology, Software, Writing – original draft, Writing – review & editing. **Trang Hoang:** Supervision, Formal analysis, Methodology, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data associated with the study has been deposited into a publicly available repository. Data was uploaded to GitHub: https://github.com/Steve-Dang459/tcadas.git or https://github.com/hoangtranghcmut/tcadas.

Acknowledgement

We acknowledge the support of time and facilities from Ho Chi Minh City University of Technology (HCMUT), VNU-HCM for this study.

References

[1] W. Hu, Z. Sheng, X. Hou, H. Chen, Z. Zhang, D.W. Zhang, P. Zhou, Ambipolar 2d semiconductors and emerging device applications, Small Methods 5 (1) (2021) 2000837.
[2] S. Sahoo, Conduction and switching behavior of e-beam deposited polycrystalline Nb_2O_5 based nano-ionic memristor for non-volatile memory applications, J. Alloys Compd. 866 (2021) 158394.
[3] S. Preethi, M. Venkatesh, M. Karthigai Pandian, G. Lakshmi Priya, Analytical modeling and simulation of gate-all-around junctionless MOSFET for biosensing applications, Silicon 13 (10) (2021) 3755–3764.
[4] S. Chander, R. Chaudhary, S.K. Sinha, TCAD analysis of tunnel field effect transistor using Ge material for low power application, Mater. Today Proc. 50 (2022) 2398–2403.
[5] A. Hamzah, N.E. Alias, R. Ismail, Low-voltage high-speed programming gate-all-around floating gate memory cell with tunnel barrier engineering, Jpn. J. Appl. Phys. 57 (6S3) (2018) 06KC02.
[6] D. Kang, H. Shin, Improving the cell characteristics using arch-active profile in NAND flash memory having 60 nm design-rule, Solid-State Electron. 54 (11) (2010) 1263–1268.
[7] C.T. Dabhi, G.C. Patil, Underlap channel silicon-on-insulator quantum dot floating-gate MOSFET for low-power memory applications, J. Comput. Electron. 15 (4) (2016) 1563–1569.
[8] R. Dhavse, K. Prashant, C. Dabhi, A. Darji, R. Patrikar, Fabrication and investigation of low-voltage programmable flash memory gate stack, in: Proceedings of the International Conference on Microelectronics, Computing & Communication Systems: MCCS 2015, Springer, 2018, pp. 35–49.
[9] P. Pavan, L. Larcher, A. Marmiroli, Floating Gate Devices: Operation and Compact Modeling, Springer Science & Business Media, 2007.
[10] T. Ikegami, K. Fukuda, J. Hattori, H. Asai, H. Ota, A TCAD device simulator for exotic materials and its application to a negative-capacitance FET, J. Comput. Electron. 18 (2019) 534–542.
[11] F.R. Palomo Pinto, Y. Gurimskaya, E.G. Villani, M. Moll, J. Schwandt, R. Millán, Sissa: TCAD device simulations of irradiated silicon detectors, PoS (2020) 051.
[12] K. Ko, J.K. Lee, M. Kang, J. Jeon, H. Shin, Prediction of process variation effect for ultrascaled GAA vertical FET devices using a machine learning approach, IEEE Trans. Electron Devices 66 (10) (2019) 4474–4477.
[13] J. Hattori, T. Ikegami, K. Fukuda, Technology computer-aided design simulation of phonon heat transport in semiconductor devices, Jpn. J. Appl. Phys. 60 (SB) (2021) SBBA03.
[14] T. Dutta, C. Medina-Bailon, A. Rezaei, D. Nagy, F. Adamu-Lema, N. Xeni, Y. Abourrig, N. Kumar, V.P. Georgiev, A. Asenov, TCAD simulation of novel semiconductor devices, in: 2021 IEEE 14th International Conference on ASIC (ASICON), IEEE, 2021, pp. 1–4.
[15] J.E. Sanchez, Q. Chen, Element edge based discretization for TCAD device simulation, IEEE Trans. Electron Devices 68 (11) (2021) 5414–5420.
[16] S. Chiu, Y. Xu, X. Ji, Y. Liao, F. Wu, F. Yan, An advanced tunnel oxide layer process for 65 nm nor floating-gate flash memories, Semicond. Sci. Technol. 30 (10) (2015) 105032.
[17] S. Chiu, Y. Xu, X. Ji, F. Yan, Investigation of impact of post-metallization annealing on reliability of 65 nm nor floating-gate flash memories, Solid-State Electron. 126 (2016) 125–129.
[18] D. Shum, J. Power, R. Ullmann, E. Suryaputra, K. Ho, J. Hsiao, C. Tan, W. Langheinrich, C. Bukethal, V. Pissors, et al., Highly reliable flash memory with self-aligned split-gate cell embedded into high performance 65 nm cmos for automotive & smartcard applications, in: 2012 4th IEEE International Memory Workshop, IEEE, 2012, pp. 1–4.
[19] D. Kang, H. Shin, Improving the cell characteristics using arch-active profile in NAND flash memory having 60 nm design-rule, Solid-State Electron. 54 (11) (2010) 1263–1268.
[20] G. Servalli, D. Brazzelli, E. Camerlenghi, G. Capetti, S. Costantini, C. Cupeta, D. DeSimone, A. Ghetti, T. Ghilardi, P. Gulli, et al., A 65 nm nor flash technology with 0.042/spl mu/m/sup 2/cell size for high performance multilevel application, in: IEEE InternationalElectron Devices Meeting, 2005, in: IEDM Technical Digest., IEEE, 2005, pp. 849–852.
[21] E. Bestelink, O. de Sagazan, L. Motte, M. Bateson, B. Schultes, S.R.P. Silva, R.A. Sporea, Versatile thin-film transistor with independent control of charge injection and transport for mixed signal and analog computation, Adv. Intell. Syst. 3 (1) (2021) 2000199.

[22] S. Agarwal, D. Garland, J. Niroula, R.B. Jacobs-Gedrim, A. Hsia, M.S. Van Heukelom, E. Fuller, B. Draper, M.J. Marinella, Using floating-gate memory to train ideal accuracy neural networks, IEEE J. Explor. Solid-State Comput. Devices Circuits 5 (1) (2019) 52–57.

[23] T. Kim, K. Park, T. Jang, M.-H. Baek, Y.S. Song, B.-G. Park, Input-modulating adaptive neuron circuit employing asymmetric floating-gate MOSFET with two independent control gates, Solid-State Electron. 163 (2020) 107667.

[24] C. Zhang, S.R. Hasan, A new floating-gate MOSFET model for analog circuit simulation and design, Analog Integr. Circuits Signal Process. 101 (2019) 1–11.