

Article

# A CMOS PSR Enhancer with 87.3 mV PVT-Insensitive Dropout Voltage for Sensor Circuits

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**Abstract:** A new power supply rejection (PSR) based enhancer with small and stable dropout voltage is presented in this work. It is implemented using TSMC-40 nm process technology and powered by 1.2 V supply voltage. A number of circuit techniques are proposed in this work. These include the temperature compensation for Level-Shifted Flipped Voltage Follower (LSFVF) and the Complementary-To-Absolute Temperature (CTAT) current reference. The typical output voltage and dropout voltage of the enhancer is 1.1127 V and 87.3 mV, respectively. The Monte-Carlo simulation of this output voltage yields a mean *T.C.* of 29.4 ppm/°C from −20 °C and 80 °C. Besides, the dropout voltage has been verified with good immunity against Process, Temperature and Process (PVT) variation through the worst-case simulation. Consuming only 4.75 μA, the circuit can drive load up to 500 μA to yield additional PSR improvement of 36 dB and 20 dB of PSR at 1 Hz and 1 MHz, respectively for the sensor circuit of interest. This is demonstrated through the application of an enhancer on the instrumentation Differential Difference Amplifier (DDA) for sensing floating bridge sensor signal. The comparative Monte-Carlo simulation results on a respective DDA circuit have revealed that the process sensitivity of output voltage of this work has achieved 14 times reduction in transient metrics with respect to that of the conventional counterpart over the operation temperature range in typical operation condition. Due to simplicity without voltage reference and operational amplifier(s), low power and small consumption of supply voltage headroom, the proposed work is very useful for supply noise sensitive analog or sensor circuit applications.

**Keywords:** PSR enhancer; regulator; dropout voltage; temperature compensation; current reference; voltage reference; FVF circuit; PVT variation; sensor circuit; Differential Difference Amplifier; operational amplifier



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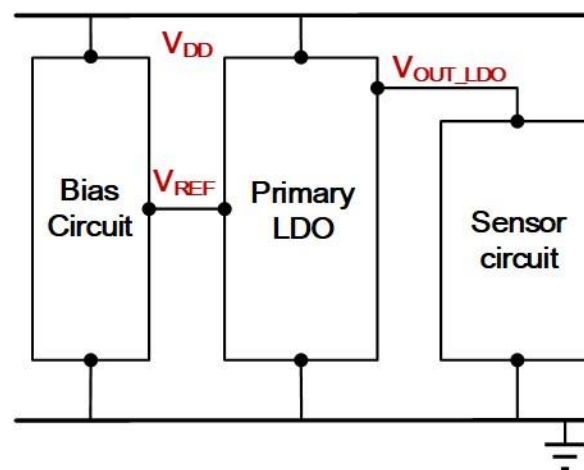


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## 1. Introduction

With the continuous advancement of integrated circuit design and manufacturing technology, sensor circuits and systems tend to be integrated together on one single chip. For analog circuits, especially sensor circuits, a high-quality supply source is often needed to maintain their function and accuracy. Although specific circuit methods can be employed to improve the performance of sensor circuits arising from the reduced supply sensitivity in VCO based sensor [1] and reduced supply noise in image sensor [2], these methods are only applicable for the limited case examples. In order to increase power supply rejection (PSR), the sensor circuit employing the feedback design [3,4] to the bridge sensing elements is a popular method. However, it relies on splitting a full bridge sensing element into two half bridge sensors. This may not be adequate for many general applications. Due to the feedback mechanism, the loop gain, and the stability become the critical parameters that deal with the PSR performance and frequency compensation, respectively. Besides, other temperature sensors [5–7] and an optical mouse sensor [8] have addressed the importance of supply issues based on the impact of supply sensitivity or supply noise on the sensor circuit performance. Regarding recent trend towards low-power consumption, one of the

previously reported supply circuits [9] can consume low power. Unfortunately, the circuit topology suffers from the disadvantage of requiring higher supply. Therefore, low-power low-voltage performance becomes one of main agendas in sensor circuit design. The exemplary circuits are low-voltage, low dropout wireless sensor node [10] and low-power low-voltage biomedical sensor IC [11]. Based on the above discussed sensor applications, the Low Dropout (LDO) Regulator is regarded as the common building block used to produce a stable supply voltage to sustain the sensor circuit performance whilst providing adequate PSR as another important characteristic in sensor circuits and systems. Figure 1 shows the general structure of a sensor circuit powered by a LDO regulator in which a voltage reference is generated by a bias circuit to define the output voltage of a regulator.



**Figure 1.** A Sensor Circuit Powered by a LDO Regulator.

However, in the event that the PSR offered by the regulator is not adequate, a PSR enhancer [12], which usually serves as the secondary regulator, can be employed in analog circuit design. The exemplary circuit block diagram is depicted in Figure 2. As can be seen, the enhancer comprises a voltage reference and a LDO regulator with scaling function. Its output voltage,  $V_{OUT}$ , is designed to be close to the primary LDO regulator output line in which the output voltage is denoted as  $V_{OUT\_LDO}$ . The difference between  $V_{OUT}$  and  $V_{DD\_OUT}$  of the PSR enhancer defines the dropout voltage. Such the dropout voltage should be made as small as possible in order to offer maximal operation headroom because the price paid for that will be the reduction of sensor supply headroom. More importantly, when the sensor circuit is targeted for low voltage applications, this raises the design challenges about the stability of dropout voltage contributed by the PSR enhancer in context of process, voltage, and temperature (PVT) variation. This is then translated to the problems arising from the stability of the enhancer's voltage reference, as well as its driving LDO circuit, with the ultimate goal to produce a small dropout voltage which can sustain the proper operation of a PSR enhancer. For an example, consider a dropout voltage of 0.1 V from 1.2 V supply voltage or below in a sensor circuit, this requires a lot of circuit design considerations dedicated to low-power low-supply voltage reference design, as well as scaling regulator design in conjunction with simultaneously addressing PSR concerns. Apart from that, the PSR enhancer serves as an extra block in the sensor applications, thus increasing the cost as the penalty. To relax the issue, the circuit topology of the PSR enhancer should be designed with simplicity. This raises the motivation of this work to design a cost-effective PSR enhancer, not only to improve PSR, but also to produce a stable and small dropout voltage with good immunity against the PVT variation.

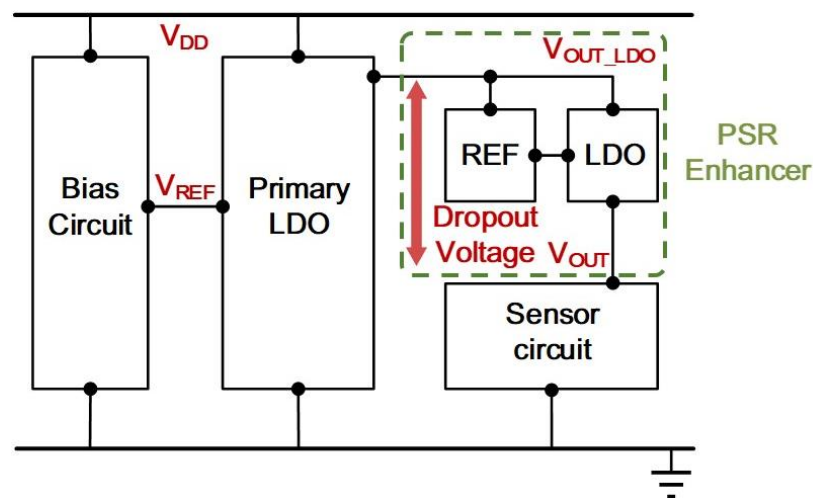


Figure 2. A Sensor Circuit Powered by a LDO Regulator with a PSR Enhancer.

## 2. Conventional PSR Enhancer Circuit and Its Design Considerations

PSR enhancers with low dropout voltage are necessary for sensitive or accurate sensor circuits. To meet the requirement of high PSR for sensor circuit in low-voltage low-power applications, circuit design considerations are conducted. At this juncture, MOSFET device operated in the sub-threshold region [13] is often preferred over the Bipolar Junction Transistor (BJT) counterparts [14]. To provide the driving characteristic, a LDO regulator or buffer-like operational amplifier (op-amp) circuit is often needed. Of particular note, the regulator/buffer should be arranged in a separate driving stage design, rather than embedding with the voltage reference in the topology of the merged design. The reason for using cascade topology is that any influence arising from the small dropout voltage will not contribute the stress to the output of the voltage reference stage if it were designed with an embedded buffer. It is important to note that sufficient headroom allowed for the voltage reference output is easily scaled to the targeted dropout voltage through the regulator or op-amp, etc. with a scaling network. Attention is also paid to the PSR issue, which pertains to the circuit topology or frequency compensation technique in regulator or op-amp design. Furthermore, the output stage of the regulator or op-amp buffer should tolerate the change of dropout voltage without deteriorating the open-loop gain function, as the change of dropout voltage will stress the output transistor of the regulator or op-amp based buffer circuit.

Based on these design considerations, an exemplary op-amp based PSR enhancer that features good PSR topology [15,16] for the enhancer design is depicted in Figure 3. The enhancer comprises a reference voltage generator and a LDO regulator.

For the Reference Voltage Generator,  $M_1$  and  $M_2$  work in the subthreshold region. As such, the temperature characteristic similar to that of BJT. The  $V_{REF}$ , which is equal to  $V_{SG1}$  plus  $V_{R1}$ , is a combination of PTAT and CTAT voltage. The output of OA1 yields the reference voltage as:

$$V_{REF}(T) = V_{SG1}(T) + \frac{R_1}{R_2} nV_T \ln\left(\frac{S_2}{S_1}\right) \quad (1)$$

where  $S_1$  and  $S_2$  are the aspect ratio of  $M_1$  and  $M_2$ , respectively. Thus, a temperature insensitive,  $V_{REF}$ , can be realized through adjusting the ratio of  $R_1$  and  $R_2$ . Besides, the employment of sub-threshold based MOS transistors permits the reference voltage generator to operate at low supply voltage and consume low power. The OA1, shown in Figure 4, is a PMOS-input two-stage amplifier with a source follower output stage to avoid the resistive loading effect that influences the open-loop function, resulting in the degradation of PSR. Due to the use of source follower, the output headroom is reduced at the trade-off of  $V_{REF}$  and is unable to produce the small dropout voltage design. Regarding the low-dropout voltage design requirement,  $V_{REF}$  denoted in Figure 3, will be scaled

in the LDO regulator through the scale factor  $(1 + R_4/R_5)$ . To minimize the regulator's circuit complexity, the power transistor stage can be arranged to cascade with the first-stage differential amplifier  $OA2$  to form a two-stage amplifier topology as shown in Figure 5. The well-known cascode compensation technique [17] is applied to obtain a good PSR metric. Finally, the size of each component pertaining to Figures 3–5 in the conventional enhancer design is listed in Table 1.

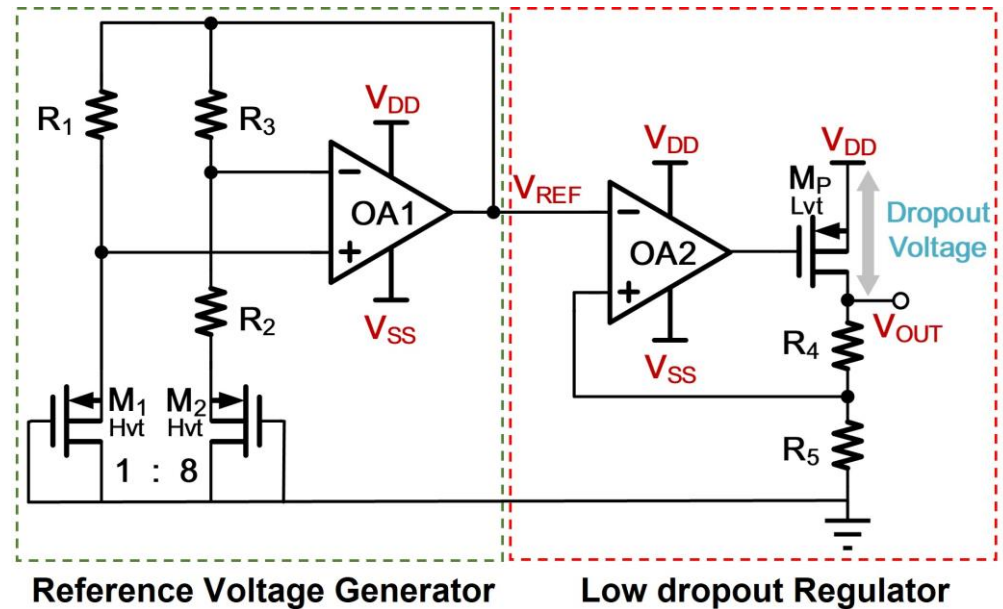


Figure 3. Conventional PSR Enhancer with PSR Design Aware.

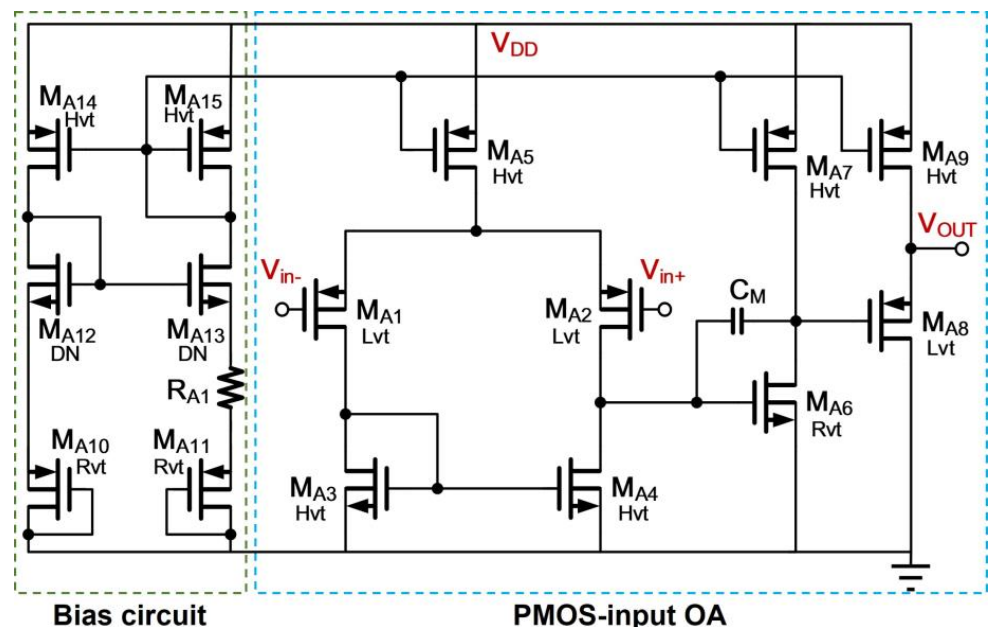


Figure 4. Schematic of  $OA1$  for Reference Voltage Generator in Enhancer.

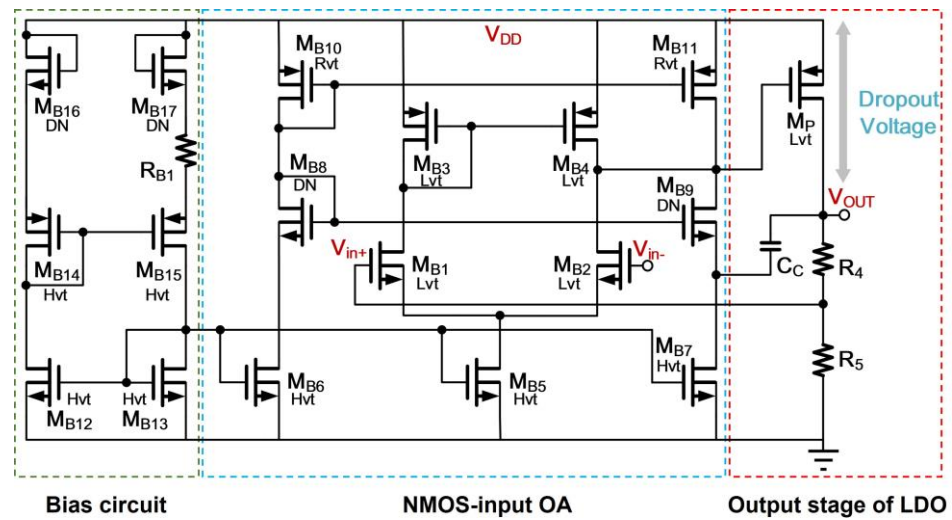


Figure 5. Schematic of OA2 for Regulator in Enhancer.

Table 1. Sizes of the Devices in the Conventional Design.

Device	Size	Device	Size
$M_1$	40/4 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B1,2}$	10/0.5 ( $\mu\text{m}/\mu\text{m}$ )
$M_2$	320/4 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B3,4}$	10/2 ( $\mu\text{m}/\mu\text{m}$ )
$M_P$	1000/0.16 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B5}$	8.7/1 ( $\mu\text{m}/\mu\text{m}$ )
$M_{A1,2}$	50/1 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B6,7}$	5.6/1 ( $\mu\text{m}/\mu\text{m}$ )
$M_{A3,4}$	3/1 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B8,9}$	2/0.5 ( $\mu\text{m}/\mu\text{m}$ )
$M_{A5}$	2/1 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B10,11}$	10/1 ( $\mu\text{m}/\mu\text{m}$ )
$M_{A6}$	1.7/1 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B12,13}$	5/1 ( $\mu\text{m}/\mu\text{m}$ )
$M_{A7}$	1.4/1 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B14,15}$	2/0.16 ( $\mu\text{m}/\mu\text{m}$ )
$M_{A8}$	20/2 ( $\mu\text{m}/\mu\text{m}$ )	$M_{B16,17}$	4/2 ( $\mu\text{m}/\mu\text{m}$ )
$M_{A9}$	10/1 ( $\mu\text{m}/\mu\text{m}$ )	$R_1$	283 k $\Omega$
$M_{A10,11}$	6/1 ( $\mu\text{m}/\mu\text{m}$ )	$R_2$	99 k $\Omega$
$M_{A12,13}$	5/0.2 ( $\mu\text{m}/\mu\text{m}$ )	$R_3$	283 k $\Omega$
$M_{A14,15}$	1/1 ( $\mu\text{m}/\mu\text{m}$ )	$R_4$	515 k $\Omega$
$R_{A1}$	18.9 k $\Omega$	$R_5$	614 k $\Omega$
$R_{B1}$	27.8 k $\Omega$	$C_M$ for OA1	0.8 pF
		$C_C$ for OA2	0.4 pF

### 3. Proposed PSR Enhancer with PVT-Insensitive Dropout Voltage

#### 3.1. Proposed Enhancer Design

The proposed PSR enhancer is shown in Figure 6. It is composed of the Level-Shifted Flipped Voltage Follower (LSFVF) [18] based on the LDO regulator and the CTAT bias current generator with a capacitive start-up circuit. The FVF based regulator has the key advantage of simplicity. The use of LSFVF topology is to relax the power transistor operation headroom at the expense of a slight increase in complexity. This is considered an important design consideration due to small dropout voltage requirement. Moreover, the LSFVF topology also provides a fast response in terms of transient performance, even biased with low quiescent conditions. This helps to reduce the transient spikes in the supply line of low-power sensor circuit. Referring to the LSFVF regulator, it consists of the power transistor  $M_8$ , the control transistor  $M_7$ , the cascode current source with transistors  $M_{11}$  and  $M_{12}$ , and the source follower-based level shifter with transistors  $M_9$  and  $M_{10}$ . The intrinsic dc biasing to the control transistor  $M_7$  is obtained from the composite transistor ( $M_5$  and  $M_6$ ) with the cascode current source ( $M_{13}$  and  $M_{14}$ ) and the pseudo-resistor [19] based low-pass filter (LPF). Further details of the design of LPF will be discussed in the subsequent Section. Of particular note, in order to avoid the influence of leakage effect to the dc biasing of control transistor  $M_7$ , high threshold transistors  $M_5$ ,  $M_6$ , and  $M_7$



are employed. Such the biasing implementation has the key advantage of eliminating the complicated voltage generator as well as voltage reference in typical FVF regulator design [20]. Good PSR is still obtained due to the use of LPF for filtering the dc supply noise. As the result, the proposed topology offers a more compact topology with respect to that of the conventional counterpart.

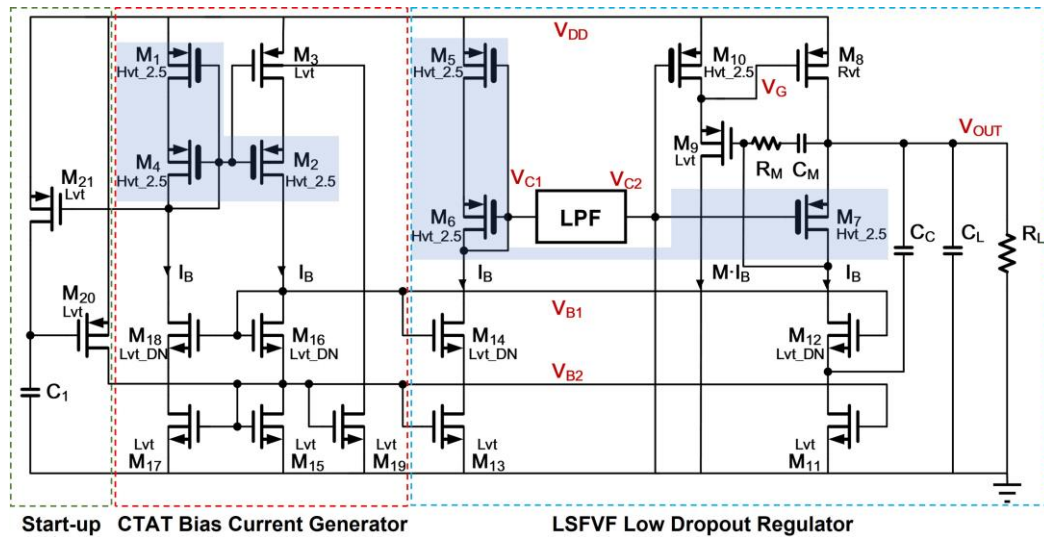


Figure 6. Proposed PSR Enhancer.

Regarding the biasing circuit in Figure 6, it is designed in a form of a new CTAT current source, comprising transistors  $M_1$ – $M_4$  and  $M_{15}$ – $M_{19}$  together with the start-up network comprising transistors  $M_{20}$ – $M_{21}$  and a capacitor  $C_1$ . This self-biasing network usually performs PTAT current generation in a conventional design. However, by connecting the gate of triode transistor  $M_3$  to the gate of the composite transistor ( $M_1$  and  $M_4$ ), it is possible that the negative temperature coefficient ( $T.C.$ ) effect of the triode transistor dominates the PTAT effect arising from the current source topology. Consequently, the current source behaves CTAT characteristic. However, the concern is that under high temperature and fast corner case, the transistor  $M_3$  may cut off itself. In order to sustain the operating temperature range for 100 degree C, a limited current is injected to the bulk of  $M_3$  so as to reduce its threshold voltage.

The rationale for this design is that the replica clamping structure formed by  $M_1$ ,  $M_4$  and  $M_2$  in the biasing circuit matches the clamping structure formed by  $M_5$ ,  $M_6$  and  $M_7$  in the LSFVF topology. Therefore, the design has addressed the tracking issue so as to minimize the impact on the dropout voltage in the presence of process variation. Besides, the generated  $\Delta V_{SG}$  in each structure is almost independent of supply voltage change. This is translated to the dropout voltage insensitive to the supply voltage. Finally, referring to the temperature compensation, the generated CTAT current will compensate the change of dropout voltage against the temperature. Consider the output voltage of LSFVF regulator, it decreases with increasing temperature due to the PTAT effect of clamping structure ( $M_5$ – $M_7$ ). In other words, the increase in dropout voltage comes from the increase in temperature. Besides, it is interesting to observe that if the loop produced by the source-gate voltage of  $M_8$ , the source-gate voltage of  $M_9$  and the source-drain voltage of  $M_7$  are made negative  $T.C.$ , it is able to compensate the positive  $T.C.$  introduced by the clamping structure ( $M_5$ – $M_7$ ). However, if a long channel transistor of  $M_7$  is employed with small channel length modulation (CLM) effect, its  $V_{SD7}$  will absorb the temperature-induced voltage change caused by the sum of source-gate voltages through  $M_8$  and  $M_9$ . Therefore, it may be difficult to impose the negative  $T.C.$  voltage change caused by  $V_{SG8}(T)$  and  $V_{SG9}(T)$  on  $V_{OUT}(T)$ . To tackle the issue, the CTAT current source and the short-channel length  $M_7$  with CLM effect are employed in this proposed design; this permits  $V_{SD7}(T)$  to behave

negative  $T.C.$  characteristic. Further proof will be given in the subsequent Section. As such, the combined negative  $T.C.$  contributed by the temperature compensation transistor structure ( $M_7$ – $M_9$ ) becomes the key part for temperature compensation. In brief, due to the use of the replica structure, simple temperature compensation in the topological network and all transistor-based designs for obtaining a better tracking characteristic, the dropout voltage of the PSR enhancer is almost independent of PVT variation. This yields a stable output voltage from the enhancer to power the sensor circuit of interest.

Regarding the frequency compensation of the regulator, it is stabilized by the cascode compensation [21] in conjunction of Miller RC frequency compensation. This leads to good stability under low quiescent power design.

### 3.2. Low-Pass Filter in PSR Enhancer

The LPF circuit is depicted in Figure 7. Taking into account the small silicon area design, it is based on a first-order filter design using a pseudo resistor  $R_F$  and a MOS capacitor  $C_F$ . The pseudo resistor comprises 5 units ( $M_{R1}$ – $M_{R5}$ ) in series topology to realize a large resistance for use in low frequency, which starts from 1 Hz and above. Due to the extremely large value, high threshold MOS transistors are employed in order to reduce the leakage current. This suggests the potential  $V_{C1}$  is close to  $V_{C2}$ . Regarding the MOS capacitor, it is based on a thick-oxide MOS high-threshold transistor with the gate as the top plate terminal and the shorted drain-source and bulk to form the bottom plate terminal. The formation of a large time constant by the LPF will cause the slow start-up of the circuit. To tackle this issue, a digital start-up, which comprises a capacitive start-up network formed by a transistor  $M_{22}$ , six inverter transistors ( $M_{23}$ – $M_{28}$ ), a capacitor  $C_2$  and five MOS switching transistors ( $M_{29}$ – $M_{33}$ ), which are connected in parallel with respective pseudo resistor unit, is proposed. When the system is powered on, a peak voltage of  $V_{C3}$  will appear due to the charging of  $C_2$ . Hence, a reversed pulse signal is generated on  $V_{C4}$ , which will turn on the switches realized by  $M_{29}$  to  $M_{33}$ . This allows  $V_{C1}$  to charge  $C_F$  rapidly. After the pulse signal, all the switches will be turned off. Then, the LPF establishes a RC circuit with a charged  $C_F$  to provide the dc biasing. Of particular note, the off resistance of each MOS switch is not infinite. It will reduce the MOS pseudo resistor unit resistance value when paralleling with a non-ideal OFF switch. This leads to the employment of five serial pseudo resistors. Nevertheless, the effective silicon area of each pseudo resistor is considered small. The penalty for the increase of pseudo resistors is of little concern.

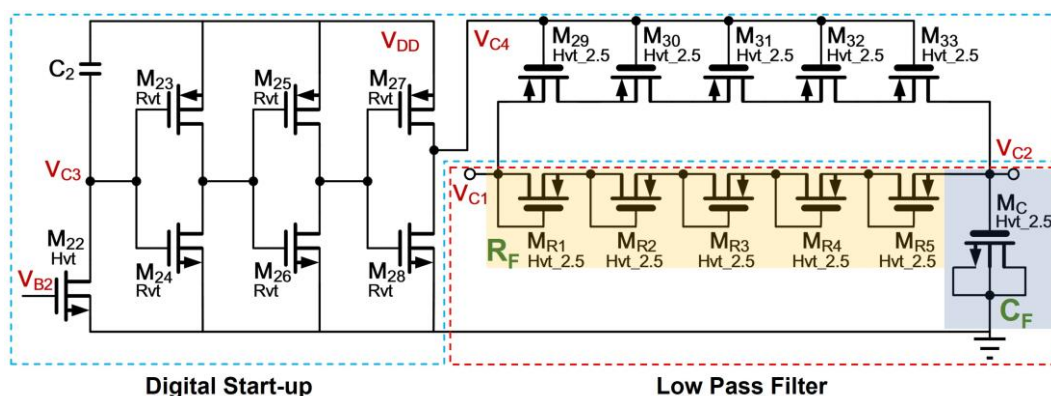


Figure 7. Low pass filter with digital start-up.

The size of each component, which are pertaining to the proposed PSR enhancer in Figure 6 and the low pass filter in Figure 7 are given in Table 2.

**Table 2.** Sizes of the devices in the proposed design.

Device	Size	Device	Size
$M_1$	1.7/0.3 ( $\mu\text{m}/\mu\text{m}$ )	$M_{22}$	0.32/4 ( $\mu\text{m}/\mu\text{m}$ )
$M_{2,4}$	20/0.3 ( $\mu\text{m}/\mu\text{m}$ )	$M_{23,25,27}$	4/0.04 ( $\mu\text{m}/\mu\text{m}$ )
$M_3$	2.1/4.5 ( $\mu\text{m}/\mu\text{m}$ )	$M_{24,26,28}$	2/0.04 ( $\mu\text{m}/\mu\text{m}$ )
$M_5$	3/0.3 ( $\mu\text{m}/\mu\text{m}$ )	$M_{29-33}$	0.32/1 ( $\mu\text{m}/\mu\text{m}$ )
$M_{6,7}$	14/0.3 ( $\mu\text{m}/\mu\text{m}$ )	$M_{R1-R5}$	0.32/1 ( $\mu\text{m}/\mu\text{m}$ )
$M_8$	1000/0.16 ( $\mu\text{m}/\mu\text{m}$ )	$M_C$	100/100 ( $\mu\text{m}/\mu\text{m}$ )
$M_9$	10/0.1 ( $\mu\text{m}/\mu\text{m}$ )	$R_M$	5 k $\Omega$
$M_{10}$	1.9/0.3 ( $\mu\text{m}/\mu\text{m}$ )	$C_1$	0.1 pF
$M_{11,13,15,17}$	4/2 ( $\mu\text{m}/\mu\text{m}$ )	$C_2$	1 pF
$M_{12,14,16,18}$	5/1 ( $\mu\text{m}/\mu\text{m}$ )	$C_M$	1 pF
$M_{19}$	0.12/5 ( $\mu\text{m}/\mu\text{m}$ )	$C_C$	2.5 pF
$M_{20,21}$	1/0.3 ( $\mu\text{m}/\mu\text{m}$ )	$C_L$	1 pF–10 pF

### 3.3. Temperature Analysis of the Building Blocks in PSR Enhancer

#### 3.3.1. CTAT Biasing Current $I_B(T)$

When a PMOS transistor works in subthreshold region [22–24], the source-drain current  $I_{SD}(T)$  is obtained as

$$\begin{aligned}
 I_{SD}(T) &= \mu_p(T) C_{OX} V_T^2 \left( \frac{W}{L} \right) \cdot e^{\frac{V_{SG}(T) + V_{tp}(T)}{nV_T}} \cdot [1 - e^{-\frac{V_{SD}(T)}{V_T}}] \cdot [1 - \lambda V_{SD}(T)] \\
 &= I_S \cdot S \cdot e^{\frac{V_{SG}(T) + V_{tp}(T)}{nV_T}} \cdot [1 - e^{-\frac{V_{SD}(T)}{V_T}}] \cdot [1 - \lambda V_{SD}(T)]
 \end{aligned} \quad (2)$$

where  $I_S = \mu_p C_{OX} V_T^2$ ,  $\mu_p$  is the carrier mobility,  $C_{OX}$  is the gate oxide capacitance,  $n$  is the subthreshold slope which is a constant between 1 and 3,  $V_T = KT/q$  is the thermal voltage,  $K$  is the Boltzmann constant,  $T$  is the temperature,  $q$  is the electronic charge,  $S = W/L$  is the aspect ratio,  $W$  is the channel width,  $L$  is the channel length.  $\lambda$  is the channel length modulation factor and it has a negative value for PMOS transistor. Further to that, the temperature-dependent threshold voltage and mobility are given as follows:

$$V_{tp}(T) = V_{tp0} + k_t(T - T_0) \quad (3)$$

$$\mu_p(T) = \mu_p(T_0) \cdot (T/T_0)^{-m} \quad (4)$$

where  $V_{tp0}$  is the threshold voltage at reference temperature  $T_0 = 300$  K,  $k_t$  and  $m$  are constants pertaining to process technology. When  $V_{SD}(T) > 3V_T$ , the exponential  $V_{SD}(T)$  term in (2) can be ignored and (2) can be rewritten as follows:

$$I_{SD}(T) \approx I_S \cdot S \cdot e^{\frac{V_{SG}(T) + V_{tp}(T)}{nV_T}} \cdot [1 - \lambda V_{SD}(T)] \quad (5)$$

Thus, the approximated expression of  $V_{SG}(T)$  for a long channel length transistor becomes

$$V_{SG}(T) \approx -V_{tp}(T) + nV_T \ln \left[ \frac{I_{SD}(T)}{S \cdot I_S} \right] \approx -V_{tp}(T) \quad (6)$$

where  $I_{SD}(T) \approx S \cdot I_S$ . To compensate the negative temperature coefficient of the output voltage, a bias circuit without a resistor, which aims to generate an appropriate CTAT bias current, is proposed in Figure 6.  $M_1, M_2$  and  $M_4$  operate in the subthreshold region over the targeted temperature range ( $-20$  to  $80$  °C). Through selecting same type of high threshold voltage transistor and establishing the replica  $\Delta V_{SG}(T)$  clamping topology (shaded area) in CTAT current generator with respect to that in core regulator as illustrated in Figure 6, such



as the  $\Delta V_{SG}(T)$  becomes the source-drain voltage across the triode transistor  $M_3$ . Therefore,  $V_{SD3}(T) = V_{SG1}(T) - V_{SG2}(T) = \Delta V_{SG}(T)$ . Since  $V_{SD1}(T)$  and  $V_{SD2}(T) > 3V_T$ , this gives

$$\begin{aligned} V_{SD3}(T) &= V_{SG1}(T) - V_{SG2}(T) = [V_{tp2}(T) - V_{tp1}(T)] + n \frac{KT}{q} \ln\left(\frac{S_2}{S_1}\right) \\ &\approx n \frac{KT}{q} \ln\left(\frac{S_2}{S_1}\right) \end{aligned} \quad (7)$$

In view of the identical type of transistor being used for  $M_1$  and  $M_2$ , the threshold voltage difference is negligible. Based on (7),  $V_{SD3}(T)$  can be regarded as a PTAT voltage.  $M_3$  works in linear region to act as an active resistor, the equivalent resistance between the source and drain of  $M_3$  is given as

$$R_3(T) = \frac{1}{\mu_p(T)C_{OX}S_3 \left[ V_{SG1}(T) + V_{tp3}(T) - \frac{1}{2}V_{SD3}(T) \right]} \quad (8)$$

Using (6)–(8), the bias current expression is obtained as follows:

$$\begin{aligned} I_B(T) &= \frac{V_{SD3}(T)}{R_3(T)} \\ &\approx \mu_p(T)C_{OX}S_3 \cdot n \frac{KT}{q} \ln\left(\frac{S_2}{S_1}\right) \cdot \left\{ V_{tp3}(T) - \frac{1}{2} [V_{tp1}(T) + V_{tp2}(T)] \right\} \end{aligned} \quad (9)$$

$$= C_1 T^{-m} \cdot (C_2 T - C_3 T^2) \quad (10)$$

$$\frac{dI_B(T)}{dT} = -C_4 T^{-m} + C_5 T^{1-m} \quad (11)$$

where

$$C_1 = \mu_p(T_0)T_0^m C_{OX}S_3 n \frac{K}{q} \ln\left(\frac{S_2}{S_1}\right), \quad C_2 = V_{tp0_3} - \frac{V_{tp0_1} + V_{tp0_2}}{2} + T_0 C_3,$$

$$C_3 = k_{t1} - k_{t3}, \quad C_4 = (m - 1)C_1 C_2, \quad C_5 = (m - 2)C_1 C_3,$$

Since  $M_1$  and  $M_2$  are the same type of transistors, the  $k_{t1}$  and  $k_{t2}$  are identical. Factor  $m$  has a typical value of 2.2 for silicon [25], and the parameters  $C_1, C_2, C_3, C_4, C_5$  are constants with positive value. From (11), it can be deduced that  $I_B(T)$  exhibits a CTAT characteristic over the temperature range of  $T < C_4/C_5$ , and the estimation of  $I_B(T)$  will be discussed in the subsequent Section. Of particular note, the value of  $C_4/C_5$  is above  $2T_0$  (600 K) which is beyond the operation temperature range of the transistor. Thus, the CTAT bias current  $I_B(T)$  is used for temperature compensation of  $V_{OUT}(T)$ . Although  $I_B(T)$  slightly exhibits nonlinearity, it does not jeopardize the temperature compensation significantly. Due to the fact that the bias circuit is designed with all MOS transistors, it offers better tracking characteristics in terms of process variation as another key advantage. As such, the entire PVT performance will be promising by means of the proposed CTAT current source.

### 3.3.2. Temperature-Compensated $V_{OUT}(T)$ in LSFVF Topology

The output voltage of the enhancer, which is shown in Figure 6, can be expressed as

$$V_{OUT}(T) = V_{DD} - V_{SG5}(T) + V_{SG7}(T) \quad (12)$$

Since the transistors  $M_5$ – $M_8$  work in the subthreshold region, it is apparent that  $V_{OUT}(T)$  is a CTAT voltage because  $\Delta V_{SG}(T)$  is a PTAT voltage based on (7).

For  $M_7$ , due to the use of a short channel transistor, the CLM is taken into consideration. This yields:

$$V_{SG7}(T) = nV_T \ln \left\{ \frac{I_B(T)}{I_S S_7 [1 - \lambda V_{SD7}(T)]} \right\} - V_{tp7}(T) \quad (13)$$

Substituting (13) into (12), we get

$$\begin{aligned} V_{OUT}(T) &= V_{DD} - nV_T \ln \left( \frac{S_7}{S_5} \right) - V_{tp7}(T) + V_{tp5}(T) - nV_T \ln [1 - \lambda V_{SD7}(T)] \\ &\approx V_{DD} - n \frac{KT}{q} \ln \left( \frac{S_7}{S_5} \right) + n\lambda \frac{KT}{q} V_{SD7}(T) \end{aligned} \quad (14)$$

From (14), it is obvious that if  $V_{SD7}(T)$  in the third term of  $V_{OUT}(T)$  is made CTAT characteristic, the last two terms will counteract each other. Regarding Figure 6, the  $V_{SD7}(T)$  can be written as

$$\begin{aligned} V_{SD7}(T) &= V_{OUT}(T) - V_{D7}(T) \\ &= V_{DD} - \Delta_k - [V_{DD} - V_{SG8}(T) - V_{SG9}(T)] = -\Delta_k + V_{SG8}(T) + V_{SG9}(T) \end{aligned} \quad (15)$$

where  $\Delta_k$  is the design value of the temperature-insensitive dropout voltage and  $\Delta_k = V_{DD} - V_{OUT} = 87.3$  mV. Since both  $M_8$  and  $M_9$  work in the subthreshold region, substituting the expressions for  $V_{SG8}(T)$ ,  $V_{SG9}(T)$  using (6), and rewriting (15), we obtain

$$V_{SD7}(T) \approx -\Delta_k - [V_{tp0_8} + V_{tp0_9} + (T - T_0) \cdot (k_{t8} + k_{t9})] - n \frac{KT}{q} \ln \left[ \frac{I_{S8} \cdot I_{S9} \cdot S_8 \cdot S_9}{M \cdot I_B(T)^2} \right] \quad (16)$$

where factor  $M$  is the current mirror ratio between  $M_{10}$  and  $M_5$ . As can be observed from (16),  $-\Delta_k$  is a constant term,  $-[V_{tp0_8} + V_{tp0_9} + (T - T_0) \cdot (k_{t8} + k_{t9})]$  is a CTAT term for PMOS, and the CTAT  $I_B(T)$  will translate the last term into CTAT counterpart. As a result,  $V_{SD7}(T)$  yields the CTAT characteristic. Substituting (16) into (14),  $V_{OUT}(T)$  can be rewritten as follows:

$$\begin{aligned} V_{OUT}(T) &= V_{DD} - n \frac{KT}{q} \ln \left( \frac{S_7}{S_5} \right) + n(-\lambda) \frac{KT}{q} [\Delta_k + V_{tp0_8} + V_{tp0_9} - T_0(k_{t8} + k_{t9})] \\ &\quad + (-\lambda) T^2 \left\{ \left( \frac{nK}{q} \right)^2 \ln \left[ \frac{I_{S8} \cdot I_{S9} \cdot S_8 \cdot S_9}{M \cdot I_B(T)^2} \right] + \frac{nK}{q} (k_{t8} + k_{t9}) \right\} \end{aligned} \quad (17)$$

$$= V_{DD} - N_1 \cdot T + N_2 \cdot T + N_3 \cdot T^2 \quad (18)$$

where

$$N_1 = n \frac{K}{q} \ln \left( \frac{S_7}{S_5} \right) \quad N_2 = -n\lambda \frac{K}{q} [\Delta_k + V_{tp0_8} + V_{tp0_9} - T_0(k_{t8} + k_{t9})]$$

$$N_3 = -\lambda \left( \frac{nK}{q} \right)^2 \ln \left[ \frac{I_{S8} \cdot I_{S9} \cdot S_8 \cdot S_9}{M \cdot I_B(T)^2} \right] - \lambda \frac{nK}{q} (k_{t8} + k_{t9})$$

As indicated in (18), the negated PTAT term  $-N_1 \cdot T$  will be counteracted by the positive CTAT terms which are contributed by dominant linear term  $N_2 \cdot T$  and small quadratic  $N_3 \cdot T^2$ . They are introduced by the temperature-dependent threshold voltages  $V_{tp8}(T)$  and  $V_{tp9}(T)$ , the design value of dropout voltage  $\Delta_k$ , the channel length modulation factor  $\lambda$  of  $M_7$  and the CTAT current source  $I_B(T)$ . The small quadratic term will display the quadratic effect only at high temperature.

#### 4. Results and Discussions

The proposed PVT-insensitive PSR enhancer, as depicted in Figure 6, is simulated using TSMC-40 nm CMOS process technology.

Figure 8 shows the simulated PSR at different capacitive loads and load currents. From Figure 8, the enhancer offers  $-36$  dB PSR from 1 Hz to 100 kHz. In this design, the maximum load current of the enhancer is  $500 \mu\text{A}$ . When the load current exceeds its maximum value, the power transistor  $M_8$  will enter the linear region, and the circuit performance will be compromised. Therefore, there is a trade-off between the driving capacity and the silicon area. In this work, the proposed enhancer is focused on light load current which is less than  $1 \text{ mA}$  and the typical frequency range for the sensor system is of few MHz or less. Therefore, there is no strict demand on layout issues in view of the insignificant routing parasitics.

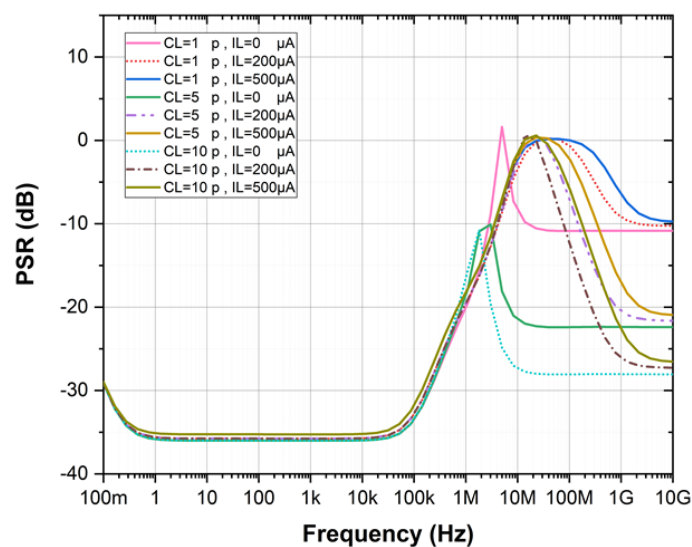


Figure 8. PSR of the Proposed Design at Different Capacitive Loads and Load Currents.

Figure 9a illustrates the variation of CTAT bias current  $I_B(T)$  at different process corners (FF, TT, SS) at the operation temperatures, ranging from  $-20 \text{ }^\circ\text{C}$  to  $80 \text{ }^\circ\text{C}$ . The  $I_B(T)$  decreases with increasing temperatures across the operation temperature range. It shows  $0.8 \mu\text{A}$  under the SS corner at  $80 \text{ }^\circ\text{C}$ ,  $0.49 \mu\text{A}$  under the TT corner at  $80 \text{ }^\circ\text{C}$  and  $0.2 \mu\text{A}$  under the FF corner at  $80 \text{ }^\circ\text{C}$ . This confirms the CTAT characteristic as revealed in (10). Regarding the output voltage,  $V_{OUT}(T)$ , it is evaluated with different process corners, temperatures and loading currents. The simulated results are shown in Figure 9b. Based on the nominal value of  $V_{OUT}(T)$  of  $1.1127 \text{ V}$  at  $27 \text{ }^\circ\text{C}$  in TT case under the load current of  $60 \mu\text{A}$ , the maximum variation is only  $+1.8 \text{ mV}/-1.6 \text{ mV}$  across two extreme temperature corners. For other load currents of  $0 \mu\text{A}$  and  $500 \mu\text{A}$ , the change of  $V_{OUT}(T)$  is  $+2.9 \text{ mV}/-1.8 \text{ mV}$  at  $27 \text{ }^\circ\text{C}$ . For variation of process corners,  $V_{OUT}(T)$  shifts up/down by about  $+11.3 \text{ mV}/-9.7 \text{ mV}$  from the nominal value case. This is considered acceptably small. Besides, it is observed that  $V_{OUT}(T)$  displays an increase at a high temperature of  $85 \text{ }^\circ\text{C}$  under FF corner and little rise at TT corner, this is due to the decrease in  $I_B(T)$ , causing the circuit more sensitive to biasing parameters.

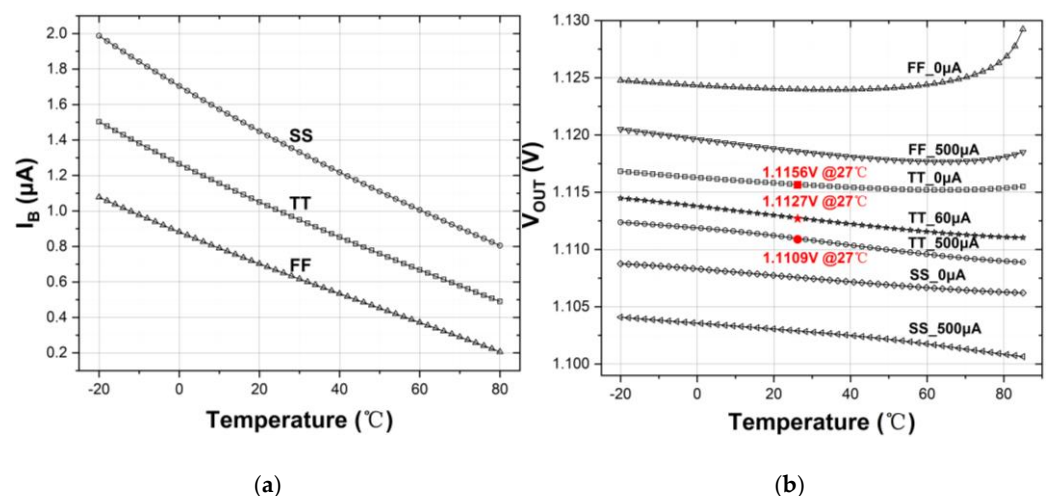


Figure 9. (a) Temperature characteristic of  $I_B(T)$ ; (b) Temperature characteristic of  $V_{OUT}(T)$ .

The comparison between the theoretical estimation of  $I_B(T)$  and  $V_{OUT}(T)$  on basis of (10) and (18) and their simulation results are depicted in Figure 10a,b, respectively. It has been suggested that the theoretical predictions correlate very well with the simulation results for both parameters.

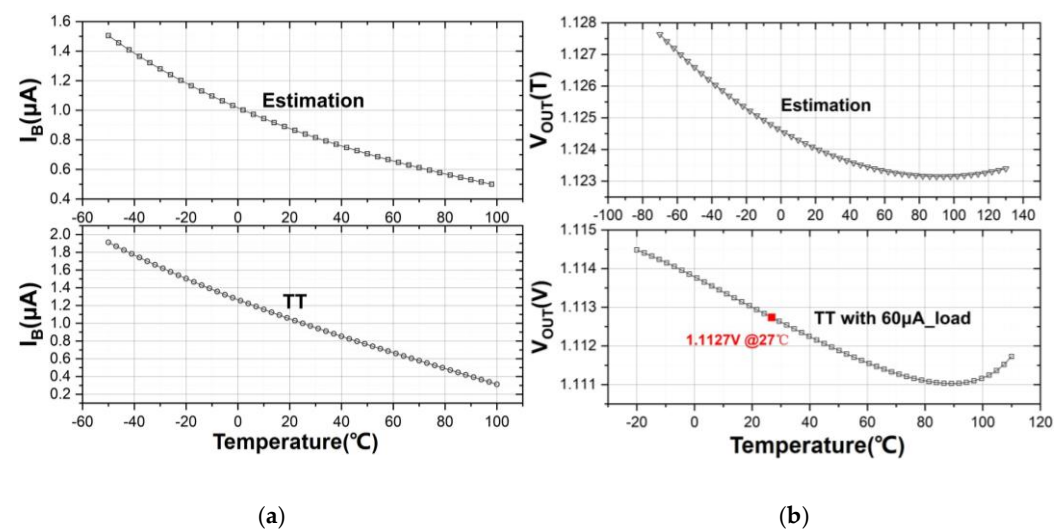


Figure 10. Comparison between theoretical predictions and simulation results under typical case of (a)  $I_B(T)$ ; (b)  $V_{OUT}(T)$ .

Besides, different simulations are conducted to observe the dropout voltage under three process corners,  $1.2\text{ V} \pm 10\%$  on  $V_{DD}$  and different operation temperatures in Figure 11. The results have indicated 87.3 mV under the TT corner at  $27^\circ\text{C}$ , 95.2 mV under the SS corner at  $27^\circ\text{C}$ , and 79.5 mV under the FF corner at  $27^\circ\text{C}$ . The dropout voltage has been observed to be almost invariant to the change of supply voltage; a few mV shifts across the entire operation temperature range and about a few mV change over extreme process corners. This led to the total change of  $+9.9\text{ mV}/-9.5\text{ mV}$  under the extreme PVT case consideration. The result has confirmed that the dropout voltage exhibits good immunity against the combined PVT effect.

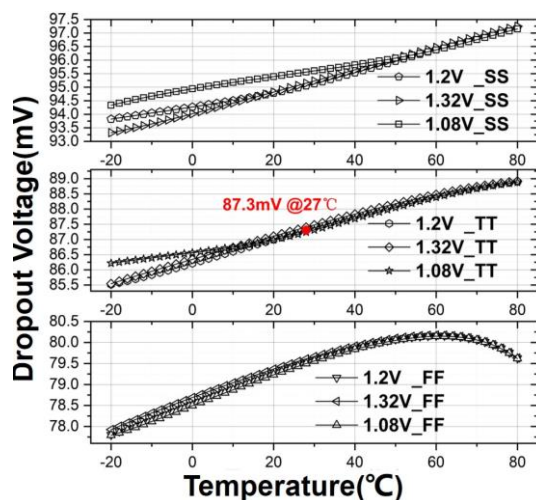


Figure 11. Variation of dropout voltage at different process corners, supply voltages and temperatures.

To demonstrate the performance of the PSR enhancer for sensor circuit application, a Differential Difference Amplifier (DDA) [26], which serves as the instrumentational amplifier for detecting a full bridge sensor signal is employed. For fair comparison, the conventional enhancer and the proposed enhancer are designed with identical static power consumption and identical supply voltage of 1.2 V using TSMC 40 nm CMOS technology. Table 3 summarizes the static power of building blocks in each design. The schematic of DDA is depicted in Figure 12. It is a standard architecture with the first- being a stage folded-cascade differential amplifier and the second being a non-inverting gain stage with a feedforward path to form the push-pull output stage. The current consumption of the DDA is 60  $\mu\text{A}$  at about 1.1 V supply line from each enhancer. This is treated as the typical operation condition for each enhancer. The performance summary is listed in Table 4.

Table 3. Power allocation in proposed and conventional enhancer with 1.2 V supply voltage.

Enhancer	Total Power	Bias Circuit	Power Output Stage	Additional Block
Proposed Work	4.75 $\mu\text{A}$	1.96 $\mu\text{A}$	0.98 $\mu\text{A}$	None
Conventional Design	4.75 $\mu\text{A}$	1.96 $\mu\text{A}$	0.98 $\mu\text{A}$	$V_{REF}$ Generator 8.67 $\mu\text{A}$

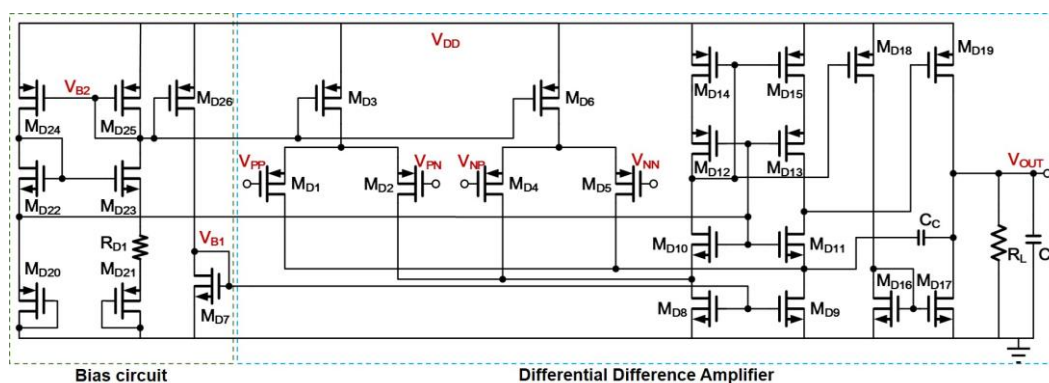


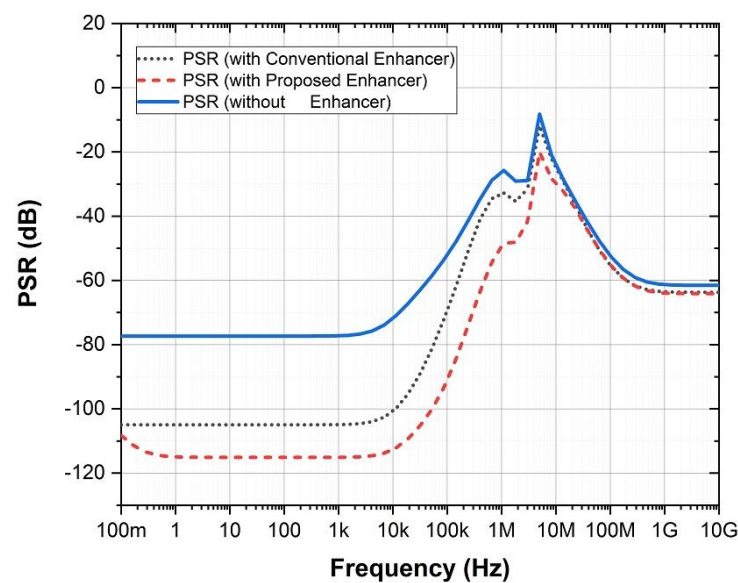
Figure 12. Schematic of the DDA.



**Table 4.** Performance summary of the DDA.

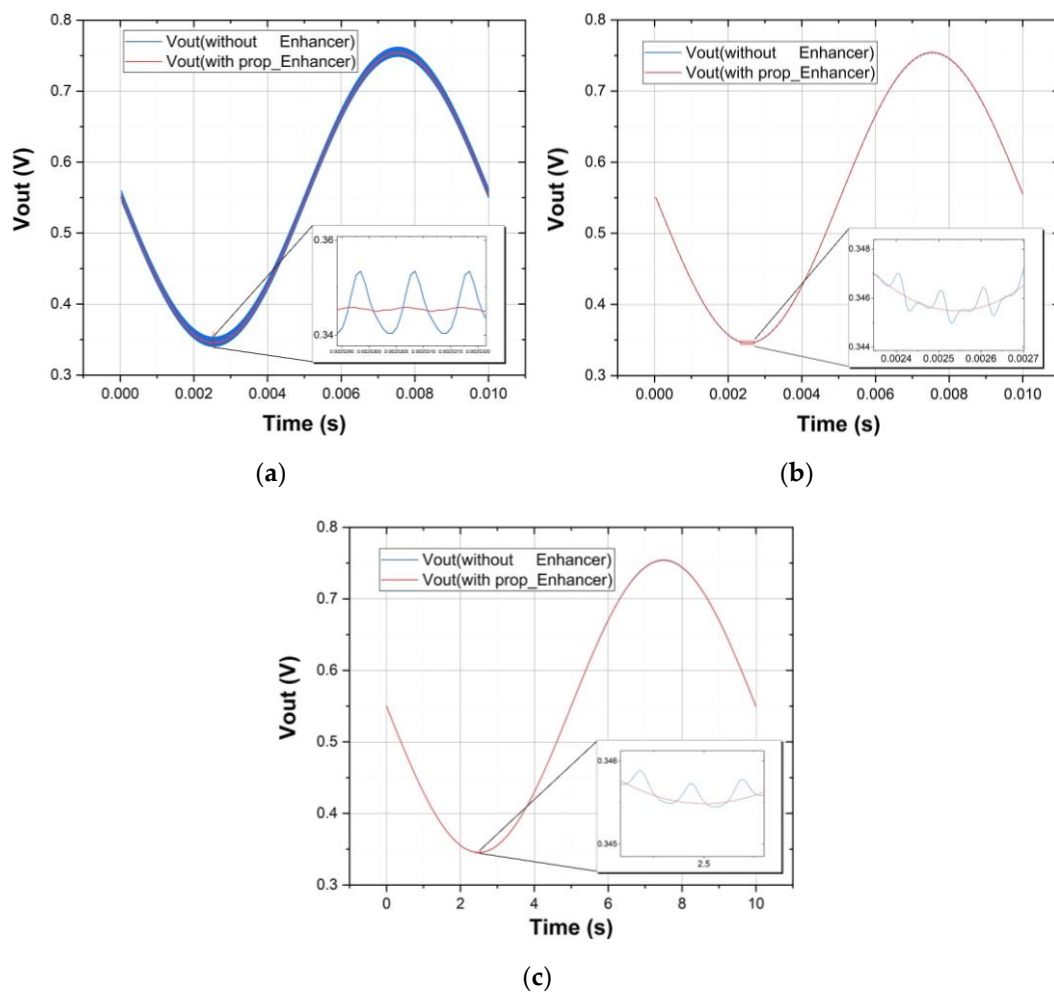
Supply Voltage	Power Consumption	$R_L$	$C_L$
1.1 V	60 $\mu$ A	100 k $\Omega$	30 pF
Open Loop Gain	PSR	CMRR	Bandwidth
77.8 dB	−77.4 dB@1 Hz	87.4 dB	315 Hz
Unit Gain Frequency	Phase Margin	Input-Referred Noise	
2.2 MHz	69°	97 nV/ $\sqrt{\text{Hz}}$ @1 kHz	

The comparative simulation results are given in Figure 13 and Table 5. It can be concluded that both low-frequency and high-frequency PSR are improved using the proposed design, with respect to the DDA designs with and without a conventional enhancer.

**Figure 13.** Comparison of PSR for DDA under different design cases.**Table 5.** Comparison of PSR at low and high frequency for DDA under different design cases powered about 1.1 V from the respective enhancer with 1.2 V supply.

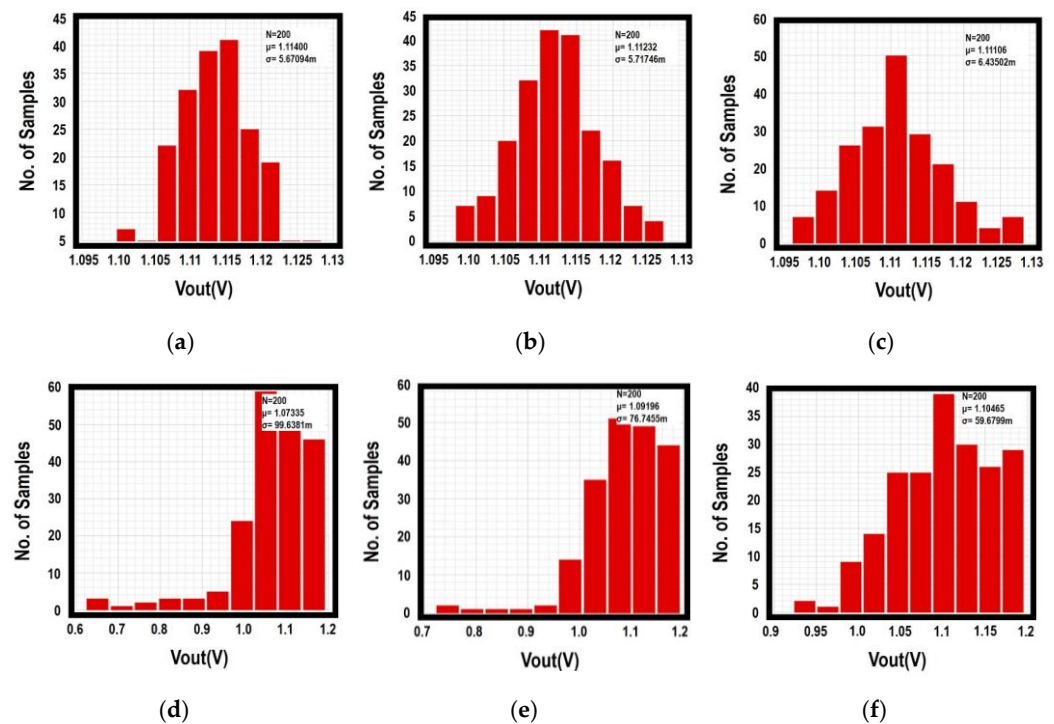
Frequency	Without Enhancer	Conventional Enhancer	Proposed Enhancer
1 Hz	−77 dB	−105 dB	−115 dB
1 MHz	−26 dB	−32 dB	−50 dB

For time-domain evaluation, the respective noise signal with amplitude of 100 mV<sub>pp</sub>@1 MHz, 100 mV<sub>pp</sub>@10 kHz and 100 mV<sub>pp</sub>@20 Hz is applied on the  $V_{DD}$  of DDA which is configured with a closed-loop gain of 20. In this simulation, the input common-mode dc signal is 550 mV, whereas the differential-mode signal is 20 mV<sub>pp</sub>. The time-domain output responses of the DDA, are compared with and without the proposed enhancer in Figure 14. It can be observed that the supply noise associated with the amplified input signal is significantly attenuated at the output of DDA.



**Figure 14.** Comparison of time-domain output responses of DDAs with and without proposed enhancer at different noise levels: (a) 100 mV<sub>pp</sub>@1 MHz; (b) 100 mV<sub>pp</sub>@10 kHz; (c) 100 mV<sub>pp</sub>@20 Hz.

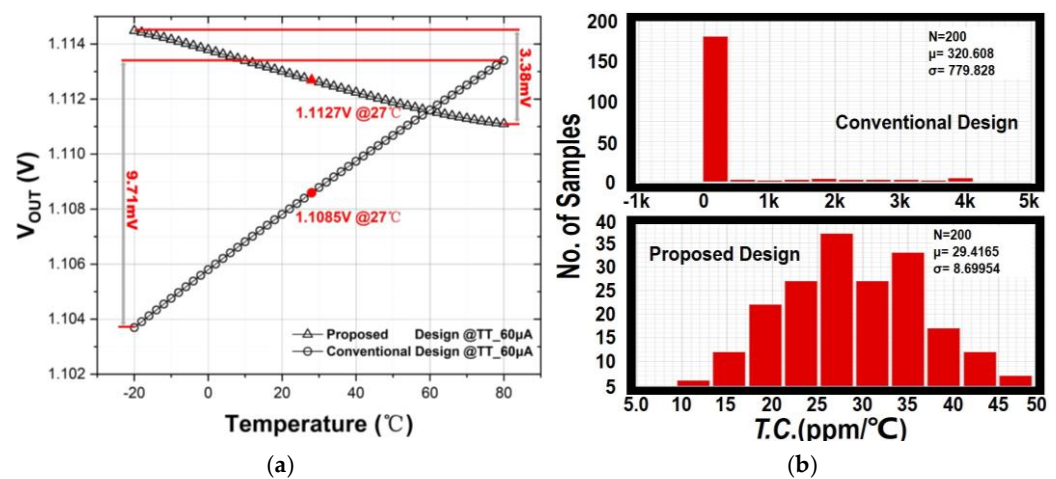
Figure 15 depicts the spread of output voltage for the proposed PSR enhancer, and the conventional one at a typical load current of 60  $\mu$ A is compared with the Monte-Carlo simulation runs pertaining to process and temperature variations. With 200 simulation runs, the mean output voltage of the proposed enhancer is between 1.1106 V to 1.1140 V at different temperatures. As observed, the maximum standard derivation is about 6.5 mV across the operation temperature range. On the contrary, the conventional design displays the mean output voltage between 1.0735 V and 1.10465 V, but the maximum standard derivation can reach up to about 100 mV. Compared to the conventional circuit with (i) 2.9% change in mean  $V_{OUT}$  and (ii)  $\Delta V_{OUT} \approx 100$  mV in maximum standard derivation, the proposed design displays 0.3% change in mean  $V_{OUT}$  and  $\Delta V_{OUT} \approx 6.5$  mV for maximum standard derivation, respectively. From these results, the proposed design offers very good stability of output voltage in worst case consideration. Consider the process sensitivity, it is defined as (Standard Derivation/Mean value)  $\times$  100%. This gives 7.028% for conventional design and 0.514% for the proposed design at 27  $^{\circ}$ C. This shows that the proposed work has a 14-fold improvement in the reduction of process sensitivity for  $V_{OUT}$ .



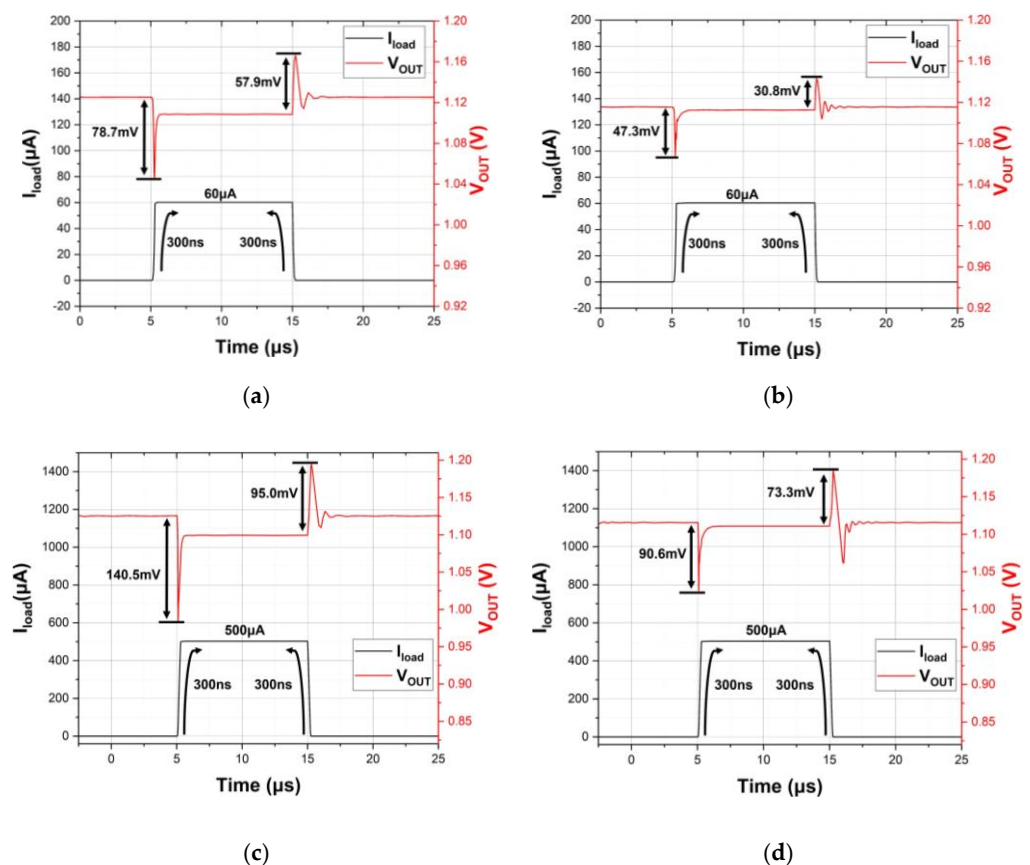
**Figure 15.** Monte-Carlo simulation of  $V_{OUT}$  of the proposed enhancer (a) @ $-20^{\circ}\text{C}$ ; (b) @ $27^{\circ}\text{C}$ ; (c) @ $80^{\circ}\text{C}$ ; and conventional enhancer (d) @ $-20^{\circ}\text{C}$ ; (e) @ $27^{\circ}\text{C}$ ; (f) @ $80^{\circ}\text{C}$ .

For  $T.C.$  evaluation, Figure 16a shows the output voltage change against the temperature for the proposed and conventional PSR enhancer under  $60\ \mu\text{A}$  typical loading condition and  $1.2\ \text{V}$  supply voltage, Over the entire operation temperature range, the variation of  $V_{OUT}$  is only  $3.38\ \text{mV}$  in the proposed design, whereas that of  $9.71\ \text{mV}$  in the conventional design. This yields the nominal  $T.C.$  of  $30.38\ \text{ppm}/^{\circ}\text{C}$  and  $87.60\ \text{ppm}/^{\circ}\text{C}$  for both circuits, respectively. They are considered comparable in nominal operation conditions. In order to assess the sustainability of  $T.C.$  under process variation, Figure 16b depicts the Monte-Carlo simulation results of the  $T.C.$  for  $V_{OUT}$  in both circuits. The obtained mean  $T.C.$  and standard derivation of the proposed work is  $29.4\ \text{ppm}/^{\circ}\text{C}$  and  $8.7\ \text{ppm}/^{\circ}\text{C}$ , respectively. These figures are interpreted as at least 10 times and 100 times smaller than those of the conventional counterpart under MC evaluation. It has suggested that it is not easy for the conventional circuit to sustain its output stability against the temperature and process variation when encountering small dropout voltage design.

Figure 17 illustrates the load transient responses with two load current steps for  $60\ \mu\text{A}$  and  $500\ \mu\text{A}$  for each enhancer based on the circuit capacitive load of  $5\ \text{pF}$ . At the edge time of  $300\ \text{ns}$ , the undershoots of the proposed work are  $47.3\ \text{mV}@60\ \mu\text{A}$  and  $90.6\ \text{mV}@500\ \mu\text{A}$ , whereas the overshoots are  $30.8\ \text{mV}@60\ \mu\text{A}$  and  $73.3\ \text{mV}@500\ \mu\text{A}$ , respectively. Referring to the conventional design, the undershoots are  $78.7\ \text{mV}@60\ \mu\text{A}$  and  $140.5\ \text{mV}@500\ \mu\text{A}$  and the overshoots are  $57.9\ \text{mV}@60\ \mu\text{A}$  and  $95.0\ \text{mV}@500\ \mu\text{A}$ . It can be concluded that the proposed enhancer has achieved smaller undershoot and overshoot. This has demonstrated the advantage of using LSFVF topology for ease of obtaining better transient metrics.



**Figure 16.** Comparison between conventional design and proposed work of (a) temperature characteristic of  $V_{OUT}$  under nominal case; (b) Monte-Carlo simulation of T.C. of  $V_{OUT}$ .



**Figure 17.** Transient response with 60  $\mu$ A current pulse of (a) conventional design; (b) proposed work; and with 500  $\mu$ A current pulse of (c) conventional design; (d) proposed work.

The comparison between the conventional PSR enhancer and the proposed work is summarized in Table 6. As can be revealed, the proposed enhancer offers better performance such as reduced process sensitivity in  $V_{OUT}$ , improved transient metrics, better PSR metrics and simpler circuit topology with respect to those of conventional design at identical power consumption, supply voltage and process technology under low-power circuit design. Further performance enhancement can also be achieved if higher power is allowed in the design.

**Table 6.** Performance comparison of the simulation results between the conventional PSR enhancer and the Proposed Work at Typical Case.

	Conventional Design	This Work
Process Technology	40 nm CMOS	40 nm CMOS
Power Transistor Size	PMOS (1 mm/160 nm)	PMOS (1 mm/160 nm)
Current Consumption $I_Q$ ( $\mu\text{A}$ )	4.75	4.75
Supply Voltage (V)	1.2	1.2
$V_{OUT}$ @60 $\mu\text{A}$ _Load (V)	1.1085	1.1127
Minimum $I_{LOAD, min}$ ( $\mu\text{A}$ )	0	0
Maximum $I_{LOAD, max}$ ( $\mu\text{A}$ )	500	500
$\Delta I_{LOAD}$ ( $\mu\text{A}$ )	500	500
Voltage Reference Required	Yes	No
Op-amp Required	Yes	No
$\Delta V_{OUT}$ (−20–80 °C) (mV)	9.71 <sup>1</sup>	3.38 <sup>1</sup>
PSR Bandwidth (kHz)	65.5	107.2
PSR @ 1 Hz, 1 MHz (dB)	−31.6, −8.1	−36.0, −20.2
Mean of $V_{OUT}$ (V), 200 samples	1.0920	1.1123
SD of $V_{OUT}$ (mV), 200 samples	76.7	5.72
T.C. (1 sample @nominal) (ppm/°C)	87.60 <sup>1</sup>	30.38 <sup>1</sup>
Mean T.C. (200 samples) (ppm/°C)	320.6 <sup>2</sup>	29.4 <sup>2</sup>
SD T.C. (200 samples) (ppm/°C)	779.8	8.7
Process Sensitivity for $V_{OUT}$	7.028%	0.514%
Edge Time ( $\mu\text{s}$ )	0.3	0.3
$\Delta V_{OUT}$ (mV) @500 $\mu\text{A}$	140.5	90.6
Edge Time Ratio K	1	1
FOM <sup>3</sup> [27] (mV)	1.33475	0.86070

<sup>1</sup> At TT corner with 60  $\mu\text{A}$  load condition <sup>2</sup> Monte-Carlo simulation results under 60  $\mu\text{A}$  load condition and T.C. =  $[\Delta V_{OUT}/(\Delta T \times V_{OUT\_normal})] \times 10^6$  ppm/°C,  $V_{OUT\_normal} = V_{OUT}$  @27 °C <sup>3</sup> FOM =  $K \cdot \Delta V_{OUT} \cdot (I_Q + I_{LOAD, min})/\Delta I_{LOAD}$ .

## 5. Conclusions

A new PVT-insensitive dropout voltage based PSR enhancer on the basis of LSFVF topology dedicated to sensor circuit applications is presented. Its functions are similar to the second regulator, which is inserted between the main regulator and the sensor circuit and is subject to performance degradation under a noisy supply line. Through the proposed topological temperature compensation method, the new CTAT current source, the replica circuit block design approach and all MOS transistors design approaches in critical circuit building blocks for obtaining better tracking characteristics, the proposed work permits a small value of dropout voltage in the design whilst providing good immunity against PVT variation. This is translated to the good stability of output voltage. The circuit is verified by extensive simulation results. Besides, the circuit eliminates the use of operational amplifier(s) as well as the voltage reference. Taking advantage of circuit simplicity, it reduces the silicon area and dissipates low static power consumption. The proposed PSR enhancer and its circuit design techniques will be easily extended to other analog circuit applications, in which the supply voltage headroom, the stability of dropout voltage and the limited circuit's PSR parameter are of main concern.

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