





# Preliminary demonstration of a persistent Josephson phase-slip memory cell with topological protection

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Superconducting computing promises enhanced computational power in both classical and quantum approaches. Yet, scalable and fast superconducting memories are not implemented. Here, we propose a fully superconducting memory cell based on the hysteretic phase-slip transition existing in long aluminum nanowire Josephson junctions. Embraced by a superconducting ring, the memory cell codifies the logic state in the direction of the circulating persistent current, as commonly defined in flux-based superconducting memories. But, unlike the latter, the hysteresis here is a consequence of the phase-slip occurring in the long weak link and associated to the topological transition of its superconducting gap. This disentangles our memory scheme from the large-inductance constraint, thus enabling its miniaturization. Moreover, the strong activation energy for phase-slip nucleation provides a robust topological protection against stochastic phase-slips and magnetic-flux noise. These properties make the Josephson phase-slip memory a promising solution for advanced superconducting classical logic architectures or flux qubits.

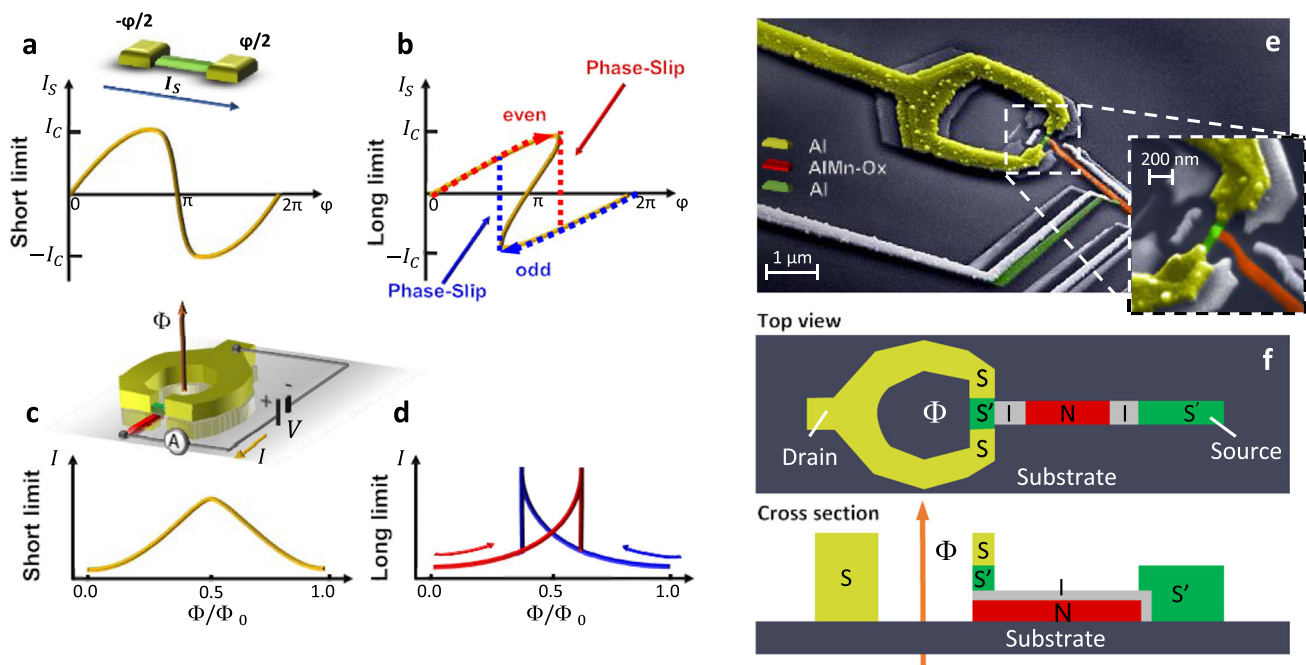
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**A** Josephson junction (JJ) consists of a localized discontinuity (weak link) in the order parameter of two superconducting electrodes<sup>1</sup>, where the dissipationless current ruled by the Cooper pairs transport is controlled by the macroscopic quantum phase difference ( $\varphi$ ) across the junction. Weak links are typically realized in the form of a thin insulator, a semiconductor or metallic wire, or a narrow superconducting constriction<sup>1,2</sup>. The junction current-phase relation (CPR) strongly depends on the structural attributes of the constriction, i.e., on how its effective length ( $L$ , i.e., the distance between the superconducting leads), width ( $w$ ), and thickness ( $t$ ) compare with the superconducting coherence length ( $\xi_w$ )<sup>2</sup>. In a fully superconducting one-dimensional JJ ( $w, t \ll \xi_w$ ) the CPR evolves from the single-valued distorted sinusoidal characteristic, typical of the short-junction limit ( $L \ll \xi_w$ , Fig. 1a) and of non-superconducting weak links, to the multi-valued function obtained in the long regime ( $L \gg \xi_w$ , Fig. 1b)<sup>2</sup>. In the latter scenario, multiple (odd) solutions are available to the system at fixed  $\varphi$ , and the steady state will depend on the history of  $\varphi$ . In the specific example of Fig. 1b, three solutions are possible for the Josephson current ( $I_s$ ) at  $\varphi$  close to  $\pi$ . Two of them are energetically stable, they correspond to two local minima in the Josephson energy<sup>3</sup> and are topologically discriminated by the parity of the winding number of the superconducting phase along the wire<sup>4,5</sup> which reflects into two opposite directions of  $I_s(\varphi)$ <sup>6</sup>, as indicated in Fig. 1b by the even (red) and odd (blue) branches of  $I_s$ . In order to switch between these two stable branches, a  $2\pi$  slippage of the superconducting phase along the weak link is required. The slippage passes through the third backward solution in the CPR, a metastable state which corresponds to a saddle point in the Josephson energy separating the two stable minima and

forming the barrier of a double-well potential. In analogy with the physics of topological insulators, this intermediate metastable state is gapless, and is associated with the formation of a phase-slip center in the middle of the junction<sup>3,7</sup>. The large superconducting condensation energy lost in this gapless center is at the origin of the strong phase-slip energy barrier separating the two topological branches. We take advantage of this topologically protected double-well potential to implement a robust and permanent superconducting memory: The Josephson phase-slip memory (PSM). Differing from similar quantum phase-slip memories<sup>8</sup>, the geometry of the PSM has been conceived for deterministic control of the state via an external magnetic field, while stochastic quantum or thermally-activated phase slips are exponentially suppressed. As described below, these events are negligible thanks to the low resistance of the nanowire  $R_N < R_q L / \xi_w$ , where  $R_q = h/e^2 = 6.5 \text{ k}\Omega$ <sup>9</sup>.

## Results

**Implementation of the memory cell.** The design of a proof-of-concept PSM requires an architecture enabling the tuning of the superconducting phase and the definition of an efficient readout scheme. To finely control  $\varphi$ , the JJ is inserted in a superconducting loop, where an external magnetic field gives rise to a total flux ( $\Phi$ ) piercing the ring area. Stemming from fluxoid quantization<sup>10</sup>, the superconducting phase difference across the weak link is given by  $\varphi = 2\pi\Phi/\Phi_0$  (where  $\Phi_0 \approx 2.067 \times 10^{-15} \text{ Wb}$  is the flux quantum) while the phase drop along the loop is negligible (see “Methods” section for details). The phase difference, together with the topological index, determines the amplitude of the superconducting gap in the local density of states (DOS) of the wire<sup>9</sup>, which can be probed by



**Fig. 1 Phase-slip memory working principle and structure.** **a, b** Sketch of the current-phase relation (CPR,  $I_s(\varphi)$ ) for a S-S'-S weak link (schemed on top) in the short **a** and long **b** junction regime. The CPR (yellow curve) evolves from a deformed sinusoid to a multi-valued function as the junction length increases. In the latter, the transition between the two topologically protected states, corresponding to even and odd topological index<sup>4</sup>, occurs via phase-slips in the wire<sup>2,31</sup> and corresponds to the vertical jump indicated by the colored arrows between the two current branches (red and blue). **c, d** Dependence of the tunnel current ( $I$ ) on the normalized applied magnetic flux ( $\Phi/\Phi_0$ , with  $\Phi_0 = h/2e \approx 2 \times 10^{-15} \text{ Wb}$  the flux quantum), at fixed bias voltage ( $V$ ) for a SQUIPT in the short **c** and long **d** junction regime. In the latter case, the current evolution shows a hysteretic profile (red and blue curves), which stems from the multi-valued CPR. Top: scheme of a voltage-biased DC SQUIPT in a two-wire configuration.  $\Phi$  is the magnetic flux piercing the ring. **e** Pseudo-color scanning electron micrograph of a typical PSM. An Al nanowire (green) is inserted in a micron-size Al ring (yellow), whereas an  $\text{Al}_{0.98}\text{Mn}_{0.02}$  probing electrode (red) is tunnel-coupled to the middle of the nanowire and to a second Al electrode (green) via an insulating oxide layer (gray) to allow the memory operation. Inset: blow-up of the weak-link region. The passive replicas due to the three-angle shadow-mask metal deposition are visible. **f** Schematic top-view and cross-section of the device.

a metallic electrode tunnel-coupled to the middle of the junction, thereby implementing a superconducting quantum interference proximity transistor (SQUIPT)<sup>11</sup>, as sketched on top of Fig. 1c. As a result, at fixed  $\Phi$  the amplitude of the tunneling current ( $I$ ) flowing through the probing electrode will depend on the even/odd parity of the topological index of the junction codifying the logic [0] and [1] states of the PSM cell (Fig. 1d). Encoding the memory state in the parity of the winding number is a common feature to all flux-based superconducting memories, including, e.g., nano-SQUIDS<sup>12,13</sup> flux qubits<sup>14</sup> or kinetic-inductance memories<sup>15</sup> from which it shares the low dissipation and high operation speeds. But, differing from the latter approaches, the dynamics of the memory cell here is entirely dominated by the physics of the weak link. The readout in the SQUIPT is based on tunneling spectroscopy of the weak link and the hysteresis in the magnetic flux is not a consequence of an unbalance between the ring and junction inductance but is an intrinsic property of the CPR.

The scanning electron micrograph (SEM) of a representative PSM cell is shown in Fig. 1e together with a top-down and cross-section scheme in Fig. 1f. Realized through a suspended-mask lithography technique (see “Methods” for fabrication details), the weak link consists of a one-dimensional Al nanowire (green,  $t = 20$  nm and  $w = 90$  nm) with a length  $L \sim 400$  nm, embedded in a micron-sized 70-nm-thick Al ring (yellow). In addition, a 15-nm-thick normal metal electrode (red,  $\text{Al}_{0.98}\text{Mn}_{0.02}$ ) is tunnel-coupled to the center of the wire (with a normal-state tunnel resistance  $R_{t1} \simeq 65$  k $\Omega$ ). To measure the tunneling current, a second Al lead (green) is tunnel-coupled to the normal metal electrode (with a normal-state resistance  $R_{t2} \simeq 90$  k $\Omega$ )<sup>16</sup>. Based on the device structural parameters, we estimate the ratio  $L/\xi_{w,0} \simeq 6$ , where  $\xi_{w,0} \simeq 65$  nm is the zero-temperature coherence length<sup>17</sup>, thereby providing the frame of the long-junction regime<sup>2,9</sup> (see “Methods” for details). Within these geometrical constraints and thanks to the low resistivity of Al ( $\rho < R_q \xi_w$ ), both quantum and thermally-activated phase slips are negligibly small, with rates  $< 10^{-289}$  Hz (see “Methods” for more details on the estimate). Notably, the PSM is completely made of aluminum compounds thus ensuring high-quality tunnel barriers and full compatibility of all fabrication steps for industrial scaling.

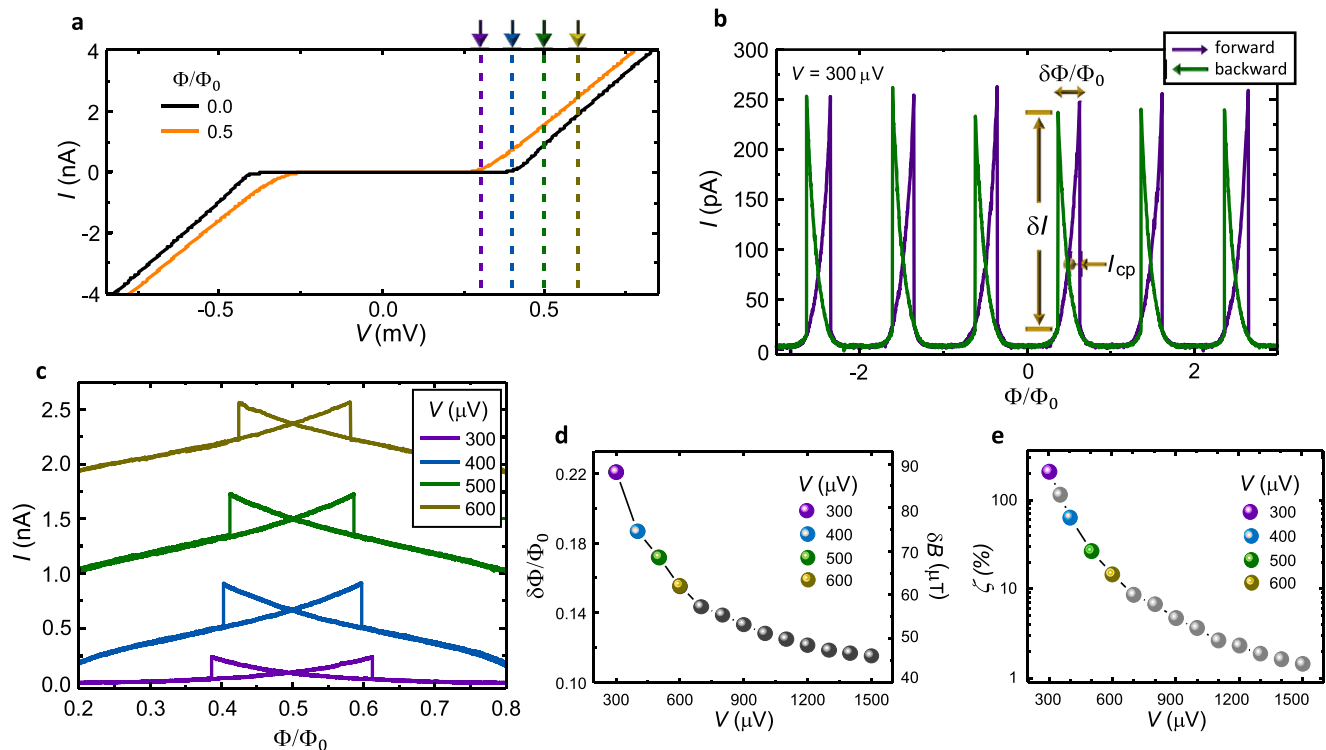
**Magneto-electric response.** To test the PSM transport properties and assess the operation parameters of the memory cell, we first performed a preliminary magneto-electric characterization at bath temperature  $T = 25$  mK. Figure 2a shows the current vs voltage characteristics ( $I(V)$ ) of a typical device measured at  $\Phi = 0$  (black curve) and  $\Phi = \Phi_0/2$  (orange curve). At zero magnetic flux, the quasiparticle tunnel current is suppressed for  $|V| \lesssim 400 \mu\text{V}$  due to the presence of two S-I-N tunnel junctions in series and is consistent with the Al gap of  $\simeq 200 \mu\text{eV}$  for both the readout lead ( $\Delta_{\text{Al}}$ ) and the weak link ( $\Delta_w(\Phi = 0)$ ). The latter can be modulated by the external magnetic flux<sup>11,16</sup>, showing a reduction of about 50% at  $\Phi = \Phi_0/2$  (orange line),  $\Delta_w(\Phi = \Phi_0/2) \simeq 100 \mu\text{eV}$  (see also Supplementary Fig. 1 for more details).

Differently from short-junction SQUIPTS<sup>16,18</sup>, the  $I(\Phi)$  characteristic is not only  $\Phi_0$ -periodic, but it is also strongly hysteretic in  $\Phi$ . This is highlighted in Fig. 2b, where the tunnel current measured at  $V = 300 \mu\text{V}$  as a function of increasing (purple trace) and decreasing (green trace) magnetic flux is shown. The forward trace exhibits periodic maxima followed by sudden jumps corresponding to the nucleation of a phase-slip center in the superconducting nanowire<sup>2,7,9</sup>. Accordingly, the backward trace evolves in a totally specular fashion. The evolution of  $I(\Phi)$  on the bias voltage is shown in Fig. 2c. The hysteresis loop drawn by the back and forth  $I(\Phi)$  exhibits a reduction of its width ( $\delta\Phi$ ) by increasing  $V$ , as quantified also in Fig. 2d. This trend can be ascribed to a local overheating in the weak link induced by the quasiparticle current flowing through the

probing junction which enlarges  $\xi_w(T)$ <sup>1</sup> thereby deviating the CPR towards the single-valued non-hysteretic form<sup>2,9</sup>. The relative separation between the two  $I(\Phi)$  branches can be quantified by a parameter ( $\zeta$ ) defined as the ratio between the current drop at the phase-slip transition and the current at the hysteresis crossing point,  $\zeta = \delta I/I(\Phi = n\Phi_0/2)$ , where  $n$  is an integer odd number. A large  $\zeta$  improves the visibility of the PSM logic states. Similarly to  $\delta\Phi$ , the increase of  $V$  induces a monotonic reduction of  $\zeta$ , as shown in Fig. 2e.

**Memory operation with DC readout.** The typical operation cycle of the PSM memory cell is sketched in Fig. 3a. A bias flux ( $\Phi_B$ ) is required to access the multi-valued state enclosed within the hysteretic domain ( $\Phi_{B\_min} = (\Phi_0 - \delta\Phi)/2$ ,  $\Phi_{B\_max} = (\Phi_0 + \delta\Phi)/2$ ). Writing (erasing) operations are performed by lowering (increasing) the total flux below (above) the hysteretic domain by means of short pulses. As a consequence, the parity of the topological index switches between odd and even and the tunneling current between low and high current state. Figure 3b shows a real-time writing/erasing operation in the continuous-read mode, i.e., with a fixed bias voltage  $V = 300 \mu\text{V}$ . The bias flux is set at  $0.54\Phi_0$ , just above the crossing point of the hysteresis to avoid degeneracy in the current amplitude (Fig. 2c). The memory is then initialized in the [0] state corresponding to a current  $I \simeq 43$  pA. By applying a negative flux pulse down to  $\Phi_w = 0.33\Phi_0$ , the PSM logic state suddenly transits to [1] as detected by the current jump to  $I \simeq 90$  pA. Conversely, the logic state [0] is recovered via a positive erasing flux pulse up to  $\Phi_E = 0.75\Phi_0$ . The device unequivocally shows the typical behavior of a memory cell upon many erasing/writing cycles. From the real-time characteristic is also possible to quantify the energy required for the writing/erasing operations. This can be estimated from the energy difference of the system in the two flux configurations that can be simplified in  $E(\Phi_{B\_max, B\_min}) - E(\Phi_0) \simeq \frac{\Phi_0 \delta\Phi}{2\mathcal{L}_K}$ , where  $\mathcal{L}_K$  is the kinetic inductance of the JJ<sup>8</sup>. In our experimental configuration, the estimated energy is  $\sim 0.1$  eV, which is consistent with the predictions for the energy of the topological barrier  $U \sim \Delta_w \frac{\hbar}{e^2 R_N} \frac{L}{\xi_w}$ <sup>9</sup>. Notably, differing from conventional flux-based superconducting memories, the inductance of the PSM ring is not relevant for the device which can be made negligibly small without any loss of hysteresis or functionality. This allows the miniaturization of the PSM that could be further operated with a flux generated by supercurrents directly injected in a small portion of the superconducting ring<sup>19</sup>, therefore eliminating the requirement of an external magnetic field but with the disadvantage of an additional feed line integrated in the device.

The ability of a memory cell to retain the data even when the power is temporarily turned off is called non-volatility, which, even if not essential for RAM memory, is an adding value for energy saving and data storage. The PSM requires two power sources: one to generate the bias flux  $\Phi_B$  and one for the readout signal. The former was provided by an external superconducting magnet controlled by a current source, then power dependent. To overcome this limitation  $\Phi_B$  could also be generated by a permanent dissipationless superconducting coil as well as a metallic ferromagnetic layer buried in the semiconducting substrate or by directly employing a ferromagnetic insulator as dielectric substrate<sup>20,21</sup>. Alternatively, a proper phase bias might be generated with an additional ferromagnetic pi-junction<sup>22</sup> inserted in the ring or through a phase-battery<sup>23</sup>. The readout voltage is only required to probe the resistance state of the PSM. As demonstrated in Figure 3c, temporarily and repeated measures of both logic states do not affect the stored data with a readout dissipation as low as  $P_{[0]} \simeq 25$  fW and  $P_{[1]} \simeq 40$  fW for the logic state [0] and [1], respectively, and only limited by the noise of the current amplifier. This low dissipated power combined with the intrinsic cutoff time  $\tau_R \simeq 30$  ps estimated from the RC circuit of the tunnel junctions (see “Methods” section for details) yields predicted tiny

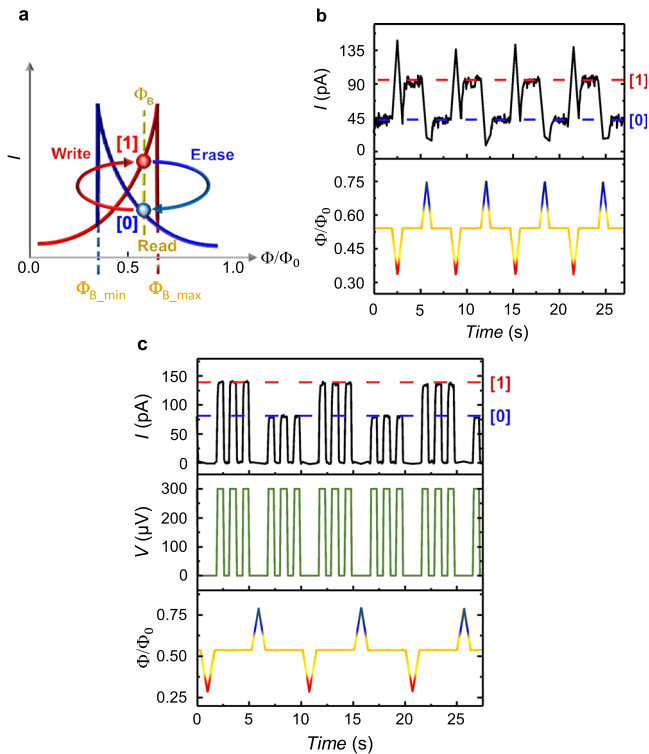


**Fig. 2 Phase-slip memory magneto-electric response.** **a** Current vs voltage characteristics acquired at  $\Phi = 0$  (black trace) and  $\Phi = \Phi_0/2$  (orange trace). The magnetic flux modulates  $\Delta_w$  and, therefore, the  $I - V$  tunnel characteristics. **b**  $I(\Phi)$  of a typical memory cell biased at  $V = 300 \mu\text{V}$ . The purple and green arrows indicate the magnetic flux sweep directions. The width of the hysteretic loop ( $\delta\Phi$ ), the current drop ( $\delta I$ ), and the current at the hysteresis crossing point ( $I_{cp} = I(\Phi_0/2)$ ), are also indicated. **c** Evolution of  $I(\Phi)$  acquired for selected values of  $V$ , as indicated by the colored arrows in **a**.  $I_{cp}$  increases by rising  $V$ . **d** Dependence of the hysteresis width ( $\delta\Phi$ ) on  $V$ .  $\delta\Phi$  monotonically drops by increasing  $V$ . **e** Relative variation of the tunneling current ( $\zeta = \delta I/I_{cp}$ ) vs  $V$ . All these measurements were taken at  $T = 25 \text{ mK}$ .

energy required per bit readout  $J_{[0]} = P_{[0]}\tau_R \simeq 4.7 \mu\text{eV}$  and  $J_{[1]} = P_{[1]}\tau_R \simeq 7.5 \mu\text{eV}$ . These values were only estimated and stem from the severe bandwidth limitations of the cryogenic filters. Similar to rapid single flux quantum, the writing/erasing process is expected with a switching time of  $\sim 1 \text{ ps}$  which is typical for small superconducting loops<sup>24–26</sup>. The PSM speed is therefore expected to be on par with current state-of-the-art superconducting memories both in the reading and in the writing/erasing process<sup>24,25,27–29</sup>.

**Memory robustness and operation with AC readout.** The robustness of the PSM against flux fluctuations is tested by superimposing to the working biasing flux a sizable sinusoidal signal ( $\Phi_{AC}$ , Fig. 4a). The PSM shows optimal stability with respect to flux oscillations, as shown in Fig. 4b for  $V = 300 \mu\text{V}$  and  $\Phi_B = 0.56\Phi_0$ . The memory preserves the stored state and keeps the readout value of the two logic states well separated for fluctuations  $\Phi_{AC} \simeq 0.08\Phi_0$ , then  $\sim 50\%$  of the hysteretic domain of the memory  $\delta\Phi$ , at least. Interestingly, thanks to the opposite sign of the magnetoconductance of PSM in the two topological states (visible for instance in Fig. 2b, c), the AC flux modulation induces an AC response in the tunneling current which acquires a  $\pi$  shift when switching between the two logic states [0] and [1]. This phase shift provides a complementary and efficient method to probe the parity of the JJ winding number, which is not affected by the position of  $\Phi_B$  within the hysteretic domain, or by the low visibility of the DC readout signal (see also Supplementary Figs. 4 and 5 for more details). This allows operating the memory cell also in the degenerate point  $\Phi_B = \Phi_0/2$ , where the energies of the [0] and [1] states are equal, a basic condition to implement a phase-slip qubit<sup>8,14</sup>. Therefore, the PSM provides an alternative low-frequency method for the qubit readout. With the phase-based readout, the persistency of the PSM have been tested up

to almost three days, as shown in Fig. 4c. The memory is initialized to logic state [1], and the readout is performed every 4 h. No sign of signal degradation has been observed even after  $\sim 3$  days of measurement confirming the vanishing phase-slip rate ( $\sim 10^{-289} \text{ Hz}$ ) as estimated from our parameters<sup>7,9</sup> (see “Methods” for details on the estimate). As a consequence, the memory error rate expected for quantum and thermally-activated phase slips is infinitesimally small and errors can be generated only by large magnetic-flux fluctuations ( $\gtrsim \delta\Phi$ ) of the driving magnetic flux. The other source of error that might degrade the memory state is the reading current which could switch the memory via inductive coupling to the ring or by quenching the superconductivity of the weak-link, as commonly happens for superconducting kinetic inductance memories<sup>13</sup>. Differing from the latter, the high resistance of the probing tunnel barrier strongly limits the reading current to  $\lesssim \text{nA}$ , then much smaller than the current required for switching ( $\sim \text{mA}$ )<sup>19</sup> and the critical current of the weak-link ( $\gtrsim \mu\text{A}$  for an Al nanowire<sup>30</sup>). This makes also the error rate during readout operation negligible. High temperature can degrade the performance of PSM by increasing  $\xi_w(T)$ <sup>1</sup> thereby lowering the JJ effective length and driving the nanowire junction towards the non-hysteretic single-valued CPR occurring for  $L \lesssim 3.5\xi_w$ <sup>2,31</sup>. In addition, thermal activation can substantially increase the phase-slip rate in the vicinity of the transition, that is at  $\phi \lesssim \phi_{B_{max}}$  and  $\phi \gtrsim \phi_{B_{min}}$ <sup>9</sup>. Figure 5a shows the evolution of the hysteresis loop at several bath temperatures ( $T$ ). The hysteresis progressively fades out by increasing  $T$ , but persists up to 1.1 K, which corresponds to  $\sim 85\%$  of the nanowire critical temperature, with  $\delta\Phi$  reduced to about the 12% of the base temperature value (Fig. 5b). Consequently, also the contrast  $\zeta(T)$  lowers by increasing  $T$ , as shown in Fig. 5c. Still, the visibility of the hysteresis loop at high temperatures demonstrates the strength of the PSM with substantial



**Fig. 3** Operation of the phase-slip memory with DC readout. **a** Sketch of the memory operation principle at a constant voltage bias ( $V$ ). Low (blue,  $I_{[0]}$ ) and high (red,  $I_{[1]}$ ) current branches at the bias flux ( $\Phi_B \in (\Phi_0/2, \Phi_{B\_max})$ ) encode the [0] and [1] logic states, respectively. The erase (write) operation is performed by applying a flux pulse with amplitude  $\Phi_E > \Phi_{B\_max}$  ( $\Phi_W < \Phi_{B\_min}$ ). The memory can also be operated in the complementary part of the hysteresis at  $\Phi_B \in (\Phi_{B\_min}, \Phi_0/2)$  by exchanging the erase and write fluxes. **b** Evolution of the readout tunneling current (top panel) measured at  $V = 300 \mu\text{V}$  for  $\Phi$  composed by a bias flux  $\Phi_B = 0.54\Phi_0$  (yellow trace) interrupted by writing ( $\Phi_W = 0.33\Phi_0$ , red) and erase ( $\Phi_E = 0.75\Phi_0$ , blue) pulses (bottom panel). **c** Same as in **b** but now the voltage bias (central panel, green trace) is applied only during the readout operation to minimize power consumption and demonstrate the non-volatility of the memory cell. All the measurements were taken at  $T = 25 \text{ mK}$ .

protection of the topological state even in the presence of a sizable amount of hot quasiparticles<sup>4</sup>. Although the low  $\delta\Phi$  achieved at high temperature degrades the robustness of the memory with respect to flux noise, it also allows writing the memory cell with smaller fluxes for a total cost of operation down to  $\sim 10 \text{ meV}$ .

## Discussion

In summary, we have envisioned and demonstrated an original persistent Josephson phase-slip single memory cell that takes advantage of fluxoid quantization to codify two logic states in the topological index of the system, i.e., the parity of the superconducting winding number<sup>5</sup>. Differing from conventional superconducting loops<sup>12,13,25</sup>, here the separation between the two topological states is provided by the large phase-slip barrier, which is unique to long superconducting JJs<sup>4,9</sup>. Moreover, its operation mechanism is completely independent of the size or inductance of the superconducting loop thus allowing device miniaturization only limited by fabrication capabilities. The memory exploits conventional superconductors thereby avoiding the use of complex ferromagnetic metals typical of present superconducting memories<sup>24,26–29,32</sup>. Notably, the performances of the PSM are competing with state-of-the-art superconducting memories with an extremely low energy dissipation per

bit operation ( $\sim 10^{-24} \text{ J}$  and  $\sim 10^{-20} \text{ J}$  for readout and write, respectively) and high operation speed (up to  $\sim 30 \text{ ps}$  and  $\sim 1 \text{ ps}$  for readout and write, respectively). Thanks to the topological protection, the PSM shows endurance, persistence, and high-temperature operation (up to  $\sim 1 \text{ K}$ ), only limited by the Al critical temperature. The use of vanadium<sup>18</sup> or niobium<sup>33</sup>, therefore, could extend the memory operation above liquid He temperature, and further promote miniaturization thanks to the lower coherence length of these metals with respect to Al.

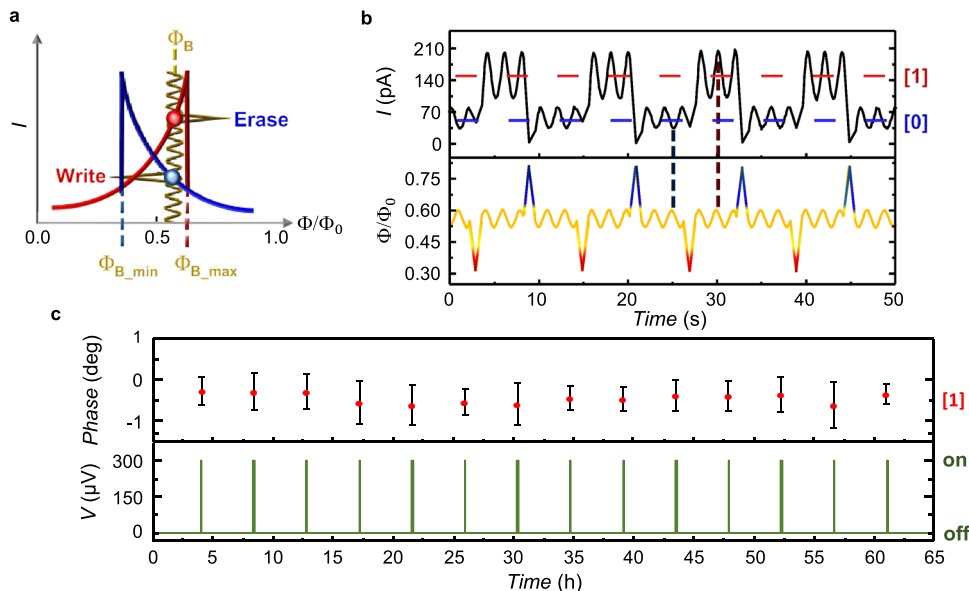
In addition, our phase-based readout scheme ensures protection against magnetic flux fluctuations and provides ideal visibility in all the operation ranges. In fact, despite being intrinsically slower than conventional methods (high-speed lock-in amplifiers reach nowadays a clock frequency of  $\sim 600 \text{ MHz}$ ), the phase-based readout can be a valuable approach for the readout of phase-slip qubits. Furthermore, scalability to large arrays of PSM cells might be designed by taking advantage of the well-known architectures employed for transition-edge sensors, since both devices are based on precise resistance measurement. In particular, frequency-domain multiplexing or microwave resonators together with SQUID amplifiers<sup>34</sup> could be used for the selective readout of each PSM composing the total memory.

Sneak currents can be avoided by employing strongly non-linear resistors between each single memory unit, such as superconductor/insulator/normal metal/insulator/superconductor Josephson junctions. Integrating superconducting current feed lines in the ring<sup>19</sup> will allow scaling also the writing procedure with the additional cost of wiring complexity. Yet, the presence of independent write and read lines, with the former characterized by a low impedance, increases stability against perturbations of the read current and might simplify the integration of the PSM with existing superconducting logic elements including rapid single flux quantum<sup>24–26</sup>, reciprocal quantum logic<sup>35</sup>, quantum flux parametrons<sup>36</sup>, Josephson field-effect transistors<sup>37</sup>, and gate-controlled cryotrons<sup>17,38,39</sup>. Yet, the strong topological protection and stability observed in the PSM make our approach promising in light of the implementation of phase-slip flux qubits<sup>8,14</sup> and quantum memories.

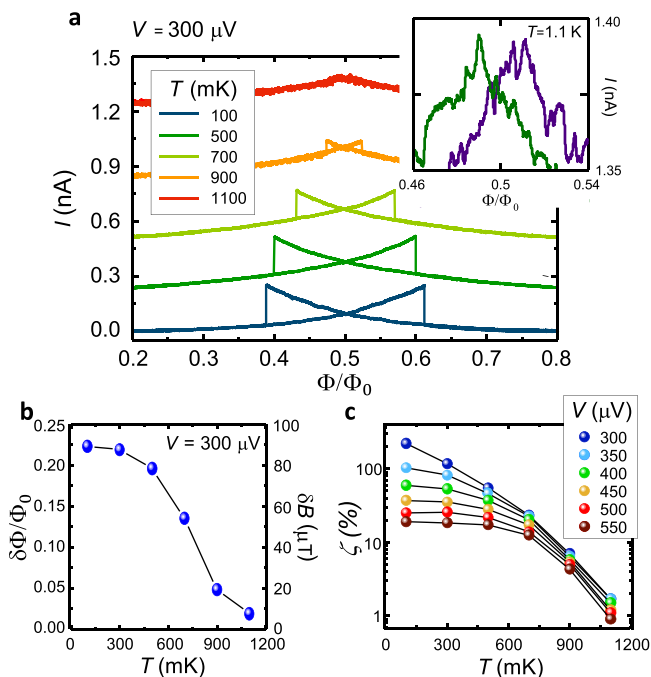
## Methods

**Device fabrication details.** The hybrid memory cells were realized by the shadow-mask lithography technique. The suspended resist-mask was defined by electron-beam lithography (EBL) onto a  $\text{SiO}_2$  wafer. All metal-to-metal clean interfaces, and metal-to-oxide barriers were realized in an ultra-high vacuum (UHV) electron-beam evaporator (EBE) with a base pressure of  $10^{-11} \text{ Torr}$  equipped with a tiltable sample holder suitable for multi-directional depositions. In order to obtain wire/ring transparent interfaces, which is crucial for the device operation, the use of the same material is strongly recommended<sup>16</sup>. Therefore, the nanowire and the ring of the PSM were realized with aluminum. Furthermore, the Al film evaporation is relatively simple, and its high-quality native oxide allows the realization of good tunnel barriers through oxygen exposure at room temperature. At first,  $15 \text{ nm}$  of  $\text{Al}_{0.98}\text{Mn}_{0.02}$  were evaporated at an angle of  $-18^\circ$  to realize the normal metal electrode. Subsequently, the sample was exposed to  $60 \text{ mTorr}$  of  $\text{O}_2$  for  $5 \text{ min}$  in order to form the thin insulating AlMnOx layer. Next, the sample holder was tilted to  $10^\circ$  for the deposition of  $20 \text{ nm}$  of Al realizing the SQUIPT nanowire (length  $L = 400 \text{ nm}$ , width  $w = 90 \text{ nm}$ , and thickness  $t = 20 \text{ nm}$ ) and the superconducting electrodes. Finally, a thicker layer of Al ( $t_R = 70 \text{ nm}$ ) was evaporated at  $0^\circ$  to realize the superconducting loop of circumference  $\sim 7.6 \mu\text{m}$ , and average width  $w_{R,ave} \approx 600 \text{ nm}$ .

**Magneto-electric characterization.** The magneto-electric characterization of the samples was performed at cryogenic temperatures in a  $^3\text{He}$ - $^4\text{He}$  dilution refrigerator (Triton 200, Oxford Instruments) equipped with RC-filters of resistance  $\sim 2 \text{ k}\Omega$ . The out-of-plane magnetic field was applied via a superconducting magnet driven by a low-noise current source (Series 2600, Keithley Instruments). The DC measurements were performed in a two-wire voltage-bias configuration through a low-noise voltage DC source (GS200, Yokogawa) coupled with a room-temperature current preamplifier (Model 1211, DL Instruments) (Fig. 1c). The AC characterization was performed via a combination of DC bias and low-frequency lock-in technique. A DC bias voltage ( $V$ ) was applied to the device. A current given by the sum of a DC and AC sinusoidal modulation energized the superconducting magnet. The readout current oscillations induced by variation of  $\Phi$ , and the phase



**Fig. 4 Operation of the phase-slip memory with AC readout.** **a** Sketch of the memory operation in the presence of a sinusoidal flux oscillation ( $\Phi_{AC}$ , yellow trace) around  $\Phi_B \in (\Phi_0/2, \Phi_{B\_max})$ . **b** Evolution of the readout current (top panel) measured at  $V = 300 \mu\text{V}$  and  $\Phi$  composed by a flux bias ( $\Phi_B = 0.56\Phi_0$ ) superimposed with a sinusoidal oscillation  $\Phi_{AC} = \pm 0.04\Phi_0$  (yellow trace in the bottom panel). Write ( $\Phi_W = 0.32\Phi_0$ , red) and erase ( $\Phi_E = 0.81\Phi_0$ , blue) flux pulses are applied to switch the logic state of the memory cell. Notice that the two current signals oscillate with a  $\pi$  shift making the phase of the AC signal a very sensitive readout observable. Vertical dashed lines highlight the signals phase shift with respect to the magnetic flux. **c** Demonstration of persistent memory operation at  $\Phi = \Phi_0/2$  obtained by measuring the signal phase with a lock-in amplifier (top) every 4 h and only when the readout voltage is turned on ( $V = 300 \mu\text{V}$ , bottom). State [1] was measured for almost 3 days showing no sign of degradation, and low dissipation being  $V = 0$  for most of the time. The error bar was estimated from the root mean square of the sampled signal. All the data were recorded at  $T = 25 \text{ mK}$ .



**Fig. 5 Temperature dependence of the phase-slip memory.** **a** Current modulation  $I(\Phi)$  for several bath temperatures ( $T$ ) at  $V = 300 \mu\text{V}$ . The hysteresis loop narrows and fades out by increasing the temperature since the superconducting nanowire approaches the short-junction limit at high  $T$ . Inset: blow-up of the  $I(\Phi)$  characteristics around  $\Phi_0/2$  at 1.1 K. Forward (purple) and backward (green) traces highlight the presence of hysteresis. **b** Temperature dependence of  $\delta\Phi$  measured at  $V = 300 \mu\text{V}$ .  $\delta\Phi$  monotonically decreases with temperature. **c**  $\zeta$  vs  $T$  for selected values of  $V$ .  $\zeta$  drops with temperature, and by increasing  $V$ . Black lines in panels b and c are guides for the eye.

of the signal (with respect to the flux oscillations) were recorded by a lock-in amplifier (SR830, Stanford Research Systems). Further details on the readout scheme can be found in the note 5 of the Supplementary Information.

**Device parameters.** Based on the device structure, we estimate the zero-temperature nanowire coherence length  $\xi_{w,0} = \sqrt{\hbar D/\Delta_{w,0}} \simeq 65 \text{ nm}$ , where  $\hbar$  is the reduced Planck constant,  $D \simeq 18 \text{ cm}^2/\text{s}$  is the diffusion coefficient, and  $\Delta_{w,0} \simeq 200 \mu\text{eV}$  is the zero-temperature gap in Al. The nanowire critical temperature is  $T_{C,w} = \Delta_{w,0}/1.764k_B \simeq 1.31 \text{ K}$ , where  $k_B$  is the Boltzmann constant. At low temperature, the ratio  $L/\xi_{w,0} \simeq 6$  confirming the frame of the long JJ regime for the PSM<sup>2</sup>. The single-valued CPR limit (achieved for  $\xi_{w,short} \gtrsim L/3.5 \sim 114 \text{ nm}$ ) is reached at temperature  $T_{short} = T_{C,w}(1 - 0.852^2 \frac{\xi_{w,0}^2}{\xi_{w,short}^2}) \sim 1.29 \text{ K}^2$ , where  $l = 3D/v_F \simeq 3 \text{ nm}$  is the nanowire mean free path, and  $v_F = 2.03 \times 10^6 \text{ m/s}$  is the Fermi velocity of Al.

The kinetic inductance ( $\mathcal{L}_K$ ) of a long JJ depends on the geometry and superconducting properties of the nanowire<sup>9</sup>. In our case, at 25 mK it takes the value  $\mathcal{L}_K = \frac{R_N \hbar}{\pi \Delta_w \tanh \frac{\Delta_w}{2k_B T}} \simeq 18 \text{ pH}^{40}$ . The nanowire normal-state resistance is given by

$R_N = \frac{l}{wt\sigma} \simeq 17 \Omega$ , where  $\sigma = DN_e^2 \simeq 1 \times 10^7 \text{ S/m}$  is the Al film conductivity (with  $N_f = 2.15 \times 10^{47} \text{ J/m}^3$  the density of states at the Fermi energy of Al). Analogously, the ring total inductance (including both the geometric and kinetic contributions) takes the value  $\mathcal{L}_R \sim 1 \text{ pH}^{16}$  (with normal-state resistance  $R_R \simeq 1.4 \Omega$ ). The contribution of the ring to the total inductance of the SQUIPT yields a screening parameter  $\beta = \mathcal{L}_R/\mathcal{L}_K \lesssim 0.1$ . The small  $\beta$  cannot account for the hysteretic behavior of the PSM, which stems, differently, from the long-junction regime of the Josephson nanowire. The writing/erasing time ( $\tau_{W,E}$ ) is mainly due to the time required to polarize the SQUIPT with the external flux. It is given by  $\tau_{W,E} = \mathcal{L}_{SQUIPT}/R_{SQUIPT} \sim 1 \text{ ps}$ , where  $\mathcal{L}_{SQUIPT} = \mathcal{L}_K + \mathcal{L}_R$  and  $R_{SQUIPT} = R_N + R_R$  are the total inductance and resistance of the SQUIPT, respectively. The readout time ( $\tau_R$ ) is predominantly limited by the characteristic time of the two tunnel barriers,  $\tau_R = \tau_{t1} + \tau_{t2} \sim 30 \text{ ps}$ , where  $\tau_{t1} = R_{t1}C_{t1} \sim 20 \text{ ps}$  is the characteristic time of the first tunnel junction, and  $\tau_{t2} = R_{t2}C_{t2} \sim 10 \text{ ps}$  is the time constant of the second junction. The junction capacitances ( $C_{t1} \sim 0.3 \text{ fF}$  and  $C_{t1} \sim 0.1 \text{ fF}$ ) are estimated from the area and the typical specific capacitance of AlOx tunnel barriers  $\sim 50 \text{ fF}/\mu\text{m}^2$ .

**Phase-slip rates.** Stochastic phase-slips are possible via quantum tunneling and thermal activation. They scale exponentially with the phase-slip barrier, the former with  $-U/\Delta_{w,0}$  while the latter with  $-U/k_B T$ . Both of them are small for  $R_\xi < R_q$  (where  $R_\xi =$

$R_N \xi_w/L$ , as demonstrated in the following. The quantum phase-slip rate is<sup>8</sup>:

$$\Gamma_{qps} = \Omega_{qps} \exp -0.3 \frac{R_q}{R_\xi}, \quad (1)$$

where  $\Omega_{qps} \simeq 0.85 \frac{\Delta_w}{\hbar} \frac{L}{\xi_w} \sqrt{\frac{R_q}{R_\xi}} \simeq 75$  THz is the quantum phase-slips attempt frequency. With the parameters of our experiment, we obtain the negligibly small  $\Gamma_{qps} \sim 2 \times 10^{-289}$  Hz. Thermally-activated phase-slips rate reads<sup>7</sup>:

$$\Gamma_{TAPS} = \Omega_{TAPS} \exp -\frac{\delta F}{k_B T}, \quad (2)$$

where  $\delta F = 2.7 \frac{T_c - T}{T} U$  is the free energy difference of the potential barrier and  $\Omega_{TAPS} \simeq 5.5 \frac{k_B T}{\hbar} \frac{L}{\xi_w} \sqrt{\frac{\delta F}{k_B T}}$  is the attempt frequency. In the temperature range of the experiment  $T < T_c$ ,  $\Gamma_{TAPS}$  is expected to be even smaller than  $\Gamma_{qps}$ . As an example, at  $T = 100$  mK the attempt frequency is  $\Omega_{TAPS} \simeq 500$  THz and  $\Gamma_{TAPS} \sim 10^{-474}$  Hz. From these equations is possible to see that  $\Gamma_{TAPS}$  is relevant only at a temperature very close to  $T_c$ .

## Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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## Author contributions

E.S. and F.G. conceived the experiment. N.L. fabricated the samples with inputs from F.P. N.L. and E.S. performed the measurements. N.L. analyzed the experimental data with inputs from E.S. and F.G. All the authors discussed the results and their implications equally at all stages and wrote the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

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