



# Neuromorphic log-domain silicon synapse circuits obey bernoulli dynamics: a unifying tutorial analysis

Konstantinos I. Papadimitriou<sup>1</sup>, Shih-Chii Liu<sup>2</sup>, Giacomo Indiveri<sup>2</sup> and Emmanuel M. Drakakis<sup>1\*</sup>

<sup>1</sup> Bioinspired VLSI Circuits and Systems Group, Department of Bioengineering, Imperial College London, London, UK

<sup>2</sup> Institute of Neuroinformatics, University of Zurich and ETH Zurich, Zurich, Switzerland

## Edited by:

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## \*Correspondence:

Emmanuel M. Drakakis, Bioinspired VLSI Circuits and Systems Group, Department of Bioengineering, Imperial College London, South Kensington Campus, London SW7 2AZ, UK  
e-mail: e.drakakis@imperial.ac.uk

The field of neuromorphic silicon synapse circuits is revisited and a parsimonious mathematical framework able to describe the dynamics of this class of log-domain circuits in the aggregate and in a systematic manner is proposed. Starting from the Bernoulli Cell Formalism (BCF), originally formulated for the modular synthesis and analysis of externally linear, time-invariant logarithmic filters, and by means of the identification of new types of Bernoulli Cell (BC) operators presented here, a generalized formalism (GBCF) is established. The expanded formalism covers two new possible and practical combinations of a MOS transistor (MOST) and a linear capacitor. The corresponding mathematical relations codifying each case are presented and discussed through the tutorial treatment of three well-known transistor-level examples of log-domain neuromorphic silicon synapses. The proposed mathematical tool unifies past analysis approaches of the same circuits under a common theoretical framework. The speed advantage of the proposed mathematical framework as an analysis tool is also demonstrated by a compelling comparative circuit analysis example of high order, where the GBCF and another well-known log-domain circuit analysis method are used for the determination of the input-output transfer function of the high (4<sup>th</sup>) order topology.

**Keywords:** analog VLSI (aVLSI), generalized bernoulli cell formalism, log-domain circuits, subthreshold MOSFETs, synaptic dynamics

## 1. INTRODUCTION

Almost 20 years ago, a novel, systematic, transistor-level formalism for the analysis and synthesis of externally-linear, internally-nonlinear (ELIN) (Tsvividis, 1997) log-domain filters was introduced. The formalism was termed “*The Bernoulli Cell Formalism*” in an attempt to highlight its key element, the Bernoulli differential equation describing the time-dependent behavior of a forward-biased BJT collector current when a linear capacitor is connected to its emitter terminal (Drakakis et al., 1997b). A similar mathematical description holds for the drain current of a weakly-inverted MOST, when a linear capacitor is connected to its source terminal.

By arranging many BC topologies in cascade form, where the input of the next BC becomes the output of the previous one, a set of general coupled equations termed “*Log-Domain State Space*” (LDSS) is generated (Drakakis et al., 1999b). The resulting set of linearised differential equations of the LDSS stems from the non-linear differential equation governing each BC and constitutes a powerful and handy tool, well suited for the transfer function derivation of any order of log-domain filter. Several high-order log-domain filter circuit examples in literature confirm the above statement and identify the BCF as a parsimonious analysis and synthesis tool (Drakakis et al., 1997a; Drakakis, 2006; Ip et al., 2009; Katsiamis et al., 2009; Kardoulaki et al., 2013).

A review of past literature reveals that the BCF constitutes a complete, systematic mathematical framework not only for ELIN

but also for intrinsically non-linear log-domain circuits. When it comes to the synthesis of purely non-linear log-domain circuits, a variant of the BCF, termed Non-linear Bernoulli Cell Formalism (NBCF), is able to implement challenging non-linear dynamics, based on the “*Coupled BC Formation*,” where the input and output currents of the BCs are interconnected in a non-sequential way, in contrast to the cascaded LDSS topology. A new category of bioinspired circuits, termed “*CytoMimetic*” has thus been born, which is able to emulate cellular and molecular dynamics in a systematic manner (Papadimitriou and Drakakis, 2012; Papadimitriou et al., 2013). Intriguingly, apart from the aforementioned linear and non-linear VLSI systems, Bernoulli dynamics are identified in the case of ideal memristors as well (Drakakis and Payne, 2000a; Drakakis et al., 2010; Georgiou et al., 2012a,b). The resemblance between the dynamics of ideal memristors and artificial or not synaptic circuits has been identified repeatedly in literature.

From the research so far, one could claim that the BCF is a “*chimera*” formalism, able to describe both linear and non-linear state-spaces in a systematic manner. It is this systematic nature of the formalism that significantly simplifies the analysis or synthesis attempts in both circuit categories. Identifying and setting the BC as the circuit’s central point, its analysis unfolds conveniently, regardless of the order or complexity of the system’s equations. The scope of this tutorial paper is to expand and enrich the BCF and apply the outcome of this endeavor on the promising

synaptic computation circuit field. In neural networks, synapses are important, key elements regarding information, computation and transmission.

Given the importance of these specialized biological structures, major effort has been put regarding the implementation of single synapses or synaptic networks by means of aVLSI circuits. In this paper we revisit a number of proposed in the literature synaptic circuits and classify them according to the type of their innate Bernoulli Cell operator. With the help of this work it is genuinely hoped that the interested reader will develop a deep understanding for the functionality of this class of low-power circuits and will appreciate the systematic nature of the formalism by consolidating the advantages of using one single framework to describe multiple, different, but in principle similar, log-domain synaptic topologies. This alternative treatment of aVLSI synaptic circuit succeeds in unifying the past analysis approaches of the same circuits under a common aegis and underlines the tutorial value of this paper. Finally, in order to reason for the versatility of the GBCF and to highlight its comparative speed advantage as an analysis tool, an indicative, high-order log-domain circuit topology is drawn from the international literature and is analyzed using both the GBCF and another common log-domain circuit analysis method. The compelling comparison results stress the advantages of using a single mathematical formalism for the description of any log-domain circuit, regardless of its linearity or order of complexity.

## 2. EXPANDING THE BERNOULLI CELL FORMALISM

We start our mathematical analysis by mentioning briefly the equations that are characterizing an emitter/source connected linear capacitor and a BJT/MOST. Thereafter, the base/gate connected linear capacitor case is shown. It is important to stress at this point that the following analysis has been made for an npn-BJT and an n-type MOST. It has been left to the interested reader to verify the existence of a BC-operator in the case, when a pnp-BJT as well as a p-type MOST are emitter/source-connected to a linear capacitor. Further information can be found in the analysis here (Papadimitriou and Drakakis, 2012; Papadimitriou et al., 2013).

Furthermore, in all cases below, it has been assumed that the other plate of the capacitor is held at constant zero voltage (ground). Again, the reader can verify the existence of a BC-operator, when the capacitor's other plate is held at a random constant voltage,  $V_{DD}$ , in all types of transistors. For the MOST analysis, we set the substrate-source voltage ( $V_{BS}$ ) equal to zero to achieve approximately the ideal exponential behavior by eliminating the "body effect." Finally, all MOSTs are assumed to be in deep saturation, so that all transistors are operating qualitatively as constant current sources.

### 2.1. EMITTER/SOURCE-CONNECTED CAPACITOR BC TOPOLOGY

In the past work of Drakakis (Drakakis et al., 1997b, 1999a,b; Drakakis and Payne, 2000b), an explicit analysis has been illustrated regarding the current relation between an emitter-connected capacitor and a BJT. A similar analysis has been also presented regarding the current relation between a weakly-inverted MOST and a source-connected capacitor in

Papadimitriou and Drakakis (2012); Papadimitriou et al. (2013). Both analyses led to the existence of a similar BC-operator and consequently are defined by a similar set of equations. The Bernoulli differential equations of the collector and drain currents of the aforementioned cases are shown below:

#### BJT Case:

$$\dot{I}_C(t) - \left( \frac{\dot{V}_B(t)}{U_T} + \frac{[u(t) - v(t)]}{CU_T} \right) I_C(t) + \frac{I_C^2(t)}{CU_T} = 0 \quad (1)$$

#### Subthreshold MOST Case:

$$\dot{I}_D(t) - \left( \frac{\dot{V}_G(t)}{nU_T} + \frac{[u(t) - v(t)]}{nCU_T} \right) I_D(t) + \frac{I_D^2(t)}{nCU_T} = 0, \quad (2)$$

where  $U_T$  denotes the thermal voltage ( $\sim 26$  mV at 300 K) and  $n$  is the MOST's slope factor ( $n = 1/\kappa$ ). In both cases, the currents  $u(t)$  and  $v(t)$  are the input and output currents of the aforementioned BC-operator (Drakakis et al., 1997b, 1999a,b; Drakakis and Payne, 2000b; Papadimitriou and Drakakis, 2012; Papadimitriou et al., 2013). By applying the non-linear substitution  $I_C(t) = 1/T(t) = I_D(t)$ , relations (1) and (2) are transformed into the following linearised form:

#### BJT Case:

$$\dot{T}(t) + \left( \frac{\dot{V}_B(t)}{U_T} + \frac{[u(t) - v(t)]}{CU_T} \right) T(t) - \frac{1}{CU_T} = 0 \quad (3)$$

#### Subthreshold MOST Case:

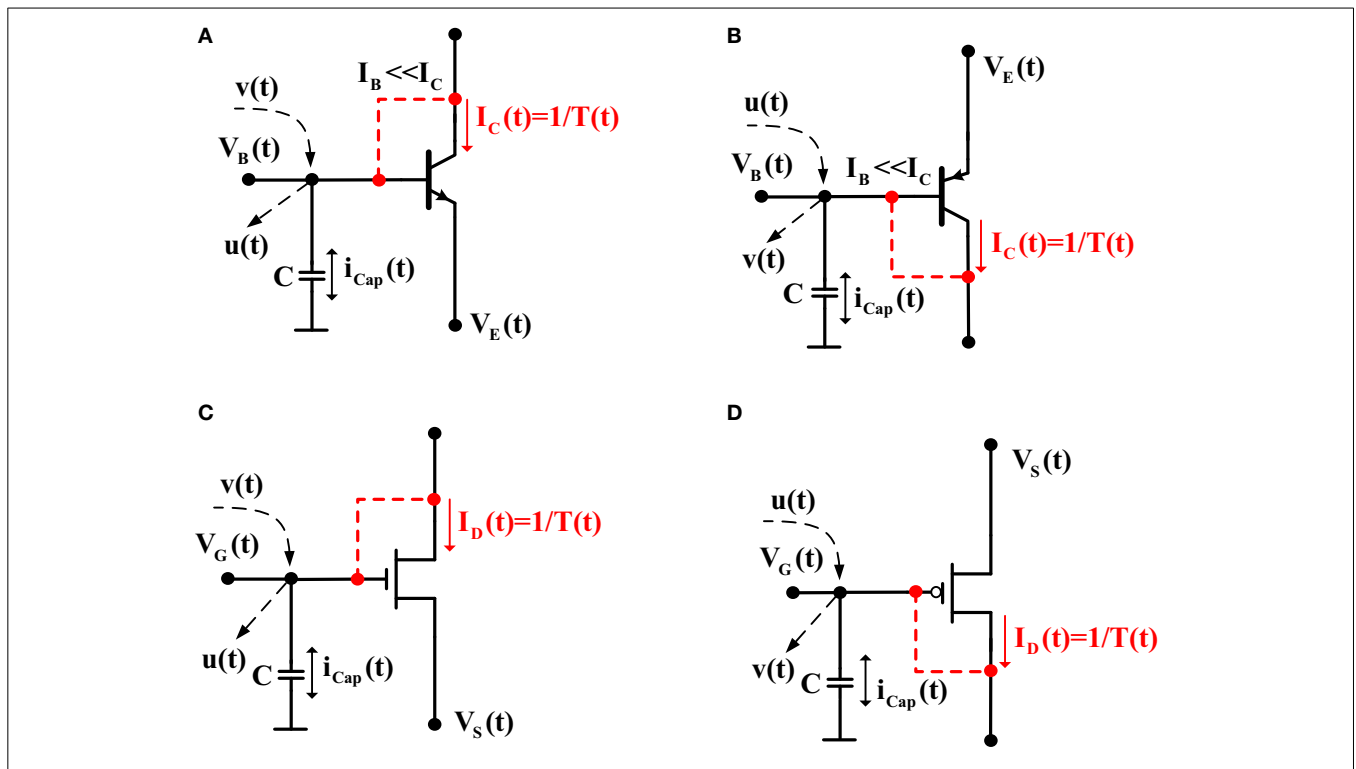
$$\dot{T}(t) + \left( \frac{\dot{V}_G(t)}{nU_T} + \frac{[u(t) - v(t)]}{nCU_T} \right) T(t) - \frac{1}{nCU_T} = 0. \quad (4)$$

The essence of the usefulness of the linearised forms of the BCs is located in the versatility that they provide, when the transfer function of a system is required (Drakakis et al., 1997b, 1999a,b; Drakakis and Payne, 2000b).

### 2.2. BASE/GATE-CONNECTED CAPACITOR BC TOPOLOGY

A closer look at the transistor-capacitor connections in **Figure 1** will illustrate the existence of a different—in principle—BC operator. In this case, there are two possible circuital/connection combinations between the base/gate connected capacitor and the BJT/MOST. The first case, which is going to be explicitly analyzed in the following paragraphs, is the "diode-connected" topology. The second case, which is a subcategory of the first one (and not a focal point of this paper), is when the transistor's current is not responsible for the capacitor's charging and discharging behavior. Both cases will be mathematically analyzed, however, the first case is the most common one that directly exploits the Bernoulli differential equation to describe the transistor's current.

A diode-connected capacitor topology for a BJT is presented in **Figures 1A,B**, while for a subthreshold MOST the topology is shown in **Figures 1C,D**. For the BJT case analysis, we have assumed that the base current of the device is negligible compared to its collector current by considering very large values of  $\beta$ . However, it can be easily verified that even when the base current



**FIGURE 1 | Base/gate-connected capacitors to npn-, pnp-BJT and n-, p-MOSTs that consist the new BC operator.** The arrows defining the direction of the capacitor current are bidirectional, since the BC analysis holds, whether the capacitor is connected to ground or  $V_{DD}$ . The dashed lines reveal the diode-connected transistor case. Although the base current

has been assumed to be significantly smaller than the collector current, the interested reader can verify even if it is comparable to the collector current value, it can still be assumed as a part of the  $u(t)$  output current. **(A)** An npn-BJT-based BC operator; **(B)** A pnp-BJT-based BC operator; **(C)** An n-MOST-based BC operator; **(D)** A p-MOST-based BC operator.

value is comparable to the collector current, it can be interpreted as one of the input/output currents of the BC topology and be assimilated into them. The following analysis will take place for a diode-connected npn-BJT and an n-type MOST.

Applying KCL at the capacitor node (see **Figures 1A,C**), we obtain for the input/output currents of the BC:  $v(t) = u(t) + I_{C,D}(t) + i_{Cap}(t)$ , for the BJT and MOST case, respectively. In both cases, it holds that the capacitor current  $i_{Cap}(t)$  is equal to  $C\dot{V}_{B,G}$ . By differentiating the ideal expressions of  $I_C$  and  $I_D$ , as explicitly shown in Drakakis et al. (1997b, 1999a), Drakakis et al. (1999b); Drakakis and Payne (2000b) the following Bernoulli differential equations are generated:

**BJT Case:**

$$\dot{I}_C(t) + \left( \frac{\dot{V}_E(t)}{U_T} + \frac{[u(t) - v(t)]}{CU_T} \right) I_C(t) + \frac{I_C^2(t)}{CU_T} = 0 \quad (5)$$

**Subthreshold MOST Case:**

$$\dot{I}_D(t) + \left( \frac{\dot{V}_S(t)}{nU_T} + \frac{[u(t) - v(t)]}{nCU_T} \right) I_D(t) + \frac{I_D^2(t)}{nCU_T} = 0. \quad (6)$$

By applying the non-linear substitution  $I_C(t) = 1/T(t) = I_D(t)$ , as shown before, (5) and (6) are converted into the following linearised form:

**BJT Case:**

$$\dot{T}(t) - \left( \frac{\dot{V}_E(t)}{U_T} + \frac{[u(t) - v(t)]}{CU_T} \right) T(t) - \frac{1}{CU_T} = 0 \quad (7)$$

**Subthreshold MOST Case:**

$$\dot{T}(t) - \left( \frac{\dot{V}_S(t)}{nU_T} + \frac{[u(t) - v(t)]}{nCU_T} \right) T(t) - \frac{1}{nCU_T} = 0. \quad (8)$$

The interested reader should note that relations (5–8) exhibit striking similarities compared to the relations (1–4) that hold for the original BC operator case. One of the differences between the relations that describe the two BC operators is located at the sign after the time derivative of the state variable current, i.e.  $\dot{I}_D$  or  $\dot{I}_C$ . Moreover, relations (5–8) demonstrate a dependence on the time derivative of the source/emitter terminal’s voltage of the MOST/BJT rather than on the time derivative of the gate/base terminal’s voltage, as (1–4) do. It needs to be mentioned that the analysis holds, whether the capacitor is connected to ground or  $V_{DD}$ . Finally, regarding the PMOS- or pnp-based “diode-connected” BC operator, trivial circuit analysis will reveal that the sign of the parameter  $\dot{V}_S$  or  $\dot{V}_E$  will change. Once again, all terms of equation (5) and (6) (and consequently 7–8) can be calculated by examining the currents that enter and/or leave at the capacitor node of the BC, except of the term  $\dot{V}_S(t)$  or  $\dot{V}_E(t)$ , which primarily depends on the overall circuit’s setup, as it will be revealed later.

The existence of the new BC operator mainly depends on the existence of a “diode connection” in the MOST or BJT device. When a “diode connection” is present, the state variable current  $I_D(t)$  of the MOST (or  $I_C(t)$  of the BJT) will be responsible for the charging or discharging phases of the capacitor. If one assumes that in the topologies shown in **Figure 1**, the “diode connections,” denoted by the red, dashed lines, are absent, then the transistor’s current will not be involved in the KCL at the capacitor node and relations (5) and (6) are transformed into the following equations:

**BJT Case:**

$$\dot{I}_C(t) + \left( \frac{\dot{V}_E(t)}{U_T} + \frac{[u(t) - v(t)]}{CU_T} \right) I_C(t) = 0 \quad (9)$$

**Subthreshold MOST Case:**

$$\dot{I}_D(t) + \left( \frac{\dot{V}_S(t)}{nU_T} + \frac{[u(t) - v(t)]}{nCU_T} \right) I_D(t) = 0. \quad (10)$$

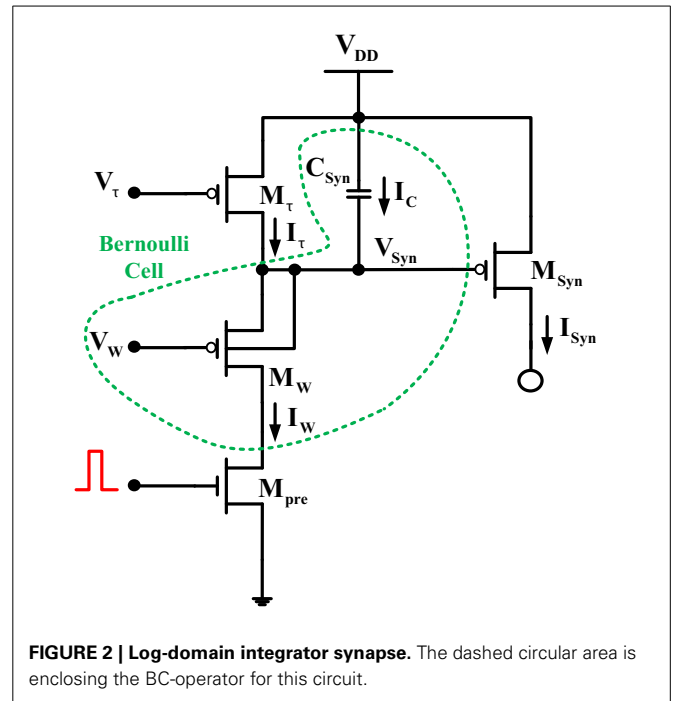
Relations (9) and (10) are not of the Bernoulli form, however, this type of connection can consist a subcategory of the new “diode connection” BC operator case. If one of the input/output currents of the BC is a function of the state-variable current, i.e. if  $u_j$  (and/or  $v_j$ ) =  $\mathcal{F}(I_{C,D})$ , then the Bernoulli differential equation is constructed again. A typical circuit case that verifies this subcategory of the BC topology is the log-domain synaptic circuit originally proposed in Shi and Horiuchi (2004).

### 3. EXEMPLARY SYNAPTIC CIRCUITS’ ANALYSES BASED ON THE GENERALIZED BC FORMALISM

An interesting application, on which the GBCF could be applied, is the popular subcategory of neuromorphic circuits, the silicon synaptic circuits. In neural networks, synapses consist important, key elements regarding information computation and transmission (Bartolozzi and Indiveri, 2007). Given the importance of these specialized structures, major effort has been made regarding the implementation of single synapses or synaptic networks by means of aVLSI circuits. By exploiting the exponential current-voltage relation of weakly-inverted MOSTs a wide variety of circuits has been implemented, capable of simulating different types of synaptic behaviors.

Silicon synapses are able to transform a voltage pulse, which simulates a pre-synaptic signal, into post-synaptic currents that stimulate the membrane of targeted neighboring neurons. Moreover, the gain of such post-synaptic signal, usually referred as synaptic weight, can be also introduced by the specific circuits by simply altering specific electrical parameters, which correspond to equivalent biological parameters (Liu et al., 2001; Bartolozzi and Indiveri, 2007). As these circuits are usually very compact in size, the implementation of very large synaptic networks is possible.

In the following paragraphs, an indicative number of synaptic circuits is going to be analyzed based on the proposed formalism, proving the systematic nature of the GBCF. The selection of the presented circuits is only based on their popularity and extensive



**FIGURE 2 | Log-domain integrator synapse.** The dashed circular area is enclosing the BC-operator for this circuit.

use by the neuromorphic community, as well as on their relatively complicated nature, compared to other similar circuits in this category (Bartolozzi and Indiveri, 2007; Indiveri et al., 2011).

#### 3.1. LOG-DOMAIN INTEGRATOR SYNAPSE

In the tutorial paper of Bartolozzi and Indiveri (Bartolozzi and Indiveri, 2007) a useful synaptic circuit is presented, called “Log-Domain Integrator Synapse” (LDI). The properties of this linear integrator circuit are explicitly presented in Bartolozzi and Indiveri (2007) as well as in the original publications (Merolla and Boahen, 2004, 2006; Arthur and Boahen, 2006) and are similar to the linear properties of a log-domain filter. The  $M_{pre}$  transistor is triggered by a sequence of voltage pulses, where  $t^-$  is the time at which the  $i^{th}$  input spike arrives and  $t^+$  is the time at which it ends.

In order to start the BC-based circuit analysis, it is important to identify first the BC-operator of the given topology. In this case, the BC-operator is enclosed by the dashed green line (see **Figure 2**). Applying KCL at the capacitor node  $V_{Syn}(t)$  reveals:  $I_W(t) = I_\tau(t) + I_C(t)$  with  $I_C(t)$  been equal to  $-C\dot{V}_{Syn}(t)$ . The relation between the state variable current of the BC,  $I_W(t)$  and the output current of the circuit  $I_{Syn}(t)$  can be easily determined:

$$\left. \begin{aligned} I_W(t) &= I_O e^{\frac{V_{Syn}(t) - V_W(t)}{nU_T}} \\ I_{Syn}(t) &= I_O e^{\frac{V_{DD} - V_{Syn}(t)}{nU_T}} \end{aligned} \right\} \Rightarrow I_W(t)I_{Syn}(t) = I_O I_{WO}$$

where the current  $I_{WO}$  is defined as  $I_O \exp(- (V_W(t) - V_{DD}) / (nU_T))$  with  $I_O$  denoting the leakage current of the transistors. The current  $I_{WO}$  designates the initial current that flows through the transistor  $M_W$  when

$V_{DD} = V_{Syn}(t)$  (Bartolozzi and Indiveri, 2007). By differentiating  $I_W(t)$  with respect to time, it yields:

$$\dot{I}_W(t) + \left( \frac{\dot{V}_W(t)}{nU_T} - \frac{I_\tau(t)}{nCU_T} \right) I_W(t) + \frac{I_W^2(t)}{nCU_T} = 0. \quad (11)$$

Since  $V_W$  is a constant bias voltage, its time derivative should be equal to zero, therefore:

$$\dot{I}_W(t) - \frac{I_\tau(t)}{nCU_T} I_W(t) + \frac{I_W^2(t)}{nCU_T} = 0. \quad (12)$$

The time behavior of the state variable current of the BC  $I_W(t)$  is governed by the Bernoulli differential equation. Moreover, based on the relation between the currents  $I_W(t)$  and  $I_{Syn}(t)$ , and between  $I_W(t)$  and  $I_\tau(t)$ , (12) can be re-written as:

$$\tau \dot{I}_{Syn}(t) + I_{Syn}(t) = \frac{I_O I_{WO}}{I_\tau(t)}, \quad (13)$$

with  $\tau = nCU_T/I_\tau(t)$ . The explicit solution of (13) must be separated into two different phases: (a) charge phase of the capacitor, where input current enters the BC and (b) discharge phase of the capacitor, where no input current enters the BC. Summing up both solutions for both phases, the following expressions for the output current  $I_{Syn}(t)$  are obtained:

$$I_{Syn}(t) = \begin{cases} \text{Charge phase:} \\ \frac{I_O I_{WO}}{I_\tau(t)} \left( 1 - e^{-\frac{(t-t_i^-)}{\tau}} \right) + I_{Syn}^- e^{-\frac{(t-t_i^-)}{\tau}} \\ \text{Discharge phase:} \\ I_{Syn}(t)^+ e^{-\frac{(t-t_i^+)}{\tau}} \end{cases}$$

### 3.2. DIFFERENTIAL PAIR INTEGRATOR SYNAPSE

The ‘‘Differential-Pair Integrator (DPI) Synapse’’ was firstly presented in the same tutorial paper of Bartolozzi and Indiveri (Bartolozzi and Indiveri, 2007) in 2007 and is able to reproduce the exponential dynamics observed in both excitatory and inhibitory post-synaptic currents of biological synapses. The idea behind the design of such a circuit is the development of a topology, which maintains its filtering properties while overcoming the LDI’s shortcoming of generating sufficiently large charge packets sourced into the capacitor for brief input spikes. The DPI synapse does not require any additional pulse-extender circuits and in addition it can be manufactured without requiring isolated well structures.

A detailed analysis of this circuit is sufficiently presented in Bartolozzi and Indiveri (2007). Following a series of well-based hypotheses, the authors conclude to the following differential

equation expression of the output current of the circuit,  $I_{Syn}(t)$  (see Figure 3):

$$\tau \dot{I}_{Syn}(t) + I_{Syn}(t) = \frac{I_W(t) I_{Gain}(t)}{I_\tau(t)}, \quad (14)$$

where the term  $I_{Gain}(t) = I_O \exp(-(V_{DD} - V_{THR})/(nU_T))$  represents a virtual p-type MOST and  $\tau = nCU_T/I_\tau(t)$ . The logic assumptions leading to (14) are:  $I_W \gg I_\tau$  and  $I_{Syn} \gg I_{Gain}$ . Based on these assumptions, it is obvious that (14) implements a first order equation similar to one presented for the LDI circuit. The interested reader should note the resemblance between the solutions of the DPI and LDI synaptic circuits. The only fundamental difference, from a mathematical point of view, is that the current  $I_O$  has been replaced by the current of the virtual MOST  $I_{Gain}$ .

For the BC-analysis of the DPI circuit, a similar systematic analysis approach will be applied as in the previous example. The BC has been identified and encircled by the blue dashed line (see Figure 3). Applying KCL at node  $V_{Syn}(t)$  shows that:

$$I_{IN}(t) = I_\tau(t) + I_C(t) \Leftrightarrow \dot{V}_{Syn}(t) = (I_\tau(t) - I_{IN}(t))/C,$$

where  $I_C(t) = -C\dot{V}_{Syn}(t)$ . Considering the drain current of the diode-connected BC transistor:

$$I_{IN}(t) = I_O \exp((V_{Syn}(t) - V_O(t))/(nU_T))$$

as the circuit’s state variable and by differentiating it with respect to time, it yields:

$$\dot{I}_{IN}(t) + \left( \frac{\dot{V}_O(t)}{nU_T} - \frac{I_\tau(t)}{nCU_T} \right) I_{IN}(t) + \frac{I_{IN}^2(t)}{nCU_T} = 0. \quad (15)$$

In order to create an ODE, where all factors can be computed, the time behavior of the term  $\dot{V}_O(t)$  in (15) must be investigated. Starting from the well known relation that holds for the differential pair topology:

$$I_W(t) e^{\frac{V_O(t)}{nU_T}} = I_O \left( e^{\frac{V_{Syn}(t)}{nU_T}} + e^{\frac{V_{THR}}{nU_T}} \right) \quad (16)$$

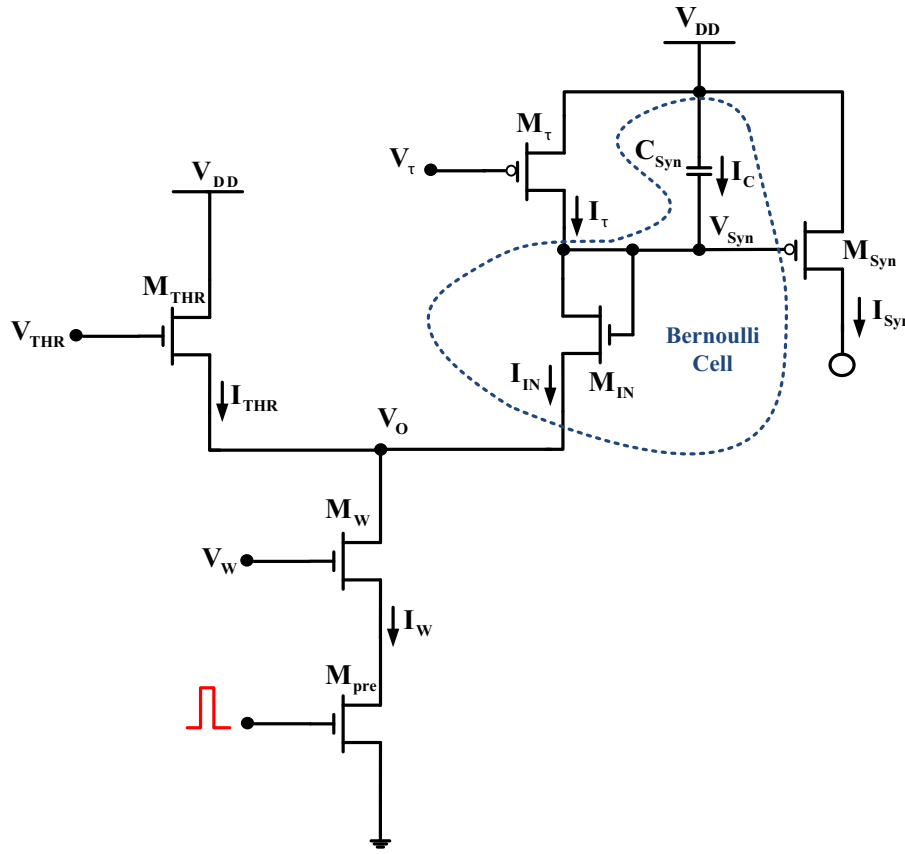
and by differentiating both sides of (16), it holds that:

$$I_W(t) e^{\frac{V_O(t)}{nU_T}} \frac{\dot{V}_O(t)}{nU_T} = I_O e^{\frac{V_{Syn}(t)}{nU_T}} \frac{\dot{V}_{Syn}(t)}{nU_T} + \overbrace{I_O e^{\frac{V_{THR}}{nU_T}} \frac{\dot{V}_{THR}(t)}{nU_T}}^{V_{THR} = const. \Rightarrow \dot{V}_{THR} = 0}$$

After the above treatment, it yields that  $\dot{V}_O(t) = \dot{V}_{Syn}(t) I_{IN}(t)/I_W(t)$ . By substituting this expression into (15), we end up with the following form of ODE:

$$\dot{I}_{IN}(t) + \frac{I_{IN}^2(t) I_\tau(t)}{I_W(t) nCU_T} - \frac{I_{IN}^2(t)}{I_W(t) nCU_T} \frac{I_{IN}(t)}{I_{IN}(t)} + \frac{I_{IN}^2(t)}{nCU_T} - \frac{I_{IN}(t) I_\tau(t)}{nCU_T} = 0$$

or equivalently:



**FIGURE 3 | Differential pair integrator synapse.** The dashed circular area is again enclosing the BC-operator for this circuit.

$$\dot{I}_{IN}(t) - \frac{I_{IN}(t)I_{\tau}(t)}{nCU_T} + \frac{I_{IN}^2(t)}{nCU_T} \left[ \frac{I_{\tau}(t)}{I_W(t)} + \frac{I_{THR}(t)}{I_W(t)} \right] = 0. \quad (17)$$

Based on the valid assumptions that the authors did in Bartolozzi and Indiveri (2007), it holds that  $I_W \gg I_{\tau}$  and also  $I_{THR} \approx I_W$ , thus, (17) is finally transformed into:

$$\dot{I}_{IN}(t) - \frac{I_{IN}(t)I_{\tau}(t)}{nCU_T} + \frac{I_{IN}^2(t)}{nCU_T} = 0. \quad (18)$$

Equation 18 is a Bernoulli ODE with respect to  $I_{IN}(t)$  and can be solved by using the usual non-linear transformation. A brief mathematical explanation why  $I_{THR} \approx I_W$  is provided in the Appendix of the paper. In the final solution of  $I_{IN}(t)$ , we can select to substitute  $I_{IN}(t)$  with its equivalent equation which includes  $I_{Syn}(t)$ . This equivalent expression is derived as follows from the differential pair's key equation:

$$I_{IN}(t) = \frac{I_W(t)\exp(V_{Syn}(t)/(nU_T))}{\exp(V_{Syn}(t)/(nU_T)) + \exp(V_{THR}/(nU_T))} \quad (19)$$

and by multiplying both the numerator and denominator by  $\exp(-V_{DD}/(nU_T))$ , it is easy to express  $I_{IN}$  as:

$$I_{IN}(t) = (I_W(t)I_{Gain}(t)) / (I_{Gain}(t) + I_{Syn}(t)), \quad (20)$$

where  $I_{Gain}$  has been defined above. Therefore, if (20) is placed into the explicit solution of (18) and bearing in mind that  $I_{Syn} \gg I_{Gain}$ , the final expressions for the current  $I_{Syn}(t)$  during charge and discharge phases are described below:

$$I_{Syn}(t) = \begin{cases} \text{Charge phase:} \\ \frac{I_{Gain}(t)I_W(t)}{I_{\tau}(t)} \left( 1 - e^{-\frac{(t-t_i^-)}{\tau}} \right) + I_{Syn}^- e^{-\frac{(t-t_i^-)}{\tau}} \\ \text{Discharge phase:} \\ I_{Syn}^+ e^{-\frac{(t-t_i^+)}{\tau}} \end{cases}$$

It has been left to the reader again to verify that the above solution is similar to the one presented in the original paper, derived for a sequence of voltage pulses with  $\tau = nCU_T/I_{\tau}(t)$ .

#### 4. CURRENT-MODE CIRCUITS FOR DEPRESSING AND FACILITATING SYNAPSES IMPLEMENTATION

Dynamical synapses can be depressing, facilitating or even a combination of these two (Liu, 2003). aVLSI circuits implementing depressing and facilitating synaptic behaviors have been extensively presented and analyzed in literature (Rasche and Hahnloser, 2001; Liu, 2003). In this paper, due to lack of space

reasons, only the mathematical description of a facilitating synaptic circuit will be presented. An identical analysis holds for the description of a circuit emulating a depressing synaptic behavior (Liu, 2003).

**4.1. BC-BASED ANALYSIS OF A FACILITATING SYNAPSE CIRCUIT**

A typical configuration of a circuit implementing a facilitating silicon synapse is the one shown in **Figure 4**. From this Figure one can identify two, distinct “circuit stages,” due to the existence of the two capacitors. In each one of these stages a BC-operator can be identified and will be analyzed separately below. The first BC operator is encircled by the red dashed line, while the second operator is encircled by the blue dashed line.

• **BC-1:** KCL at node  $V_X$  yields that  $I_{D_1}(t) = I_r(t) + I_{C_1}(t)$ , where the capacitor current  $I_{C_1}(t)$  can be also defined as  $C_1 \dot{V}_X$  or  $\dot{V}_X(t) = (I_{D_1}(t) - I_r(t))/C_1$ . The time-derivative of the state variable current of the first BC  $I_{D_1}(t) = I_0 \exp((V_A - V_X)/(nU_T))$  will be:

$$\dot{I}_{D_1}(t) - \frac{I_r(t)}{nC_1U_T}I_{D_1}(t) + \frac{I_{D_1}^2(t)}{nC_1U_T} = 0. \quad (21)$$

As expected, (21) is the Bernoulli ODE governing the drain current dynamics of the diode-connected MOST  $M_1$ . For the calculation of the output current of the first “stage” of the circuit, we need to find the relation between  $I_{D_1}(t)$  and  $I_{Syn_1}(t)$  and substitute it back to (21). The relation between these two currents can be easily derived by writing their full exponential expressions:

$$\frac{I_{D_1}(t)}{I_{Syn_1}(t)} = e^{\frac{V_A - V_{Syn_1}(t) + V_{Syn_1}(t) - V_*}{nU_T}} = \delta = const. ,$$

where  $V_*$  is the source voltage of  $M_5$ , which as illustrated in **Figure 4** is constant. Therefore, (21) transforms into:

$$\dot{I}_{Syn_1}(t) - \frac{I_r(t)}{nC_1U_T}I_{Syn_1}(t) + \frac{\delta I_{Syn_1}^2(t)}{nC_1U_T} = 0. \quad (22)$$

• **BC-2:** For the  $BC_2$ , KCL at the capacitor node  $V_Y$  shows that:  $I_{D_2}(t) + I_{C_2}(t) = I_{Syn_1}(t)$ . Moreover, the capacitor current  $I_{C_2}(t)$  can be also defined as  $C_2 \dot{V}_Y$ , which finally gives  $\dot{V}_Y(t) = (I_{Syn_1}(t) - I_{D_2}(t))/C_2$ . The derivative of the state variable current of the  $BC_2$ ,  $I_{D_2}(t) = I_0 \exp((V_Y(t) - V_b)/(nU_T))$  yields:

$$\dot{I}_{D_2}(t) - \frac{I_{Syn_1}(t)}{nC_2U_T}I_{D_2}(t) + \frac{I_{D_2}^2(t)}{nC_2U_T} = 0. \quad (23)$$

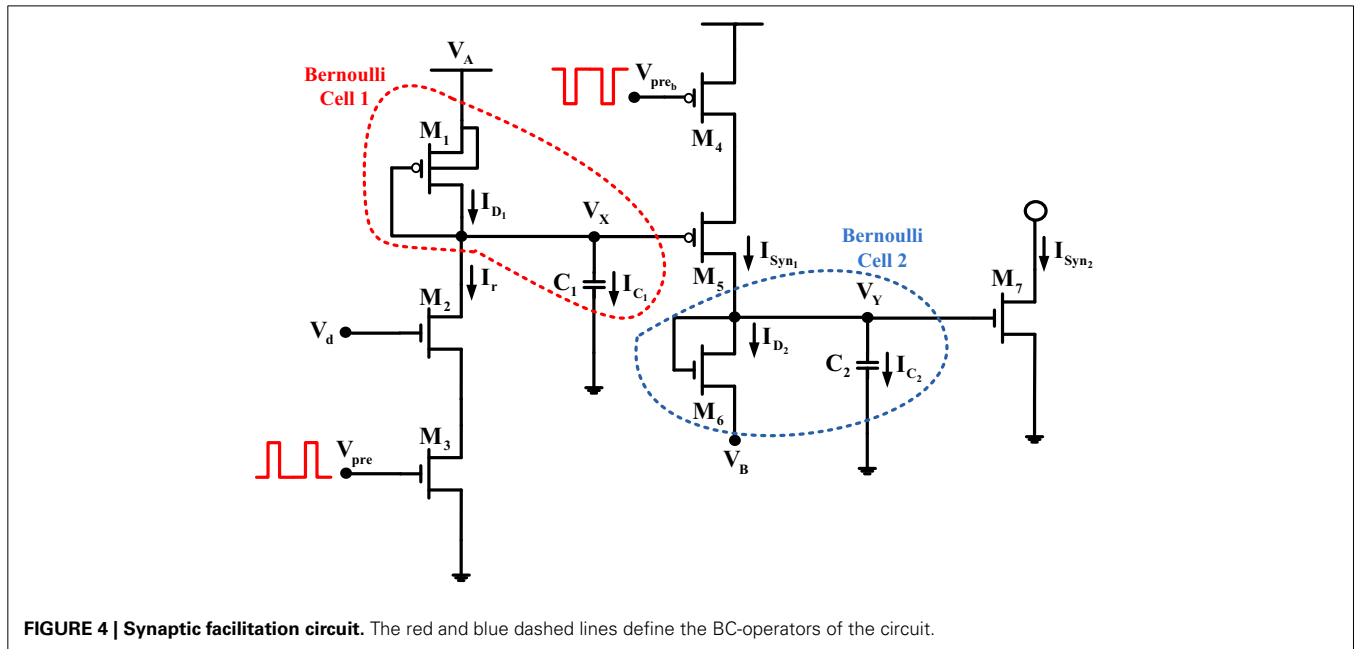
Again, relation (23) identifies the Bernoulli ODE dynamics of the diode-connected MOST  $M_6$ . Moreover, in this “stage” of the circuit, the relation between  $I_{D_2}(t)$  and  $I_{Syn_2}(t)$  is given by the following equation:

$$\frac{I_{D_2}(t)}{I_{Syn_2}(t)} = e^{\frac{V_Y - V_B - V_Y}{nU_T}} = \theta = const. .$$

Thus, the new ODE for the output synaptic current  $I_{Syn_2}(t)$  can be calculated by:

$$\dot{I}_{Syn_2}(t) - \frac{I_{Syn_1}(t)}{nC_2U_T}I_{Syn_2}(t) + \frac{\theta I_{Syn_2}^2(t)}{nC_2U_T} = 0. \quad (24)$$

At this point it would be useful to stress that relation (24) is a BC-cascaded relation, where the output of the first BC is included in the differential equations of the second BC, as a  $v(t)$  current.



**FIGURE 4 | Synaptic facilitation circuit.** The red and blue dashed lines define the BC-operators of the circuit.

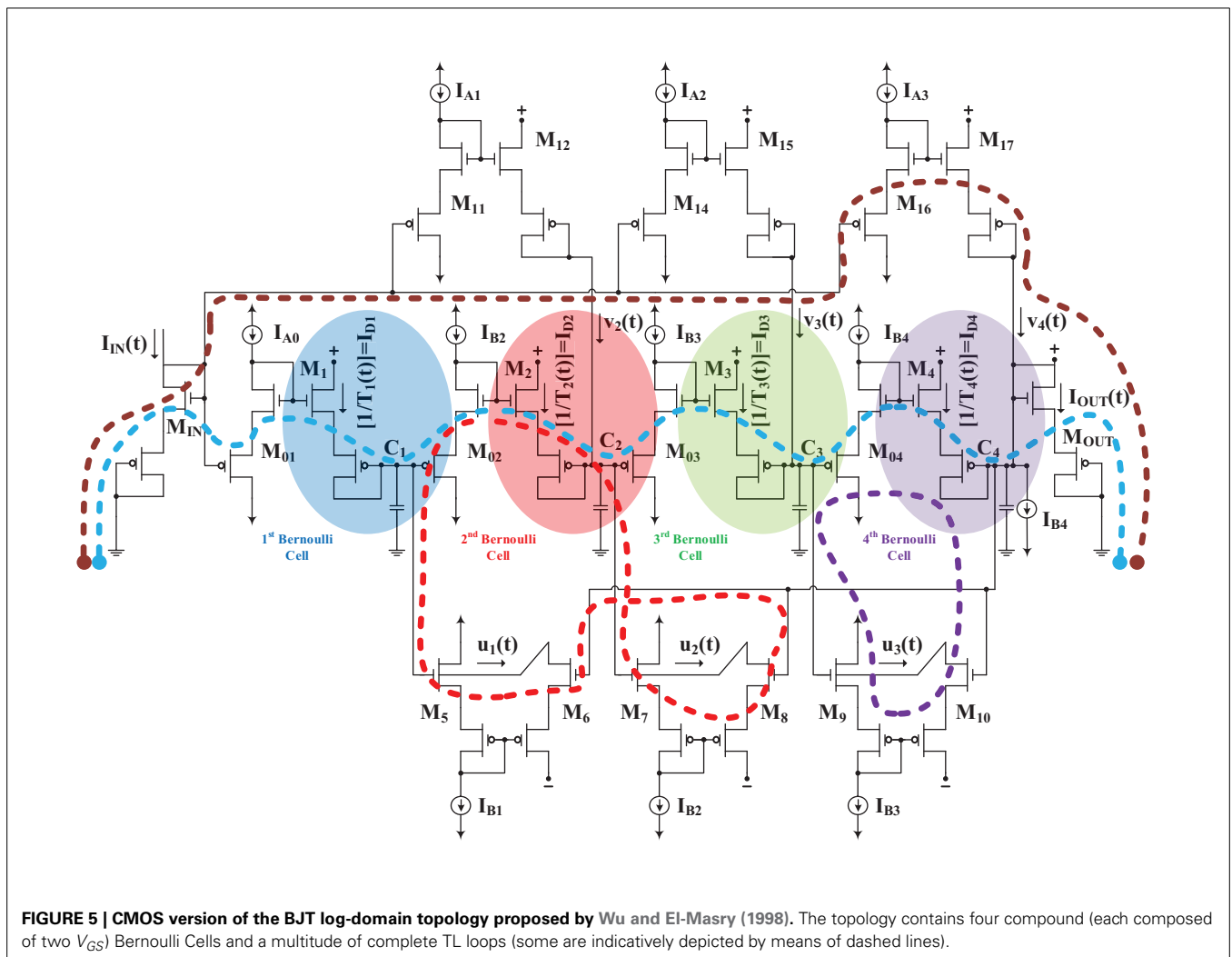
## 5. COMPARATIVE ANALYSIS OF A LOG-DOMAIN TOPOLOGY WITH A HIGH NUMBER OF BERNOULLI CELLS - THE "SPEED UP" IMPACT OF THE FORMALISM

The previous Sections (3 and 4) have proven the reasons why the core dynamics of three well-known log-domain synaptic circuits proposed by different researchers comply with the same distinct Bernoulli dynamics in a formal manner. This mathematical fact alone offers deep and unifying insight since many neuromorphic circuits can be described by the GBCF (see later **Table 2**). It can be argued that the Bernoulli dynamics constitute a formal insightful re-expression of KCL when the derivation of the specific differential equation (which considers the application of KCL at the capacitor node) is born in mind. Such a re-expression is directly applicable/exploitable in a purely TL environment; the same TL environment for which the celebrated Gilbert's TLP can be viewed as a profound re-expression of KVL which has led to the conception of many new, mostly non-linear, monolithic circuits.

Apart from being useful as a taxonomy tool and apart from facilitating researchers to comprehend the essence of the functionality of various log-domain synaptic circuits, is there any additional practical advantage when adopting the Bernoulli Cell

formalism? Experience reveals that the higher the number of Bernoulli Cells present in a log-domain topology be it a non-linear (such as a synapse) or an ELIN one, the faster and less prone to errors its hand-analysis becomes. In order to exemplify vividly how sped up the analysis becomes, in this section we analyse a high-order ELIN log-domain topology both by the general method proposed by Mulder (Mulder et al., 1997; Mulder, 1998) and by the GBCF. The example topology, shown in **Figure 5**, contains four BCs and has been proposed in the international literature by Wu and El-Masry in Wu and El-Masry (1998). In its original form it involved only BJT devices. Here we have substituted the BJT devices for MOSTs and we assume that the n- and p- devices are identical in size and physical properties. This maintains the complexity of the analyses manageable and, most importantly, thus serves the tutorial character of this paper. The aim of this section of the paper is to provide compelling comparative analysis results which shed light in a tutorial manner on "how much" the GBCF speeds up the analysis of a log-domain topology which contains many BCs.

Referring to **Figure 5** and before proceeding with its analysis, it should also be noted that we assume that the dc biasing





currents of the circuit are of such values that each device in the circuit will have a valid dc operating point. This translates into the satisfaction of certain biasing constraints (Drakakis and Burdett, 2003). According to (Mulder et al., 1997; Mulder, 1998), the following steps are necessary, in order to analyse any log-domain topology and derive the relationship between the input and the output (input-output transfer function) in the case of “Externally-Linear-Internally-Nonlinear” log-domain topologies<sup>1</sup>:

**Step 1:** The application of KCL at the integrating nodes of the log-domain topology in question must be considered; the capacitor currents are treated as unknowns.

**Step 2:** The application of the TLP along convenient TL loops must be considered.

**Step 3:** The capacitor currents (the unknowns) must be derived in terms of other currents in the circuit; this can be done by means of mesh analysis treating a capacitor voltage  $V_{C_j}(t)$  and a certain number of MOSTs (gate-source voltage difference) in series with the capacitor as a loop. Expressing  $V_{C_j}(t)$  in terms of the MOST terminal voltages within this loop leads to an equation of the form:

$$V_{C_j}(t) = nU_T \sum \pm \ln \left[ \frac{I_{D_j}(t)}{[W/L]_j I_{D_0}} \right],$$

with the drain currents, the process parameter  $I_{D_0}$  and the aspect ratios of the transistors involved, respectively. Once this has taken place the capacitor currents can be expressed as:

$$i_{C_j}(t) = C_j \dot{V}_{C_j}(t) = nC_j U_T \sum_j \pm \frac{\dot{I}_{D_j}(t)}{I_{D_j}(t)}.$$

Relations of this kind are then used to eliminate the capacitor currents derived during steps 1 and 2; *to derive the final transfer function all capacitor currents must be expressed in terms of the input the output and their derivatives.*

Applying step 1, it can be observed that:

$$I_{D_1}(t) = u_1(t) + i_{C_1}(t) \tag{25a}$$

$$I_{D_2}(t) = u_2(t) - v_2(t) + i_{C_2}(t) \tag{25b}$$

$$I_{D_3}(t) = u_3(t) - v_3(t) + i_{C_3}(t) \tag{25c}$$

$$I_{D_4}(t) = u_4(t) - v_4(t) + i_{C_4}(t), \tag{25d}$$

where  $I_{D_j}(t)$ , ( $j = 1, \dots, 4$ ) the drain current of  $M_j$ , ( $j = 1, \dots, 4$ ). For step 2, applying the TLP along the complete TL loops:  $M_{02}M_2M_7M_8M_6M_5$ ,  $M_7M_8M_{10}M_9M_3M_{03}$ ,  $M_9M_{10}M_4M_{04}$ ,  $M_{IN}M_{01}M_1M_{02}M_2M_{03}M_3M_{04}M_4M_{OUT}$  will lead to the following Translinear current relationships (in **Figure 5** we mark

indicatively a few of the TL loops present to make the analysis more vivid):

$$u_1(t)I_{B2} [u_2(t) - v_2(t) + i_{C_2}(t)] = I_{B1}I_{B2}u_2(t) \tag{26a}$$

$$u_2(t)I_{B3} [u_3(t) - v_3(t) + i_{C_3}(t)] = I_{B2}I_{B3}u_3(t) \tag{26b}$$

$$u_3(t) [I_{B4} - v_4(t) + i_{C_4}(t)] = I_{B3}I_{B4} \tag{26c}$$

$$I_{IN}I_{A0}I_{B2}I_{B3}I_{B4} = [u_1(t) + i_{C_1}(t)] [u_2(t) - v_2(t) + i_{C_2}(t)] [u_3(t) - v_3(t) + i_{C_3}(t)] [I_{B4} - v_4(t) + i_{C_4}(t)] I_{OUT}. \tag{26d}$$

Proceeding to step 3, the capacitor currents  $i_{C_j}(t)$ , ( $j = 1, \dots, 4$ ) that have been treated as unknowns, now have to be related to other output currents in a convenient way. For the capacitor current  $i_{C_4}(t)$ , an elegant expression can be derived:

$$i_{C_4}(t) = 2nC_4U_T \frac{\dot{I}_{OUT}(t)}{I_{OUT}(t)}.$$

However, for the rest of the capacitor currents such a simple expression cannot be similarly obtained. Among the variety of possible ways in which to express the capacitor currents as functions of (internal) circuit currents, certain meshes which seem to result into simple expressions for the capacitor currents are chosen. Considering the paths  $C_3M_9M_{10}M_{OUT}$ ,  $C_2M_7M_8M_{OUT}$ , and  $C_1M_5M_6M_{OUT}$  leads to the following capacitor voltage and current relations, respectively:

$$V_{C3}(t) = 2nU_T \ln \left[ \frac{I_{B3}}{[W/L]I_{D_0}} \right] - 2nU_T \ln \left[ \frac{u_3(t)}{[W/L]I_{D_0}} \right] + 2nU_T \ln \left[ \frac{I_{OUT}(t)}{[W/L]I_{D_0}} \right] \tag{27a}$$

$$V_{C2}(t) = 2nU_T \ln \left[ \frac{I_{B2}}{[W/L]I_{D_0}} \right] - 2nU_T \ln \left[ \frac{u_2(t)}{[W/L]I_{D_0}} \right] + 2nU_T \ln \left[ \frac{I_{OUT}(t)}{[W/L]I_{D_0}} \right] \tag{27b}$$

$$V_{C1}(t) = 2nU_T \ln \left[ \frac{I_{B1}}{[W/L]I_{D_0}} \right] - 2nU_T \ln \left[ \frac{u_1(t)}{[W/L]I_{D_0}} \right] + 2nU_T \ln \left[ \frac{I_{OUT}(t)}{[W/L]I_{D_0}} \right], \tag{27c}$$

which in turn leads to:

$$i_{C_\rho} = C_\rho \dot{V}_{C_\rho}(t) = 2nC_\rho U_T \left[ \frac{\dot{I}_{OUT}(t)}{I_{OUT}(t)} - \frac{\dot{u}_\rho(t)}{u_\rho(t)} \right] (\rho = 1, 2, 3). \tag{28}$$

As mentioned previously  $i_{C_4}(t)$  is in the right “form” being directly related to the output current. However, the other three capacitor currents are not in a desirable form; the currents  $u_3(t)$ ,

<sup>1</sup>The analysis method articulated in Mulder et al. (1997), Mulder (1998) concerned BJT log-domain topologies. Here it is applied for MOSTs log-domain topologies.

$u_2(t)$ ,  $u_1(t)$  must first be expressed in terms of the input, the output and their derivatives. This procedure is cumbersome. In order to demonstrate the difficulty in expressing the aforementioned currents in the correct “form,” only the procedure to express the current  $u_3(t)$  in terms of the input, the output and their derivatives will be demonstrated. Taking relation (26c) into consideration,  $u_3(t)$  can be described as:

$$u_3(t) = \frac{I_{B3}I_{B4}}{I_{B4} - v_4(t) + i_{C4}(t)},$$

with  $i_{C4}(t)$  given before. The current  $v_4(t)$  however must also be written in a convenient format; considering the complete TL loop  $M_{IN}M_{16}M_{17}M_{OUT}$  yields:

$$I_{IN}(t)I_{A3} = v_4(t)I_{OUT}(t) \Rightarrow v_4(t) = I_{A3} \frac{I_{IN}(t)}{I_{OUT}(t)}.$$

From the previous relations for  $i_{C4}(t)$  and  $v_4(t)$ , it is a matter of complicated algebraic substitutions to express the current  $u_3(t)$  in the “correct form” (i.e. expressed in terms of the input current, the output current and their derivative) as:

$$u_3(t) = \mathcal{F}_{u_3}(I_{OUT}, \dot{I}_{OUT}) = \frac{I_{B3}I_{B4}}{I_{B4} - \frac{I_{A3}I_{IN}}{I_{OUT}} + 2nC_4U_T \frac{\dot{I}_{OUT}}{I_{OUT}}}.$$

Substituting the relation for  $u_3(t)$  into (28) ( $\rho = 3$ ) results into the following expression, just for  $i_{C3}(t)$ :

$$i_{C3}(t) = \mathcal{F}_{C3}(I_{OUT}, \dot{I}_{OUT}, \ddot{I}_{OUT}, \dot{I}_{IN}) = \left( \begin{array}{c} -I_{B3}I_{B4} \left( -I_{A3} \frac{\partial}{\partial t} \left( \frac{I_{IN}}{I_{OUT}} \right) + 2nC_4U_T \frac{\partial}{\partial t} \left( \frac{\dot{I}_{OUT}}{I_{OUT}} \right) \right) \\ \frac{\dot{I}_{OUT}}{I_{OUT}} - \frac{\left( I_{B4} - \frac{I_{A3}I_{IN}}{I_{OUT}} + 2nC_4U_T \frac{\dot{I}_{OUT}}{I_{OUT}} \right)^2}{\frac{I_{B3}I_{B4}}{I_{B4} - \frac{I_{A3}I_{IN}}{I_{OUT}} + 2nC_4U_T \frac{\dot{I}_{OUT}}{I_{OUT}}}} \end{array} \right) \quad (29)$$

In a similar manner, all the remaining currents  $i_{C2}(t)$ ,  $i_{C1}(t)$ ,  $u_1(t)$ ,  $u_2(t)$  etc. need to be defined in the “correct form.” Having reached that point, we would finally need to substitute to, say, (26d) all the expressions of the “correct form” found and determine the input-output transfer function. Or one might choose to substitute all the “correct form” expressions to the TL equality:

$$I_{IN}(t)I_{A0}u_1(t) = [u_1(t) + i_{C1}(t)] I_{B1}I_{OUT}(t),$$

which correspond to the TL loop  $M_{IN}M_{01}M_1M_5M_6M_{OUT}$  and again determine the input-output transfer function.

Clearly this analysis procedure is tedious, time-consuming and prone to errors since all the “intermediate”  $u_j(t)$  and  $v_j(t)$  currents must be expressed in the right format. These requirements are

compounded when large topologies with a large number of intermediate currents are considered, making the method difficult to apply as far as hand calculations are considered. At this point it is worth mentioning that the situation is somewhat improved, when a variation of the method is considered which consists of the incorporation of additional “fictitious” exponential expansion stages which convert the logarithmically compressed capacitor voltages  $V_{C1}(t)$ ,  $V_{C2}(t)$  and  $V_{C3}(t)$  to exponentially expanded currents, without affecting the circuit operation. These additional stages add complexity to the circuit but lead to the formation of three more, perhaps more convenient complete TL loops, which relate the “fictitious” output currents with the real output current  $I_{OUT}$  shown in **Figure 5**. However, further elaboration on that analysis method is beyond the scope of this work.

Now let us analyse the same log-domain structure by means of the GBCF. Four distinct BCs can be identified; the first one is logarithmically driven by the input current  $I_{IN}(t)$ . This cascade of compound BCs can be described by means of the following LDSS equations, i.e.:

$$2nC_1U_T\dot{w}_1(t) + [u_1(t) - v_1(t)] w_1(t) = I_{IN}(t) \quad (30a)$$

$$2nC_2U_T\dot{w}_2(t) + [u_2(t) - v_2(t)] w_2(t) = w_1(t) \quad (30b)$$

$$2nC_3U_T\dot{w}_3(t) + [u_3(t) - v_3(t)] w_3(t) = w_2(t) \quad (30c)$$

$$2nC_4U_T\dot{w}_4(t) + [u_4(t) - v_4(t)] w_4(t) = w_3(t). \quad (30d)$$

The products  $u_j(t)w_j(t)$  and  $v_j(t)w_j(t)$  are determined as required by applying the TLP along complete TL loops. Considering the time-domain current product equalities resulting from the TL loops: (i)  $M_5M_6M_4M_{04}M_3M_{03}M_2M_{02}$ , (ii)  $M_7M_8M_4M_{04}M_3M_{03}$ , (iii)  $M_9M_{10}M_4M_{04}$ , (iv)  $M_{01}M_1M_{02}M_2M_{12}M_{11}$ , (v)  $M_{01}M_1M_{02}M_2M_{03}M_3M_{15}M_{14}$ , (vi)  $M_{01}M_1M_{02}M_2M_{03}M_3M_{04}M_4M_{17}M_{16}$ , and (vii)  $M_{IN}M_{01}M_1M_{02}M_2M_{03}M_3M_{04}M_4M_{OUT}$  yields respectively:

$$u_1(t)w_1(t) = I_{B1}I_{B2}I_{B3}I_{B4}T_4(t)T_3(t)T_2(t)w_1(t) = I_{B1}I_{B2}I_{B3}I_{B4}w_4(t) \quad (31a)$$

$$u_2(t)w_2(t) = I_{B2}I_{B3}I_{B4}T_4(t)T_3(t)w_2(t) = I_{B2}I_{B3}I_{B4}w_4(t) \quad (31b)$$

$$u_3(t)w_3(t) = I_{B3}I_{B4}T_4(t)w_3(t) = I_{B3}I_{B4}w_4(t) \quad (31c)$$

$$v_2(t)T_2(t)T_1(t)I_{IN}(t) = v_2(t)w_2(t) = \frac{I_{A1}}{I_{A0}I_{B2}}I_{IN}(t) \quad (31d)$$

$$v_3(t)T_3(t)T_2(t)T_1(t)I_{IN}(t) = v_3(t)w_3(t) = \frac{I_{A2}}{I_{A0}I_{B2}I_{B3}}I_{IN}(t) \quad (31e)$$

$$v_4(t)T_4(t)T_3(t)T_2(t)T_1(t)I_{IN}(t) = v_4(t)w_4(t) = \frac{I_{A3}}{I_{A0}I_{B2}I_{B3}I_{B4}}I_{IN}(t) \quad (31f)$$

$$I_{OUT}(t) = I_{A0}I_{B2}I_{B3}I_{B4}T_4(t)T_3(t)T_2(t)T_1(t)I_{IN}(t) = I_{A0}I_{B2}I_{B3}I_{B4}w_4(t). \quad (31g)$$

Substituting the relations (31a)–(31g) into the LDSS equations (30) results in the following system of differential equations:

$$2nC_1U_T\dot{w}_1(t) + I_{B1}I_{B2}I_{B3}I_{B4}w_4(t) = I_{IN}(t) \quad (32a)$$

$$2nC_2U_T\dot{w}_2(t) + I_{B2}I_{B3}I_{B4}w_4(t) - \frac{I_{A1}}{I_{A0}I_{B2}}I_{IN}(t) = w_1(t) \quad (32b)$$

$$2nC_3U_T\dot{w}_3(t) + I_{B3}I_{B4}w_4(t) - \frac{I_{A2}}{I_{A0}I_{B2}I_{B3}}I_{IN}(t) = w_2(t) \quad (32c)$$

$$2nC_4U_T\dot{w}_4(t) + I_{B4}w_4(t) - \frac{I_{A3}}{I_{A0}I_{B2}I_{B3}I_{B4}}I_{IN}(t) = w_3(t). \quad (32d)$$

This system of equations combined with  $I_{OUT}(t) = I_{A0}I_{B2}I_{B3}I_{B4}w_4(t)$  (which corresponds to the Bernoulli “backbone” TL loop  $M_{IN}M_{01}M_1M_{02}M_2M_{03}M_3M_{04}M_4M_{OUT}$ ) results in the following transfer function  $I_{OUT}(s)/I_{IN}(s)$ :

$$\frac{I_{OUT}(s)}{I_{IN}(s)} = \frac{I_{A3}}{2nC_4U_T} \frac{s^3 + \frac{I_{A2}I_{B4}}{I_{A3}2nC_3U_T}s^2 + \frac{I_{A1}I_{B3}I_{B4}}{I_{A3}C_2C_3(2nU_T)^2}s + \frac{I_{A0}I_{B2}I_{B3}I_{B4}}{I_{A3}C_1C_2C_3(2nU_T)^3}}{s^4 + \frac{I_{B4}}{C_42nU_T}s^3 + \frac{I_{B3}I_{B4}}{C_3C_4(2nU_T)^2}s^2 + \frac{I_{B2}I_{B3}I_{B4}}{C_2C_3C_4(2nU_T)^3}s + \frac{I_{B1}I_{B2}I_{B3}I_{B4}}{C_1C_2C_3C_4(2nU_T)^4}}. \quad (33)$$

Clearly this BC-based analysis of log-domain structures with a large number of Bernoulli Cells seems to be simpler in its application, faster in its execution and less prone to errors for hand-analysis purposes.

### 6. GENERAL CLASS OF LOG-DOMAIN SYNAPTIC CIRCUITS

The systematic properties of the BCF emerge naturally from the analysis of all the previous synaptic circuit examples so far. The output currents of each circuit ( $I_{Synj}(t)$ ) were described either by a linear or a Bernoulli DE. However, all of them stem from the Bernoulli DE characterizing the BC-operator. The presence of the BC-operator in the aforementioned circuits allowed us to articulate certain “rules-of-thumb” regarding the analysis strategy that needs to be followed, when this category of circuits is investigated. These “rules-of-thumb” are only aiming to help the designer simplify the analysis/synthesis process, by exploiting the systematic nature of the BCF.

One may also note that for each one of the presented circuit topologies, a certain number of specific steps has been followed, in order to reach a final form of ODE that could describe the  $I_{Synj}(t)$  current. Many of these steps served the purpose of clarifying to the reader that the BC-based analysis was behind the

final form of the solution of the various output synaptic currents. Now that this point has been proved, it is time to group synaptic circuits under one general class of neuromorphic log-domain circuits, whose state-variable current could be governed by a specific set of equations, as shown in **Table 1**.

Regardless of the circuit topology that has been selected from the designer to implement a synaptic function, the BC-operator is always governed by the Bernoulli differential equation, whose linearised form is shown in (34) in general form. When a source-connected capacitor topology is present, (+) holds, while (–) holds when a diode-connected capacitor topology exists. As graphically shown in **Figure 6**, one can identify the dynamics of each circuit by simply examining the current relation that takes place in the circuit’s “basic computation unit,” i.e. the BC. The parameter  $\dot{V}_X$  in (34) denotes the potential of either the source or the gate terminal of the BC MOST, depending on the type of the BC operator.

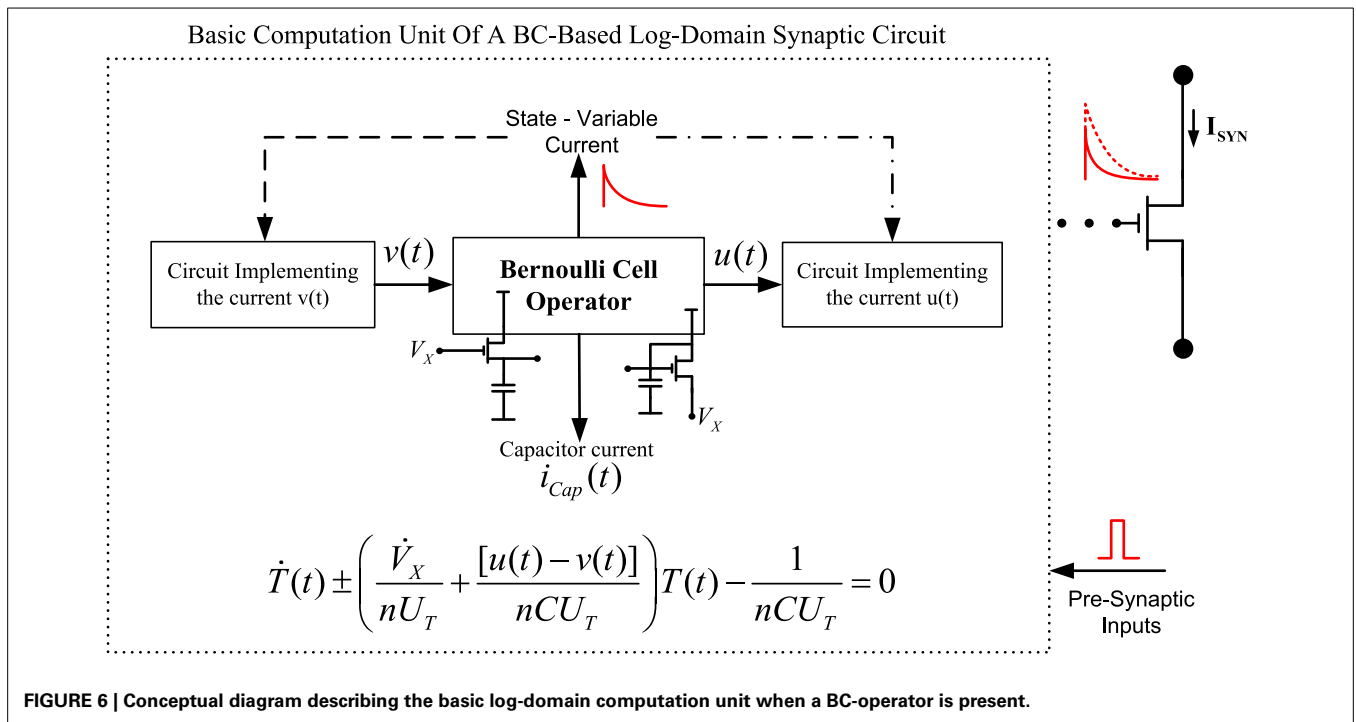
$$\dot{T}(t) \pm \left( \frac{\dot{V}_X(t)}{nU_T} + \overbrace{\left[ \frac{u(t) - v(t)}{nCUT} \right]}^{\text{Time Constant Factors}} \right) T(t) - \frac{1}{nCUT} = 0. \quad (34)$$

The input/output currents  $u(t)$  and  $v(t)$  entering the BC (including the state-variable current  $I_D(t)$  for the MOST case) are responsible for the charging and discharging phases of the circuit’s capacitor; therefore, define the circuit’s “rate constants” and consequently the form of the synaptic current. By identifying and analysing the BC-operator of each circuit, one is able to instantly define the dynamics of the circuit’s output current by simply observing the relation between the BC’s state variable current and the desired output current. A linear relation between the BC-state variable and the output synaptic current, e.g.,  $I_D \propto \text{constant} \times I_{Syn}$  will lead to a Bernoulli ODE for the description of  $I_{Syn}(t)$ , while a non-linear relation, e.g.,  $I_D \propto \text{constant}/I_{Syn}$ , will lead to a linear ODE for the computation of  $I_{Syn}(t)$  dynamics. All the above practical guidelines can be easily summarized into the following three basic circuit analysis steps/guidelines:

- Step 1:** Identify the BC-operator(s) by simply observing the connection between the circuit’s capacitor(s) and the neighboring transistor(s);
- Step 2:** Once the BC-operator(s) is/are located, identify the relation between the state-variable current(s) of the operator(s) and the circuit’s output current(s);
- Step 3:** If the relation between the BC operator(s) and the circuit’s output current(s) is linear, then substitute the new relation for the output synaptic current  $I_{Synj} = \mathcal{F}(\text{state variable})$

**Table 1 | Forms of ODEs and their solutions stemming from the proposed general log-domain class of synaptic circuits.**

	Linear equation	Bernoulli equation
Form of ODE	$g(t)y'_t = f_1(t)y + f_0(t)$	$g(t)y'_t = f_1(t)y + f_n(t)y^n, n \neq 0, 1$
General solution	$y = Ke^\Lambda + e^\Lambda \int e^{-\Lambda} f_0(t)/g(t)dt$	$y^{(1-n)} = Ke^\Lambda + (1-n)e^\Lambda \int e^{-\Lambda} f_n(t)/g(t)dt$
$\Lambda$	$\int f_1(t)/g(t)dt$	$(1-n) \int f_1(t)/g(t)dt$



current) into (34) and solve the resulting differential equation. If their relation is of the form  $I_D \propto \text{constant}/I_{Syn}$ , then a linear DE will be inevitably generated and the factor  $(I_{Syn_i}/\text{constant})$  should directly substitute the factor  $T(t)$  in (34);

The interesting attempt of Mitra et al. (2010) to provide a global parametric control of synaptic time constants and gain generates the ideal breeding ground for the application of this general class of synaptic dynamics created by the GBCE. For the various log-domain integrator circuit cases presented and analyzed in Mitra et al. (2010) (with a method similar to the one presented by Perry and Roberts in Perry and Roberts (1995), but “silicon-synapse-oriented”), the BC-operator will produce the exact similar solutions for the synaptic output current but all based on the different forms of the parameters  $V_X$  and  $[u(t) - v(t)]$  sourcing from the different topologies. **Table 2** provides an indicative number of neuromorphic topologies that could be easily implemented by the proposed GBCE.

At this point, an inverse question that arises is how one can design a synaptic aVLSI circuit, based on the fact that it will always be described by the specific type of equations? The answer to this synthesis question relates to the determination of the function  $F$  which links the BC state variable with  $I_{Syn_j}(t) = \mathcal{F}(\text{state variable current})$  in such a way that the current  $I_{Syn_j}(t)$  has certain pre-specified time profile properties. Issues, such as the practicality of the circuit, in conjunction with the form of the desired dynamics and its total chip area will definitely play a major role in the selection of the final form of the synaptic circuit. However, its “analog heart” implemented by the BC will be identical in all cases.

**Table 2 | An indicative list of neuromorphic circuits that could be described by the BC formalism.**

Authors	Number of BCs
Arthur and Boahen (2011)	3
Benjamin et al. (2012)	2
Boahen (1997)	1
Gao et al. (2012)	2
Hahnloser et al. (2000)	1
Hynna and Boahen (2003)	2
Merolla and Boahen (2006)	2
Mitra et al. (2010)	3
Thanapitak and Toumazou (2013)	1
van Schaik et al. (2010)	2
Wang and Liu (2010)	3
Yu and Cauwenberghs (2010)	1

Finally, for the sake of completeness, it would be useful to remind the reader that all previous mathematical formulas have been derived based on the valid assumption that the voltage difference between the bulk and source terminal of the subthreshold MOSTs is zero, i.e.  $V_{BS} = 0$ . However, this assumption represents the ideal operation of a weakly-inverted MOST, without taking into consideration the impact of the “body effect” upon the devices’ overall performance. Other indicative limitations that restrain a MOST in the subthreshold regime and affect the device’s performance are the output resistance, matching, bandwidth and noise limitations, as well as short-channel effects, such as the drain induced barrier lowering (DIBL) (Andreou and Boahen, 1996). Useful mathematical relationships that manage

to quantify the aforementioned limitations and therefore, provide useful guidelines when it comes to the selection of critical MOST parameters can be found in Andreou and Boahen (1996).

The most common limitation for a MOST in weak-inversion involves the non-zero voltage difference between its bulk and source terminals. The effect of this limitation upon the GBCF can be shown in the following indicative mathematical analysis. Starting from the full mathematical expression that defines the current of a subthreshold n-type MOST (Tsvividis, 1996), assuming again that the device is in deep saturation, it holds that:

$$I_D = \frac{W}{L} I_{D0} \exp\left(\frac{(n-1)V_{BS}}{nU_T}\right) \exp\left(\frac{V_{GS} - V_{TH}}{nU_T}\right),$$

where  $I_{D0}$  is a process-dependent parameter,  $W/L$  is the aspect ratio of the transistor and  $n$  is again the subthreshold slope parameter (Tsvividis, 1996). This expression can be re-written equivalently as:

$$I_D = \hat{I}_{D0} \exp\left(\frac{V_{GS} + (n-1)V_{BS}}{nU_T}\right),$$

where  $\hat{I}_{D0} = (W/L) I_{D0} \exp(-V_{TH}/(nU_T))$ . For the circuit topologies originally mentioned in Section 2 and under the assumption that the bulk terminal of the device has been tied to a constant voltage source, the time derivative of the new expression of  $I_D$  current, when a linear capacitor is connected to its source terminal would lead to the following linearised expression (using the same transformation as shown in section 2, i.e.  $I_D(t) = 1/T(t)$ ), depending on the type of the BC operator:

$$\dot{T}(t) \pm \left( \frac{\dot{V}_X(t)}{nU_T} + \overbrace{\frac{[u(t) - v(t)]}{CU_T}}^{\text{Time Constant Factors}} \right) T(t) - \frac{1}{CU_T} = 0, \quad (35)$$

with the parameter  $\dot{V}_X$  in (35) denoting again the potential of either the source or the gate terminal of the BC MOST, depending on the type of the BC operator. The interested reader should verify that unit consistency has been preserved in (35), in complete analogy with (34). Interestingly enough, from (35), it can be extracted that the time constant factor does not exhibit a dependence upon the subthreshold slope parameter  $n$ . In other words, the effect of this MOST non-ideality has led to the following conclusion regarding GBCF, i.e.:

$$\frac{\text{Silicon Synaptic Time Constant Factor}_{V_{BS} \neq 0}}{\text{Silicon Synaptic Time Constant Factor}_{V_{BS} = 0}} = n \times$$

Once again, in complete analogy with the above analysis, the interested reader could investigate the effect of other MOST limitations upon the overall performance and consequently acquire handy relations that could inform, in a quantitatively and qualitative manner, about the deviation of the device from its ideal behavior.

## 7. DISCUSSION

The paper discussed in a tutorial manner an alternative transistor-level method to treat log-domain synaptic circuits. An extended version of the BCF proved the existence of BC-operators not only when a linear capacitor is connected to the emitter/source of a transistor but also when a linear capacitor is connected to the base/gate of a diode-connected transistor. The usefulness of this endeavor lies in the handiness of the BCF when it comes to the analysis (or synthesis) of linear and/or non-linear log-domain circuits. By providing one more topology, the “diode-connected” BC operator where the BCF applies, this paper extends the solid mathematical background, where engineers can rely upon when it comes to the study and design of log-domain circuits for neuromorphic or other applications.

The analysis of the synaptic circuits presented and analyzed in the previous sections stresses the taxonomic prowess of the BCF. The core operation of synaptic circuits is based ultimately on the exponentiation of a capacitor voltage during its charging/discharging phases facilitated by a MOST. The rest of the circuit is used to provide the correct weights and time constants of the artificial synapse, so that a more faithful representation of the biological synapse model is achieved. The independent nature of the BC-operator’s input and output currents [ $u(t)$  and  $v(t)$ ] allows, in principle, for the designer to determine the appropriate circuit topology that will generate the desired dynamics.

It is left to the readers to evaluate the benefits of using the aforementioned parsimonious formalism for log-domain synaptic and other neuromorphic circuits. It is genuinely hoped that the tutorial nature of this paper will provide a helping hand to engineers wishing to explore aVLSI synaptic circuits in a more intuitive way, streamlining their mathematical analysis in a rigorous manner.

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**APPENDIX**

Starting for the fact that in the given circuit  $I_{Syn} \gg I_{Gain}$ , then their full expressions should be:

$$I_O e^{\frac{V_{DD} - V_{Syn}}{nU_T}} \gg I_O e^{\frac{V_{DD} - V_{THR}}{nU_T}}$$

or

$$e^{-\frac{V_{Syn}}{nU_T}} \gg e^{-\frac{V_{THR}}{nU_T}}$$

which easily leads to the following inequality for the two voltages:  $V_{THR} \gg V_{Syn}$ , or equivalently  $I_{THR} \gg I_{IN}$ .