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Transparent Thin-Film Transistors Based on Sputtered Electric Double Layer

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Abstract: Electric-double-layer (EDL) thin-film transistors (TFTs) have attracted much attention due to their low operation voltages. Recently, EDL TFTs gated with radio frequency (RF) magnetron sputtered SiO_2 have been developed which is compatible to large-area electronics fabrication. In this work, fully transparent Indium-Gallium-Zinc-Oxide-based EDL TFTs on glass substrates have been fabricated at room temperature for the first time. A maximum transmittance of about 80% has been achieved in the visible light range. The transparent TFTs show a low operation voltage of 1.5 V due to the large EDL capacitance (0.3 μF/cm^2 at 20 Hz). The devices exhibit a good performance with a low subthreshold swing of 130 mV/dec and a high on-off ratio > 10^5. Several tests have also been done to investigate the influences of light irradiation and bias stress. Our results suggest that such transistors might have potential applications in battery-powered transparent electron devices.

Keywords: electric-double-layer (EDL); radio frequency (RF) magnetron sputtered SiO_2; transparent thin-film transistors (TFTs)

1. Introduction

Oxide semiconductors have gained much attention particularly in the last decade due to their high mobility, good uniformity over large area, low fabrication temperature, and low cost [1–3]. Nowadays, transparent oxide-based thin-film transistors (TFTs) have been used in many applications such as active-matrix liquid crystal displays and organic light-emitting diode displays [4,5]. However, by using conventional dielectrics, such TFTs usually require large operation voltages, resulting in high power consumption and thus making them unsuitable for battery-powered portable applications.

In order to lower the operation voltage, the most common method is using a thin dielectric layer, like ultrathin cross-linked films or self-assembled monolayers [6–8]. However, this might cause a large gate leakage because of the challenges of maintaining a very high degree of uniformity over a large area. Another way is using high-κ dielectrics to increase the gate coupling between the electrode and the channel layer [9–11]. In 2015, Zhou and coworkers reported that, by using high-κ $Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT) as dielectric layer, the operation voltage of the devices could be reduced to 1 V [10]. However, such high-κ dielectric materials usually have a problem of threshold voltage control due to the large fixed charge trap densities and therefore the devices might have a serious issue of long-term reliability [12].

Recently, many groups have tried using polymer electrolytes (polyelectrolytes) or ionic liquids (ion gels) as gate dielectric to reduce the operation voltage due to the large electric-double-layer (EDL) capacitance formed at the channel/dielectric interface [13–15]. Pu et al. reported on MoS_2-based EDL TFTs using ion gel as gate dielectric in 2012 and achieved an operation voltage less than 1 V [16]. However, the chemical stability of polymer electrolytes is not good, especially at high temperatures.

Ionic liquids or ion gels also have limitations due to the difficulties of controlling their shapes, uniformity, and thickness. Some solid-state electrolytes, mainly SiO_2 and Al_2O_3, were therefore introduced [17–21]. Jiang et al. reported transparent EDL-based TFTs that could reach an operation voltage of 1 V and a current on-off ratio larger than 10^6 by using plasma-enhanced chemical vapor deposition (PECVD) deposited SiO_2 as a dielectric layer [22]. However, the processing gases and the by-products of PECVD might be toxic, flammable, and explosive.

In manufacturing, sputtering techniques offer a more cost-effective way for the fabrication of large area oxide-semiconductor based electronics. Recently, we developed a novel way to produce SiO_2 electrolyte using sputtering method and the obtained TFTs showed an 1 V operation voltage and a subthreshold swing close to the theoretical limit [23]. The devices however were fabricated using non-transparent source-drain and gate electrodes.

In this paper, we report transparent EDL-based TFTs that are fabricated at room temperature with radio-frequency (RF) magnetron sputtering method only, which is, to the best of our knowledge, the first all sputtered, transparent, EDL transistor to date. The transistors have an operation voltage of 1.5 V and a maximum transmittance about 80% in the visible light region. Also, the transistors show good electrical properties with a current on-off ratio larger than 10^5 and a subthreshold swing about 130 mV/dec.

2. Materials and Methods

Transparent Indium-Gallium-Zinc-Oxide (IGZO)-based TFTs were fabricated on glass substrates at room temperature using bottom gate top contact structure. A schematic diagram of the transistors is shown in Figure 1a. First, 200-nm-thick ITO was deposited on as the gate electrode by RF magnetron sputtering using indium tin oxide (ITO) target (90 wt % In_2O_3 and 10 wt % SnO_2) at 40 W. Then, a 200-nm-thick SiO_2 gate dielectric layer was deposited on by RF magnetron sputtering using SiO_2 target at 85 W. After that, a 70-nm-thick IGZO as the channel layer was deposited on by RF magnetron sputtering at 40 W. Finally, 200-nm-thick ITO source and drain electrodes were deposited on by RF magnetron sputtering using ITO target at 40 W. The sputtering processes were kept at a pressure of 5×10^{-3} mbar in pure argon. All layers were patterned using shadow masks. The channel length and width were 60 μm and 2 mm, respectively. The electrical properties of the devices were measured using Agilent E5270B semiconductor analyzer (Agilent, Santa Clara, CA, USA) and Agilent E4980A LCR metre (Agilent) in air ambient. The cross-sectional view of SiO_2 was investigated by using FEI Nova NanoSEM 450 scanning electron microscope (SEM, FEI, Hillsboro, OR, USA).

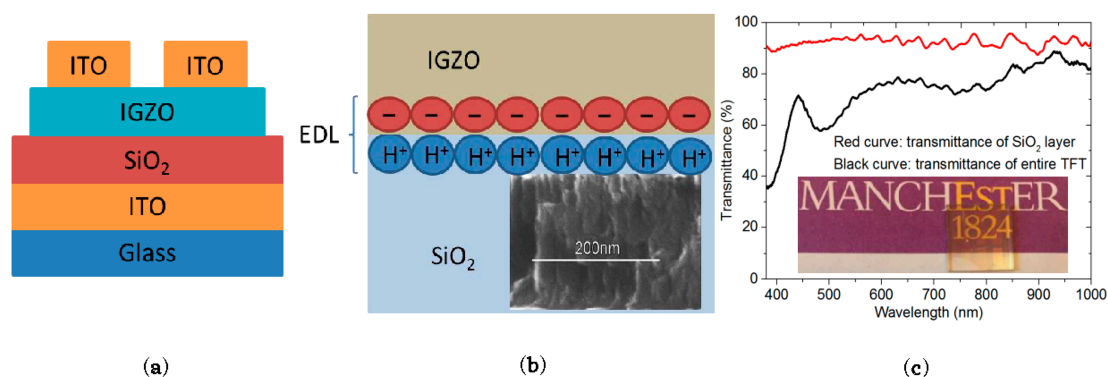

Figure 1. (**a**) Schematic diagram of transparent EDL transistors; (**b**) Schematic cross-sectional view of an EDL TFT when applying a positive gate voltage. Inset: cross-sectional scanning electron microscope view of the gate dielectric layer; (**c**) Optical transmission spectra of the thickest part in the TFT (black curve) and SiO_2 layer (red curve). Inset: a photo of the transparent TFT on glass substrate.

3. Results and Discussion

Figure 1a shows a schematic diagram of the devices. The inset of Figure 1b shows a cross-sectional SEM image of SiO_2 gate dielectric layer, indicating a porous microstructure (full image can be found in Supplementary Figure S1). As such, our previous study indicates that the SiO_2 layer might absorb some water molecules from the ambient air [23]. When a positive bias is applied to the gate electrode, the ionized protons inside the gate electrolyte are accumulated close to the dielectric/channel interface due to the electric field and thus induce electrons inside the IGZO channel layer to accumulate at channel/dielectric interface, which behaves like a normal EDL, as shown in Figure 1b.

Figure 1c shows the optical transmission spectra of the thickest part in the TFT and a 200-nm-thick sputtered SiO_2 layer on glass from 380 to 1000 nm. The maximum transmittance of the TFTs in the visible spectrum (400–800 nm) is about 80%, indicating that the TFTs are transparent to visible light. This can be further demonstrated by the inset of Figure 1c, as the background graph can be seen clearly through the TFT arrays. The drop in the transmittance between 450 nm and 550 nm is caused by the interference of multiple reflections in the transparent films [24–27].

Figure 2a shows the output characteristics of the transparent TFTs with the gate voltage V_G varying from 0 V to 1.5 V in a step of 0.3 V, indicating the devices operate in N-type enhanced mode. It shows a good linear region at low drain voltages, V_D, indicating a low resistance of the source/drain contacts. A good saturation region is also obtained at large V_D and a drain current, I_D, of 19 μA is obtained under a bias condition of V_D = 1.5 V and V_G = 1.5 V. The decrease of I_D in the saturation regime may be attributed to the charge trapping effect at the channel/dielectric interface [28]. Figure 2b shows the corresponding transfer characteristics of the devices measured at a 1.5 V-fixed drain voltage. The gate leakage current, I_G, is found to be about 2.6 nA at V_G = 1.5 V, which is far less than the I_D. The TFT exhibits a good performance with a large current on-off ratio > 10^5, a low subthreshold swing about 130 mV/dec, and a turn-on voltage around 0 V. From $I_D^{1/2}$ as a function of V_G shown in Figure 2b, the threshold voltage is calculated to be about 0.4 V by using the x-axis intercept of the curve.

Figure 2c shows the specific gate capacitance of SiO_2 electrolyte in the frequency range between 20 Hz and 1 MHz using ITO/SiO_2/Al test structure, as shown in the inset of Figure 2c. For conventional SiO_2, which has a dielectric constant of 3.9, a 200-nm-thick SiO_2 insulator layer has a specific capacitance of ~17.3 nF/cm^2, which is independent of frequency. In Figure 2c, it is found that the capacitance of the sputtered SiO_2 electrolyte decreases with increasing frequency. At 20 Hz, the specific capacitance is 300 nF/cm^2 and at 1 MHz, it drops to 70 nF/cm^2. The high capacitance is probably due to the mobile protons in the SiO_2 electrolyte [23,29]. Three coordinate oxygen centres, Si-OH$^+$-Si, are formed in the SiO_2 layer due to the absorption of H_2O molecules [17,30,31]. Since the bonds between oxygen and hydrogen are not stable, the external electric field will draw the proton from the hydroxyl group to the neighbouring ones. When applying a positive bias, the protons will accumulate at the dielectric/channel interface, forming a thin boundary layer, and induce electrons in the channel. Such process is similar to the formation mechanism of EDL in transistors gated by ionic liquids or ion gels [13,32]. As the protons in the SiO_2 electrolyte have a low ionic mobility, at high frequencies, the protons do not have enough time to move to the interface [29]. This results in the frequency-dependent capacitance shown in Figure 2c. In this experiment, the large EDL gate capacitance enables the low operation voltage of the IGZO TFTs.

The mobility (μ_{FE}) in the saturation region can be derived from the following equation:

$$I_{DS} = (\frac{W}{2L}\mu_{FE}C)(V_{GS} - V_{TH})^2 \quad (1)$$

where W is the channel width, L is the channel length, and C is the capacitance per unit area. By using the capacitance value at 100 Hz, the estimated mobility is ~3 cm^2/Vs. As the devices use a 70-nm-thick channel layer without any post-treatment, this mobility value is considered to be reasonable and can be further improved by thermal annealing or reducing the channel thickness [33–35].

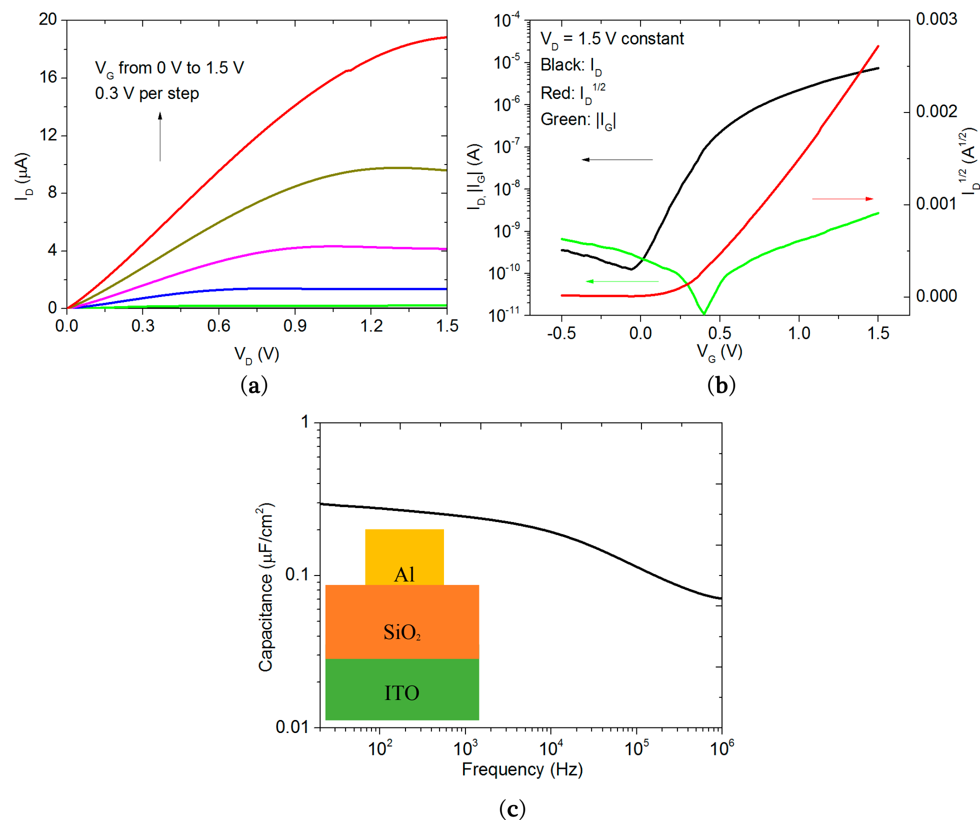

Figure 2. Electrical properties of the TFTs (**a**) Output characteristics with V_D swept from 0 V to 1.5 V and V_G swept from 0 V to 1.5 V with a step of 0.3 V; (**b**) Drain current, gate leakage current and square root of drain current with V_G swept from −0.5 V to 1.5 V at V_D = 1.5 V; (**c**) Capacitance of SiO_2 gate dielectric as a function of frequency (20 Hz to 1 MHz) with inset showing the capacitance test structure. The channel length and width used for the devices are 60 μm and 2 mm, respectively. The SiO_2 thickness used for capacitance measurement is 200 nm.

For the transparent TFTs, it is important to investigate the influence of light irradiation on the electrical performance. In order to make the change more obvious, a 2-V fixed drain voltage has been used for the tests under different light conditions and the obtained transfer characteristics are shown in Figure 3. Off current increases clearly when increasing the light, which changes from 0.02 nA in the dark to 0.28 nA under normal room light (around 300 lx) and further to 1.5 nA under strong light (around 2000 lx) with a white light LED about 3 cm away from the device, resulting in a decrease of current on-off ratio. The threshold voltage also shifts towards negative direction after exposure to light. The light stress stability under around 2000 lx white light has also been tested as shown in Supplementary Figure S2. The subthreshold swing remains almost the same but the threshold voltage decreases around 0.1 V after six hours. There might be two reasons for the shift in V_{TH}. Firstly, light can induce extra free electrons in the IGZO layer [36]. As IGZO is reported to be sensitive to the ambient environment, the other reason might be the adsorption or desorption of illumination induced O_2 molecules in the IGZO layer [37,38]. Some O_2 molecules might be pre-absorbed and react with the conducting electrons in the channel layer to form O_2^-. Under light illumination, the holes generated from the light induced electron-hole pairs might react with these O_2^- causing desorption of O_2 and resulting in the decrease of threshold voltage.

After switching off the strong light, the sample has then been measured in the dark and the transfer characteristics change back to the initial values shown as the red curve in Figure 3. Such behavior indicates that the changes induced by light are reversible.

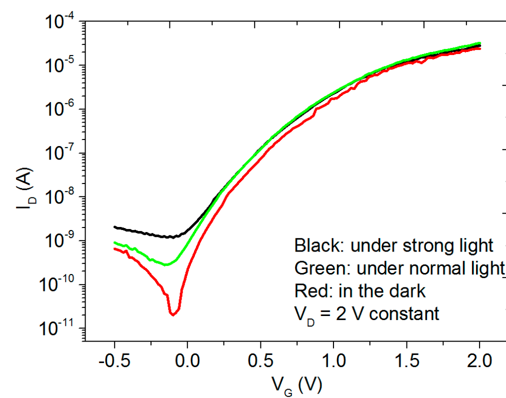

Figure 3. Electrical properties of the transistors under different light conditions when V_G swept from -0.5 V to 2 V at V_D = 2 V. Black curve: under strong light (around 2000 lx giving by a white light LED three centimetres away from the sample). Green curve: under normal room light (around 300 lx). Red curve: in the dark. The channel length and width used for the devices are 60 µm and 2 mm, respectively.

In order to investigate the stability of the transparent EDL TFTs, both positive and negative bias stress tests are carried out by applying constant gate biases at 1 V for positive bias stress test and -1 V for negative bias stress test. Figure 4 shows the transfer characteristics of the devices before and after bias stresses. The subthreshold swing remains almost the same after negative bias and increases to 0.2 V/dec after positive bias. The threshold voltage shows a slight right shift, +0.01 V, after negative bias and a left shift, -0.12 V, after positive bias. These changes are typical for SiO_2-based EDL transistors [39,40]. When the gate is positively biased, the protons inside the gate electrolyte continuously accumulate at the dielectric/channel interface due to the applied electric field and thus induce the electrons inside the channel layer to accumulate at channel/dielectric interface, which results in a decrease of threshold voltage and an increase of on current. When the gate is negatively biased, the protons inside the dielectric are repelled to the dielectric/gate interface. Therefore, the number of electrons accumulating at channel/dielectric interface decreases. This results in a right shift of threshold voltage and a decrease of on current. After removing the bias and leaving the devices in air for 10 minutes, the transfer characteristics of the device return to its initial condition, which means the change induced by bias stress is reversible. By using a capping layer, it is possible that the stability of our devices can be further improved [41].

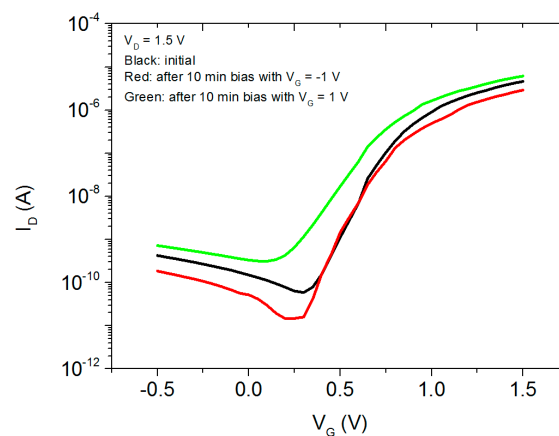

Figure 4. Bias stress testing. Transfer characteristics of the TFT with V_D = 1.5 V at different bias stress voltages. Black curve: initial transfer curve. Red curve: transfer curve after 10 minutes' constant bias at V_G = -1 V. Green curve: transfer curve after 10 minutes' constant bias at V_G = 1 V. The channel length and width used for the devices are 60 µm and 2 mm, respectively.

4. Conclusions

In conclusion, we report, to the best of our knowledge, the first all-sputtered, transparent EDL TFTs fabricated at room temperature. The operation voltage is low due to the large specific EDL capacitance formed by the sputtered-SiO_2 solid gate dielectric. The TFTs exhibit good electrical properties with a current on-off ratio > 10^5 and a subthreshold swing of about 130 mV/dec. A maximum transmittance of about 80% is also observed in the visible light range. Considering the low operation voltage and transparent features of the EDL TFTs, our results demonstrate the potential in transparent electronics and low power circuit applications. Also, as the entire transistors are deposited only by RF magnetron sputtering, the method is compatible with large-area electronics manufacturing.

Supplementary Materials: The following are available online at www.mdpi.com/1996-1944/10/4/429/s1. Figure S1: Cross-sectional SEM image of the sputtered SiO_2 electrolyte. Figure S2: (a) Transfer characteristics; (b) threshold voltage and subthreshold swing of the TFT after white-light stress (around 2000 lx) for several durations.

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Author Contributions: W.C. contributed to the design of experiments, the fabrication of TFTs, the electrical measurements, and the writing of the manuscript. X.M. and J.Z. helped analyzing the experimental results and the writing of the manuscript. A.S. supervised the research and also contributed to the analysis of the experimental results and the writing of the manuscript. All authors participated in the discussion and commented on the paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Fortunato, E.; Correia, N.; Barquinha, P.; Pereira, L.; Gonçalves, G.; Martins, R. High-performance flexible hybrid field-effect transistors based on cellulose fiber paper. *IEEE Electron Device Lett.* **2008**, *29*, 988–990. [CrossRef]
2. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **2004**, *432*, 488–492. [CrossRef] [PubMed]
3. Yabuta, H.; Sano, M.; Abe, K.; Aiba, T.; Den, T.; Kumomi, H.; Nomura, K.; Kamiya, T.; Hosono, H. High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature rf-magnetron sputtering. *Appl. Phys. Lett.* **2006**, *89*, 2123. [CrossRef]
4. Hirao, T.; Furuta, M.; Hiramatsu, T.; Matsuda, T.; Li, C.; Furuta, H.; Hokari, H.; Yoshida, M.; Ishii, H.; Kakegawa, M. Bottom-gate Zinc oxide thin-film transistors (ZnO TFTs) for AM-LCDs. *IEEE Trans. Electron Devices* **2008**, *55*, 3136–3142. [CrossRef]
5. Görrn, P.; Sander, M.; Meyer, J.; Kröger, M.; Becker, E.; Johannes, H.H.; Kowalsky, W.; Riedl, T. Towards see-through displays: Fully transparent thin-film transistors driving transparent organic light-emitting diodes. *Adv. Mater.* **2006**, *18*, 738–741. [CrossRef]
6. Roberts, M.E.; Queraltó, N.; Mannsfeld, S.C.; Reinecke, B.N.; Knoll, W.; Bao, Z. Cross-linked polymer gate dielectric films for low-voltage organic transistors. *Chem. Mater.* **2009**, *21*, 2292–2299. [CrossRef]
7. Yoon, M.-H.; Yan, H.; Facchetti, A.; Marks, T.J. Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross-linked polymers as gate dielectrics. *J. Am. Chem. Soc.* **2005**, *127*, 10388–10395. [CrossRef] [PubMed]
8. Collet, J.; Tharaud, O.; Chapoton, A.; Vuillaume, D. Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films. *Appl. Phys. Lett.* **2000**, *76*, 1941–1943. [CrossRef]
9. Zhang, L.; Li, J.; Zhang, X.; Jiang, X.; Zhang, Z. High performance ZnO-thin-film transistor with Ta_2O_5 dielectrics fabricated at room temperature. *Appl. Phys. Lett.* **2009**, *95*, 2112. [CrossRef]
10. Zhou, C.; Wang, X.; Raju, S.; Lin, Z.; Villaroman, D.; Huang, B.; Chan, H.L.-W.; Chan, M.; Chai, Y. Low voltage and high on/off ratio field-effect transistors based on CVD MoS_2 and ultra high-k gate dielectric PZT. *Nanoscale* **2015**, *7*, 8695–8700. [CrossRef] [PubMed]
11. Brox-Nilsen, C.; Jin, J.; Luo, Y.; Bao, P.; Song, A.M. Sputtered ZnO thin-film transistors with carrier mobility over 50 cm^2/Vs. *IEEE Trans. Electron Devices* **2013**, *60*, 3424–3429. [CrossRef]

12. Tan, S. Challenges and performance limitations of high-k and oxynitride gate dielectrics for 90/65 nm CMOS technology. *Microelectron. J.* **2007**, *38*, 783–786. [CrossRef]
13. Yuan, H.; Shimotani, H.; Tsukazaki, A.; Ohtomo, A.; Kawasaki, M.; Iwasa, Y. High-density carrier accumulation in ZnO field-effect transistors gated by electric double layers of ionic liquids. *Adv. Funct. Mater.* **2009**, *19*, 1046–1053. [CrossRef]
14. Cho, J.H.; Lee, J.; Xia, Y.; Kim, B.; He, Y.; Renn, M.J.; Lodge, T.P.; Frisbie, C.D. Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic. *Nat. Mater.* **2008**, *7*, 900–906. [CrossRef] [PubMed]
15. Dhoot, A.S.; Yuen, J.D.; Heeney, M.; McCulloch, I.; Moses, D.; Heeger, A.J. Beyond the metal-insulator transition in polymer electrolyte gated polymer field-effect transistors. *Proc. Natl. Acad. Sci. USA* **2006**, *103*, 11834–11837. [CrossRef] [PubMed]
16. Pu, J.; Yomogida, Y.; Liu, K.-K.; Li, L.-J.; Iwasa, Y.; Takenobu, T. Highly flexible MoS_2 thin-film transistors with ion gel dielectrics. *Nano Lett.* **2012**, *12*, 4013–4017. [CrossRef] [PubMed]
17. Sun, J.; Wan, Q.; Lu, A.; Jiang, J. Low-voltage electric-double-layer paper transistors gated by microporous SiO_2 processed at room temperature. *Appl. Phys. Lett.* **2009**, *95*, 222108. [CrossRef]
18. Lu, A.; Sun, J.; Jiang, J.; Wan, Q. Low-voltage transparent electric-double-layer ZnO-based thin-film transistors for portable transparent electronics. *Appl. Phys. Lett.* **2010**, *96*, 043114. [CrossRef]
19. Jiang, J.; Sun, J.; Lu, A.; Wan, Q. Self-assembled ultralow-voltage flexible transparent thin-film transistors gated by-based solid electrolyte. *IEEE Trans. Electron Devices* **2011**, *58*, 547–552. [CrossRef]
20. Zhou, J.; Liu, N.; Zhu, L.; Shi, Y.; Wan, Q. Energy-efficient artificial synapses based on flexible IGZO electric-double-layer transistors. *IEEE Electron Device Lett.* **2015**, *36*, 198–200. [CrossRef]
21. Zhang, H.; Guo, L.; Wan, Q. Nanogranular Al_2O_3 proton conducting films for low-voltage oxide-based homojunction thin-film transistors. *J. Mater. Chem. C* **2013**, *1*, 2781–2786. [CrossRef]
22. Jiang, J.; Wan, Q.; Sun, J.; Lu, A. Ultralow-voltage transparent electric-double-layer thin-film transistors processed at room-temperature. *Appl. Phys. Lett.* **2009**, *95*, 152114. [CrossRef]
23. Ma, X.; Zhang, J.; Cai, W.; Wang, H.; Wilson, J.; Wang, Q.; Xin, Q.; Song, A. A sputtered silicon oxide electrolyte for high-performance thin-film transistors. *Sci. Rep.* **2017**, *7*, 809. [CrossRef] [PubMed]
24. Chiu, C.; Yu, P.; Chang, C.; Yang, C.; Hsu, M.; Kuo, H.; Tsai, M. Oblique electron-beam evaporation of distinctive indium-tin-oxide nanorods for enhanced light extraction from InGaN/GaN light emitting diodes. *Opt. Express* **2009**, *17*, 21250–21256. [CrossRef] [PubMed]
25. Caffrey, D.; Norton, E.; Coileáin, C.Ó.; Smith, C.M.; Bulfin, B.; Farrell, L.; Shvets, I.V.; Fleischer, K. Decoupling the refractive index from the electrical properties of transparent conducting oxides via periodic superlattices. *Sci. Rep.* **2016**, *6*. [CrossRef] [PubMed]
26. Benzitouni, S.; Zaabat, M.; Khial, A.; Rechem, D.; Benaboud, A.; Bouras, D.; Mahdjoub, A.; Toubane, M.; Coste, R. High sensitivity of porous Cu-doped SnO_2 thin films to methanol. *Adv. Nanopart.* **2016**, *5*, 140. [CrossRef]
27. Inguva, S.; Vijayaraghavan, R.K.; McGlynn, E.; Mosnier, J.-P. Highly transparent and reproducible nanocrystalline ZnO and AZO thin films grown by room temperature pulsed-laser deposition on flexible Zeonor plastic substrates. *Mater. Res. Express* **2015**, *2*, 096401. [CrossRef]
28. Zhang, B.; Li, H.; Zhang, X.; Luo, Y.; Wang, Q.; Song, A. Performance regeneration of InGaZnO transistors with ultra-thin channels. *Appl. Phys. Lett.* **2015**, *106*, 093506. [CrossRef]
29. Guo, L.-Q.; Yang, Y.-Y.; Zhu, L.-Q.; Wu, G.-D.; Zhou, J.-M.; Zhang, H.-L. Effects of humidity on performance of electric-double-layer oxide-based thin-film transistors gated by nanogranular SiO_2 solid electrolyte. *AIP Adv.* **2013**, *3*, 072110. [CrossRef]
30. Liu, H.; Sun, J.; Tang, Q.; Wan, Q. Ultralow-voltage electric double-layer SnO_2 nanowire transistors gated by microporous SiO_2-based solid electrolyte. *J. Phys. Chem. C* **2010**, *114*, 12316–12319. [CrossRef]
31. Godet, J.; Pasquarello, A. Proton diffusion mechanism in amorphous SiO_2. *Phys. Rev. Lett.* **2006**, *97*, 155901. [CrossRef] [PubMed]
32. Ono, S.; Seki, S.; Hirahara, R.; Tominari, Y.; Takeya, J. High-mobility, low-power, and fast-switching organic field-effect transistors with ionic liquids. *Appl. Phys. Lett.* **2008**, *92*, 103313. [CrossRef]
33. Nomura, K.; Kamiya, T.; Hosono, H. Interface and bulk effects for bias—light-illumination instability in amorphous-In-Ga–Zn–O thin-film transistors. *J. Soc. Inf. Disp.* **2010**, *18*, 789–795. [CrossRef]
34. Kikuchi, Y.; Nomura, K.; Yanagi, H.; Kamiya, T.; Hirano, M.; Hosono, H. Device characteristics improvement of a-In-Ga–Zn–O TFTs by low-temperature annealing. *Thin Solid Films* **2010**, *518*, 3017–3021. [CrossRef]

35. Fuh, C.-S.; Sze, S.M.; Liu, P.-T.; Teng, L.-F.; Chou, Y.-T. Role of environmental and annealing conditions on the passivation-free In-Ga–Zn–O TFT. *Thin Solid Films* **2011**, *520*, 1489–1494. [CrossRef]
36. Görrn, P.; Lehnhardt, M.; Riedl, T.; Kowalsky, W. The influence of visible light on transparent Zinc Tin Oxide thin film transistors. *Appl. Phys. Lett.* **2007**, *91*, 3504. [CrossRef]
37. Kang, D.; Lim, H.; Kim, C.; Song, I.; Park, J.; Park, Y.; Chung, J. Amorphous Gallium Indium Zinc Oxide thin film transistors: Sensitive to oxygen molecules. *Appl. Phys. Lett.* **2007**, *90*, 192101. [CrossRef]
38. Chen, T.-C.; Chang, T.-C.; Hsieh, T.-Y.; Tsai, C.-T.; Chen, S.-C.; Lin, C.-S.; Hung, M.-C.; Tu, C.-H.; Chang, J.-J.; Chen, P.-L. Light-induced instability of an InGaZnO thin film transistor with and without SiO_x passivation layer formed by plasma-enhanced-chemical-vapor-deposition. *Appl. Phys. Lett.* **2010**, *97*, 192103. [CrossRef]
39. Guo, L.; Huang, Y.; Shi, Y.; Cheng, G.; Ding, J. Indium-Zinc-Oxide electric-double-layer thin-film transistors gated by silane coupling agents 3-triethoxysilylpropylamine–graphene oxide solid electrolyte. *J. Phys. D Appl. Phys.* **2015**, *48*, 285103. [CrossRef]
40. Jiang, J.; Wan, Q.; Zhang, Q. Transparent junctionless electric-double-layer transistors gated by a reinforced chitosan-based biopolymer electrolyte. *IEEE Trans. Electron Devices* **2013**, *60*, 1951–1957. [CrossRef]
41. Huang, S.-Y.; Chang, T.-C.; Chen, M.-C.; Chen, S.-C.; Tsai, C.-T.; Hung, M.-C.; Tu, C.-H.; Chen, C.-H.; Chang, J.-J.; Liau, W.-L. Effects of ambient atmosphere on electrical characteristics of Al_2O_3 passivated InGaZnO thin film transistors during positive-bias-temperature-stress operation. *Electrochem. Solid-State Lett.* **2011**, *14*, H177–H179. [CrossRef]

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