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## A High-Frequency-Compatible Miniaturized Bandpass Filter with Air-Bridge Structures Using GaAs-Based Integrated Passive Device Technology

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**Abstract:** This paper reports on the use of gallium arsenide-based integrated passive device technology for the implementation of a miniaturized bandpass filter that incorporates an intertwined circle-shaped spiral inductor and an integrated center-located capacitor. Air-bridge structures were introduced to the outer inductor and inner capacitor for the purpose of space-saving, thereby yielding a filter with an overall chip area of 1178  $\mu$ m × 970  $\mu$ m. Thus, not only is the chip area minimized, but the magnitude of return loss is also improved as a result of selective variation of bridge capacitance. The proposed device possesses a single passband with a central frequency of 1.71 GHz (return loss: 32.1 dB), and a wide fractional bandwidth (FBW) of 66.63% (insertion loss: 0.50 dB). One transmission zero with an amplitude of 43.42 dB was obtained on the right side of the passband at 4.48 GHz. Owing to its miniaturized chip size, wide *FBW*, good out-band suppression, and ability to yield high-quality signals, the fabricated bandpass filter can be implemented in various L-band applications such as mobile services, satellite navigation, telecommunications, and aircraft surveillance.

**Keywords:** air-bridge structure; bandpass filter; capacitor; gallium arsenide; integrated passive device technology; intertwined inductor

#### 1. Introduction

With the rapid development of modern wireless and telecommunication systems, microwave filters have come to play an important role in various radio frequency (RF)/microwave applications because they allow frequency selection. Among the various types of microwave filters, bandpass filters (BPFs) have been extensively studied as a key building block in the design of RF/microwave integrated circuits and systems. However, emerging applications continue to challenge BPF efficacy with increasingly rigorous demands for lower cost, smaller size, higher performance, etc. [1–3].

To satisfy the increasingly stringent requirements of RF and microwave systems, a wide range of materials and techniques that can be used to modify existing lumped passive components have been incorporated into recently developed fabrication processes [4]. Recent advances in novel fabrication techniques, including the implementation of low-temperature co-fired ceramics (LTCC), high-temperature superconductor (HTS), micro-electromechanical system (MEMS), monolithic microwave integrated circuit (MMIC), and micro-fabrication techniques, have accelerated the rapid development of filters for various RF/microwave applications [5]. With LTCC technology, a variety of passive components such as strip lines, filters, antennas, and resonators, which are manufactured by using inexpensive yet highly conductive metals with low electrical resistance and low conductor loss

at high frequencies, can be employed. However, this technology has two major disadvantages: (1) Post-firing ceramic shrinkage limits the size of the board to be processed, and (2) modules that require heat dissipation must be equipped with a heat sink that is applied after heating [6]. High-temperature superconductors are attractive because of their very low surface resistance in comparison to even the most conductive normal metals. Furthermore, their low loss properties allow the microwave passive components to be fabricated with a far more compact geometry than that of conventional materials. Despite its well-known advantages, the high cost and increased system complexity during low-temperature operation prevent HTS technology from being widely applied [7]. Micro-electromechanical system processing enables the batch fabrication of miniature structures that range in size from a few micrometers to a few millimeters; this technique facilitates cost, size, and weight reductions. Furthermore, the ability to seamlessly integrate mechanical components into electronics at the same wafer level is one of the most prominent properties of MEMS technology. However, MEMS components have a considerably short life cycle in addition to undefined power handling capability and an unstable ultimate dynamic range [8]. Alternatively, gallium arsenide and other advanced III-V materials allow MMICs to be applied in the millimeter wavelength region with increased functional capability, improved system reliability, and reduced weight, volume, and cost [9]. The major drawback of this technology is that the circuits can yield performance results for certain parameters that are worse than those observed from the same devices made with separate components [10].

Recently, some groups are researching the implementation of BPFs with emerging technologies such as complementary metal-oxide-semiconductor (CMOS) and stimulated Brillouin scattering (SBS). With regard to low-cost mass production, high integration capability, and lower power consumption, CMOS has proven to be a promising fabrication technique. However, this technology causes serious issues in the realization of high-quality passive components due to losses, especially at high frequencies [11–13]. Stimulated Brillouin scattering-based microwave photonics filtering has attracted significant interest over classical microwave techniques for its low propagation loss, ultra-broad transmission bandwidth, light-weight, and small-footprint. The bandwidth of the SBS-based filter can be adjusted by tailoring the pump profile and therefore provides the device with wide bandwidth tunability (MHz–GHz). Apart from the perfection, the SBS-based device is hard to be monolithically integrated with other on-chip photodetectors and electro-optic modulators [14–16]. In general, lumped elements have a lower Q value (for CMOS, Q factor is less than 15) [17,18]; to some extent, this problem can be mitigated by implementing integrated passive device (IPD) technology (Q factor >30), as is described in our previous reports [19–22]. Integrated passive device technology employs a newly developed fabrication technique that achieves the desired trade-off for package integration systems and affords complete module solutions; thus, overall improved system performance can be achieved through integration with other functionalities. This technique facilitates the design of a simplified and compact passive module with excellent parametric control capability and higher performance as compared to standard discrete systems owing to the reduced parasitic effect.

In this paper, we describe the design and implementation of a miniaturized bandpass filter with air-bridge structures that is fabricated on a gallium arsenide substrate by using IPD technology and is purposed for RF/microwave applications. An equivalent circuit was constructed for the model in consideration of the second-order parasitic effect that is generated under the condition of high frequency. Additionally, the current density was simulated at four selected frequency points by using a three-dimensional (3D) electromagnetic (EM) current simulator. Then, the influence of the inner radius of the BPF was experimentally investigated from the perspective of the S-parameter and lumped parameters.

#### 2. Materials and Methods

#### 2.1. Equivalent Circuit

As illustrated in Figure 1, a quasi-interdigital capacitor was fabricated between the two divisions of a circle-shaped spiral inductor to build up a compact RF resonator. The proposed BPF was constructed with three copper layers, which, from bottom to top, are the Bond layer, Text layer, and Leads layer, having thicknesses of 5  $\mu$ m, 1.8  $\mu$ m, and 5  $\mu$ m, respectively. Figure 2a–c illustrates the configurations of each of these three layers; their geometric parameters are respectively listed in Tables 1–3. A schematic diagram showing the cross-sectional view of the fabricated chip for the IPD is presented in Figure 2d.



**Figure 1.** Three-dimensional layout of the proposed bandpass filter (BPF), showing the three laminated layers (bottom to top: Bond layer, Text layer, Leads layer).

Parameter	а	b	С	d	е	f	r <sub>in</sub>
Unit (µm)	20	15	1178.5	970	60	258.7	300

Table 1. Dimensional parameters of the Bond layer.

Table 2. Dimensional parameters of the Text layer.

Parameter	а	b	С	d	е	f	r <sub>in</sub>
Unit (µm)	16	19	1174.5	966	64	254.7	300

 Table 3. Dimensional parameters of the Leads layer.

Parameter	а	b	С	d	е	f	r <sub>in</sub>
Unit (µm)	20	15	1178.5	970	N/A	258.7	300



Unit: µm



(c)

(**d**)

**Figure 2.** Configuration of the (**a**) Bond layer, (**b**) Text layer, and (**c**) Leads layer, and (**d**) a cross-sectional view of the fabricated integrated passive device (IPD) chip.

The proposed BPF can be simplified as an LC resonant circuit, where an inductor (L) and a capacitor (C) are connected and have a resonant frequency, which is determined by the equation below:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}\tag{1}$$

where *L* and *C* denote the inductance and capacitance, respectively. Moreover, the transmission zero can be derived using:

$$w_0 = \omega_{\rm mid} \frac{\Omega_{\rm c} \times FBW + \sqrt{(\Omega_{\rm c} \times FBW)^2 + 4}}{2}$$
(2)

where  $\omega_{mid}$  is the midband frequency,  $\Omega_c$  is the passband cut-off frequency of the higher frequency area, and *FBW* is the fractional bandwidth, which can be calculated using:

$$FBW = \frac{\omega_2 - \omega_1}{\omega_0} \tag{3}$$

and

$$\omega_0 = \sqrt{\omega_1 \omega_2} \tag{4}$$

where  $\omega_1$  and  $\omega_2$  indicate the passband-edge angular frequency, and  $\omega_0$  denotes the center frequency.

Figure 3 illustrates the complex equivalent circuit model with three laminated layers;  $R_0$  and  $L_0$  represent the resistance and inductance, respectively, of the electrodes and terminations. Because of parasitic effects, the capacitance and resistance of the substrate between the planar pattern and ground

take the form of  $C_G$  and  $R_G$ , respectively [23].  $R_i$ ,  $L_i$ , and  $C_i$  (i = 1, 2, 3) are the resistance, inductance, and coupling capacitance between neighboring turns of the Bond layer, Text layer, and Leads layer, respectively. In addition,  $C_{inter}$  is the capacitance of the inner quasi-interdigital capacitor of the bottom Bond layer. Moreover,  $C_{SiN}$  is the capacitance of the SiN<sub>x</sub> layer between the substrate and the pattern.



Figure 3. Equivalent circuit of the proposed BPF.

The proposed BPF has a multilayer structure, which induces various parasitic effects at high frequencies [24]. The second-order coupling capacitance  $C_{p2}$  represents the parasitic effect between two adjacent layers and was implemented at high frequencies. The coupling capacitance between these layers is related to the number of layers, the overlay area, and the relative dielectric constant of the materials.

The above-listed parameters  $C_G$ ,  $R_G$ ,  $C_{SiN}$ ,  $R_i$ ,  $L_i$ ,  $C_i$ , and  $C_{inter}$  were calculated as follows:

$$C_{\rm G} = \frac{1}{2} l W C_{\rm sub} \tag{5}$$

$$R_{\rm G} = \frac{2}{lWG_{\rm sub}} \tag{6}$$

$$C_{\rm SiN} = \frac{1}{2} l W \frac{\varepsilon_{\rm SiN}}{t_{\rm SiN}} \tag{7}$$

where  $C_{sub}$  and  $G_{sub}$  are the capacitance and conductance per unit area of the gallium arsenide substrate, and  $\varepsilon_{SiN}$  and  $t_{SiN}$  are the dielectric constant and thickness of the SiN<sub>x</sub> layer separating the pattern and substrate, respectively.

Then,

$$R_i = \frac{\rho l}{W\delta(1 - e^{t/\delta})} \tag{8}$$

$$L_i = 0.002l \left( ln \frac{2l}{W+t} + 0.50049 + \frac{W+t}{3l} \right)$$
(9)

$$C_i = \frac{1}{L_i (2\pi f_0)^2}$$
(10)

$$C_{\rm inter} = 0.10 \times \frac{\varepsilon_r l'}{W'} \tag{11}$$

where  $\rho$  is the resistance coefficient, l is the total circle length, W is the conductor width,  $\delta$  is the skin depth, t is the thickness of the metal line,  $f_0$  is the resonance frequency,  $\varepsilon_r$  is the dielectric constant, l' is the finger length, and W' is the finger width [25].

#### 2.2. Current Density

Advanced Design System (ADS) software (Version 2016.01, Keysight Technologies, Inc., Santa Rosa, CA, USA) was employed as a unified interface to simulate momentum in an electromagnetic simulation purpose to evaluate the system design in terms of S-parameter calculation accuracy, surface current, and fields of various planar circuits, including microstrip, stripline, coplanar waveguide, slotline, and other topologies. Interlayer topologies such as air-bridges and vias were incorporated to enable the simulation of multilayer RF/microwave-based printed circuit boards (PCBs), integrated circuits, and multichip modules. Additionally, the simulation was performed in 3D in order to yield a more comprehensive representation of the current flow through slots and conductors through varying degrees of shading, arrows, and contours. The simulated frequency points were selected adaptively for the computation performed through a wide frequency domain that will require a large amount of CPU hardware resources and disk space. Thus, although the frequency range for the electromagnetic (EM) simulation setup was set as 0.1 GHz to 10 GHz, the following 10 frequency points were selected and implemented in the simulation: 0.1 GHz, 1.2 GHz, 1.75 GHz, 3.4 GHz, 5.05 GHz, 6.7 GHz, 7.525 GHz, 8.35 GHz, 9.175 GHz, and 10 GHz. Figure 4a shows the variation of current density under different frequencies with the effects of 1.75 GHz on the simulated current density throughout the proposed BPF illustrated in Figure 4b, which shows that the current flowed through most segments of the simulated BPF with a relatively high density when the frequency was 1.75 GHz, which is within the passband.



**Figure 4.** Simulated current density. (**a**) Frequency–current density illustration, and (**b**) Effects of 1.75 GHz on the simulated current density throughout the proposed BPF.

#### 3. Results and Discussion

The influence of the inner radius of the outer inductor on performance was experimentally explored, as this parameter was varied from 250  $\mu$ m to 350  $\mu$ m in intervals of 25  $\mu$ m. Figure 5 illustrates the variation of S-parameter and other lumped parameters as functions of BPF frequency and inner radius. Figure 5a indicates that the positions of the resonant mode and transmission zero tended to shift to areas of lower frequency in response to a larger inner radius. Because the inductance will increase with a bigger inner radius, thus, according to Equation (1), the bigger the inductance, the smaller the resonant frequency. It should also be noted that the impact on S<sub>21</sub> is more prominent. According to Equations (2)–(4), there are many terms that need to be calculated; we therefore calculated them and tabulated them all in Table 4, which shows that the location of transmission zero definitely moves to

areas of lower frequency with the increase of inner radius. Furthermore, inductance, capacitance, and resistance were derived based on the Y-parameters by using the following equations:

$$L(nH) = \frac{1.0 \times 10^{-9} \times imag\left(\frac{1}{Y(1,1)}\right)}{2\pi f}$$
(12)

$$C(pF) = -\frac{1.0 \times 10^{-12}}{2\pi f \times imag\left(\frac{1}{Y(1,1)}\right)}$$
(13)

$$R(\Omega) = real\left(\frac{1}{Y(1,1)}\right) \tag{14}$$

where Y is the admittance, f is the frequency of operation, and *imag* and *real* represent the imaginary and real parts, respectively. As illustrated in Figure 5b–d, the first self-resonant frequency tended to decrease as the inner radius was increased. Furthermore, it was confirmed that, at high frequencies, the substrate capacitance reduced the self-resonant frequency (Figure 5c).



**Figure 5.** Simulated results illustrating the influence of the inner radius on the respective relationships between S-parameter and lumped parameters and frequency. (**a**) Simulated S-parameters, (**b**) simulated inductance, (**c**) simulated capacitance, and (**d**) simulated resistance.

Terms	$\omega_{ m mid}$ (GHz)	$Ω_{c}$ (GHz)	$\omega_1$ (GHz)	$\omega_2$ (GHz)	$\omega_0$ (GHz)	FBW (%)	$w_0$ (GHz)
250 μm	2.026	2.749	1.303	2.749	1.893	76.401	5.066
275 µm	1.929	2.625	1.234	2.625	1.800	77.233	4.703
300 µm	1.834	2.519	1.148	2.519	1.701	80.581	4.474
325 µm	1.775	2.451	1.099	2.451	1.641	82.397	4.315
350 µm	1.694	2.352	1.037	2.352	1.562	84.232	4.063

Table 4. Values and calculated results of the terms in Equations (2)-(4).

As previously mentioned, the proposed BPF was designed and simulated by using ADS software. In the design of the experimental BPF, the input and output ports were both connected to  $50-\Omega$  impedance-matching transmission lines of the PCB by golden wire bonding; the results were subsequently measured and recorded by using an Agilent 8510C vector network analyzer (VNA) (Agilent Technologies, Santa Clara, CA, USA). The experimental setup for the proposed BPF is illustrated in Figure 6 with enlarged views of various parts. The simulated and measured results for the BPF are depicted in Figure 7 along with photographs of the fabricated onboard chip. The results demonstrate that the proposed IPD BPF possesses a single passband with a central frequency of 1.71 GHz (return loss: 32.1 dB, insertion loss: 0.50 dB), and a wide *FBW* of 66.63%. One transmission zero with an amplitude of 43.42 dB was obtained on the right side of the passband at 4.48 GHz. The results of a comparison between the proposed IPD BPF and four previously developed IPD BPFs, as tabulated in Table 5, show that our device features a relatively small chip area and wide *FBW*.



**Figure 6.** S-parameter measurement setup for the proposed BPF. (**a**) Bandpass filter-vector network analyzer (VNA) cable connection; (**b**) a magnified view of the BPF and its input/output ports; (**c**)  $50 \times$ -magnified top view of the BPF wire bonded to the printed circuit board (PCB); (**d**) a microscopic view of the fabricated onboard chip; (**e**) a microscopic view showing the BPF input-/output-port wire bond to the input/output pad.



Figure 7. Simulated and measured results for the proposed BPF.

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	Reference	Fabrication Process	Circuit Area (mm <sup>2</sup> )	Passband (GHz)	Fractional Bandwidth (%)
	[26]	Si-IPD	3.74	2.20	73.00 (3-dB)
	[27]	Glass-IPD	<1.00	2.60	49.62 (3-dB)
	[28]	Si-IPD	11.6	0.9/2.6	N/A
	[29]	Si-IPD	3.9	1.7	16 (10-dB)
	This work	GaAs-IPD	1.14	1.71	66.63 (3-dB)

Table 5. Comparison of IPD BPF performance.

#### 4. Conclusions

In this paper, we reported on the design of an IPD technology-based BPF that was fabricated onto a gallium arsenide substrate, and was able to realize a small footprint, a wide *FBW*, a good out-band suppression, and high-frequency operational capability. The chip was fabricated onto a 6-in. gallium arsenide substrate with a dielectric constant of 12.85, loss tangent of 0.006, and thickness of 200.1  $\mu$ m. Additionally, an equivalent circuit that considers the second-order parasitic effect was modeled in order to simulate device behavior under high-frequency operation. Furthermore, the current distributions were simulated for four different frequencies by using the 3D EM current simulator in ADS software. The influence of the geometric structure was also explored by varying the inner radius. The theoretical predictions and measurements performed on the fabricated bandpass filter were found to be in agreement, thus indicating that the proposed IPD BPF is a good candidate for RF/Microwave applications.

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