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Modeling of Statistical Variation Effects on DRAM Sense Amplifier Offset Voltage

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Abstract: With the downscaling in device sizes, process-induced parameter variation has emerged as one of the most serious problems. In particular, the parameter fluctuation of the dynamic random access memory (DRAM) sense amplifiers causes an offset voltage, leading to sensing failure. Previous studies indicate that the threshold voltage mismatch between the paired transistors of a sense amplifier is the most critical factor. In this study, virtual wafers were generated, including statistical V_T variation. Then, we numerically investigate the prediction accuracy and reliability of the offset voltage of DRAM wafers using test point measurement for the first time. We expect that this study will be helpful in strengthening the in-line controllability of wafers to secure the DRAM sensing margin.

Keywords: dynamic random access memory; sense amplifier; sensitivity; offset voltage; variation; threshold voltage mismatch

Citation: Koo, K.M.; Chung, W.Y.; Lee, S.Y.; Yoon, G.H.; Choi, W.Y. Modeling of Statistical Variation Effects on DRAM Sense Amplifier Offset Voltage. *Micromachines* **2021**, *12*, 1145. https://doi.org/10.3390/mi12101145

Academic Editor: Jung Ho Yoon

Received: 24 August 2021
Accepted: 20 September 2021
Published: 23 September 2021

1. Introduction

Artificial intelligence (AI) and 5G networks are emerging as major topics in information technology (IT). These applications require high-density and low-power memory. Dynamic random access memory (DRAM) can play an important role, owing to its fast switching speed, low bit cost, and high memory density [1]. Figure 1a shows a schematic of a DRAM cell connected to a sense amplifier (SA). The cell part consists of a cell transistor acting as a switch and a cell capacitor storing charge. The cell plate voltage (V_{CP}) is connected to half-V_{DD} to optimize the leakage current of the cell capacitor. An SA is a complementary metal-oxide-semiconductor (CMOS) latch using the half-V_{DD} precharge-sensing method [2]. The basic operating mechanism of read '1' is as follows: In the standby mode, the bit-line (BL) pair voltage is precharged to half-V_{DD}. When the word-line (WL) voltage is raised to the 'high' level, the charge stored in the cell capacitors is transferred to the BLs. Then, the BL voltage deviates from half-V_{DD}, and a small voltage difference (V_S) between BL and BL/ is generated as follows:

$$V_S = \frac{V_{DD}/2}{1 + C_{BL}/C_C} \quad (1)$$

where C_{BL} and C_C are the BL capacitance and the cell capacitance, respectively. With SA activation, the BL voltage is amplified up to V_{DD} by the positive feedback of the latched inverters of the SA, and data '1' is read. However, accurate data sensing is feasible only when V_S exceeds the SA offset voltage, as shown in Figure 1b. Therefore, if V_S becomes lower than the SA offset voltage, the sensed data read inaccurately.

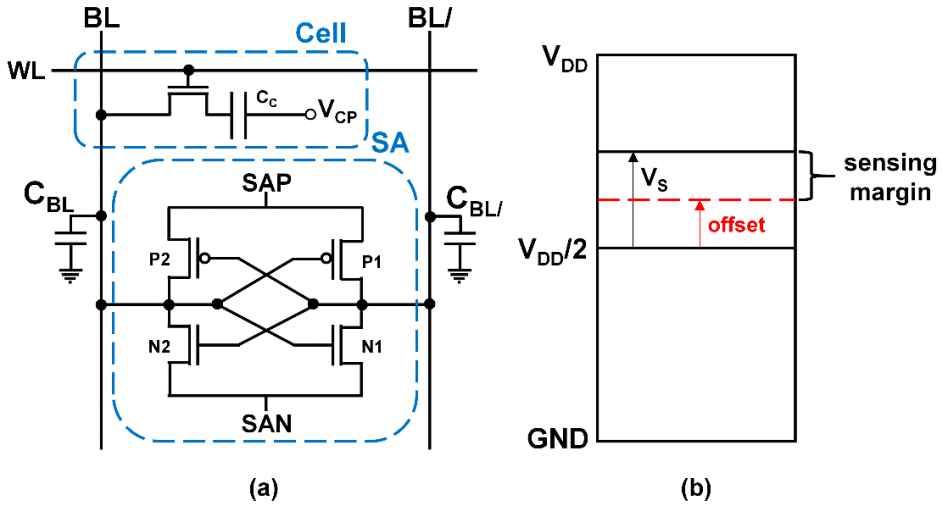

Figure 1. (**a**) Schematic illustration of DRAM, which consists of a cell and an SA. (**b**) Voltage diagram of the sensing margin. V_S must be larger than the relevant offset voltage for correct sensing; otherwise, the opposite data value will be read.

With advances in DRAM generation, both V_{DD} and C_C are being scaled down [3,4], thereby reducing the V_S. This reduction in cell transistor size also increases the threshold voltage (V_T) variation [5], resulting in a larger offset voltage. Thus, the offset voltage characterization becomes more important in SA sensitivity improvement.

R. Kraus et al. derived the offset voltage theoretically by using differential equations, confirming that simultaneous sensing was more advantageous than one-delayed sensing [6]. R. Sarpeshkar et al. derived a rigorous formula considering various parameter mismatches and showed a good agreement compared with HSPICE simulation results [7]. Among the various sources of offset voltage, including parasitic capacitance and β and V_T variation, V_T mismatch (ΔV_T) of the SA transistors has been considered as the most dominant factor [7–9]. At the chip (die) level, offset voltage is calculated by statistically measuring many SAs in a die. S. M. Kim et al. [10] investigated the SA sensing failure percentage in a die according to the V_{DD}, the V_T variation, and the channel width ratio of NMOS and PMOS using a Monte Carlo simulation. Because the V_T in a die follows the Gaussian distribution [11], the offset voltage also is assumed to follow the same distribution. Thus, the V_T standard deviation can be a good indicator of estimating the die offset voltage. S. H. Woo et al. [12] proposed an offset voltage variance estimation model considering the secondary effects such as drain-induced barrier lowering (DIBL), differential charge injection (DCI), and stack effects. Y. Li et al. [13] investigated the DRAM-SA mismatch analytically using small-signal analysis and optimized the result to obtain the minimum offset voltage variance. Then, they derived a linear model considering the sensing delay of SAs and confirmed that simultaneous sensing minimized the die level offset voltage. However, to the best of our knowledge, no study has been attempted to cover the offset voltage at a wafer level.

In this study, virtual wafers are generated based on the global and local variation theory, and the statistical simulation results of the offset voltage distribution at the die and wafer levels are obtained using test point measurement, which is widely used for wafer property identification. Finally, we numerically analyze the offset voltage prediction accuracy and probability of DRAM wafers for the first time. We expect that this study can be used as important information in the DRAM process line and consequently help secure the sensing margin of the DRAM.

The remainder of this study is organized as follows: in Section 2, the V_T variation theory is explained. Then, the assumption of generating virtual wafers and the methodology of extracting data is described in Section 3. Finally, the results are discussed in Section 4.

2. V_T Variation

With the reduction in device sizes, the device parameter fluctuations and short-channel effects need a thorough investigation [14]. It is widely known that the process variations, including random dopant fluctuation (RDF), line edge roughness (LER), and work function variation (WFV), affect nonuniform V_T distribution [5,15–17]. Especially, process variation was classified into two categories: global and local variations [18].

First, the global variation includes lot-to-lot variation (LTLV, Figure 2a), wafer-to-wafer variation (WTWV, Figure 2b), and die-to-die variation (DTDV, Figure 2c). Because global variation is location-dependent, it can be characterized by wafer maps. For a simple and concise discussion, a Gaussian distribution was applied to global variation, as shown in Figure 3a.

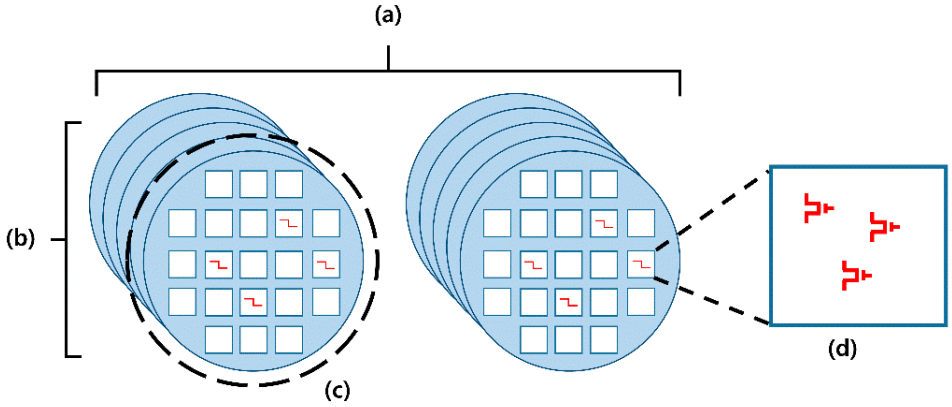

Figure 2. Classification of variations. Global variations include (**a**) lot-to-lot variation (LTLV), (**b**) wafer-to-wafer variation (WTWV), and (**c**) die-to-die variation (DTDV). Local variation means (**d**) within-die variation (WIDV).

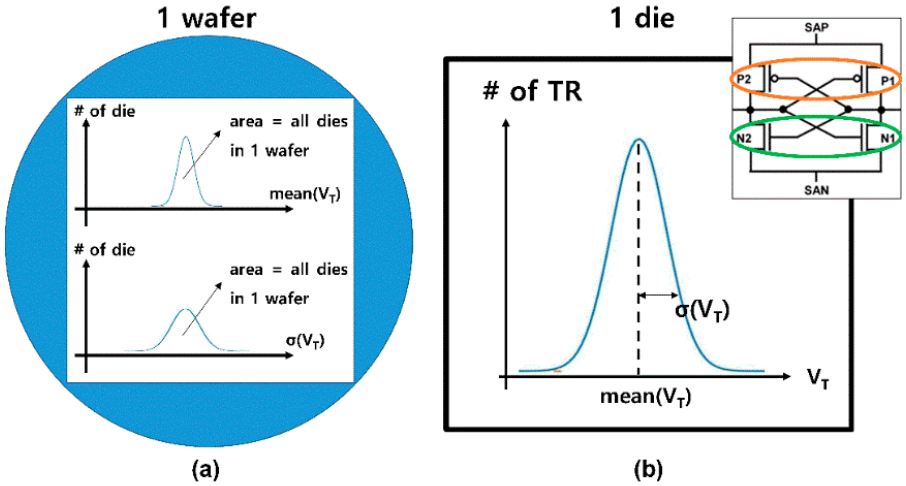

Figure 3. DTDV and WIDV in this work. (**a**) DTDV of mean(V_T)s and σ(V_T)s are assumed to follow the Gaussian distribution. (**b**) WIDV exists in a normal distribution. Transistor pairs ({N1, N2} or {P1, P2}) have same distribution properties.

Second, the local variation includes the within-die variation (WIDV) shown in Figure 2d. Within a die, V_T follows a Gaussian distribution with a certain mean (mean(V_T)) and standard deviation (σ(V_T)) independent of location (random distribution). In this study, V_T of the SA's transistors is assumed to follow a Gaussian distribution and the V_Ts of the transistor pair sharing the same SA follow the same Gaussian distribution, as shown in Figure 3b.

3. Simulation Methodology

First, we modeled the offset voltage distribution of one die by referring to [13], which statistically investigated the offset voltage using small-signal analysis and showed good agreement with simulation results. According to [13], the variance of offset voltage of simultaneously latched CMOS SAs in one die is expressed as follows:

$$\sigma^2(V_{OS}) = \frac{2\sigma^2(\Delta V_{TP})\sigma^2(\Delta V_{TN})}{\sigma^2(\Delta V_{TP}) + m\sigma^2(\Delta V_{TN})} \quad (2)$$

where V_{OS} is the offset voltage of one SA in a die. Moreover, ΔV_{TN} and ΔV_{TP} represent the V_T mismatch of paired NMOS and PMOS in a SA, respectively. The constant m is expressed as follows:

$$m = \frac{V_{DD} - (2 + (1/\alpha))V_{TN} + (1/\alpha)|V_{TP}|}{V_{DD} - |V_{TP}| - V_{TN}} \quad (3)$$

where α is expressed in terms of V_{DD} and V_T:

$$\alpha = \frac{V_{DD} - 2|V_{TP}|}{V_{DD} - 2V_{TN}} \quad (4)$$

In this article, V_{DD} is assumed to be 1.2 V. In addition, the average V_{TN} and V_{TP} are assumed to be 0.423 V and −0.365 V, respectively. Accordingly, α and m are calculated as 1.328 and 0.7534, respectively.

As the offset voltage of a die ($V_{OS,die}$) is statistically defined, we choose the 4σ value of the single SA offset voltage distribution, which is calculated by using Equation (5):

$$V_{OS,die} = 4\sigma(V_{OS}) \quad (5)$$

Then, the offset voltage map according to $\sigma(\Delta V_{TN})$ and $\sigma(\Delta V_{TP})$ is plotted as shown in Figure 4. It is observed that $V_{OS,die}$ increases as $\sigma(\Delta V_{TN})$ or $\sigma(\Delta V_{TP})$ increases.

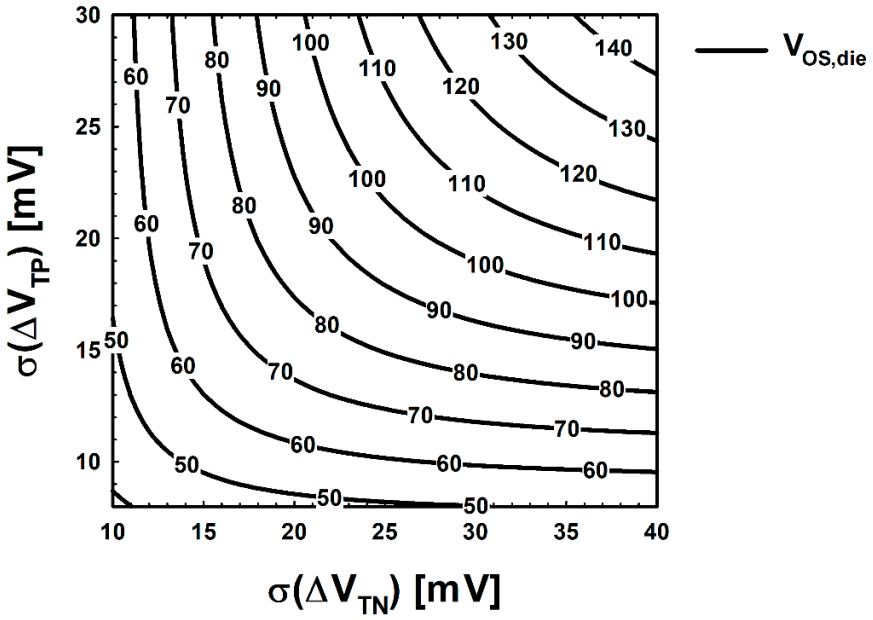

Figure 4. Contours of $V_{OS,die}$ used in this study.

Next, we made a virtual wafer including 1000 DRAM dies. Additionally, for a simple and concise discussion, we assumed that each DRAM die had 10,000 SAs, since a desirable Gaussian distribution can be formed with just that number. As a result, the V_Ts of SAs in a die follow a Gaussian distribution. Because it has been proven by previous studies that the major factor that affects the offset voltage is ΔV_T, we considered only $\sigma(V_T)$ and

$\sigma(\Delta V_T)$ for the concise discussion. Thus, the average values of $\sigma(V_{TN})$ and $\sigma(V_{TP})$ of dies in a virtual wafer are assumed to be 19.7 mV and 12.8 mV, respectively [11], which is shown in Figure 5. Then, to calculate the average offset voltage of dies in a wafer, we can apply a simple statistical equation to derive $\sigma(\Delta V_T)$ from $\sigma(V_T)$. Since we assume WIDV as a random variation, the V_T of each SA transistor pair is independent of each other. Therefore, the relationship between the variance of ΔV_T ($\sigma^2(\Delta V_T)$) and that of V_T ($\sigma^2(V_T)$) is given by the following equation [14]:

$$\sigma^2(V_{T1} - V_{T2}) = \sigma^2(\Delta V_T) = 2\sigma^2(V_T) \quad (6)$$

Accordingly, the $\sigma(\Delta V_T)$ can be expressed as follows:

$$\sigma(\Delta V_T) = \sqrt{2}\sigma(V_T) \quad (7)$$

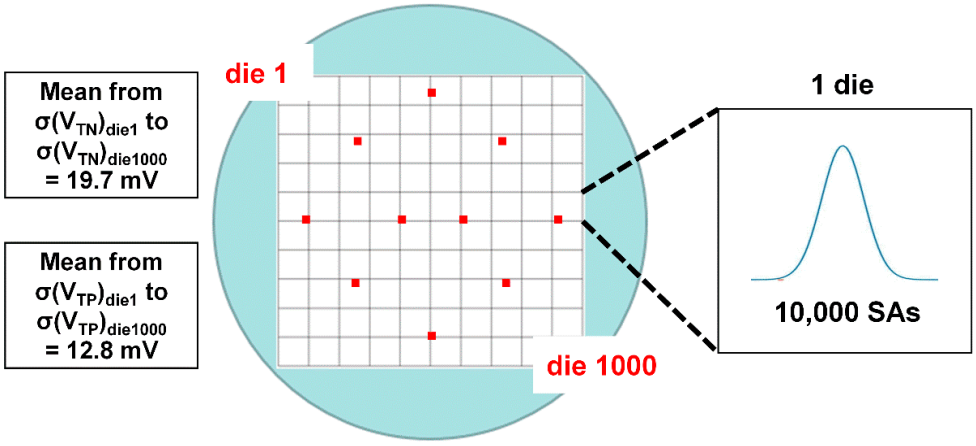

Figure 5. Assumption of virtual wafer in this work. One wafer includes 1000 DRAM dies. It is assumed that the average $\sigma(V_{TN})$ and $\sigma(V_{TP})$ of dies in wafer are 19.7 mV and 12.8 mV, respectively. There are 10,000 SAs in 1 DRAM die, and their characteristics follow the Gaussian distribution. Red dots on a wafer indicate the 10 test points.

As a consequence, when $\sigma(V_{TN})$ is 19.7 mV, $\sigma(\Delta V_{TN})$ is calculated as 27.86 mV, and when $\sigma(V_{TP})$ is 12.8 mV, $\sigma(\Delta V_{TP})$ is calculated as 18.01 mV, respectively. From $\sigma(\Delta V_{TN})$, $\sigma(\Delta V_{TP})$ and Equation (2), the average offset voltage of dies in a wafer is analytically calculated as 94.44 mV.

Here, we explain the offset voltage prediction method. The average offset voltage of dies in a wafer is predicted as follows. First, 10 test points that can represent the whole wafer are selected, as shown in Figure 5. Then, ΔV_{TN} and ΔV_{TP} are extracted from that point. Afterward, $\sigma(\Delta V_{TN})$ and $\sigma(\Delta V_{TP})$ are calculated from these 10 ΔV_{TN} and ΔV_{TP}. Then, these values would be used to predict the offset voltage. The results of prediction and analysis of accuracy will be discussed in the latter part of this paper.

4. Results and Discussion

For intuitive comparison, simulation results are pointed with an analytical point which is shown in Figure 6. The orange point in Figure 6a,b indicates the analytical point (27.86 mV, 18.01 mV), and the offset voltage at this analytical point is 94.44 mV. Black points in Figure 6b indicate the predicted points using the 10-point measurement. Each black point in Figure 6b was extracted from one of the 25 identical wafers. As shown in Figure 6b, the 10-point prediction is not trending and has a wide distribution, which is estimated to be an insufficient number of samples, which were not enough to accurately predict the offset voltage of a wafer. Furthermore, the maximum distance in Figure 6b between the analytical point and predicted a point is calculated as 24.58. However, since the distance from the analytical point does not have a linear correlation with the error (see

Figure 6a), we calculate the error between the offset voltage at the analytical point and at the predicted point to clarify the accuracy of the prediction. Figure 7 shows the predicted offset voltage (Figure 7a) and error (Figure 7b) of the 25 wafers. As shown in Figure 7, the overall predicted offset voltage is distributed far from the analytical value, and the maximum error and the average error are estimated to be 38 mV and 15 mV, respectively. The ratio of the average error, 15 mV, to the analytical offset voltage is a somewhat large value, which is equivalent to 16% and needs to be decreased for more accurate prediction.

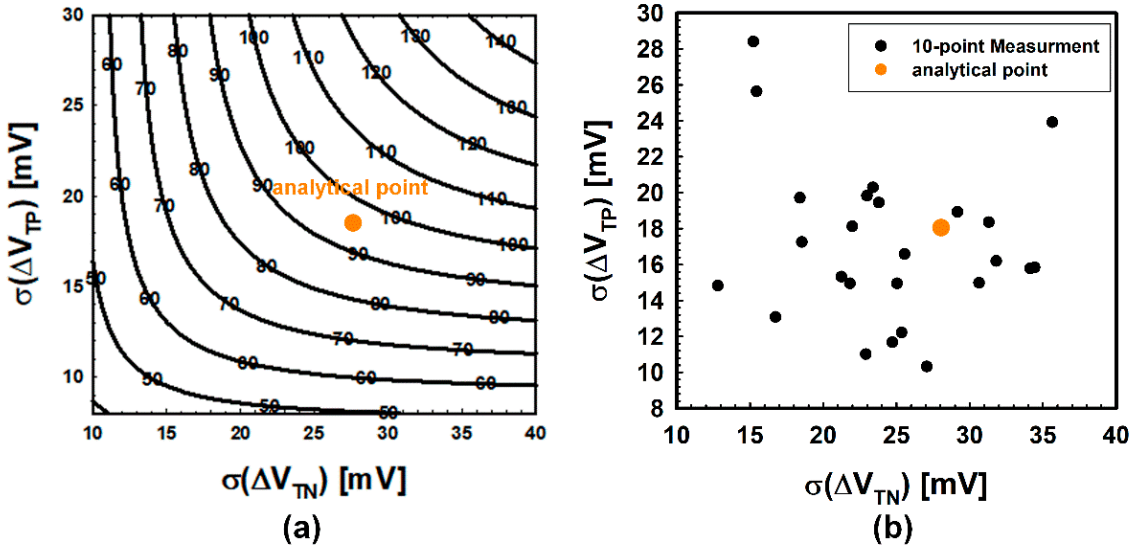

Figure 6. Offset voltage contours and prediction results. (**a**) Offset voltage contours (black line) and analytical point (orange dot). At the analytical point, the offset voltage is 94.44 mV. (**b**) Analytical point (orange dot) and predicted points (black dots) using 10-point measurements. The extracted data are distributed without a trend.

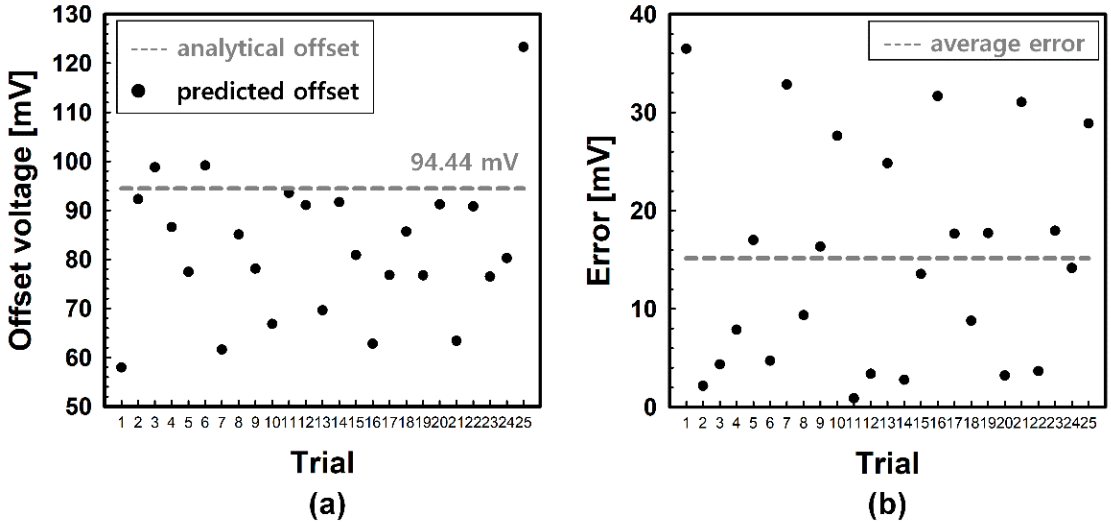

Figure 7. Predicted offset voltages and errors of 25 wafers for further investigation. (**a**) Analytical offset voltage and predicted offset voltages. (**b**) Calculated errors between analytical offset voltage and predicted offset voltages.

Hence, we increased the number of test points to strengthen the prediction accuracy and verify how much the accuracy is improved according to the number of test points. Besides 10-points measurements, 30, 50, 100, and 150 points were selected, and data were extracted in the same way. Figure 8 shows the results with various numbers of test points. As expected, it appears that the predicted points are moving toward the analytical point as the number of test points increases to 100 points. However, there seems to be

little difference between the prediction results of 100-points measurements and 150-points measurements. To further analyze the improvement in prediction accuracy, the error and the corresponding probability plot were also calculated. As the number of test points increases, the distribution of error is diminished, and the average error is reduced, as shown in Figure 9a. Notably, the average error is reduced below 3 mV when the number of test points is 100, and further improvement is minimal when the number grows from 100 points to 150 points. Likewise, the prediction probability is also enhanced as the number of test points increases, which is described in Figure 9b. Of course, the smaller the allowable error, the lower this probability is. However, when the allowable error is 5 mV, it is confirmed that the 100-point measurements show more than 90% reliability. Given these facts, it is estimated that at least 100-point measurements will be needed to reliably predict the overall offset voltage of the wafer by measuring the test points.

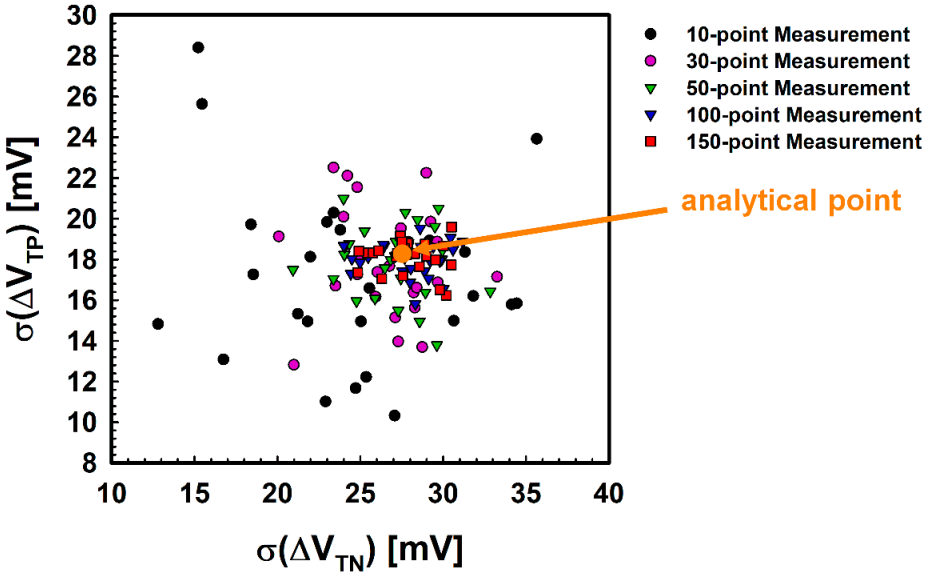

Figure 8. Analytical point and predicted points according to the number of test points. As the number of test points increases, the predicted points concentrate around the analytical point.

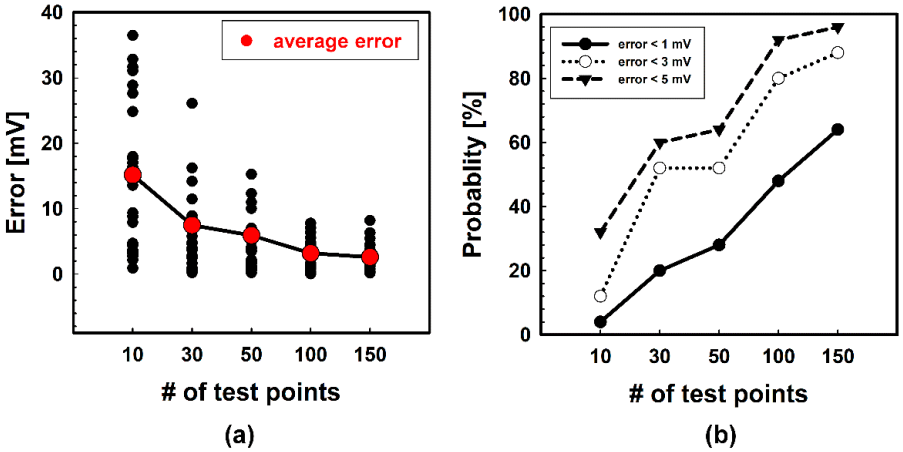

Figure 9. Errors and prediction probability of each number of test points. (**a**) Errors between the analytical point and the predicted points according to the various numbers of test points. (**b**) Prediction probability according to the various numbers of test points and allowable error.

Then, we made other types of virtual wafers to examine how the prediction accuracy changes with regard to variation properties. The aforementioned wafer was named 'w0', and the rest of the wafers (from 'w1' to 'w6') were set by increasing and decreasing the

average value of $\sigma(V_{TN})$ and $\sigma(V_{TP})$ of dies in wafer 'w0' by 20%, respectively. The variation properties and analytical offset voltages of wafers are summarized in Table 1. For an accurate comparison, the number of test points is chosen as 100, and the simulation was performed in the same way.

Table 1. Variation characteristics and analytical offset voltages of each wafer.

Wafer	w0	w1	w2	w3	w4	w5	w6
Average $\sigma(V_{TN})$ of dies (mV)	19.7	23.64	15.76	19.7	19.7	23.64	15.76
Average $\sigma(V_{TP})$ of dies (mV)	12.8	12.8	12.8	15.36	10.24	15.36	10.24
Analytical offset voltage (mV)	94.44	100.1	86.14	105.3	80.96	113.33	75.55

Figure 10 shows the result of the simulation. In Figure 10a, analytical points of each wafer are marked on the offset voltage contours. Since 100 points were measured to investigate the desirable accuracy, a number of relevant predicted points are placed near each analytical point, as shown in Figure 10b. Then, a quantitative analysis of the error is described in Figure 11. Interestingly, it is confirmed that the average error has a positive correlation with the analytical offset voltage (see Figure 11a). In other words, the wafer with the largest variation has a larger prediction error. This is because the greater the population variance is, the more the consistency of the sample variances decreases. For this reason, regarding the prediction probability, the wafer with the largest variation is more likely to make a poor prediction. Specifically, as shown in Figure 11b, when the allowable error is 3 mV, the prediction probability falls to around 50% at wafer 'w5', which has the greatest variation.

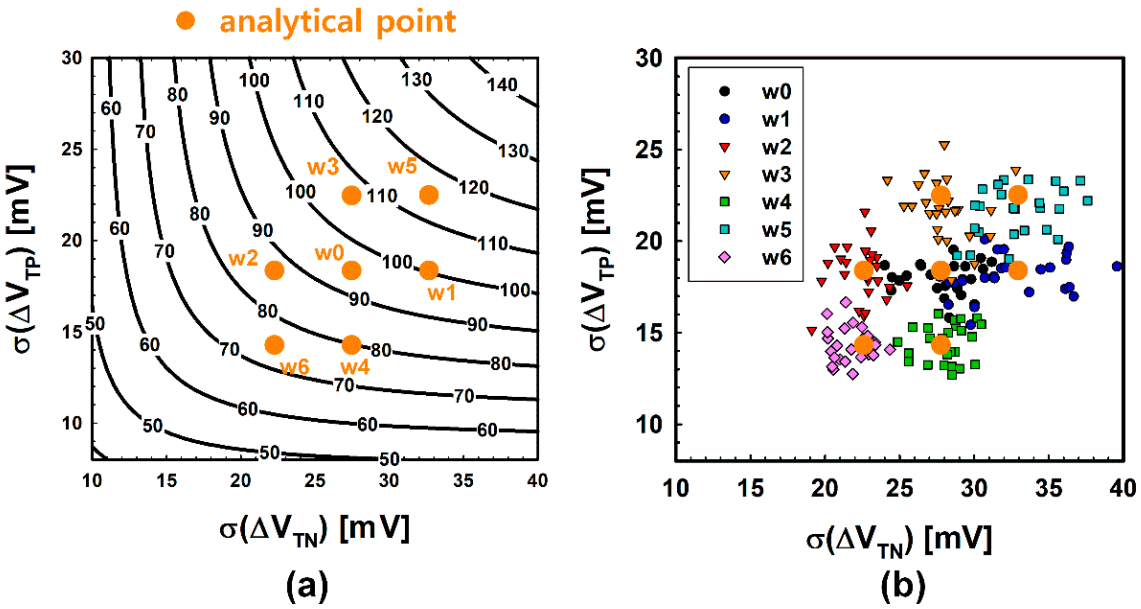

Figure 10. Offset voltage contours and predicted points of each wafer. The orange points represent the analytical offset voltages of each wafer. (**a**) Offset voltage contours. The analytical offset voltage of each point is: 'w0' = 94.44 mV, 'w1' = 100.1 mV, 'w2'= 86.14 mV, 'w3' = 105.3 mV, 'w4' = 80.96 mV, 'w5' = 113.33 mV, 'w6' = 75.55 mV. (**b**) Predicted points of each wafer. A total of 100 test points are selected in 1 wafer for a reliable prediction.

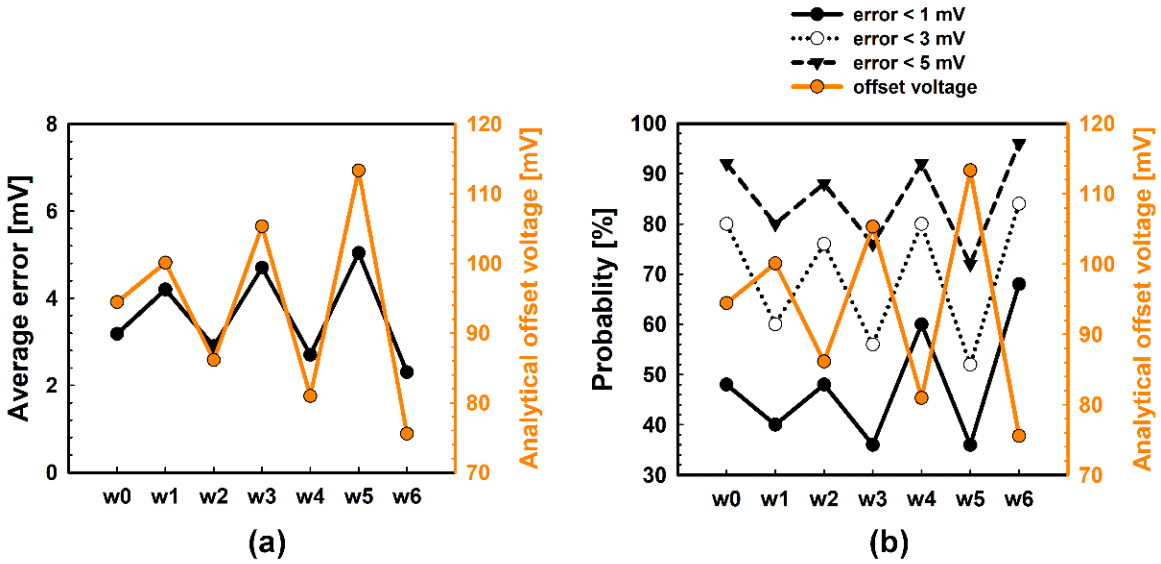

Figure 11. Average errors and prediction probability of each wafer. (**a**) The greater the variation in a wafer, the greater the average error. (**b**) Thus, the wafer with the largest variation has the worst predictive accuracy.

5. Conclusions

Owing to the increase in demand for DRAM and the scaling of device technology nodes, the offset voltage characteristics of the DRAM SA are becoming increasingly important to design a sensitive SA. In this study, we numerically analyzed the prediction accuracy and reliability of the offset voltage of DRAM wafers using test point measurement for the first time. We created a virtual wafer and then compared the analytical offset voltage of the wafer with the predicted value obtained through ΔV_T measurement at the test points. With regard to the number of test points, 100-point measurements show more than 90% reliability when the allowable error is 5 mV. Additionally, it is confirmed that the predictive reliability of wafers with small variations is higher. We expect that this study can be used as important information in the DRAM process line, and it will be helpful in strengthening the in-line controllability of wafers to secure the DRAM sensing margin.

Author Contributions: Writing—original draft and data curation, K.M.K.; Formal analysis, K.M.K.; Data fitting and project management, W.Y.C. (Woo Young Chung), S.Y.L.; Writing—review and editing, G.H.Y., W.Y.C. (Woo Young Choi); Validation, W.Y.C. (Woo Young Choi); Supervision, W.Y.C. (Woo Young Choi). All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by SK Hynix, in part by the NRF of Korea funded by the MSIT under Grant NRF-2019M3F3A1A02072089, NRF-2021M3F3A2A01037927 (Intelligent Semiconductor Technology Development Program), NRF-2021R1A2C1007931 (Mid-Career Researcher Program), in part by the IITP funded by the MSIT under Grant IITP-2020-2018-0-01421 (Information Technology Research Center Program), in part by the MOTIE/KSRC under Grant 10080575 (Technology Innovation Program), and in part by the Sogang University Research Grant 202119026.01.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: It was approved by all individuals.

Conflicts of Interest: The authors declare no conflict of interest.

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