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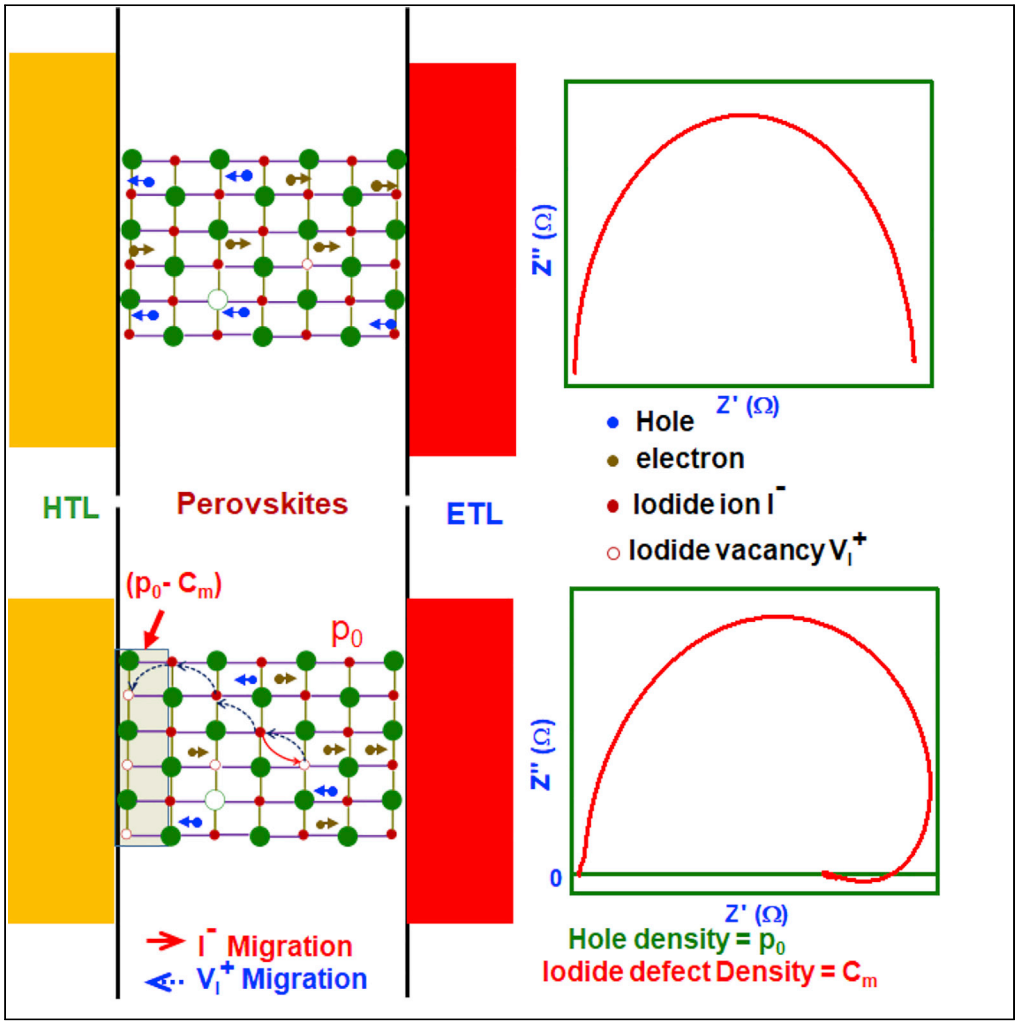

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HIGHLIGHTS

Negative capacitance in *p-i-n* device was unraveled from immittance spectroscopy

Under external bias, halide ions/vacancies migrate toward HTL/perovskites interface

Charge carriers discharge in trap states leading to the negative capacitance

In *p-i-n* devices PTAA-based HTL display improved charge transport compared with PEDOT:PSS

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Mechanistic origin and unlocking of negative capacitance in perovskites solar cells

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SUMMARY

We have unlocked the mechanistic behavior of negative capacitance in perovskite solar cells (PSCs) by analyzing impedance spectra at variable photovoltage and applied bias, temperature-dependent capacitance versus frequency (*C-f*) spectra, and current-voltage (*J-V*) characteristics. We noted that *p-i-n* type PSCs having PEDOT:PSS or PTAA as hole transport layer display negative capacitance feature at low and intermediate frequencies. The activation energies (E_a) for the observance of negative capacitance were found to be in a similar order of magnitude required for the ionic migration. Moreover, the kinetic relaxation time (τ_{kin}) estimated to be in the same order of magnitude required to activate the halide ion migration. Our investigation suggests that the primary reason for the appearance of negative capacitance in PSCs with *a p-i-n* configuration is associated with the migration of halide ions and vacancies in the perovskite layers.

INTRODUCTION

Despite the exceptional power conversion efficiency shown by perovskites solar cells (PSCs), they suffer from several eccentric behaviors such as dynamic *J-V* hysteresis (Snaith et al., 2014), giant low-frequency capacitance (Zarazua et al., 2016a, 2016b), inductive loop or negative capacitance, (Ebadi et al., 2014), and the origins of these phenomena are still not fully understood. The negative capacitance is an ambiguous feature observed in the PSCs, which harms device performance in terms of reduced open-circuit voltage (V_{oc}) and fill factor, thus yielding a reduced power conversion efficiency (Fabregat-Santiago et al., 2017). The observance of the inductive loop or negative capacitance at low and medium frequencies was explained via both bulk and interfacial effects, including ion migration and accumulation at the interface of perovskites/charge extraction layers (Guillen et al., 2014; Dualeh et al., 2014; Miyano et al., 2015), trapping/detrapping of charge carriers at interfacial trap states, frequency-induced changes in resistance (Klotz, 2019), and electrochemical reaction (Zohar et al., 2016). Additionally, the negative capacitance was also explicated through interfacial phenomenon where the charge injection from perovskite to charge-selective layer is mediated through interfacial states (Guerrero et al., 2016; Bisquert et al., 2016). Under open-circuit conditions or due to photovoltage, the interfacial states become depopulated leading to negative capacitance.

The capacitance refers to the charge held by an arrangement for an applied voltage; accordingly, negative capacitance corresponds to the drop in stored charges, on the applied voltage increases. Recently, Ebadi et al. reported that negative capacitance is not related to the classical capacitive effect and rather corresponds to slow transients in the injection current (Ebadi et al., 2014). Alvarez et al. found that the negative capacitance and inverted *J-V* hysteresis in PSC's features stemmed from the same origin, i.e., large kinetic relaxation times because of an increased recombination value (Alvarez et al., 2020). The correlation for the ionic-to-electronic current amplification for the observance of low-frequency photoinduced capacitance was established (Choi et al., 2020), while the origin of the negative capacitance through the formation of an inversion layer at interface leading to bending of energy band under illumination or open-circuit condition is also reported (Feng et al., 2018). The surface polarization model, which describes the anomalous *J-V* hysteresis was also employed to expound the negative capacitance in PSCs. In this model, the negative capacitance was assigned to the assumption of large charge accumulation at the interface of the perovskites/electron transport layer (ETL), which delays surface voltage, and subsequent detection of negative capacitance (Alvarez et al., 2020, and Ghahremanirad et al., 2017).

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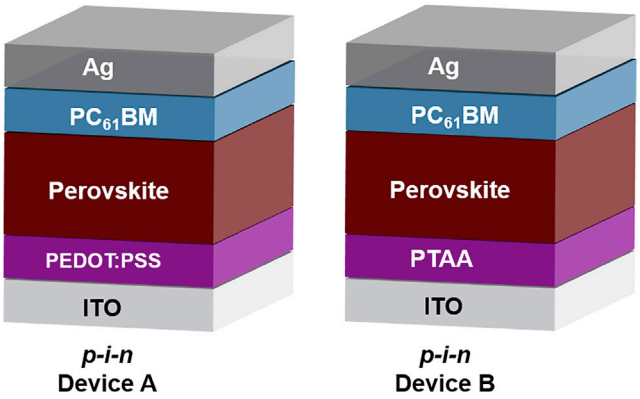

Figure 1. Schematic diagram
p-i-n devices with PEDOT:PSS and PTAA as hole transport materials (device A and B).

Inductive loop or negative capacitance is not limited to a specific device configuration and reported for both types of devices (*n-i-p or p-i-n*) (Ebadi et al., 2014; Guerrero et al., 2016), with or without charge-selective contacts (Choi et al., 2020; Feng et al., 2018 and Ghahremanirad et al., 2017); moreover, it was also noted in $MAPbBr_3$ single crystal (Kovalenko et al., 2017). Thus, inductive loop and negative capacitance in PSCs are unrelated to the grain-boundary defects or interfacial phenomenon; rather they are intrinsic properties of perovskite material itself. Arguably, negative capacitance observed in PSCs is becoming one of the firmest features to interpret. So far, most of the studies on negative capacitance in PSCs are rather speculative and lack a systematic approach to elucidate its origin. Although these studies provide significant information about negative capacitance, the adequate hypothesis for its origin has not yet been explained.

In this report, we have decipher the origin of negative capacitance by investigating the bias and illumination dependence impedance spectra, temperature-dependent capacitance versus frequency (*C-f*) spectra, and current-voltage (*J-V*) characteristics. For this study, we have employed two different p-type materials including poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) and poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine (PTAA) in inverted configuration, viz., ITO/PEDOT:PSS/PVSK/PC_{61}BM/BCP/Ag (device A) and ITO/PTAA/PVSK/PC_{61}BM/BCP/Ag (device B) (Figure 1). The perovskite composition was kept similar. It was found that negative capacitance appears under the applied bias condition or above a critical temperature in both devices. Our investigation suggests that the origin of negative capacitance is related to the migration of halide vacancies due to their low activation energies.

RESULTS

Observance of the inductive loop in impedance spectra

The impedance spectra (IS) of fabricated devices were measured at short circuit conditions and in the presence of applied bias under dark and variable illumination intensity (Figure 2). The diameter of the Nyquist plot decreases when the light illumination intensity increases. Impedance spectra under dark at short circuit conditions display a single arc, whereas under illumination, an additional arc appears. With the increase in illumination intensity the diameter of the left semicircle (high frequency) decreases, whereas the diameter increases for the right arc (low frequency). The high-frequency semicircle described the charge transfer and recombination through perovskite/charge-selective contacts, whereas the low-frequency arc was attributed to charge carrier (*e-h*) recombination, dielectric relaxation, and ionic migration in the perovskite layer. In the presence of applied bias, the low-frequency arc in both devices collapsed below the real impedance axis, drawing an inductive loop.

To analyze the IS, different equivalent circuits (EC) were used. We noted that at short circuit condition and in the presence of external field, the IS fits using EC shown in Figures S1A and S1B, respectively, and the fitting parameters are represented in Tables S1 and S2 for device A and device B, respectively. Here, R_S is the series resistance attributed to contacts and was in the range of 7–12 Ω, indicating intimate device contacts. The first capacitance, C_{bulk}, represents the geometrical or bulk capacitance of perovskite layer,

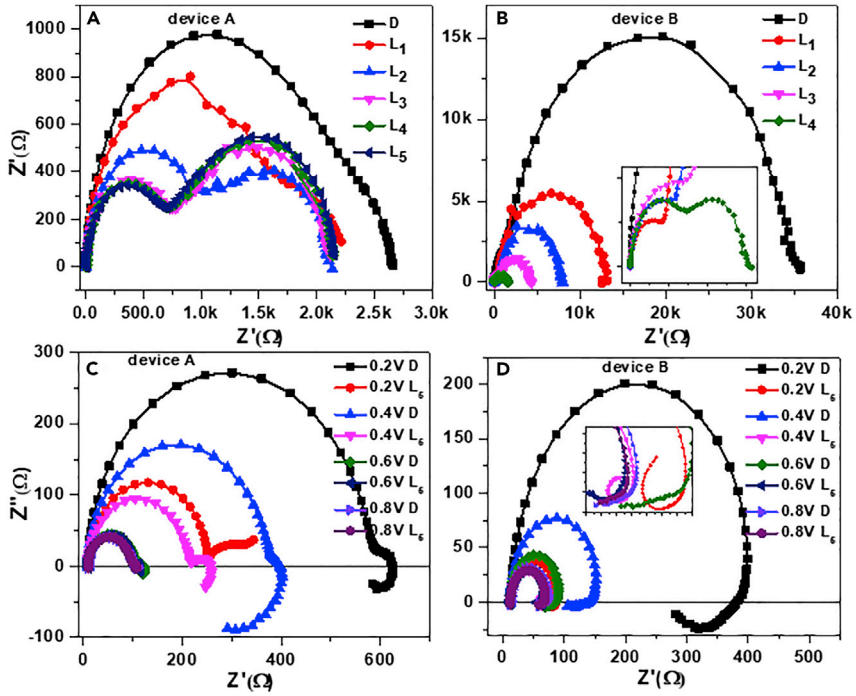

Figure 2. Impedance plot

(A–D) Impedance spectra at short circuit condition (A and B) and at different applied bias (C and D) for type A and type B devices. Here "D" stands for dark and L_1, L_2, L_3, L_4, and L_5 represent the illumination intensities of 0.1, 0.2, 0.3, 0.4, and 0.5 sun, respectively.

which with R_1 accounts for the arc at high frequencies (Zohar et al., 2016; Khan et al., 2019a, 2019b). This bulk capacitance (C_{bulk}) was extracted to be of the order of 10^{-8} F, and a small increment under illumination was noted, possibly due to photogeneration of charge carriers. The value of resistance R_1 decreases with illumination or under applied bias due to an increase in the charge carrier density. The second capacitance, C_{acc}, labels the ionic migration and accumulation at the perovskite/ETL interface under short circuit condition and in the presence of external fields, respectively. The C_{acc} with R_2 (related to recombination resistance) accounts for the low-frequency arc (Choi et al., 2020; Anaya et al., 2017; Khan et al., 2020, 2019). Ionic capacitance values in type A and type B devices under short circuit condition and dark were extracted to be 8.76×10^{-7} and 3.92×10^{-8} F, respectively; this value increased by an order of magnitude under light illumination. Under external bias, the accumulation of capacitance further increases by an order of magnitude with respective values of 1.67×10^{-5} F and 1.99×10^{-4} F. This implies that under external bias or illumination, the ionic accumulation at the interface is higher compared with the short circuit and dark condition. The interfacial charge transfer resistance R_2 defines arc radius of the inductive loop. It decreases in the presence of external fields and under illumination. According to the surface polarization model, the inductance becomes prominent for larger values of the kinetic relaxation constant $\tau_{kin} = L/R_L$ (L is the inductance and R_L is the resistance parallel to L); the loop becomes bigger and crosses the axis entering negative values (Ghahremanirad et al., 2017). The kinetic relaxation time for the device A and device B was calculated to be 0.57 s and 2.67×10^{-2} s, respectively, which is of the same order of magnitude required for the diffusion of halide vacancies (Wang et al., 2019). Arguably, the diffusion of halide vacancy is one of the primary causes for the appearance of low-frequency inductive loop in inverted PSCs.

Observation of negative capacitance

Mostly, inductance is related to the magnetic field, which is not the case here (neither magnetic field was applied nor any magnetic material was employed). Typically, inductive loop and negative capacitance are noted in the same device; therefore, inductance is considered the effect of reciprocal of negative capacitance. To investigate the origin of the inductive loop in impedance spectra, we made temperature dependence capacitance versus frequency (*C-f*) measurements (Figure 3). The *C-f* spectra show three distinct

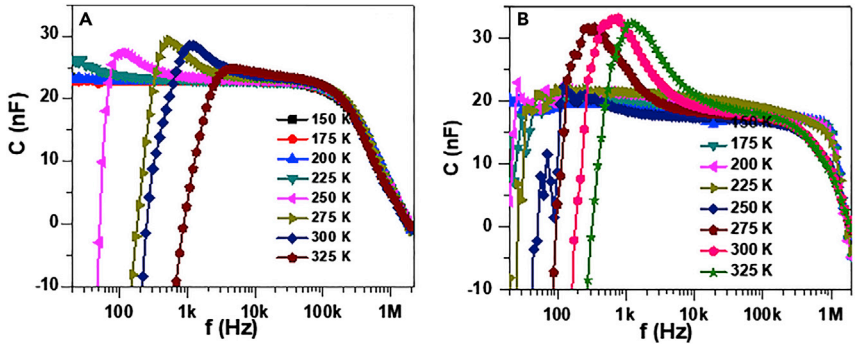

Figure 3. Capacitance versus frequency curves

Capacitance versus frequency spectra as a function of temperature of (A)device A and (B) device B.

regions in agreement with the previous report (Khenkin et al., 2019). The high-frequency capacitance corresponds to the series resistance of contact electrodes; the capacitance in the intermediate frequency range is related to the dielectric relaxation in the perovskite layer and is determined by the geometrical capacitance per unit area. The low-frequency capacitance in type A and B devices first increases exponentially and subsequently drops rapidly to below zero with a negative value of capacitance. Moreover, with an increase in temperature the onset of drop frequency increases in both devices (A and B) and shifts to intermediates frequency. The rise of low-frequency capacitance corresponds to charge accumulation at perovskites/HTL interface and the drop in capacitance to negative value at lower frequency corresponds to the discharge of interfacial accumulated charge to the defect states due to ionic migration. With an increase in temperature, ions start to migrate faster and leave behind the trap states. The shift (increase) in drop frequency with temperature is attributed to faster (decrease) recombination $\left(\tau = {}^{1}/_{f}\right)$ of charge carriers in defect states created by ionic migration.

DISCUSSION

Evidence of halide vacancy migration

The kinetic relaxation time derived for device A and device B are in the similar order required for the diffusion of halide vacancies. To further unravel the evidence for the ionic migration in the perovskite layers, the activation energy (E_a) was calculated from the Arrhenius plot of peak frequencies (f_{peak}) (extracted from $-f\,dC/df$ versus f plot and versus 1,000/T) (Figure 4). The activation energies for A and B devices were calculated to be 0.39 and 0.18 eV, respectively. The activation energies are in the range of the activation barrier for migrating I^- ions (0.08–0.58 eV) and lower than the activation energies required for migrating MA^+ ions (0.46–0.84 eV) and Pb^{2+} ions (0.80–2.31 eV) (Azpiroz et al., 2015; Eames et al., 2015; Haruyama et al., 2015). Owing to the low activation energy, most mobile ions in perovskites are suggested to be the I^- ions, which can migrate easily across the perovskite layer under external bias or with the temperature rise in PSCs, and change the local stoichiometry of the entire layer, which in turn can influence the charge transport and its characteristic resistance. The activation energy depends on several factors, e.g., migration path (grain or bulk), grain boundaries, crystallinity, and defects. The different activation energy in two configurations might be due to the variation in perovskites structure and interfacial properties of perovskites with PTAA and PEDOT:PSS. The hydrophobic surface of PTAA is favorable for the growth of compact, pinhole-free with larger grain perovskite layers (Shao and Loi, 2020). Alternatively, hydrophilic surface of PEDOT:PSS produces smaller grains and deep traps compared with PTAA. The large-sized grains in perovskite layers over PTAA provide a network for ionic migration compared with perovskites grown atop of PEDOT:PSS. We speculate that this phenomenon is responsible for the lower ionic activation barrier in PTAA as compared with PEDOT:PSS.

The migration rate of halide ions was evaluated through the equation $k = \left(k_B T/\hbar\right) e^{-E_a/RT}$, where K_B is the Boltzmann constant, T is the temperature, $\hbar = h/2\pi$ is the Planck constant, R is the ideal gas constant, and E_a is the activation energy. The halide migration rate was in the order of $\sim 10^{13}\ s^{-1}$ at room temperature. The low activation energy led to the migration of iodide ions toward ETL with a migration rate of $10^{13}\ s^{-1}$ at

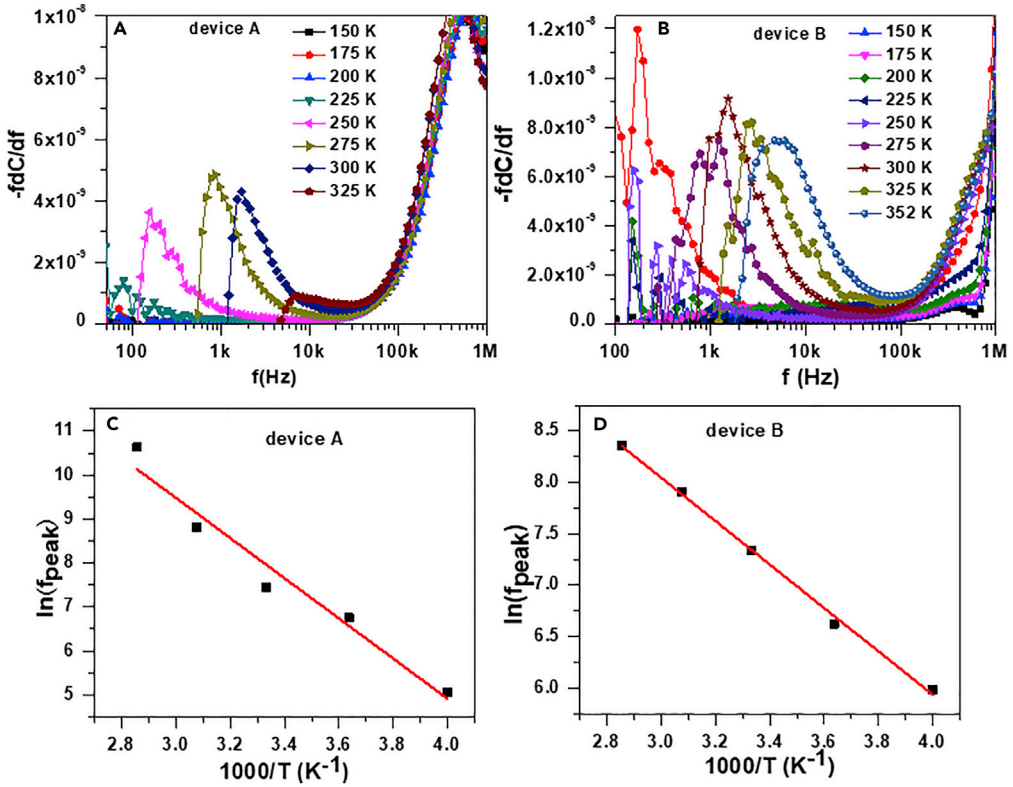

Figure 4. Derivative of capacitance versus frequency plots

(A–D) (-f × dC/df) versus frequency at different temperatures for (A) device A and (B) B device. Arrhenius plot of peak frequency (f_{peak}) versus 1000/T for (C) A and (D) B devices.

room temperature. The I^- ions migration leaves behind iodide vacancy (V_I^+) and lattice distortion due to unbalanced charge. Under the influence of external bias, these defects and iodide vacancy (V_I^+) migrate toward the hole transport layer (HTL) and accumulate at HTL/perovskites interface (Figure 5A) with a concentration of C_m. The accumulated vacancies create shallow traps at HTL/perovskite interface, electrons from the conduction band can discharge in these defects, and charge carrier density at the interface decreases to (p_0-Cm), where p_0 is the charge carrier density in the bulk of films. Thus, with an increase in external bias, the net interfacial charge decreases, resulting in the observation of negative capacitance: $C = dQ/dV$. Our findings suggest that migration of halide ions and accumulation of halide vacancies at perovskite/HTL interface are the key reason for the appearance of negative capacitance in PSCs.

Furthermore, the negative capacitance in device B starts appearing at a lower temperature as compared with device A (Figure 3); this is because the activation energy in device B is about half that of device A. Thus, the migration of halide vacancies in device B was easy when compared with that in device A; consequently, negative capacitance in device B appears at lower temperature than of device A.

At short circuit condition, these defects follow a random migration path and distribute uniformly over the perovskite layer. At an applied bias, halide vacancies migrate toward the interface of HTL/perovskites and accumulate, thus affecting the interfacial space charge region due to the Fermi level equilibration (Khenkin et al., 2019). Moreover, these defects are also thermally activated; with an increase in temperature they accumulate at the interface, affecting the interfacial space charge region. To elucidate the effect of the accumulation of iodide vacancies on interfacial space charge, we measured the temperature-dependent dark *J-V* characteristics for A and B devices (Figures 6A and 6B).

The *J-V* characteristics can be divided into two regions (i) lower field and (ii) higher field. At low applied bias, *J-V* characteristics follow Ohm's law, and electrical conductivity at room temperature was evaluated

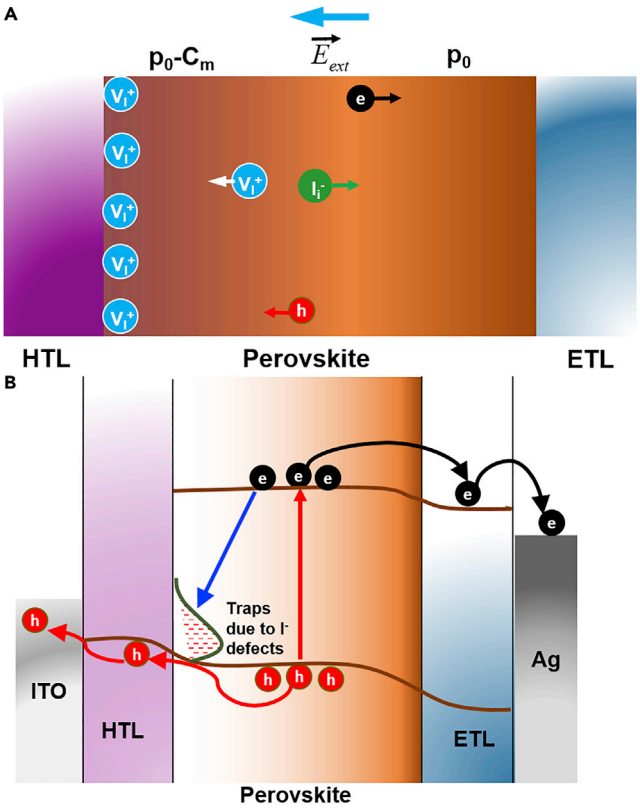

Figure 5. Schematic showing ion migration and accumulation

(A) Schematic illustration of the migration of iodide ions and vacancies migration in a perovskites layer under the external bias. The applied voltage causes diffusion of halide defects toward HTL, and compensate the iodide interstitial (I_i^-) and accumulate at HTL/perovskites interface and (B) the accumulated halide vacancies create shallow traps, where electrons recombine and reduce the interfacial charge density.

to be 7.68×10^{-9} and 4.27×10^{-8} S/cm for A and B devices, respectively. The higher conductivity in device B has an origin due to surface properties of PTAA, which favors compact, pin-hole-free devices and large grains of perovskites compared with PEDOT:PSS (Shao and Loi, 2020). This is in accordance with the device performance (Figure S2) owing to improved carrier transport (Khadka et al., 2017). The high-field region was fitted with space charge-limited current equation for distributing exponential traps (Blom et al., 1996; Khan et al., 2018; Kao and Hwang, 1981):

$$J = q^{1-l}\mu_{eff}N_{eff}\left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{l}{l+1}\frac{\varepsilon}{H_{eff}}\right)^{l}\frac{V^{l+1}}{d^{2l+1}}$$

where q is the total charge, N_{eff} is the effective density of states, ε is the permittivity of perovskite layer, d is the thickness of perovskite layer, and H_{eff} is the sum of the shallow density of traps at the edge of the valence band and conduction band. μ_{eff} is the effective carrier mobility given by (Kao and Hwang, 1981):

$$\mu_{eff} = \frac{\mu_e\mu_p}{\varepsilon\langle v\sigma\rangle}\frac{\left[B\left(\alpha/\beta v_{an}, \alpha/\beta v_{ap}\right)\right]^3}{\left[B\left(3\alpha/2\beta v_{an}, 3\alpha/2\beta v_{ap}\right)\right]^2}$$

where μ_p and μ_e hole and electron mobilities, respectively; B(m, n) is the β function; σ is the capture cross-section; v is thermal velocity; and the product v_σ is charge carrier capture rate constant or recombination rate constant. The fitting parameters used for A (B) device are: $H_{eff} = 1.3 \times 10^{16}$ cm^{-3} (2.90×10^{16} cm^{-3}), $N_{eff} = 6.0 \times 10^{17}$ cm^{-3} (6.0×10^{17} cm^{-3}), $\mu_{eff} = 4 \times 10^{-4}$ $cm^2V^{-1}s^{-1}$ (5.5×10^{-4} $cm^2V^{-1}s^{-1}$). The effective carrier mobility in device B was noted to be slightly higher than of device A, a feature that is aligned with larger grain size in device B. The free carrier concentration in perovskite layers was estimated to be 1.25×10^{14} cm^{-3} and 5.59×10^{14} cm^{-3} for A and B devices, respectively.

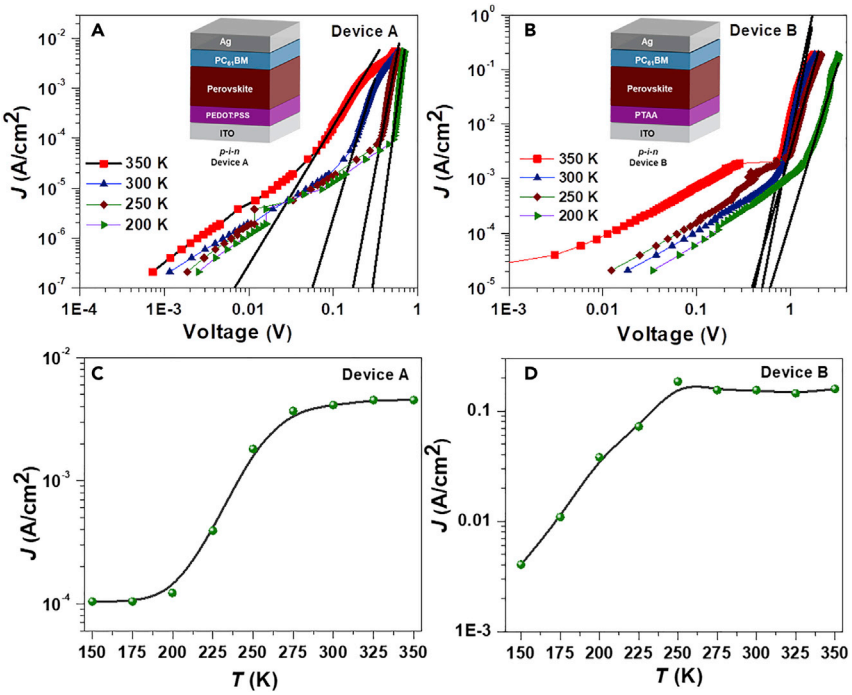

Figure 6. Current density profile

(A–D) Experimental (symbols) and calculated (solid lines) *J-V* characteristics of (A) type A and (B) type B devices. Variation of current density as a function of temperature for (C) type A (at 0.5 V) and (D) type B (at 0.7 V) devices.

Figures 6C and 6D illustrate the variation in the current density at the constant voltage at variable temperatures. We noted (Figures 6C and 6D) that the rate of current density increase below the critical temperature is low and is almost constant above the critical temperature. This implies that when the temperature reaches a critical temperature, the halide defect starts migrating toward HTL/perovskites interface, and the accumulation of these halide vacancies at interface rises, subsequently increasing accumulation of capacitance (Figures 3A and 3B). Moreover, Minns et al. reported a similar temperature (280 K) for migrating iodide defects in $MAPbI_3$ via interstitial sites, which is comparable to this work (>250 K) (Minns et al., 2017). Furthermore, we performed Mott-Schottky analysis to derive information about the HTL/perovskites interface (Figure S3). We noted that depletion capacitance is not visible in both devices, suggesting that at room temperature the contribution of capacitance due to accumulation of halide vacancies dominates depletion capacitance in type devices A and B (Futscher et al., 2018). We speculate that when the devices acquire critical temperature, iodide vacancies activate and migrate toward HTL, creating additional trap states (Figure 5). Trap density (n_{trap}) increase above critical temperature can be established from the plot of the variation of trap density versus temperature (Figure S4). It can be deduced from the figures that the rate of trap density concerning temperature starts increasing above the critical temperature, suggesting the increase in trap density beyond critical temperature. In case where the temperature of devices cross the critical temperature, the migration of iodide vacancies is activated, increasing trap density at HTL/perovskites interface (Figure 5B). The charge carriers discharged in these defect states resulted in no further increase in current (Figures 6C and 6D). Due to the recombination of charge carriers in iodide recombination centers, the interfacial charge carrier density decreases, which leads to the appearance of negative capacitance.

An alternative explanation for the appearance of negative capacitance can be assigned to the decrease in the interfacial barrier. When the concentration of iodide vacancies (positive charge) at the interface reaches the threshold, the interfacial electric field increases, reducing the barrier height, which results in more charge carrier transfer from perovskites to HTL either via tunneling or injection as a result of the increase in device current in this temperature range (Figures 6C and 6D). Subsequently, interfacial charge carrier density decreases because of negative capacitance (Chen et al., 2016). The origin of negative capacitance remains the same, i.e., the migration of halide vacancies in perovskite layer and accumulation at HTL/perovskites interface.

Conclusion

To summarize, we have unraveled that under applied bias accumulation of capacitance increases, suggesting accumulation of iodide vacancies at HTL/perovskite interface. We assign the origin of negative capacitance in perovskites solar cells to the migration of halide vacancies. The inductive loop observed on the applied external bias is required to migrate the iodine vacancies. We noted a similar kinetic relaxation time for the diffusion of iodine vacancies and the activation energies, while the activation temperature is also in the same order required for migrating iodine vacancies. Above the activation temperature, trap density increases and the value of current becomes constant, signaling the creation of additional traps due to iodine vacancies and recombination of charge carriers in these trap states. Our findings suggest that under the activation conditions, the halide defects migrate toward hole transport layers and accumulate at the interface of perovskite; charge carriers recombine in these trap states decreasing carrier density, which in turn allows the appearance of negative capacitance.

Limitations of the study

We noted the appearance of negative capacitance in lead halide perovskites solar cells and it was ascribed to the migration of halide ions/vacancies. The different activation energies in the two types of devices suggest that the role of hole-selective layers/perovskites interface in the observation of negative capacitance requires further investigations.

Resource availability

Lead contact

Further requests for resources and materials should be directed to and will be fulfilled by the Lead Contact, Shahzada Ahmad (shahzada.ahmad@bcmaterials.net).

Materials availability

This study did not yield any new unique reagents.

Data and code availability

This study did not produce datasets/code.

METHODS

All methods can be found in the accompanying Transparent methods supplemental file.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.isci.2020.102024.

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AUTHOR CONTRIBUTIONS

M.T.K performed the experiments, analyzed the data, and prepared the initial draft, P.H. fabricated the devices, A.A provided assistance to M.T.K., S.K. performed the analysis of the data, and S.A. supervised and directed the research. All authors contributed to the draft and prepared the final version.

DECLARATION OF INTERESTS

The authors declare no conflict of interest.

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Supplemental Information

Mechanistic origin and unlocking of negative capacitance in perovskites solar cells

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Supplemental information

Transparent Methods

Solar cell fabrication

For fabricating *p-i-n* (A and B) devices, the pre-cleaned ITO substrates were treated by UV ozone for 30 min. The PEDOT:PSS layer was prepared by spin-coating from PEDOT:PSS (Clevios PVP Al 4083) solution at 5000 rpm for 30 s in air, and ITO/PEDOT:PSS films were post-heated at 150 °C for 15 min and transferred into glovebox for further use. The PTAA as HTM layer was spin-coated from precursor solution (5 mg/mL PTAA in toluene) onto the ITO substrate at 5000 rpm for 30 s, and the substrates were annealed at 100 °C for 5 min in the glovebox. The perovskite layers were deposited through the two-step method (Huang et al., 2017). Firstly, 1.3 M PbI_2 was dissolved in 1 mL of DMF at 70 °C overnight. The solution was spin-coated on the ITO/HTM at 4500 rpm for 20 s, then 50 µL of the mixed solution of MAI: MACl (50: 5 mg in 1 mL IPA) was spin-coated on the PbI_2 substrate at 4500 rpm for 30 s. The as-prepared samples were annealed at 100 ^{o}C for 15 min. A thin layer of $PC_{61}BM$ (10 mg/mL in chloroform) was spin-coated on perovskite at 1500 rpm for 30 s. BCP was used as a buffer layer atop of $PC_{61}BM$ and was spun-coated from the corresponding solution (0.5 mg/mL) at 5000 rpm for 30 s. Ag electrode (100 nm) was thermally evaporated under a pressure of 4×10^{-6} Pa.

Device characterization

The current-voltage characteristics of the PSC were performed under AM 1.5G (100 mW cm^{-2}) illumination that was provided by 3A grade solar simulator (Newport). The impedance measurements were carried out in the frequency range of 2 MHz - 1 Hz under the perturbation of 20 mV ac signal using Biologic SP300 Potentiostat. A white LED was used to illuminate the device and illumination intensity was controlled by a controller and the range of light intensity for different photovoltage was c.a. 0.1 − 0.5 sun illumination. To minimize the noise and external interferences, a faradaic chamber was used for sample measurements. The measured data were analyzed through Z-view software (version 3.1c) by using equivalent circuits and characteristic parameters of devices were extracted. The *C-f* measurements at different temperatures were performed on a Keysight precision LCR meter (model E4980A) in the frequency range 2 MHz – 20 Hz. The temperature dependence dark *J-V* characteristics were measured using Keithley 2400 current source and voltmeter (Keithley 2110 5 ½ Digit). Linkam heating/cooling stage (Model LTS420E-PL8) was filled with liquid nitrogen and the temperature was controlled with the help of software. Firstly, the samples were cooled down to 150 K, and thereafter measurements were carried in heating mode in the temperature range 150 K − 350 K.

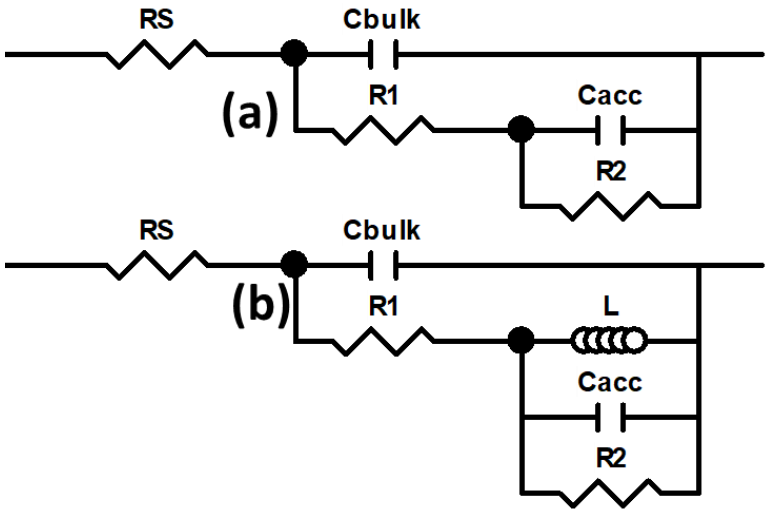

Figure S1. Equivalent circuits used to fit the impedance spectra of devices A and B. Related to Figure 2.

From the EC shown in Figure S1b, we found that the impedance of the combination of C_{acc}, L and R_2 is:

$$\frac{1}{Z_2} = \frac{1}{R_2} + i\left(C_{acc}\omega - \frac{1}{L\omega}\right)$$

The combination of Z_2 with R_1 is

$$Z_{21} = R_1 + Z_2$$

The total impedance of the EC is:

$$Z = R_S + \frac{R_2}{1 - R_2^{\,2}\left[\left(C_{bulk} + C_{acc}\right)\omega - \frac{1}{\omega L}\right]^2} - i\frac{R_2^{\,2}\left[\left(C_{bulk} + C_{acc}\right)\omega - \frac{1}{\omega L}\right]}{1 - R_2^{\,2}\left[\left(C_{bulk} + C_{acc}\right)\omega - \frac{1}{\omega L}\right]^2} = Z^{'} + iZ^{''}$$

with

$$Z^{'} = R_S + \frac{R_2}{1 - R_2^{\,2}\left[\left(C_{bulk} + C_{acc}\right)\omega - \frac{1}{\omega L}\right]^2}, \text{ and } Z^{''} = -\frac{R_2^{\,2}\left[\left(C_{bulk} + C_{acc}\right)\omega - \frac{1}{\omega L}\right]}{1 - R_2^{\,2}\left[\left(C_{bulk} + C_{acc}\right)\omega - \frac{1}{\omega L}\right]^2}$$

Impedance Z" transform from positive value to negative for the frequency

$$\omega_{NC} = \frac{1}{\sqrt{L(C_{bulk} + C_{acc})}}$$

Which was found to be of the same order of frequency obtained from the experimental data, confirm the validity of the equivalent circuit used for fitting of IS.

Table S1. The parameters used in fitting of IS of device A by using equivalent circuit. Releated to Figure 2.

Parameters	Device A SC Dark	Device A SC Light	Device A OC Dark	Device A OC Light
R_S (Ω)	7.246	7.349	9.386	9.381
C_{bulk} (F)	2.71×10^{-8}	2.79×10^{-8}	3.66×10^{-8}	3.72×10^{-8}
R_1 (Ω)	1928	684.3	83.81	83.73
C_{acc}/C_{ion} (F)	8.76×10^{-7}	1.59×10^{-6}	1.67×10^{-5}	1.15×10^{-5}
R_2 (Ω)	713.6	1512	13.48	11.96
L (H)	--------	---------	7.723	7.475

Table S2. The parameters used in the fitting of IS of device B by using equivalent circuit. Related to Figure 2.

Parameters	Device A SC Dark	Device A SC Light	Device A OC Dark	Device A OC Light
R_S (Ω)	6.95	7.617	7.83	8.49
C_{bulk} (F)	2.02×10^{-8}	2.51×10^{-8}	3.68×10^{-8}	4.15×10^{-8}
R_1 (Ω)	4285	513.9	47.2	42.61
C_{acc}/C_{ion} (F)	3.92×10^{-8}	3.87×10^{-7}	1.99×10^{-6}	1.58×10^{-6}
R_2 (Ω)	30312	12219	8.18	8.08
L (H)	------	------	0.2181	0.1945

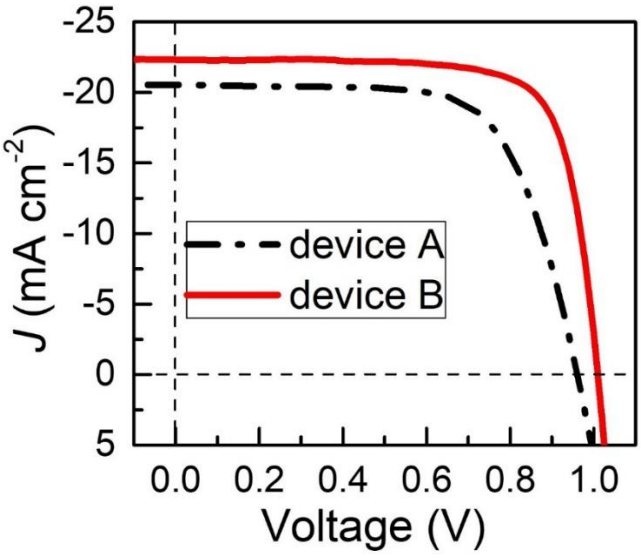

Figure S2. Representative *J-V* curves for type A and B devices under the illumination of 100 mW/cm^2. Related to Figure 2 − 4.

We performed Mott-Schottky analyses to derive information about the interface but it was found that the depletion capacitance is not visible for device A and device B. This indicates that at room temperatures the contribution of ionic capacitance due to accumulation of halide defects at HTL/perovskites in device A and device B dominates the depletion capacitance.

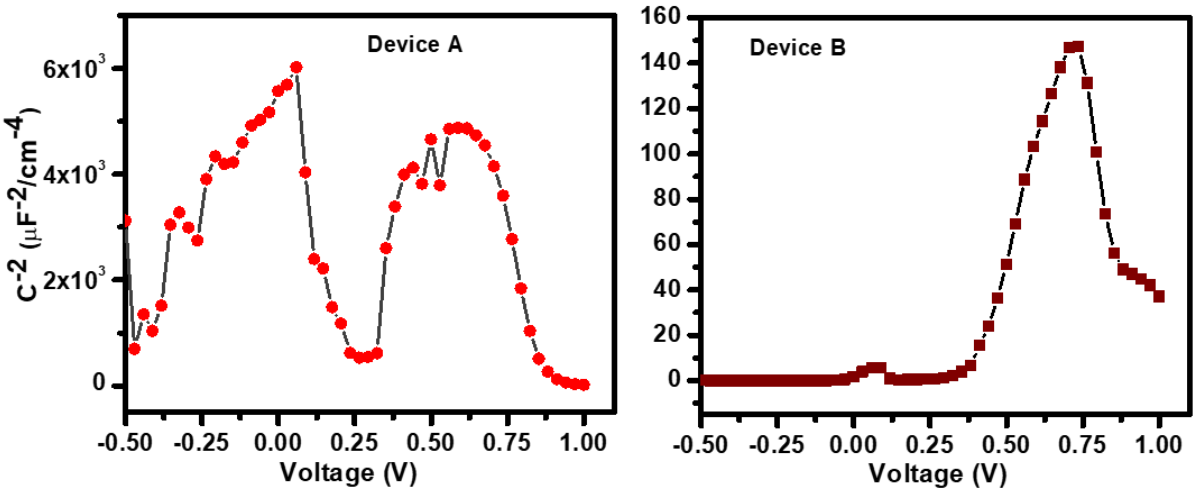

Figure S3. Mott-Schottky plot of type A and B devices. Related to Figure 5.

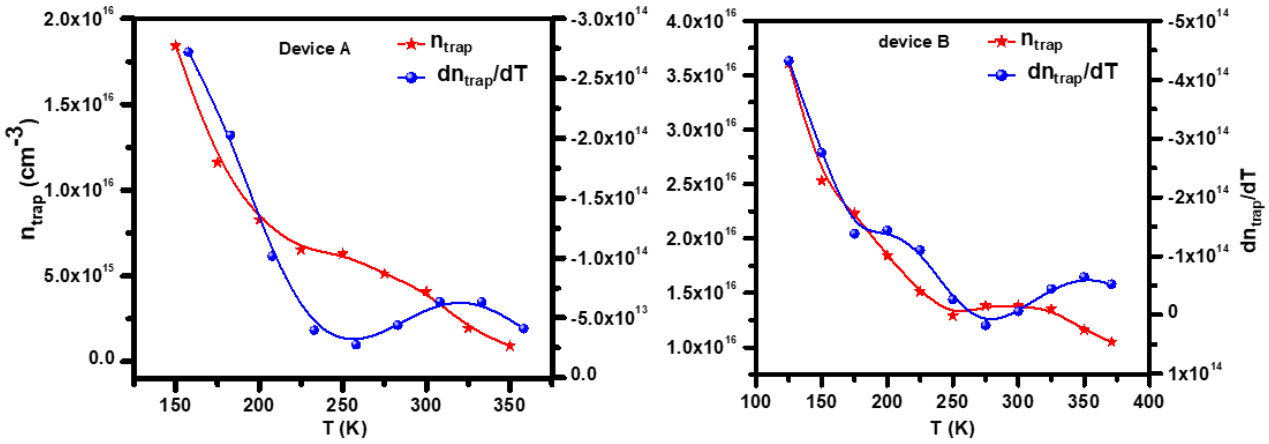

Figure S4. Variation of trap density (red) and its first derivative (blue) as a function of device temperature. Related to Figure 5 and 6.

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