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Layered Graphene Growth Directly on Sapphire Substrates for Applications

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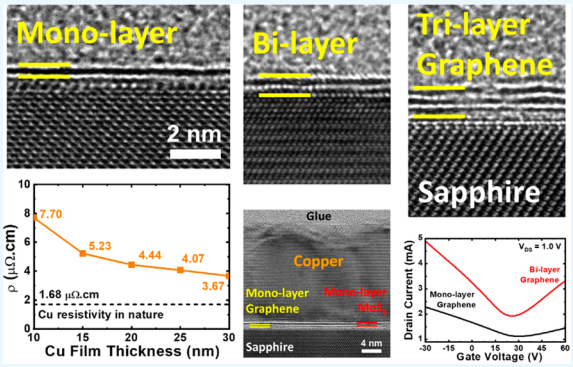
ABSTRACT: Layer-by-layer graphene growth is demonstrated by repeating CVD growth cycles directly on sapphire substrates. Improved field-effect mobility values are observed for the bottom-gate transistors fabricated by using the bilayer graphene channel, which indicates an improved crystallinity is obtained after the second CVD growth cycle. Despite the poor wettability of copper on graphene surfaces, graphene may act as a thin and effective diffusion barrier for copper atoms. The low resistivity values of thin copper films deposited on thin monolayer MoS_2/monolayer graphene heterostructures have demonstrated its potential to replace current thick liner/barrier stacks in back-end interconnects. The unique van der Waals epitaxy growth mode will be helpful for both homo- and heteroepitaxy on 2D material surfaces.



INTRODUCTION

In most 2D material research, there is more interest in monolayer instead of multilayer 2D materials.[1−6] One major reason lies on the direct to indirect bandgap transition of 2D materials such as transition-metal dichalcogenides (TMDs) with increasing layer numbers. In that case, weakened photoluminescence will be observed for multilayer 2D materials, which may hinder their possible application and publication values as light-emitting materials. However, considering the already-in-market light-emitting diodes (LEDs), there is not much room for practical applications of 2D materials in LEDs with emission wavelengths of 600−800 nm. From the first paper published at 2004 on exfoliated graphene, electronic devices have been the major potential applications for 2D materials.[1] The research evolution from graphene, TMDs, black phosphorus (bP), and 2D material heterostructures is all about better performances in electronic devices.[7] In this case, multilayer instead of monolayer 2D materials may provide higher drain currents for 2D material transistors, which is an important issue for practical applications. On the other hand, the van der Waals epitaxy on 2D material surfaces may help to improve the crystallinity of upper 2D material layers such that higher field-effect mobility values can be obtained from the 2D material transistors. In this case, the demonstration of repeating 2D material growth to form homojunctions with good layer number controllability will become an important issue for practical applications.

Graphene, as the first discovered 2D material, exhibited ultrahigh mobility values in the first paper prepared by using mechanical exfoliation.[1] It has been demonstrated in numerous publications that large-area graphene films can be grown by using chemical vapor deposition (CVD).[8,9] In previous publications, it has been demonstrated that graphene films can be grown directly on insulating substrates such as exfoliated hexagonal boron nitride flakes, glass substrates, and sapphire substrates by using CVD and the precursor methane.[10−12] It has also been demonstrated that wafer-scale and uniform graphene films can be grown directly on sapphire substrates by using CVD and the precursor ethane.[13] The major advantage of graphene grown directly on sapphire substrates is that other 2D materials can be grown directly on the graphene/sapphire substrates after the graphene growth procedure. For other approaches such as CVD-grown graphene on copper (Cu) foils, the grown graphene films have to be transferred to other substrates to prevent the reaction of the metal templates with the elements of following grown materials. In this case, the adhesion of the transferred films will be inferior than the as-grown samples, which will influence the growth of 2D materials onto the graphene surface. However, its inferior crystallinity compared with the graphene films grown on copper foils has significantly degraded the field-effect mobility of the transistor fabricated on the graphene films grown directly on sapphire substrates.[13] Since the growth mechanisms of graphene films on sapphire

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substrate include the graphene formation in the carrier gas and the flake attachment to sapphire substrates, the possible incomplete coverage of the one-time grown graphene films may also hinder the growth of the following thin films and their device performances.

In this paper, we have demonstrated that layered graphene films can be grown directly on the sapphire substrate by repeating CVD growth cycles. With optimized growth parameters, a wafer-scale and uniform second graphene layer can be grown on the first graphene layer directly on the sapphire substrate after the other CVD growth cycle. It is also possible to further expand the graphene layers to three after the third CVD growth cycle. A slight decrease in the D/G Raman peak ratio of the bilayer graphene film suggests that improved crystallinity is obtained after the second CVD growth cycle, which also results in enhanced field-effect mobility values for the bottom-gate transistors fabricated by using the bilayer graphene film. Since MoS_2 films can be nondestructively grown on the graphene surface by using the thermal evaporation, a thin stack of liner/diffusion barrier layers with monolayer MoS_2 and monolayer graphene may replace the current Ta/TaN stacks for interconnect applications.[14] With no significant resistivity increase with upon reducing the copper film thickness down to 10 nm, the MoS_2/graphene heterostructure has demonstrated its potential for thinner liner/barrier stacks for interconnect applications.

RESULTS AND DISCUSSION

For the growth of the first graphene layer, the sapphire substrate was placed at the center of a 1-in. quartz tube furnace system. The growth temperature is 1050 °C, and the background pressure is kept at 10 Torr. The Ar (300 sccm), H_2 (50 sccm), and C_2H_6 (5 sccm) mixture gas is introduced into the furnace during growth for 1 h. The scanning electron microscope (SEM) image of the sample with one-time graphene growth is shown in Figure 1a. As shown in the figure, a complete graphene film with few carbon clusters is obtained on the sapphire surfaces. Because of the high growth temperature and the different thermal expansion coefficients between the graphene film and the sapphire substrate, the wrinkles observed on the graphene surfaces should be attributed to the shrinkage of graphene films during the cooling procedure. In the ideal case there are no dangling bonds on 2D material surfaces. Therefore, severe graphene flake segregation is expected on the first graphene surface at high growth temperature. To prevent graphene flake segregation and achieve uniform and layered graphene growth, the background pressure is increased to 50 Torr for the growth of the second graphene layer and the same growth temperature 1050 °C and flow rates for both the carrier gas and the C_2H_6 precursor are maintained. The SEM image of the sample after the second graphene growth is shown in Figure 1b. As shown in the figure, although the background pressure has been increased to 50 Torr, large carbon clusters are observed on the sample surface, which indicates a severe segregation and coalescence of graphene flakes during the second CVD growth cycle.

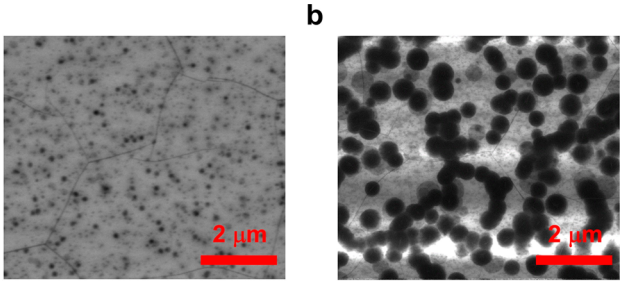

Figure 1. SEM images of two samples with (a) one and (b) two CVD growth cycles.

To prevent graphene flake segregation, another sample with a reduced growth temperature of 950 °C and background pressure 50 Torr is prepared. The SEM images of the sample are shown in Figure 2a. Compared with the sample grown at 1050 °C, fewer carbon clusters are observed on the sample surface. The results indicate that by reducing the growth temperature to 950 °C for the second CVD growth cycle the graphene flake segregation can be significantly avoided. On the other hand, it is also shown in the figure that the small carbon clusters will tend to aggregate along some wrinkles and leave others alone. Since the wrinkles are observed after the first CVD growth cycle, the results seem to indicate that after the second growth cycle the other graphene film is grown on top of the first graphene film. Since the segregation of graphene flakes is more severe at the second CVD growth cycle, the carbon cluster aggregation will be observed along the wrinkles on the second graphene film. On the other hand, since the wrinkles are formed during the cooling procedure, it is difficult for larger carbon clusters to migrate on the wafer when the temperature is reducing. In this case, the aggregation along the wrinkles is not observed for larger carbon clusters as shown in Figure 1b. Since the hydrogen balances the reactive hydrocarbon radicals during the CVD growth cycle, the increase of hydrogen flow rate may avoid excess graphene formation and avoid carbon cluster formation on the second graphene film surface. With the same growth condition except for the higher hydrogen flow rate of 200 sccm for the second CVD growth cycle, another sample with two-time graphene growth is prepared. The SEM image of the sample is shown in Figure 2b. As shown in the figure, compared with the sample with 50 sccm hydrogen flow rate, even fewer carbon clusters are observed on the sample surface. Although the same small carbon cluster aggregation along the wrinkles on the second graphene film is still observed for the sample, the results should still indicate that a uniform graphene film can be grown on the first graphene film after the modified CVD growth procedure.

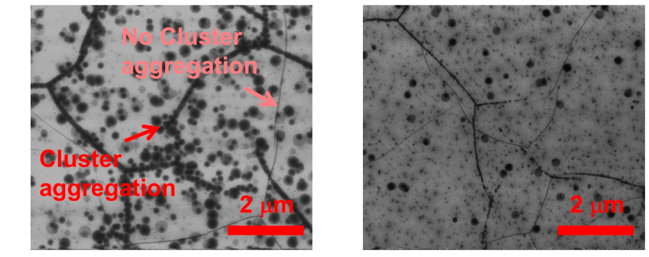

Figure 2. SEM images of the two samples grown at 950 °C with different hydrogen flow rates of (a) 50 and (b) 200 sccm.

The Raman spectra of two samples with one- and two-time graphene growth cycles are shown in Figure 3a. The growth parameters of the second growth cycle are 50 Torr background pressure, 950 °C growth temperature, and 200 sccm hydrogen

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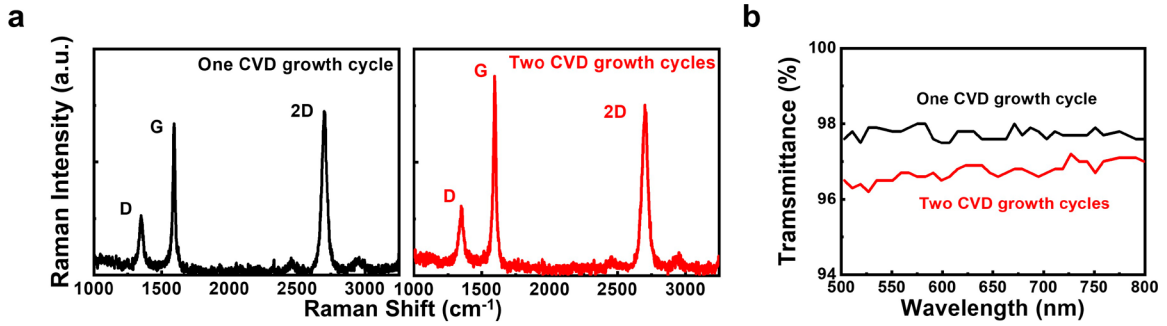

Figure 3. (a) Raman spectrum and (b) transmission spectra of the two samples with one and two CVD growth cycles.

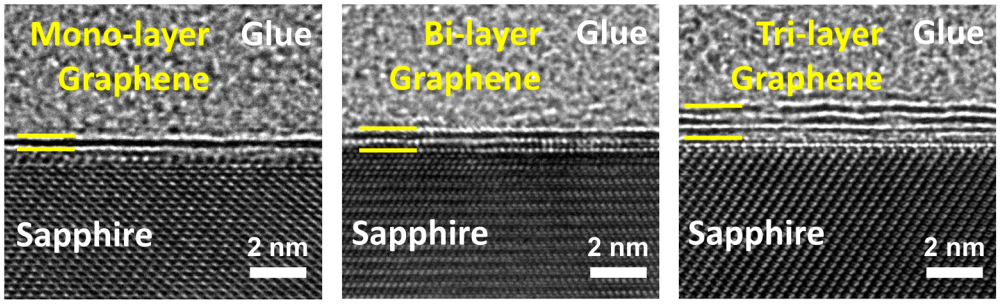

Figure 4. Cross-sectional HRTEM images of the three samples with one, two, and three CVD growth cycles. Mono-, bi-, and trilayer graphene are observed for the three samples, respectively.

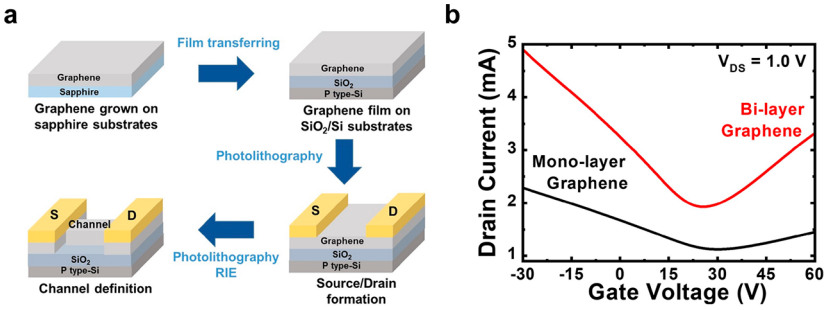

Figure 5. (a) Fabrication procedure and (b) transfer curves of the graphene bottom-gate transistors.

flow rate. As shown in the figure, the 2D/G peak ratios decrease from 1.08 to 0.85 with increasing graphene layers, which suggest that after the second graphene growth increasing graphene layers are observed for the sample. On the other hand, a slight decrease in the D/G peak ratio from 0.39 to 0.34 is observed with increasing layers. Although the slight D/G peak ratio decrease implies only a minor crystallinity improvement for the second graphene layer, the results still indicate that with the assistance of van der Waals epitaxy graphene layers with improved crystallinity can be grown on the first graphene surfaces. Besides the increase of layer numbers and improved crystallinity, wafer-scale graphene growth with good layer number controllability can also be obtained through the multi graphene growth cycles, which can be seen from the three-point Raman mappings shown in Figure S1. To confirm the layer numbers of multilayer graphene, one possible solution is through the measurement of the films' absorption. Since the light absorption for a monolayer graphene is around 2% and is wavelength insensitive, it should be possible to determine the layer numbers of graphene films directly through their transmission spectrum. The transmission spectra of the two samples with one and two CVD growth cycles in the wavelength range 500−800 nm are shown in Figure 3b. For the sample with one CVD growth cycle, the wavelength-insensitive absorption is around 2−3%, which indicates that a monolayer graphene is obtained. For the sample with two CVD growth cycles, the absorption increases to around 3−4%, which indicates that after the second CVD growth cycle a bilayer graphene should be obtained for the sample.

To further confirm the layer numbers of the graphene films, the cross-sectional high-resolution transmission electron microscope (HRTEM) images of two samples with one and two CVD growth cycles are shown in Figure 4. As shown in the figure, monolayer graphene is observed for the sample with one CVD growth cycle, while bilayer graphene is observed for the sample with two CVD growth cycles, which are consistent with the observation obtained from the transmission spectra. By repeating the same growth procedure for the second graphene layer, a third graphene layer can also be grown on the bilayer graphene layer. The HRTEM image of the sample is also shown in Figure 4. However, after three high-temperature growth cycles, the graphene film seems less adhesive to the sapphire substrate. To solve this problem, a low-temperature

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graphene growth procedure will be developed in the future. There are two possible applications for the layered graphene grown directly on sapphire substrates. Since the crystallinity of the graphene films can be improved by repeating the growth cycles, improved device applications can be obtained by using the multilayer graphene as the channel. The other application is the replacement of current liner/diffusion barrier layers in the back-end interconnects (copper; Cu) by using the multilayer 2D material layers. With the thin-body nature of 2D materials, a larger space can be left for metal filling of interconnects such that further size shrinkage of the interconnects can be achieved and the conductivity of the Cu wires can be maintained.

To demonstrate their transistor performances, mono- and bilayer graphenes are transferred to SiO_2/Si substrates for device fabrication. The fabrication procedure for the graphene bottom-gate transistors is shown in Figure 5a. After the films are transferred to the 300 nm SiO_2/p-type Si substrate, standard photolithography and metal lift-off procedures are adopted for source/drain formation, and 100 nm thick gold (Au) is deposited on the graphene surface as the metal electrode. After the source/drain formation, photolithography and reactive-ion beam etching (RIE) are adopted to form graphene channels with length/width 5/150 μm. The transfer curves of the two devices with monolayer and bilayer graphene at V_{DS} = 1.0 V are shown in Figure 5b. Much higher drain currents are observed for the device with bilayer graphene. By using the equation

$$\mu = (dI_{DS}/dV_{GS}) \times (L/W) \times (t/\epsilon) \times V_{DS}^{-1}$$

the hole and electron mobility values of the two devices derived through the transfer curves are 108/43 (monolayer) and 358/146 (bilayer) $cm^2\ V^{-1}\ s^{-1}$, respectively. Higher hole and electron field-effect mobility values are observed for the device with the bilayer graphene channel. The results have demonstrated that with the assistance of van der Waals epitaxy on the first graphene layer surface improved crystallinity can be obtained for the second graphene layer such that a lower D/G peak ratio is observed. After the graphene films are fabricated into transistors, higher drain currents and higher field-effect mobility values are observed for the device with bilayer graphene. The results have demonstrated that layered graphene growth can significantly improve the device performance of graphene transistors.

Although the wettability of Cu film is poor on graphene surfaces, the graphene films may act as a diffusion barrier to the Cu atoms (see Figures S2 and S3). In this case, it is possible to grow the other 2D material layer on the graphene surface as the liner layer. One possible candidate is the well-developed 2D material MoS_2. To demonstrate the potential of MoS_2/graphene heterostructures as the liner/barrier layer, samples with monolayer MoS_2/monolayer graphene heterostructures are prepared. By using the graphene/sapphire samples with the one-time CVD growth cycle as the substrates, a 1.0 nm MoO_3 film is deposited on the graphene/sapphire substrate by using thermal evaporation.[15] After the MoO_3 deposition procedure, a sulfurization procedure is performed on the sample. A monolayer MoS_2/monolayer graphene 2D material heterostructure is then established. The Raman spectrum of the MoS_2/graphene heterostructure is shown in Figure S4. The Raman peak difference 20.3 cm^{-1} of the MoS_2 Raman peaks suggests that monolayer MoS_2 is obtained after the sulfurization procedure. Afterward, Cu films with different thicknesses are deposited on the MoS_2 surface at rt. The cross-sectional HRTEM image of the sample with a 20 nm Cu/monolayer MoS_2/monolayer graphene is shown in Figure 6a.

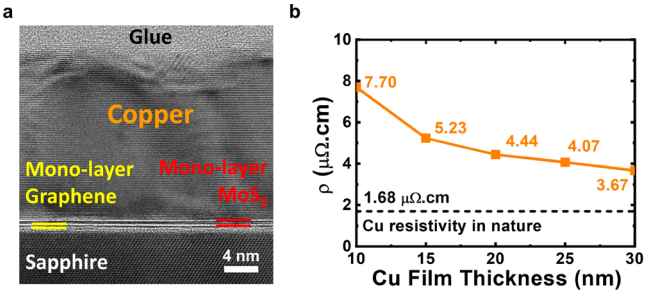

Figure 6. (a) Cross-sectional HRTEM image of the sample with 20 nm Cu/monolayer MoS_2/monolayer graphene and (b) resistivity of Cu films with different thicknesses deposited on the monolayer MoS_2/monolayer graphene 2D material heterostructures. The black dashed line is the resistivity value of Cu in nature (1.68 $\mu\Omega$·cm).

As shown in the figure, a polycrystalline Cu film is observed on the MoS_2 surface, which indicates a good wettability of Cu on the MoS_2 surface. Compared with the ∼4 nm thickness of the liner (Ta)/barrier (TaN) stacks, the thickness of monolayer MoS_2/monolayer graphene can be greatly decreased to ∼1 nm, which will leave more room for Cu filling in the interconnects, and further size shrinkage may be possible by using 2D materials as the liner/barrier stacks. The resistivity values of Cu films deposited on the samples with monolayer MoS_2/monolayer graphene films are shown in Figure 6b. The resistivity value of Cu in nature (1.68 $\mu\Omega$·cm) is also shown in the figure for comparison. With decreasing Cu film thicknesses, the resistivity values gradually increase from 3.67 (30 nm) to 7.7 (10 nm) $\mu\Omega$·cm. With no significant resistivity increasing with reduced film thicknesses, the thin MoS_2/graphene heterostructure as the liner/barrier stack can be advantageous for further interconnect scaling. The 5.23 $\mu\Omega$·cm resistivity of 15 nm Cu film in this work is close to the value ∼5 $\mu\Omega$·cm of the Cu film with the same thickness deposited on exfoliated MoS_2 flakes.[16] Since the grown MoS_2 film is a polycrystalline film, the results demonstrate that the crystallinity of the MoS_2 film will not significantly influence the wettability of Cu on MoS_2 surfaces.

CONCLUSIONS

In conclusion, we have demonstrated that wafer-scale and uniform layered graphene can be grown directly on sapphire substrates through repeating CVD growth cycles. We have also demonstrated that with the assistance of van der Waals epitaxy on 2D material surfaces improved crystallinity of the second graphene layer can be obtained by using the first graphene layer as the substrate interface. Enhanced field-effect mobility values are also observed for the bottom-gate transistors with bilayer graphene channels. By using MoS_2 as the liner layer and graphene as the diffusion barrier layer, low resistivity values of Cu films are observed. The results demonstrate that the unique van der Waals epitaxy growth mode will also help lateral growth, and therefore, film formation of thin metal films on 2D material surfaces. The scalable 2D material growth techniques and the possibility of their heterostructure establishment are advantageous for the application of 2D material liner/barrier stacks in back-end interconnects.

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EXPERIMENTAL SECTION

For the growth of the first graphene layer, the sapphire substrate was placed at the center of a 1-in. quartz tube furnace system. Then the temperature was raised to 1050 °C, and the pressure was kept at 10 Torr. After the growth temperature was reached, the Ar (300 sccm), H_2 (50 sccm), and C_2H_6 (5 sccm) mixture gases were introduced into the furnace for graphene growth. After 1 h of growth, the sample was removed from the furnace.[13] For the growth of the second graphene layer, the growth temperature was reduced to 950 °C, the background pressure was raised to 50 Torr, and the hydrogen gas flow rate was raised to 200 sccm. For device fabrication, the graphene films were transferred to the SiO_2/Si substrate. The transferring procedure was as follows: (a) After the graphene growth procedure, a poly(methyl methacrylate) (PMMA) film was deposited on the graphene surface by using a spin coater. (b) After 120 °C curing for 5 min, the sample was placed into a Petri dish filled with deionized (DI) water. (c) The PMMA/graphene film was slowly peeled from the sapphire substrate using a tweezer. (d) A SiO_2/Si substrate was used to scoop up the PMMA/graphene film floating in the DI water. (e) The sample was merged into a beaker filled with acetone to remove the PMMA film from the graphene surface. Using the graphene/sapphire sample as the new substrate, a 1.0 nm MoO_3 film was deposited on the graphene surface by using the thermal evaporation. The deposition rate was kept at 0.1 nm/s. After MoO_3 was deposited, the sample was placed in the center of a furnace for sulfurization. During the sulfurization procedure, 200 sccm Ar gas was utilized as carrier gas while the furnace pressure was kept at 50 Torr. The growth temperature of the sample was kept at 850 °C with the sulfur (S) powder placed on the upstream of the gas flow. The evaporation temperature for the S powder was kept at 160 °C. After the sulfurization procedure, monolayer MoS_2/monolayer graphene heterostructures could be established.[15] The current−voltage characteristics were taken with probes equipped with a Keithley 2636B system. The Raman spectra were obtained using a HORIBA Jobin Yvon HR800UV Raman spectroscopy system equipped with a 488 nm laser. The cross-sectional high-resolution transmission electron microscopy (HRTEM) images were obtained using a JEOL JEM-2800F TEM system operated at 200 kV.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.2c00554.

Raman mapping of graphene samples (Figure S1); AFM image of Cu deposited on graphene at rt (Figure S2); cross-sectional HRTEM image of Cu deposited on graphene at 200 °C (Figure S3); Raman spectrum of the MoS_2/graphene heterostructure (Figure S4) (PDF)

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Notes

The authors declare no competing financial interest.

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