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Communication

Frequency-Stable Ionic-Type Hybrid Gate Dielectrics for High Mobility Solution-Processed Metal-Oxide Thin-Film Transistors

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Academic Editor: Pedro Barquinha
Received: 19 April 2017; Accepted: 1 June 2017; Published: 3 June 2017

Abstract: In this paper, we demonstrate high mobility solution-processed metal-oxide thin-film transistors (TFTs) by using a high-frequency-stable ionic-type hybrid gate dielectric (HGD). The HGD gate dielectric, a blend of sol-gel aluminum oxide (AlO_x) and poly(4-vinylphenol) (PVP), exhibited high dielectric constant (ε~8.15) and high-frequency-stable characteristics (1 MHz). Using the ionic-type HGD as a gate dielectric layer, an minimal electron-double-layer (EDL) can be formed at the gate dielectric/InO_x interface, enhancing the field-effect mobility of the TFTs. Particularly, using the ionic-type HGD gate dielectrics annealed at 350 °C, InO_x TFTs having an average field-effect mobility of 16.1 cm^2/Vs were achieved (maximum mobility of 24 cm^2/Vs). Furthermore, the ionic-type HGD gate dielectrics can be processed at a low temperature of 150 °C, which may enable their applications in low-thermal-budget plastic and elastomeric substrates. In addition, we systematically studied the operational stability of the InO_x TFTs using the HGD gate dielectric, and it was observed that the HGD gate dielectric effectively suppressed the negative threshold voltage shift during the negative-illumination-bias stress possibly owing to the recombination of hole carriers injected in the gate dielectric with the negatively charged ionic species in the HGD gate dielectric.

Keywords: metal-oxide semiconductors; thin-film transistors; hybrid gate dielectric; low temperature solution-process; high mobility

1. Introduction

Solution-processed metal-oxide thin-film transistors (TFTs) are emerging as a potential replacement for amorphous and low-temperature polycrystalline silicon TFTs in active-matrix electronics including displays, sensor arrays, and driving circuits due to their relatively high carrier mobility and good scalability over a large area [1–4]. In addition, their amorphous nature and high optical transparency in the visible range may open up a new promising application for transparent and wearable electronics. In general, the metal-oxide TFTs such as indium-gallium-zinc oxide exhibit a higher carrier mobility than that of the amorphous silicon and organic TFTs [5,6]. However, in order to realize high definition, high frame-rate displays, and the relevant driving circuitry, the carrier mobility must be further improved while exhibiting good operational stability. For these reasons, various metal-oxide semiconductors [7,8], gate dielectrics [9,10], novel device structures [11,12], and post treatments [13,14] have been proposed to enhance the carrier mobility of these devices. Among the

various approaches in achieving high mobility metal-oxide TFTs, using an ionic-type gate dielectric is a promising method of achieving both the high mobility and low voltage operation characteristics [15–19]. Previously, ion-gel-type gate dielectrics [20], protonated SiO_2 gate dielectrics [21], and electrolyte gate dielectrics have been explored. Although these ionic-type gate dielectrics showed promising results for achieving high mobility devices, their limited operation at high frequencies may hinder their practical application in active-matrix electronics. In this respect, new types of ionic-type gate dielectrics, which are capable of operating at high frequencies, are now in high demand. Moreover, for the consistency in the fabrication process of oxide TFTs, solution processing of frequency-stable ionic-type gate dielectrics will be more favorable.

Here, we demonstrate solution-processed ionic-type gate dielectrics based on AlO_x and a hybrid of AlO_x and poly(4-vinylphenol) (PVP) materials. In particularly, the low-temperature solution-processed hybrid gate dielectric (HGD) exhibited reasonably high capacitance and dielectric constant, and only a slight decrease in areal capacitance was observed at high frequencies up to 1 MHz along with minimal hysteresis due to the local confinement of mobile ions inside the polymer networks and consequent suppression of electron-double-layer (EDL) effects [22]. In addition, using the solution-processed HGD gate dielectrics in indium oxide (InO_x) TFTs, relatively high mobilities up to 24 cm^2/Vs were achieved due to the formation of an acceptable EDL at the gate dielectric/InO_x interface for high frequency applications. These results demonstrate that the low-temperature solution-processed HGD gate dielectrics may enable the high-mobility, low-voltage, and high-frequency operation of oxide TFTs.

2. Experimental Procedure

For the fabrication of an AlO_x gate dielectric, an AlO_x precursor solution was prepared by dissolving 0.8 M aluminum nitrate nonahydrate in 2-methoxyethanol (2-ME) followed by vigorously stirring at 75 °C for 12 h. For the HGD gate dielectric, a poly(4-vinylphenol) (PVP) precursor was dissolved by stirring in 2-ME for 12 h to form a 5 mg mL^{-1} solution. Then, an additional 5% PVP (AlO_x: 5% PVP) was added to the AlO_x precursor solution and stirred for 6 h at 75 °C. For the InO_x channel formation by a solution process, 0.1 M indium nitrate was dissolved in 2-ME and stirred for 12 h at 75 °C. For the electrical characterization of solution-processed gate dielectrics, a heavily-doped n^+ Si wafer was used as a substrate, and Si wafer/AlO_x(or HGD)/Al (metal-insulator-metal; MIM) and Si wafer/AlO_x(or HGD)/InO_x/Al (metal-insulator-semiconductor; MIS) structures were constructed. The top Al was deposited by using a thermal evaporator with a shadow mask (effective area: 100×100 μm^2). For the fabrication of InO_x TFTs, a borosilicate glass was used as a substrate. Then, Cr gate electrode was deposited by e-beam evaporation and patterned by using standard photolithography and wet etching processes. Afterwards, the AlO_x or HGD precursor solution was spin-coated over the gate electrode to form a gate dielectric layer. Thermal annealing treatment at 150, 250, 350, and 450 °C for 30 min was carried out in an ambient air condition, resulting in thicknesses of 89, 60, 50 and 40 nm, respectively. After the formation of the gate dielectric, an InO_x precursor solution was spin-coated to form a channel layer and thermally annealed at 250 °C for 30 min, resulting in a thickness of 7 nm. For the source/drain electrodes, 60-nm-thick indium zinc oxide (IZO) was deposited by sputtering and patterned by a lift-off process (Figure 1a). The channel width and length of the InO_x TFTs were 100 μm and 10 μm, respectively. The thickness of the gate dielectric layer was measured by using spectroscopic ellipsometry, and to obtain the dielectric constant (ε_r) of the film, the capacitance value (C) was first assessed by using a precision LCR meter and the dielectric constant was extracted using the following equation:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

where C is the capacitance, A is the overlapped area between top and bottom electrodes, d is the thickness of gate dielectric layer, and ε_0 is the vacuum permittivity, respectively.

To evaluate the dielectric properties of AlO_x and HGD films, areal capacitance vs. frequency and leakage current density vs. electric field were analyzed using a precision LCR meter and

a semiconductor parameter analyzer, respectively. In addition, the electrical characterization and bias stability tests for the InO_x TFTs were carried out using a semiconductor parameter analyzer under an ambient air condition with a relative humidity of ~33% and a temperature of 24 °C. For analyzing the transfer characteristics, the gate voltage was swept from −5 to 6 V with a voltage step of 0.1 V. Additionally, it should be noted that, since the degree of hysteresis in the transfer curves and the field-effect mobility of InO_x TFTs with low-temperature annealed gate dielectric can vary with the gate-voltage sweep rate, we applied a gate-voltage sweep rate of 0.13 V/s for all TFT measurement.

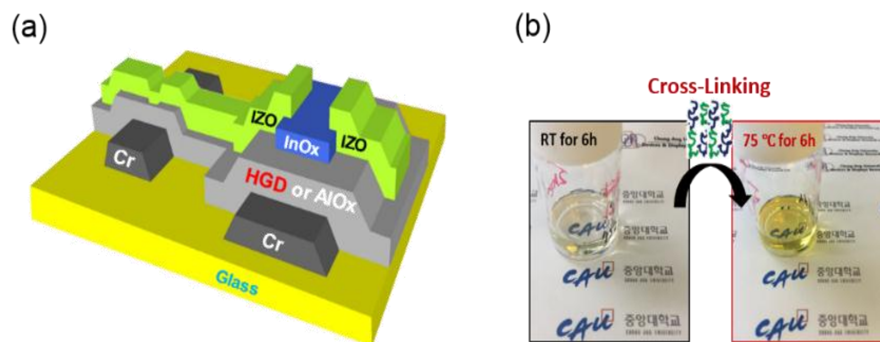

Figure 1. (**a**) Schematic illustration of InO_x TFTs using AlO_x or HGD gate dielectric layer; (**b**) Photographs of an HGD solution before and after a thermal cross-linking.

3. Results and Discussion

In order to examine the dielectric properties of solution-processed AlO_x and HGD layers, the areal capacitance vs. frequency (C-F) and the current density vs. electric field (J-E) characteristics were measured. In addition, the difference in the surface morphology of AlO_x and HGD films is negligible. Figure 2a,b show the areal capacitance vs. frequency data for AlO_x and HGD gate dielectrics, respectively. In the case of the AlO_x gate dielectric, the capacitance value and the corresponding dielectric constant showed an increasing trend with the annealing temperature. Particularly, with an annealing temperature of 150 °C, the dielectric constant was 7.09 (thickness of 89 nm), but it decreased to 6.11 and 5.11 when the annealing temperature was increased to 350 °C and 450 °C, respectively. In the case of HGD gate dielectric, a similar behavior was observed as shown in Figure 2b. With an annealing temperature of 150 °C, HGD gate dielectric exhibited a dielectric constant of 8.15, and decreased to 6.10 and 6.01 when the annealing temperature was increased to 350 °C and 450 °C, respectively. It should be noted that the areal capacitance value and the corresponding dielectric constant were higher in the HGD gate dielectric, which can be attributed to the mobile ions in the polymer network combined with AlO_x film. To further investigate the insulating properties, the current density vs. electric field measurements for AlO_x and HGD gate dielectrics were carried out. Figure 2c,d show the current density vs. electric field data for AlO_x and HGD gate dielectrics, respectively. In the case of AlO_x gate dielectric, even a low temperature annealing of 150 °C resulted in reasonable insulating properties. With the annealing temperature of 150 °C, the leakage current density was 4.45×10^{-6} A/cm^2 at an electric field of 2 MV/cm. Further increasing the annealing temperature to 350 °C and 450 °C improved the insulating properties, and the current density was decreased to 4.44×10^{-7} A/cm^2 and 8.29×10^{-10} A/cm^2, respectively. In the case of HGD gate dielectric, even a low temperature annealing of 150 °C resulted in reasonable insulating properties. At an annealing temperature of 150 °C, the leakage current density was 1.47×10^{-5} A/cm^2 at an electric field of 2 MV/cm. Increasing the annealing temperature to 350 °C and 450 °C improved the insulating properties and the current density was decreased to 1.47×10^{-6} A/cm^2 and 2.37×10^{-9} A/cm^2, respectively. Additionally, an AlO_x and HGD film with the annealing temperature of 250 °C have insulator properties similar to those of 150 °C-annealed gate dielectric films, while thickness were decreased from 89 to 60 nm. The slightly high leakage current density observed in HGD gate dielectrics provides that a profound

number of mobile ions may exist in the gate dielectric layer. However, even with the mobile ions, the leakage current density is reasonably low to be utilized as a gate dielectric layer.

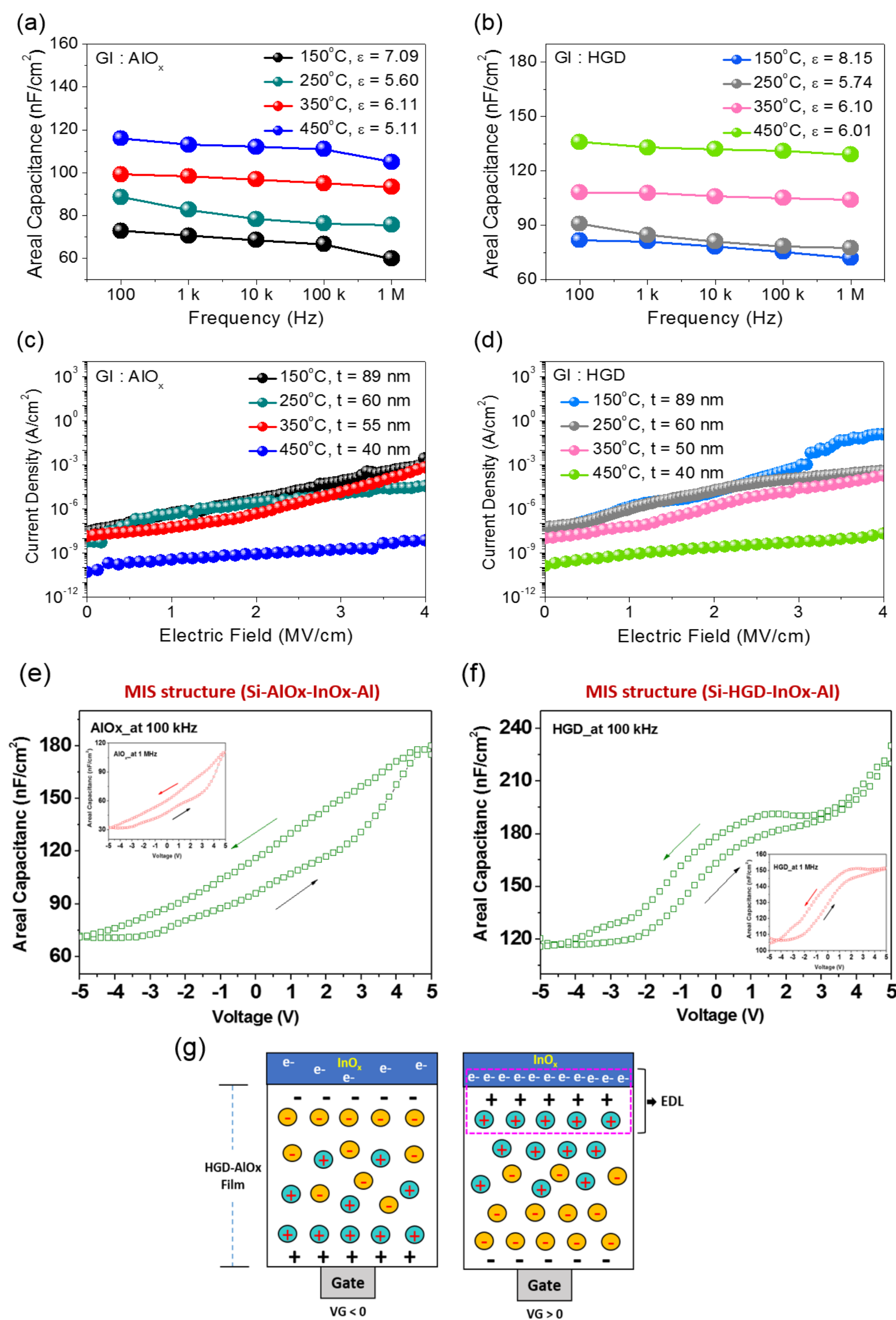

Figure 2. Electrical characteristics for solution-processed AlO_x or HGD dielectric layer using metal-insulator-metal structure (MIM; Si/AlO_x or HGD/Al) with the different annealing conditions (at 150, 250, 350, and 450 °C). The areal capacitance per area-frequency (C-F) of solution-processed (**a**) AlO_x and (**b**) HGD dielectric layer; leakage current density-electric field (J-E) of solution-processed (**c**) AlO_x and (**d**) HGD dielectric layer; the C-V characteristics of an (**e**) AlO_x and (**f**) HGD gate dielectric (150 °C) at 100 kHz and 1 MHz (inset) using metal-insulator-semiconductor structure (MIS; Si/AlO_x or HGD/InO_x/Al); (**g**) the polarization mechanisms and electric double layer formation in InO_x TFTs with HGD dielectric layer.

The presence of mobile ions in the solution-processed AlO_x and HGD gate dielectrics were further validated by measuring the areal capacitance change as a function of bias polarity. Figure 2e,f show the areal capacitance vs. voltage (C-V) plots for AlO_x and HGD gate dielectrics annealed at 150 °C, respectively. Here, the C-V characteristics were obtained using an MIS structure of Si wafer/AlO_x(or HGD)/InO_x/Al at frequencies of 100 kHz and 1 MHz (inset). As displayed, the areal capacitance increases when the bias polarity changed from negative to positive bias, which can be attributed to the formation of an EDL at the AlO_x(or HGD)/InO_x interface. Particularly, in the case of AlO_x gate dielectric, the hysteresis was comparably larger than that of an HGD gate dielectric, possibly indicating a larger amount of residual mobile ions present in the film. As schematically illustrated in Figure 2g, when a negative bias is applied to the Si wafer, positively charged mobile ions accumulate near the AlO_x(or HGD)/Si wafer interface, while the negatively charged mobile ions move toward the AlO_x or HGD/InO_x interface. Since the majority carrier in the InO_x semiconductor is an electron (an n-type), the negatively charged mobile ions near the AlO_x(or HGD)/InO_x interface repel the electrons in the InO_x channel. However, when a positive bias is applied to the Si wafer, the positively charged mobile ions move toward AlO_x(or HGD)/InO_x interface. Then, these positively charged mobile ions accumulate electrons in the InO_x channel, forming an EDL at the AlO_x(or HGD)/InO_x interface. This in turn increases the areal capacitance of the device. The different capacitance with applied bias frequency may constitute solid evidence of the formation of an EDL layer. The lower capacitance with larger hysteresis at high frequency (1 MHz) is likely due to the less responsive mobile ions inside the AlO_x films.

Using the solution-processed AlO_x and HGD layers as a gate dielectric, InO_x TFTs were fabricated. Figure 3a–c show the transfer characteristics of InO_x TFTs fabricated with AlO_x gate dielectric layer annealed at different temperatures. In the case of the 150 °C-annealed AlO_x gate dielectric, an average field-effect mobility of 183.0 cm^2/Vs was observed, which is remarkably high as compared to those made with SiO_2 gate dielectrics [23,24]. The exceptionally high mobility observed using the AlO_x gate dielectric can be attributed to the formation of an EDL due to a large amount of residual –OHs inside the AlO_x films [25]. In addition to the positive gate bias, a substantial number of electrons are accumulated near the AlO_x/InO_x interface due to the EDL formation. These additional electrons contribute to the drain current resulting in a high drain current and increased field-effect mobility, as well as a large counter-clockwise hysteresis. As mentioned above, the formation of EDL is due to the mobile ions, including –OH residues in the AlO_x gate dielectric layer. As shown in Figure 3b,c, the drain current and the field-effect mobility decreased as the annealing temperature increased. Particularly, with annealing temperatures of 250 °C and 350 °C, the field-effect mobility was decreased to 45.5 cm^2/Vs and 5.47 cm^2/Vs, respectively. At a higher annealing temperature, the number of mobile ions dramatically decreases, which drives the formation of a weak EDL and a low carrier concentration at the AlO_x/InO_x interface.

In the case of the HGD gate dielectric layer, similar behavior was observed. Figure 4a–c show the transfer characteristics of InO_x TFTs fabricated with the HGD gate dielectric layer annealed at different temperatures. The InO_x TFTs fabricated with a 150 °C-annealed HGD gate dielectric showed an average field-effect mobility of 120.2 cm^2/Vs. Additionally, in the case of 250 °C- and 350 °C-annealed HGD gate dielectrics, field-effect mobilities of 94.3 cm^2/Vs and 16.1 cm^2/Vs were observed, respectively, showing a similar decreasing trend with the annealing temperature. This decreasing trend of mobility with annealing temperature can also be attributed to the decrease of the mobile ions and corresponding weak EDL formation. The relatively superior mobility in the HGD devices can be described by the aforementioned polymer network confinement of the mobile ions in the HGD [20]. Nonetheless, the solution-processed HGD gate dielectrics allow the acceptable formation of EDL at the gate dielectric/InO_x interface, which significantly enhances the electrical properties of InO_x TFTs compared to the bare AlO_x films. In addition, due to the high dielectric constant and low thickness of the gate dielectric layers, low voltage operation below 6 V was possible, enabling low power consuming electronic devices.

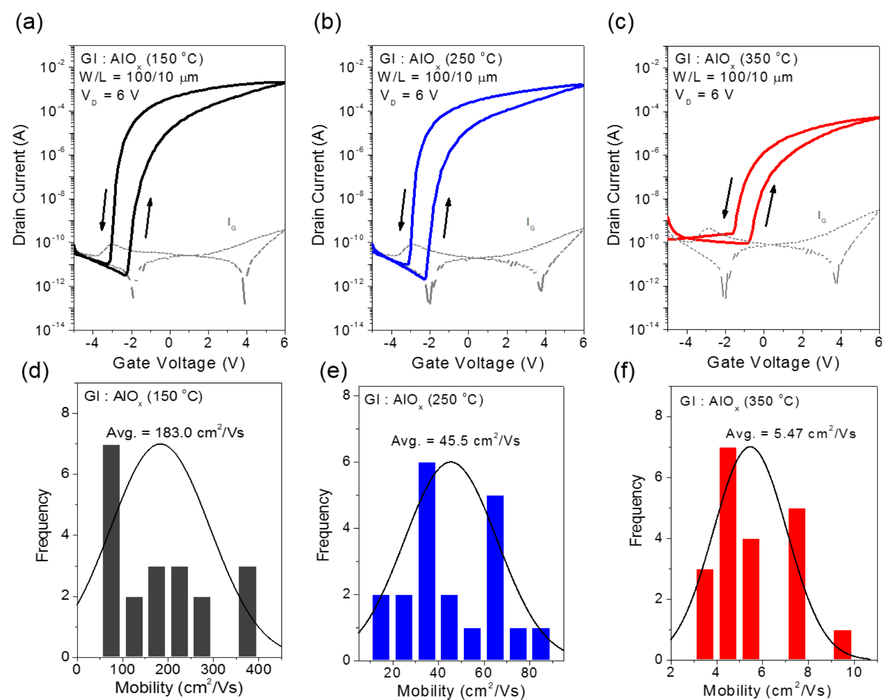

Figure 3. Electrical characteristics of various solution-processed InO_x TFTs on an AlO_x dielectric layer for the different processed conditions. The transfer curves for InO_x TFTs with (**a**) 150 °C-annealed; (**b**) 250 °C-annealed; and (**c**) 350 °C-annealed AlO_x films; the dotted lines indicate the gate leakage current. Statistical distribution of field-effect mobilities for InO_x TFTs with (**d**) 150 °C-annealed; (**e**) 250 °C-annealed; and (**f**) 350 °C-annealed AlO_x films.

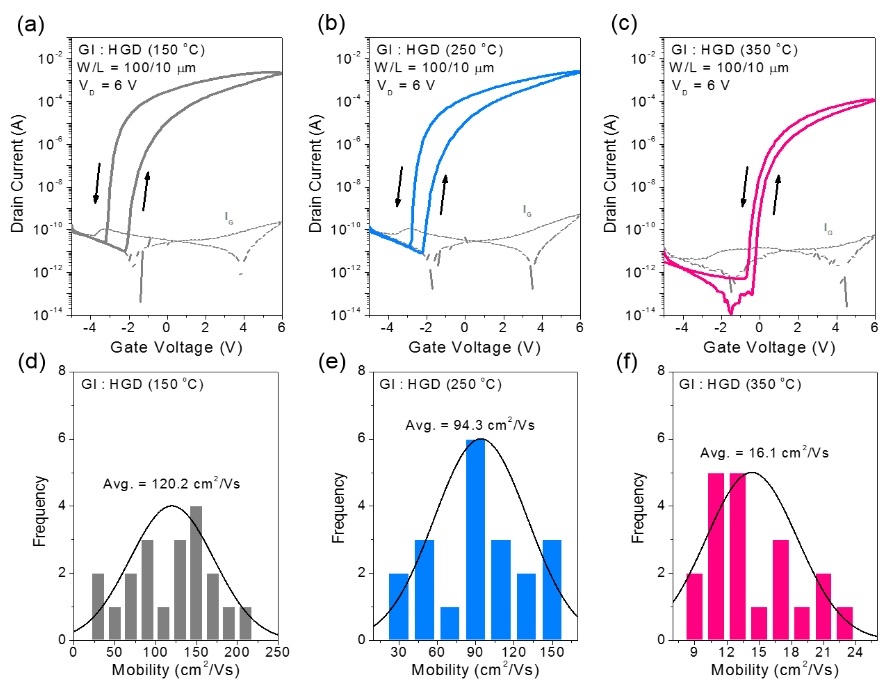

Figure 4. Electrical characteristics of various solution-processed InO_x TFTs on an HGD dielectric layer for the different processed conditions. The transfer curves for InO_x TFTs with (**a**) 150 °C-annealed; (**b**) 250 °C-annealed; and (**c**) 350 °C-annealed HGD films. The dotted lines indicate the gate leakage current. Statistical distribution of field-effect mobilities for InO_x TFTs with (**d**) 150 °C-annealed; (**e**) 250 °C-annealed; and (**f**) 350 °C-annealed HGD films.

In oxide semiconductor-based TFTs, the operational stabilities under positive gate bias stress (PBS) and negative illumination gate bias stress (NBIS) are important factors. In order to determine the operational stability of InO_x TFTs using the HGD gate dielectric, PBS and NBIS tests were carried out. Figure 5a shows the variation of transfer characteristics in InO_x TFTs under PBS. Here, the gate bias was set at +3 V, and the transfer curves were measured at 60, 360, and 3960 s. As shown in Figure 5b, the device exhibited reasonably small threshold voltage shift ($\Delta V_T = -1.67$ V) during the 3960 s of PBS. Typically, under PBS conditions, oxide TFTs tend to have positive V_T shift due to the electron trapping at the gate dielectric/semiconductor interface [26–28]. However, in the case of InO_x TFTs using the HGD gate dielectric, a negative V_T shift was observed. This opposite behavior in V_T instability is possibly caused by the mobile ions present in the HGD gate dielectric. Particularly, under a continuous PBS condition, a significant amount of positively charged mobile ions move towards the InO_x/HGD interface (Figure 6a). These positive mobile ions, then, contribute to the accumulation of electrons in the InO_x channel layer. However, due to the slow responsive characteristic of mobile ions [29–31], they tend to remain near the InO_x/HGD interface causing a negative shift of transfer curves. In addition, the stability under the NBIS condition was also analyzed. Figure 5c,d show the variation of transfer characteristics and V_T under NBIS condition, respectively. Surprisingly, the InO_x TFT showed extremely high stability against NBIS and showed ΔV_T of -0.23 V (after 3960 s). Typically, the NBIS causes a significant negative V_T shift due to the ionization of neutral oxygen vacancies and negative-bias-induced hole injection in the gate dielectric layer [32–35]. However, the InO_x TFT with HGD gate dielectric showed negligible V_T shift under a prolonged light illumination and negative bias condition. This significant reduction in the V_T shift can be attributed to the neutralization of injected holes with the negatively charged mobile ions near the InO_x/HGD interface (Figure 6b). As a consequence, the device can exhibit a high operational stability under NBIS. Furthermore, it should be noted that the InO_x TFTs with an HGD dielectric layer exhibited fast recovery after the PBS and NBIS tests. It was found that the V_T was recovered to original states after around 6 min, which can be attributed to the gradual neutralization of EDL during the recovery.

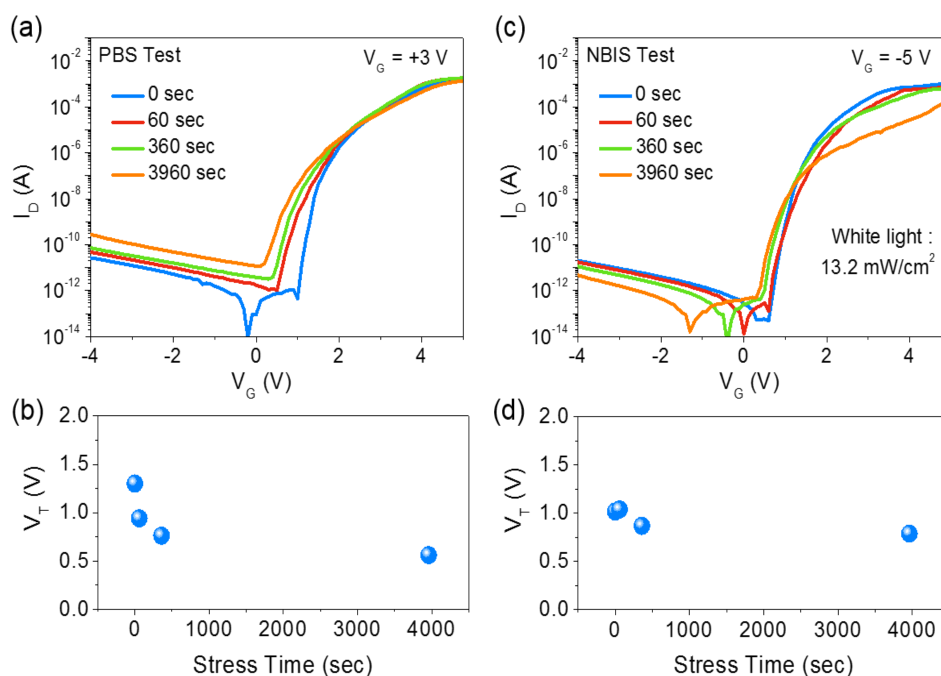

Figure 5. (**a**) Positive gate bias stability and (**b**) evolution of threshold voltage (V_T) of solution-processed InO_x TFTs with the 150 °C-annealed HGD dielectric layer (V_{GS} = +3 V, t = 3960 s); (**c**) negative gate bias illumination stability and (**d**) evolution of threshold voltage (V_T) of solution-processed InO_x TFTs with the 150 °C-annealed HGD dielectric layer ($V_{GS} = -5$ V, t = 3960 s).

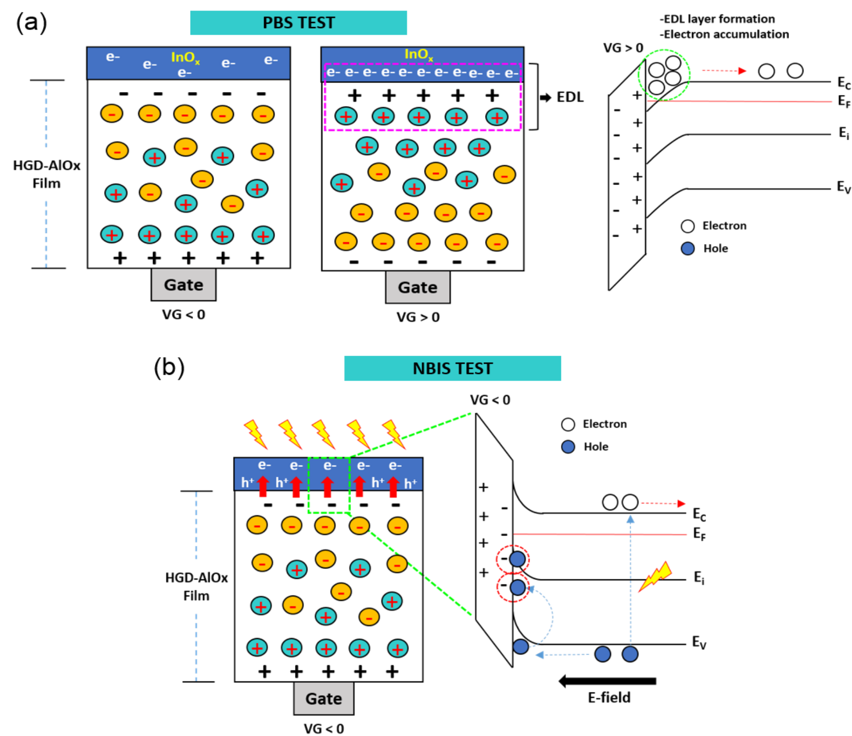

Figure 6. Schematic and energy band diagrams of corresponding V_T instability of solution-processed InO_x TFT with the 150 °C-annealed HGD dielectric layer for (**a**) PBS and (**b**) NBIS tests.

4. Conclusions

In this paper, we demonstrated high-mobility, operationally stable InO_x TFTs by using ionic-type AlO_x and HGD gate dielectrics. The solution-processed AlO_x and HGD exhibited reasonably high capacitance and dielectric constant, and only a small decrease in capacitance was observed at high frequencies, enabling a high frequency operation. Using the solution-processed HGD gate dielectrics with 350 °C annealing treatment, solution-processed InO_x TFTs were fabricated with an average field-effect mobility of 16.1 cm^2/Vs with minimal hysteresis. In addition, the HGD gate dielectric also suppressed the negative V_T shift during the NBIS condition, which enhanced the operation stability of the InO_x TFTs.

Acknowledgments: This work was partially supported by the Human Resources Development (No. 20154030200860) of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by the Korea government Ministry of Trade, Industry and Energy and by the Chung-Ang University Research Scholarship Grants in 2016.

Author Contributions: Jae Sang Heo, Seungbeom Choi, Jeong-Wan Jo, and Jingu Kang performed the experiments and the data analysis. Sung Kyu Park, Yong-Hoon Kim, and Ho-Hyun Park helped draft the manuscript and carry out data analysis and evaluation. Sung Kyu Park and Yong-Hoon Kim made substantial contributions to the concept of experiments and were responsible for leading the project. All authors read and approve the final manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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