ACS OMEGA

http://pubs.acs.org/journal/acsodf

Article

Performance Improvement with an Ultrathin p-Type Interfacial Layer in n-Type Vertical Organic Field-Effect Transistors Based on Reduced Graphene Oxide Electrode

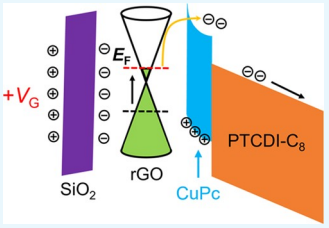
Kun Qiao, Shun Arakaki, Mitsuharu Suzuki, and Ken-ichi Nakayama*

Cite This: *ACS Omega* 2022, 7, 24468−24474

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Vertical organic field-effect transistors (VOFETs) with a large current on/off ratio and easy fabrication process are highly desirable for future organic electronics. In this paper, we proposed an ultrathin p-type copper (II) phthalocyanine (CuPc) interfacial layer in reduced graphene oxide (rGO)-based VOFETs. The CuPc interfacial layer was sandwiched between the rGO electrode and the *N*,*N*′-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C_8) organic layer. The introduced CuPc interfacial layer not only decreased the off-current density of the device but also slightly enhanced the on-current density. The threshold voltage of the device was also effectively improved and stabilized at around 0 V. The obtained device exhibited a current on/off ratio exceeding 10^6, which is the largest value reported for rGO-based VOFETs. The vertical electron mobility of the PTCDI-C_8 layer estimated by the space-charge-limited current technique was 1.14×10^{-3} $cm^2/(V\ s)$. However, it was not the main limiting factor for the current density in this device. We totally fabricated 48 devices, and more than 75% could work. Besides, the device was stable with little performance degradation after 1 month. The use of low-cost, solution-processable rGO as work-function-tunable electrode and the application of an ultrathin CuPc interfacial layer in VOFETs may open up opportunities for future organic electronics.



1. INTRODUCTION

Organic field-effect transistors (OFETs) play an important role in modern electronic devices.[1−3] They have attracted considerable interest due to their appealing features, such as low cost, easy fabrication, and flexibility.[4,5] To date, most investigated OFETs are the traditionally lateral structure.[6−8] Although some performance improvements have been achieved, the intrinsic long channel length remains a big challenge for its electrical properties. Therefore, vertical organic field-effect transistors (VOFETs) were proposed, in which the channel length is only determined by the thickness of the organic layer.[9,10] Owing to the significantly decreased channel length, these devices could be fabricated in a small size with improved electrical properties, demonstrating great potential for future organic electronics.

Graphene, a typical two-dimensional material, attracts considerable attention due to its excellent electrical and mechanical properties.[11,12] The vertical device structure based on graphene/semiconductor heterostructures has been considered as an interesting platform for electronic devices.[13−25] In these devices, the work function tunability of graphene is exploited under an external gate electrical field to modulate the injection barrier height at the graphene/semiconductor interface. However, almost all of these devices assembled to date have utilized monolayer graphene obtained via the chemical vapor deposition (CVD) method.[18−21] The rather complicated transfer process of CVD-grown graphene cannot satisfy large-scale application in VOFETs.[9] Therefore, an alternative electrode that is easy to fabricate, inexpensive, and capable of large-scale application is urgently needed.

Reduced graphene oxide (rGO) has a similar structure and properties to graphene.[26−28] Importantly, it can be easily mass-produced by the reduction of low-cost graphene oxide (GO).[29,30] Furthermore, the solution-processable rGO electrode is compatible with some industrial processing techniques such as printing and laser-direct writing.[31−33] Hence, the use of rGO to replace the CVD-grown graphene in VOFETs is highly desirable, which benefits the large-scale application in future organic electronics. The first paper on the use of rGO as work-function-tunable electrode in VOFETs has been recently reported.[34] However, the current on/off ratio of the device (>10^3) still has room for improvement. This is probably due to the relatively thick rGO electrode (approximately 6 nm thick), which is not beneficial for the Schottky barrier height modulation at the rGO/organic semiconductor interface. Therefore, the fabrication of ultrathin rGO electrode is necessary. Nevertheless, the unexfoliated graphite oxide bundles in GO dispersion always make the preparation of ultrathin rGO electrode a challenge. Moreover, as the device

Received: April 4, 2022
Accepted: June 16, 2022
Published: July 6, 2022

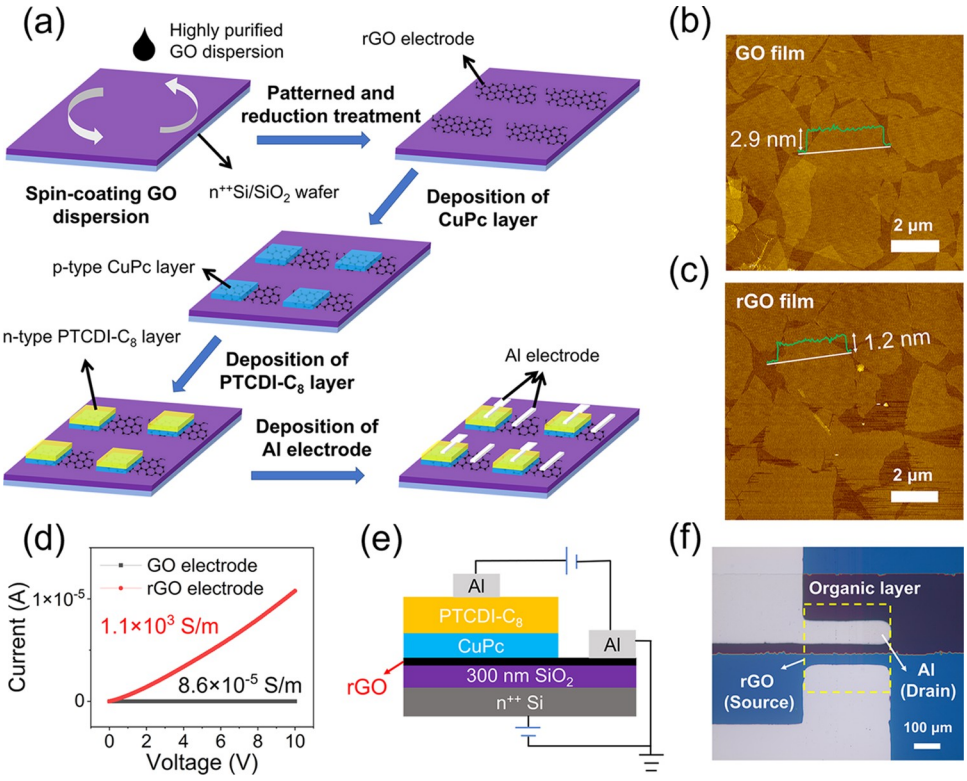


Figure 1. (a) Schematic of the device fabrication process. (b, c) AFM images of the GO and rGO films. (d) Conductivity of the GO and rGO electrodes. (e, f) Cross-sectional schematic and top-view optical image of the device.

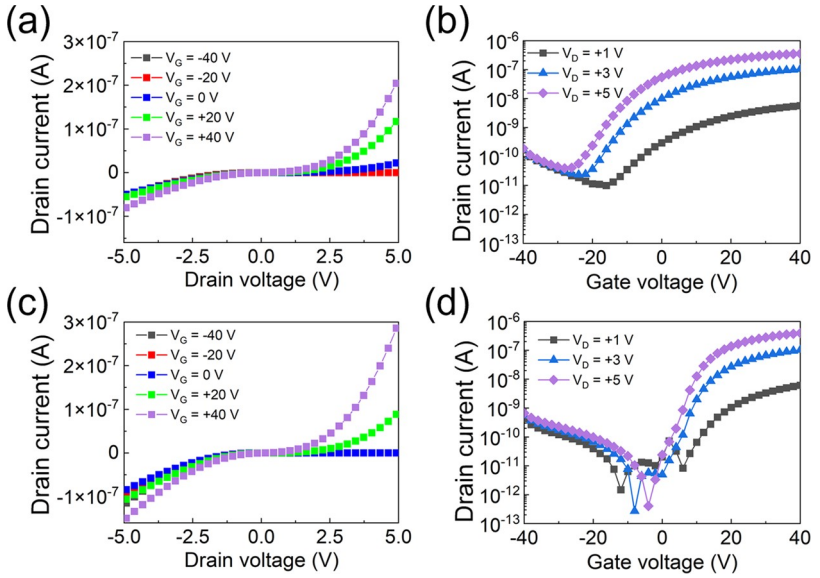


Figure 2. (a, b) Linear output and transfer characteristics of the normal rGO-VOFETs. (c, d) Linear output and transfer characteristics of the pn-rGO-VOFETs.

uses a single-type *N*,*N*′-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C_8) as the organic layer, the injection barrier height at the rGO/PTCDI-C_8 interface may not be sufficiently large to limit the off-current. This is a common problem in other graphene-based VOFETs.[9]

Hence, we fabricated pn-rGO-VOFETs based on a p−n junction of organic semiconductors on our proposed solution-processed rGO electrode. An ultrathin p-type copper (II) phthalocyanine (CuPc) interfacial layer was inserted between the rGO electrode and n-type PTCDI-C_8 layer. The high-lying lowest unoccupied molecular orbital (LUMO) level of CuPc could significantly reduce the off-current by forming a larger injection barrier height at the rGO/CuPc interface, generating the highest current on/off ratio exceeding 10^6. Notably, the effect of the p−n junction, not just the energy barrier, had an interesting impact on the threshold voltage (V_{th}) of the device.

2. RESULTS AND DISCUSSION

The fabrication process of the device is illustrated in Figure 1a. Briefly, a GO film was formed on an $n^{++}Si/SiO_2$ substrate using

https://doi.org/10.1021/acsomega.2c02085
ACS Omega 2022, 7, 24468−24474

a simple spin-coating approach. The rGO electrode was obtained after patterning and reduction treatments. The surface morphologies of the GO and rGO films were investigated using atomic force microscopy (AFM), as these films would be in close contact with the organic layer. A good surface morphology of the rGO film benefits the formation of a well interface. The AFM image of the GO film (Figure 1b) showed several discontinuous flakes, and the surface was highly uniform and smooth with a root-mean-square (RMS) roughness of 0.59 nm. The film thickness was ∼2.9 nm, suggesting that the GO film was approximately 3 layers because the thickness of the monolayer GO is around 1 nm.[11,26] The rGO film (Figure 1c) showed a similar smooth surface with an RMS of 0.54 nm. This indicated that the surface morphology was little changed after the reduction treatment. However, the thickness of the rGO film significantly decreased to ∼1.2 nm, which can be attributed to the detachment of the oxygen functional groups during the reduction process. The conductivity of the spin-coated GO electrode (Figure 1d) was rather low, i.e., only 8.6×10^{-5} S/m. By contrast, the conductivity of the rGO electrode was notably enhanced to 1.1×10^{3} S/m. Thus, our simple spin-coating and reduction method could effectively prepare an ultrathin rGO electrode with good electrical conductivity. More importantly, the obtained rGO electrode can be directly utilized as a work-function-tunable electrode without further processing.

We fabricated pn-rGO-VOFETs composed of p-type CuPc and n-type PTCDI-C_8 on this $n^{++}Si/SiO_2$/rGO substrate; 1-nm-thick CuPc, 500-nm-thick PTCDI-C_8, and 50-nm-thick Al electrode were sequentially deposited. A cross-sectional schematic and top-view optical image of the device are shown in Figure 1e,f, respectively. For comparison, normal rGO-VOFETs with only a 500-nm-thick PTCDI-C_8 without a CuPc layer were fabricated; the other parameters were the same as those of the former pn-rGO-VOFETs.

The electrical properties of the devices were tested at room temperature under dark and N_2 conditions. Figure 2a shows the linear output characteristics of the normal rGO-VOFETs without the p-type layer (drain current (I_D) versus drain voltage (V_D)) at different gate voltages (V_G). I_D increased as V_G increased positively, suggesting that the normal rGO-VOFETs were typical n-channel transistors. In addition, the asymmetric rectifying behavior was observed at the opposite side of V_D, with larger current modulation at the positive side than at the negative side. This asymmetric current modulation was attributed to the gate-tunable injection barrier height at the rGO/PTCDI-C_8 interface. At $V_D > 0$ V, electrons were injected from rGO to the LUMO of PTCDI-C_8; thus, the barrier height at the rGO/PTCDI-C_8 interface dominated electron transport. Under this circumstance, a positive V_G shifted the Fermi level (E_F) of rGO upward, thereby decreasing the barrier height. More electrons would be injected from rGO to the LUMO of PTCDI-C_8, and the device was in the "on" state. By contrast, a negative V_G moved the E_F of rGO downward, causing a larger barrier height for electron injection, and the device would be in the "off" state. While at $V_D < 0$ V, electrons were injected from the Al electrode to the LUMO of PTCDI-C_8, and the nearly fixed barrier height at the Al/PTCDI-C_8 interface resulted in a rather weak current modulation of the device.

Figure 2b shows the transfer characteristics of the normal rGO-VOFETs (I_D versus V_G). Both the on- and off-currents increased with increasing V_D because of the enhanced conductivity of the PTCDI-C_8 channel. However, the on-current increased more rapidly compared with the off-current, generating the highest current on/off ratio exceeding 10^4 at V_D = +5 V. The maximum current density was 0.73 mA/cm^2 at V_D = +5 V and V_G = +40 V. The results demonstrated that VOFETs based on this rGO source electrode could successfully operate. Nevertheless, conventional VOFETs that has a stable V_{th}. The V_{th} of the normal rGO-VOFETs exhibited a strange behavior that shifted from −15 to −28 V as V_D ranged from +1 to +5 V. In practical applications, such an unstable V_{th} is undesirable.

The carrier mobility of rGO-VOFETs cannot be measured from the I_D−V_G curves as the conventionally lateral OFETs because the operation of this device depends on the gate-tunable injection barrier height at the rGO/organic semiconductor interface. To investigate whether the current density of the device is limited by the carrier mobility, we evaluated the vertical electron mobility of the PTCDI-C_8 layer using the space-charge-limited current (SCLC) technique (Figure S1). The detailed process of the SCLC method was described in our previous report.[35] The calculated vertical electron mobility of the PTCDI-C_8 was 1.14×10^{-3} cm^2/(V s). Under this mobility, the theoretical current density of the PTCDI-C_8 layer was more than 400 mA/cm^2 at a voltage of +5 V, which was 3 orders of magnitude higher than that of the normal rGO-VOFETs (0.73 mA/cm^2). The results revealed that unlike conventionally lateral OFETs, the carrier mobility of the organic layer was not the main limiting factor for the current density of the normal rGO-VOFETs. Our further research suggested that the current density in the normal rGO-VOFETs was mainly related to the injection barrier height at the rGO/organic semiconductor interface and the whole resistance of the device.

To improve the current on/off ratio of the device further, we fabricated pn-rGO-VOFETs with a 1-nm-thick CuPc interfacial layer between the rGO electrode and the PTCDI-C_8 organic layer. The higher LUMO level of CuPc was expected to further limit the off-current in the device. In the linear output characteristics (Figure 2c), I_D increased as V_G increased positively, suggesting that electrons were the majority carriers in the device, which was the same as that of the normal rGO-VOFETs. In the transfer characteristics (Figure 2d), the off-current was significantly decreased by introducing the ultrathin p-type CuPc layer. Surprisingly, despite the larger injection barrier height at the rGO/CuPc interface, the on-current of the device did not decrease but increased slightly. The device exhibited a maximum current on/off ratio exceeding 10^6, which is also the largest value reported so far for VOFETs based on rGO electrode. More importantly, the V_{th} of the device, which decreased and stabilized at around 0 V, was also effectively improved. The electrical properties of the devices are listed in Table 1. These experimental results strongly indicated that the

Table 1. Electrical Properties of the Normal rGO-VOFETs and pn-rGO-VOFETs at V_D = +5 V

device	on-current density (mA/cm^2)	off-current density (mA/cm^2)	on/off ratio	V_{th} (V)
rGO-VOFETs	0.73 (±0.025)	7.14×10^{-5}	1.02×10^{4}	−28 (±1.24)
pn-rGO-VOFETs	0.79 (±0.027)	7.46×10^{-7}	1.06×10^{6}	−3 (±1.31)

https://doi.org/10.1021/acsomega.2c02085
ACS Omega 2022, 7, 24468−24474

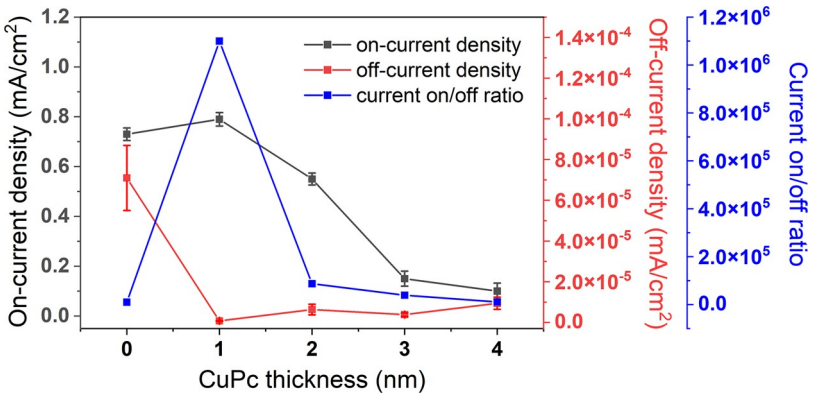


Figure 3. On-current density, off-current density, and current on/off ratio of the devices with different thicknesses of the CuPc interfacial layer at V_D = +5 V.

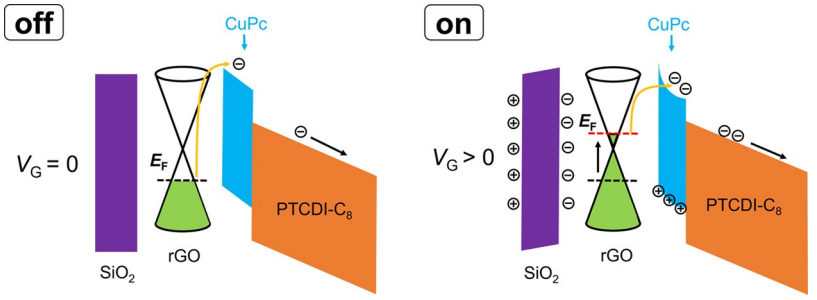


Figure 4. Schematic of the energy diagrams of the device at V_D > 0 V.

application of an ultrathin CuPc interfacial layer not only achieved a higher current on/off ratio but also improved the V_{th} of the device.

The energy level of the device was analyzed to investigate the effect of the ultrathin CuPc interfacial layer. The work function of the rGO electrode was estimated to be 5.3 eV using photoelectron yield spectroscopy (Figure S2). The LUMO level of PTCDI-C_8 is approximately 4.3 eV.[19] Due to the gate-tunable injection barrier height at the rGO/PTCDI-C_8 interface, I_D could be effectively modulated under different V_G at V_D > 0 V. When an ultrathin CuPc interfacial layer was applied, the higher LUMO level (3.5 eV) of CuPc was expected to limit both the on- and off-current densities of the device because of the intrinsically larger injection barrier height at the rGO/CuPc interface. Interestingly, only the off-current density was significantly restrained, whereas the on-current density of the device was slightly enhanced from 0.73 to 0.79 mA/cm^2. In addition, the V_{th} of the device was modified and stabilized at approximately 0 V. In this regard, the improvement in device performance cannot be simply explained by the high-lying LUMO level of the CuPc interfacial layer.

The stability and aging issue of the device are important factors for its future applications. The electrical properties of the devices (normal rGO-VOFETs and pn-rGO-VOFETs) were measured after 1 week and 1 month to evaluate the device stability and aging issue. The electrical properties of the devices were almost same after 1 week, with a slight decrease after 1 month. Notably, the electrical conductivity of the rGO electrode and Al electrode was very stable after 1 month, and thus the slight decrease in the device performance was mainly attributed to the degradation of the organic layer. It is a common problem for n-type OFETs because the electron is very sensitive to O_2 and H_2O in the atmosphere.[36] Although the aging issue seems to be unavoidable for this organic layer (PTCDI-C_8), it could be alleviated if the device is stored in a total inert atmosphere.

We further studied the electrical properties of the devices with different thicknesses of the CuPc interfacial layer. Here, 2-, 3- and 4-nm-thick CuPc layers were applied, and the electrical characteristics and properties of the devices are shown in Figure S3 and Table S1, respectively. The changing trends in the on-current density, off-current density, and current on/off ratio with the thickness of the CuPc interfacial layer are comprehensively illustrated in Figure 3. Only a 1-nm-thick CuPc interfacial layer could promote the on-current density. With a thicker CuPc interfacial layer (thickness of 2, 3, and 4 nm), the on-current density of the device gradually decreased. The off-current density could be effectively restrained by these CuPc layers, and the highest current on/off ratio exceeding 10^6 was generated with the 1-nm-thick CuPc interfacial layer.

In addition, a 1-nm-thick n-type organic semiconductor C_{60} was applied as an interfacial layer in the device to investigate whether it could have the same effect as the p-type CuPc layer (Figure S4). Notably, the LUMO level (4.0 eV) of C_{60} is higher than that of PTCDI-C_8 but lower than that of CuPc; therefore, if the C_{60} interfacial layer could also have such an effect, the on-current density of the device would be higher than that of the device with the CuPc interfacial layer. However, from the experimental results (Table S2), we can observe that both the on- and off-current densities were restrained for the device with a 1-nm-thick C_{60} interfacial layer. This result can be attributed to the larger injection barrier height at the rGO/C_{60} interface. Moreover, the V_{th} of the device was little modified. Therefore, the general band energy theory cannot fully explain the effect of the CuPc interfacial

https://doi.org/10.1021/acsomega.2c02085
ACS Omega 2022, 7, 24468−24474

layer. Obtaining a deeper understanding of the ultrathin CuPc interfacial layer in the device may be worthwhile.

Here, a plausible mechanism is proposed to explain the effect of the ultrathin CuPc interfacial layer based on the aforementioned experimental results and analysis. As schematically illustrated in Figure 4, when the device is in the "off" state (V_G < 0 V), the larger injection barrier height at the rGO/CuPc interface hinders the electron injection, and thus, the off-current density is significantly suppressed. On the contrary, when the device is in the "on" state (V_G > 0 V), the E_F of rGO would move upward and the injection barrier height may not be sufficiently large for electron injection. In addition, the positive gate voltage induces electrons on the opposite side of the SiO_2 insulator layer, which further induces holes on the surface of the p-type CuPc interfacial layer owing to the partial screening effect of the ultrathin rGO electrode.[1,25] The uniform distribution of holes on such an ultrathin CuPc layer causes the band bending of CuPc, which promotes electron injection through the tunneling effect. Due to these synergistic effects, the on-current density exhibited a slight increase after application of an ultrathin CuPc interfacial layer.

The improvement in the on-current density was limited only to the application of the 1-nm-thick ultrathin p-type CuPc interfacial layer. For devices with thicker CuPc interfacial layers (2, 3, and 4 nm), the on-current density gradually decreased. On the one hand, a thicker p-type CuPc interfacial layer inhibits electron transport. On the other hand, the tunneling effect can only occur in an ultrathin CuPc layer. Moreover, the on-current density of the device with 1-nm-thick ultrathin n-type C_{60} interfacial layer could not be enhanced. This is because the positive V_G could not induce sufficient holes on the surface of the n-type C_{60} layer and cause the band bending effect since the majority charge carriers in C_{60} are electrons.

We now discuss the modulation of V_{th} in these devices. For the normal rGO-VOFETs without the CuPc interfacial layer, V_{th} shifted more negatively with increasing V_D. This is because a higher drain electrical field assists electron injection into the PTCDI-C_8 layer and less elevation of E_F by V_G is required. When an ultrathin p-type CuPc interfacial layer was introduced, V_{th} gradually shrunk at approximately 0 V. By contrast, the n-type C_{60} interfacial layer cannot effectively modify V_{th}. As discussed above, only the positive V_G can induce sufficient holes on the surface of the p-type CuPc interfacial layer (such an effect is not available for the n-type C_{60} interfacial layer) and promote electron injection through the tunneling effect; therefore, the output current always rises at V_G = 0 V regardless of V_D. Hence, the V_{th} of the pn-rGO-VOFETs gradually decreased and stabilized at around 0 V.

3. CONCLUSIONS

We developed a promising spin-coating and reduction method to prepare an ultrathin rGO film that could be directly used as a work-function-tunable electrode in VOFETs. An ultrathin CuPc layer was applied at the rGO/PTCDI-C_8 interface. The introduced CuPc interfacial layer not only restrained the off-current density from 7.14×10^{-5} to 7.46×10^{-7} mA/cm^2, but also slightly promoted the on-current density from 0.73 to 0.79 mA/cm^2, generating the highest current on/off ratio of 1.06×10^6, which is the largest value reported so far for the rGO-based VOFETs. The applied CuPc interfacial layer also improved the V_{th} of the device, and the V_{th} of the pn-rGO-VOFETs gradually decreased and stabilized at approximately 0 V. The vertical electron mobility of the PTCDI-C_8 layer estimated by the SCLC method was 1.14×10^{-3} cm^2/(V s). However, it was not the main limiting factor for the current density in this device. We totally fabricated 48 devices, and more than 75% could work. Besides, the device was stable after 1 month with little performance degradation. The use of a low-cost, solution-processable rGO as a work-function-tunable electrode in VOFETs, along with the application of an ultrathin p-type CuPc interfacial layer, may bring new opportunities for future organic electronics.

4. EXPERIMENTAL SECTION

First, the substrate was ultrasonically cleaned in water, acetone, and IPA solution for 10 min each. Subsequently, it was dried under nitrogen flow and treated in a UV-O_3 cleaner for 20 min. A commercial GO dispersion (purchased from Graphenea) with a concentration of 4 mg/mL was highly purified via a series of centrifugation treatments and then diluted to 0.5 mg/mL. The highly purified GO dispersion (300 μL) was dripped onto an $n^{++}Si/SiO_2$ substrate and spin-coated at 500 rpm for 120 s, 1000 rpm for 30 s, and 2000 rpm for 30 s. The spin-coated GO film was then dried at 100 °C for 10 min and patterned manually. The patterned GO film was first chemically reduced under hydrazine monohydrate vapor and then thermally reduced at 300 °C for 6 h to obtain an rGO electrode. After that, 1-nm-thick p-type CuPc and 500-nm-thick n-type PTCDI-C_8 layers were deposited at the rates of 0.8 and 3 Å/s, respectively, through a shadow mask using vacuum deposition equipment. The vacuum pressure was under 4×10^{-4} Pa during the deposition of organic semiconductors. Finally, 50-nm-thick Al electrode was deposited at a rate of 8 Å/s under a vacuum pressure of 8×10^{-4} Pa through a shadow mask. The active area of the device was 50 000 μm^2, determined by the overlapping area of the rGO and top Al drain electrodes.

A total of 48 devices (half for normal rGO-VOFETs and half devices for pn-rGO-VOFETs) were fabricated, and more than 75% of the devices could stably work. There were 8 devices in one batch, and the 48 devices were fabricated in 6 batches. The same device performance was almost stable for different batches and different spatial locations because the same fabrication parameters such as deposition rate, vacuum pressure, and testing conditions were strictly kept. The error (standard deviation value) of the on-current density and V_{th} of the devices was calculated and is presented in Table 1. The errors for the on-current densities of the normal rGO-VOFETs and pn-rGO-VOFETs were ±0.025 and 0.027 mA/cm^2, respectively. The errors for the V_{th} of the normal rGO-VOFETs and pn-rGO-VOFETs were ±1.24 and 1.31 V, respectively.

The electrical characteristics of the devices were measured using a semiconductor parameter analyzer (Agilent 4155C) at room temperature in the dark and under dry N_2 conditions.

The $I-V$ curves of the GO and rGO electrodes were measured by a two-terminal method. First, the patterned GO and rGO electrodes were prepared on the $n^{++}Si/SiO_2$ substrate. Then, the Al electrode was deposited on the patterned GO and rGO electrode through a shadow mask using vacuum deposition equipment. The voltage was applied from 0 to 10 V, and the generated current was collected to obtain the $I-V$ curves of the GO and rGO electrodes.

The work function of the rGO film was measured using photoelectron yield spectroscopy under vacuum conditions. Briefly, 300 μL of highly purified GO dispersion was spin-

https://doi.org/10.1021/acsomega.2c02085
ACS Omega 2022, 7, 24468−24474

coated on an $n^{++}Si/SiO_2$ substrate. After drying and reduction treatment, an rGO film was formed on the $n^{++}Si/SiO_2$ substrate. The substrate was then fixed on a holder and placed in the chamber. After the vacuum level of the chamber reached 3×10^{-3} Pa, the measurement was started.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.2c02085.

J−*V* curves (Figure S1); work function measurement (Figure S2); electrical characteristics (Figures S3 and S4); and electrical properties (Tables S1 and S2) (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Ken-ichi Nakayama − *Division of Applied Chemistry, Graduate School of Engineering, Osaka University, Suita, Osaka 565-0871, Japan;* orcid.org/0000-0002-4176-3261; Email: nakayama@mls.eng.osaka-u.ac.jp

Authors

Kun Qiao − *Division of Applied Chemistry, Graduate School of Engineering, Osaka University, Suita, Osaka 565-0871, Japan*

Shun Arakaki − *Division of Applied Chemistry, School of Engineering, Osaka University, Suita, Osaka 565-0871, Japan*

Mitsuharu Suzuki − *Division of Applied Chemistry, Graduate School of Engineering, Osaka University, Suita, Osaka 565-0871, Japan;* orcid.org/0000-0002-0121-2561

Complete contact information is available at: https://pubs.acs.org/10.1021/acsomega.2c02085

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This research was supported by JSPS KAKENHI (JP17H03134 to K.N.).

■ REFERENCES

(1) Parui, S.; Ribeiro, M.; Atxabal, A.; Llopis, R.; Casanova, F.; Hueso, L. E. Graphene as an Electrode for Solution-Processed Electron-Transporting Organic Transistors. *Nanoscale* **2017**, *9*, 10178−10185.

(2) Li, H.; Shi, W.; Song, J.; Jang, H.-J.; Dailey, J.; Yu, J.; Katz, H. E. Chemical and Biomolecule Sensing with Organic Field-Effect Transistors. *Chem. Rev.* **2019**, *119*, 3−35.

(3) Lim, D. U.; Kim, S.; Choi, Y. J.; Jo, S. B.; Cho, J. H. Percolation-Limited Dual Charge Transport in Vertical p − n Heterojunction Schottky Barrier Transistors. *Nano Lett.* **2020**, *20*, 3585−3592.

(4) Liu, J.; Qin, Z.; Gao, H.; Dong, H.; Zhu, J.; Hu, W. Vertical Organic Field-Effect Transistors. *Adv. Funct. Mater.* **2019**, *29*, No. 1808453.

(5) Wang, C.; Zhang, X.; Dong, H.; Chen, X.; Hu, W. Challenges and Emerging Opportunities in High-Mobility and Low-Energy-Consumption Organic Field-Effect Transistors. *Adv. Energy Mater.* **2020**, *10*, No. 2000955.

(6) Devibala, P.; Balambiga, B.; Mohamed Imran, P.; Bhuvanesh, N. S. P.; Nagarajan, S. Butterfly-Like Triarylamines with High Hole Mobility and On/Off Ratio in Bottom-Gated OFETs. *Chem. - Eur. J.* **2021**, *27*, 15375−15381.

(7) Chen, H.; Zhang, W.; Li, M.; He, G.; Guo, X. Interface Engineering in Organic Field-Effect Transistors: Principles, Applications, and Perspectives. *Chem. Rev.* **2020**, *120*, 2879−2949.

(8) Yuvaraja, S.; Nawaz, A.; Liu, Q.; Dubal, D.; Surya, S. G.; Salama, K. N.; Sonar, P. Organic Field-Effect Transistor-Based Flexible Sensors. *Chem. Soc. Rev.* **2020**, *49*, 3423−3460.

(9) Kim, J. S.; Kim, B. J.; Choi, Y. J.; Lee, M. H.; Kang, M. S.; Cho, J. H. An Organic Vertical Field-Effect Transistor with Underside-Doped Graphene Electrodes. *Adv. Mater.* **2016**, *28*, 4803−4810.

(10) Dahal, D.; Paudel, P. R.; Kaphle, V.; Radha Krishnan, R. K.; Lüssem, B. Influence of Injection Barrier on Vertical Organic Field Effect Transistors. *ACS Appl. Mater. Interfaces* **2022**, *14*, 7063−7072.

(11) Huang, H.; Shi, H.; Das, P.; Qin, J.; Li, Y.; Wang, X.; Su, F.; Wen, P.; Li, S.; Lu, P.; Liu, F.; Li, Y.; Zhang, Y.; Wang, Y.; Wu, Z.; Cheng, H. The Chemistry and Promising Applications of Graphene and Porous Graphene Materials. *Adv. Funct. Mater.* **2020**, *30*, No. 1909035.

(12) Zhao, Z.; Bai, P.; Du, W.; Liu, B.; Pan, D.; Das, R.; Liu, C.; Guo, Z. An Overview of Graphene and Its Derivatives Reinforced Metal Matrix Composites: Preparation, Properties and Applications. *Carbon* **2020**, *170*, 302−326.

(13) Hlaing, H.; Kim, C.-H.; Carta, F.; Nam, C.-Y.; Barton, R. A.; Petrone, N.; Hone, J.; Kymissis, I. Low-Voltage Organic Electronics Based on a Gate-Tunable Injection Barrier in Vertical Graphene-Organic Semiconductor Heterostructures. *Nano Lett.* **2015**, *15*, 69−74.

(14) Bointon, T. H.; Jones, G. F.; De Sanctis, A.; Hill-Pearce, R.; Craciun, M. F.; Russo, S. Large-Area Functionalized CVD Graphene for Work Function Matched Transparent Electrodes. *Sci. Rep.* **2015**, *5*, No. 16464.

(15) Gao, S.; Wang, Z.; Wang, H.; Meng, F.; Wang, P.; Chen, S.; Zeng, Y.; Zhao, J.; Hu, H.; Cao, R.; Xu, Z.; Guo, Z.; Zhang, H. Graphene/MoS_2/Graphene Vertical Heterostructure-Based Broadband Photodetector with High Performance. *Adv. Mater. Interfaces* **2021**, *8*, No. 2001730.

(16) Choi, Y.; Kang, J.; Jariwala, D.; Kang, M. S.; Marks, T. J.; Hersam, M. C.; Cho, J. H. Low-Voltage Complementary Electronics from Ion-Gel-Gated Vertical Van Der Waals Heterostructures. *Adv. Mater.* **2016**, *28*, 3742−3748.

(17) Pyo, G.; Lee, G. J.; Lee, S.; Yang, J. H.; Heo, S. J.; Choi, G. H.; Cha, S.; Jang, J. E. Vertical Thin Film Transistor Based on Conductivity Modulation of Graphene Electrode by Micro-Hole Patterning. *Adv. Electron. Mater.* **2022**, *8*, No. 2101000.

(18) Kim, B. J.; Hwang, E.; Kang, M. S.; Cho, J. H. Electrolyte-Gated Graphene Schottky Barrier Transistors. *Adv. Mater.* **2015**, *27*, 5875−5881.

(19) Kim, J. S.; Choi, Y. J.; Woo, H. J.; Yang, J.; Song, Y. J.; Kang, M. S.; Cho, J. H. Schottky-Barrier-Controllable Graphene Electrode to Boost Rectification in Organic Vertical P-N Junction Photodiodes. *Adv. Funct. Mater.* **2017**, *27*, No. 1704475.

(20) Liu, Y.; Zhou, H.; Weiss, N. O.; Huang, Y.; Duan, X. High-Performance Organic Vertical Thin Film Transistor Using Graphene as a Tunable Contact. *ACS Nano* **2015**, *9*, 11102−11108.

(21) Pan, R.; Han, J.; Zhang, X.; Han, Q.; zhou, H.; Liu, X.; Gou, J.; Jiang, Y.; Wang, J. Excellent Performance in Vertical Graphene-C60-Graphene Heterojunction Phototransistors with a Tunable Bi-Directionality. *Carbon* **2020**, *162*, 375−381.

(22) Parui, S.; Pietrobon, L.; Ciudad, D.; Vélez, S.; Sun, X.; Casanova, F.; Stoliar, P.; Hueso, L. E. Gate-Controlled Energy Barrier at a Graphene/Molecular Semiconductor Junction. *Adv. Funct. Mater.* **2015**, *25*, 2972−2979.

(23) Yang, H.; Heo, J.; Park, S.; Song, H. J.; Seo, D. H.; Byun, K.-E.; Kim, P.; Yoo, I.; Chung, H.-J.; Kim, K. Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier. *Science* **2012**, *336*, 1140−1143.

(24) Zhu, Z.; Murtaza, I.; Meng, H.; Huang, W. Thin Film Transistors Based on Two Dimensional Graphene and Graphene/Semiconductor Heterojunctions. *RSC Adv.* **2017**, *7*, 17387−17397.

(25) Shih, C.-J.; Pfattner, R.; Chiu, Y.-C.; Liu, N.; Lei, T.; Kong, D.; Kim, Y.; Chou, H.-H.; Bae, W.-G.; Bao, Z. Partially-Screened Field Effect and Selective Carrier Injection at Organic Semiconductor/Graphene Heterointerface. *Nano Lett.* **2015**, *15*, 7587−7595.
(26) Tarcan, R.; Todor-Boer, O.; Petrovai, I.; Leordean, C.; Astilean, S.; Botiz, I. Reduced Graphene Oxide Today. *J. Mater. Chem. C* **2020**, *8*, 1198−1224.
(27) Yu, W.; Sisi, L.; Haiyan, Y.; Jie, L. Progress in the Functional Modification of Graphene/Graphene Oxide: A Review. *RSC Adv.* **2020**, *10*, 15328−15345.
(28) Sedki, M.; Mirabedini, P. S.; Nakama, K.; Stephens, G.; Groves, M.; Lee, I.; Neupane, M. R.; Mulchandani, A. Synthesis of Pristine Graphene-like Behaving RGO Thin Film: Insights into What Really Matters. *Carbon* **2022**, *186*, 437−451.
(29) Agarwal, V.; Zetterlund, P. B. Strategies for Reduction of Graphene Oxide − A Comprehensive Review. *Chem. Eng. J.* **2021**, *405*, No. 127018.
(30) Jiříčková, A.; Jankovský, O.; Sofer, Z.; Sedmidubský, D. Synthesis and Applications of Graphene Oxide. *Materials* **2022**, *15*, 920.
(31) Lim, D. U.; Choi, S.; Kim, S.; Choi, Y. J.; Lee, S.; Kang, M. S.; Kim, Y.-H.; Cho, J. H. All-Inkjet-Printed Vertical Heterostructure for Wafer-Scale Electronics. *ACS Nano* **2019**, *13*, 8213−8221.
(32) Samouco, A.; Marques, A. C.; Pimentel, A.; Martins, R.; Fortunato, E. Laser-Induced Electrodes towards Low-Cost Flexible UV ZnO Sensors. *Flexible Printed Electron.* **2018**, *3*, No. 044002.
(33) Carvalho, J.; Dubceac, V.; Grey, P.; Cunha, I.; Fortunato, E.; Martins, R.; Clausner, A.; Zschech, E.; Pereira, L. Fully Printed Zinc Oxide Electrolyte-Gated Transistors on Paper. *Nanomaterials* **2019**, *9*, 169.
(34) Choi, Y. J.; Kim, J. S.; Cho, J. Y.; Woo, H. J.; Yang, J.; Song, Y. J.; Kang, M. S.; Han, J. T.; Cho, J. H. Tunable Charge Injection via Solution-Processed Reduced Graphene Oxide Electrode for Vertical Schottky Barrier Transistors. *Chem. Mater.* **2018**, *30*, 636−643.
(35) Yamada, K.; Suzuki, M.; Suenobu, T.; Nakayama, K. High Vertical Carrier Mobilities of Organic Semiconductors Due to a Deposited Laid-Down Herringbone Structure Induced by a Reduced Graphene Oxide Template. *ACS Appl. Mater. Interfaces* **2020**, *12*, 9489−9497.
(36) Un, H.-I.; Zheng, Y.-Q.; Shi, K.; Wang, J.-Y.; Pei, J. Air- and Active Hydrogen-Induced Electron Trapping and Operational Instability in n-Type Polymer Field-Effect Transistors. *Adv. Funct. Mater.* **2017**, *27*, No. 1605058.

https://doi.org/10.1021/acsomega.2c02085
ACS Omega 2022, 7, 24468−24474