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Correspondence and requests for materials should be addressed to V.A.L.R. (val.roy@cityu.edu.hk)

Reversible Conversion of Dominant Polarity in Ambipolar Polymer/ Graphene Oxide Hybrids

Ye Zhou[1], Su-Ting Han[1], Prashant Sonar[2], Xinlei Ma[3], Jihua Chen[4], Zijian Zheng[3] & V. A. L. Roy[1,5]

[1]Department of Physics and Materials Science, City University of Hong Kong, Tat Chee Avenue, Kowloon Tong, Hong Kong SAR, China, [2]School of Chemistry, Physics and Mechanical Engineering, Queensland University of Technology (QUT), GPO Box 2434, Brisbane, QLD 4001, Australia, [3]Nanotechnology Center, Institute of Textiles and Clothing, The Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong SAR, China, [4]Center for Nanophase Materials Sciences, Oak Ridge National Laboratory, Oak Ridge, TN 37831, USA, [5]Shenzhen Research Institute, City University of Hong Kong, High-Tech Zone, Nanshan District, Shenzhen, 518057, China.

The possibility to selectively modulate the charge carrier transport in semiconducting materials is extremely challenging for the development of high performance and low-power consuming logic circuits. Systematical control over the polarity (electrons and holes) in transistor based on solution processed layer by layer polymer/graphene oxide hybrid system has been demonstrated. The conversion degree of the polarity is well controlled and reversible by trapping the opposite carriers. Basically, an electron device is switched to be a hole only device or vice versa. Finally, a hybrid layer ambipolar inverter is demonstrated in which almost no leakage of opposite carrier is found. This hybrid material has wide range of applications in planar p-n junctions and logic circuits for high-throughput manufacturing of printed electronic circuits.

Over the past few years materials with balanced charge carrier transport have received special interest owing to their potential applications in light emitting transistors[1–3], complementary metal oxide semiconductor (CMOS)-like logic circuits[4–6], sensors[7–9], spintronics[10] and memories[11,12]. On this aspect, the possibility to selectively modulate the charge carrier transport in semiconducting materials is extremely attractive for the development of high performance and low-power consuming ambipolar logic circuits with low leakage currents[13–15]. Independent control over charge transport is also quite important for light-emitting transistors[16]. Several approaches have been developed to control the charge injection and transport such as interface modification[17–19], split-gate[20], dielectric selection[21], exposition to oxygen[22], introduction of buffer layers[23,24], doping of other materials[25] or thermal treatment[26–28]. However, most of the methods always require a systematical selection of materials and conditions to obtain a reliable result, and cannot be a collective approach for various structures. On the other hand, these approaches cannot switch the charge transport reversibly and dynamically in a controlled manner. Therefore, exploring a simple and universal technique to achieve reversible charge transport (from holes to electrons vice versa) is attractive for wide variety of applications. A balanced charge transport can be achieved by bilayer heterostructures, blended material systems or single component materials[29–34]. Among these strategies, polymeric semiconductors are highly promising and attractive due to their large scale solution processability[35,36] and the cost-effective device fabrication procedure by using one single type of electrode[37,38]. To achieve ultimate success of practical polymer devices, a large number of efforts have been devoted to the synthesis of novel polymers, the development of new processing methods and the interface engineering in device architecture[39]. To achieve controlled charge transport in semiconducting polymers, introducing charge trapping sites with the following properties can be an effective approach: i) flattened surface with good interface quality with polymer; ii) large area with plenty of trapping sites; iii) easy processability with polymer to form hybrids. Graphene oxide (GO), the insulating analog of graphene, is a nonstoichiometrically oxidized sheet derived from the acid exfoliation of graphite[40]. The high density of oxygen-containing groups, planar structure with atom-thickness and excellent solution processabbility make chemically synthesized GO extremely promising as functional trapping layer in polymer bilayer hybrids.

Here we report a novel approach on systematic control over polarity (from holes to electron or vice versa) in transistors based on solution processed semiconducting polymer/GO hybrid system. Recently, diketopyrrolopyrrole (DPP) based polymers with planar conjugated bicyclic structure have shown some of the highest

mobilities and got particular interest for low-cost functional electronic devices including transistors, logic circuits and photovoltaics[41–43]. Poly (diketopyrrolopyrrole-thiophene-benzothiadiazole-thiophene) (PDPP-TBT) is chosen in this work due to its high and balanced hole/electron mobilities[44]. The DPP and TBT blocks can improve intermolecular interactions to form π-π stacks with a large overlapping area and ordered molecular organization[45,46]. By inserting the solution processable GO sheets between the polymer and gate dielectric, the majority carrier type in the polymer could be dynamically switched from one type to another with applied programming gate bias. The conversion degree of the polarity is well controlled by the gate bias. To the best of our knowledge, this is the first report in which the charge transport is actively switched in a transistor in a control manner by using the polymer/GO bilayer structure. High performance ambipolar-like inverter has also been fabricated based on the hybrid transistors with controlled and reversible polarity. Our proposed architecture provides a powerful way to achieve charge conversion of one polarity to another in a controlled manner and thereby relaxing the demands of materials choice in various applications such as planar p-n junctions and ambipolar-like logic circuits.

Results

Polymer/GO ambipolar device structure. Fig. 1a show the schematic illustration of the PDPP-TBT/GO hybrids adopted in the transistor structure. GO is a layered stack of puckered sheets consisting of graphene like aromatic domains of random sizes, which are decorated by epoxy, diol, hydroxyl, ether and carboxy groups[47,48]. GO suspensions were prepared according to the Hummers method with pure graphite followed by exfoliation under untrasonication[49]. The atomic force microscopy (AFM) image of the synthesized GO sheet is illustrated in Supplementary Figure 1, with thickness of around 1.5 nm. Large-area uniform GO thin films were prepared by a simple spin-casting process. The degree of oxidation of graphite oxide was confirmed by XPS and the survey spectra for graphite oxide yielded C/O atomic ratios of ~2.2 as shown in Supplementary Figure 2. The Raman spectrum of the deposited GO is shown in Supplementary Figure 3. The schematic demonstration of the PDPP-TBT on GO is also shown in Fig. 1a. Transmission electron microscopy (TEM) analysis was conducted by depositing drop casted film of PDPP-TBT on carbon coated grids. TEM images and corresponding selected area electron diffraction (SAED) pattern (inset) for PDPP-TBT film annealed at 140 degree Celsius are shown in Fig. 1b. TEM images exhibit a fibrous morphology of the polymer which clearly indicates the strong intramolecular interaction. The outer ring in the SAED pattern of the film attributes to a d-spacing of 0.36 nm, which is probably due to the pi-pi stacking distance of the PDPP-TBT chains. Fig. 1c shows the tapping mode AFM image of the GO film, displaying a uniform coverage with overlaid sheets of GO. In addition, surface root-mean-square roughness (R_{rms}) value of the GO film is determined to be 1.35 nm in area of 3×3 μm^2. The Raman spectrum of the deposited GO is shown in Supplementary Figure 2 and the band-intensity ratio I_D/I_G is about 0.96. The 30-nm-thick PDPP-TBT film was subsequently spin-casted above the GO layer and annealed at 140°C for 30 mins in nitrogen environment. To elucidate the molecular packing structure of PDPP-TBT on GO, grazing incidence X-ray diffraction (GIXRD) analysis was carried out. The crystallinity of the polymer film spin-coated on GO layer is not disturbed much as shown in Fig. 1d. The spin-cast thin film exhibits a strong primary diffraction peak at $2\theta = 4.14°$, corresponds to a *d*-spacing of 21.3 Å. The XRD patterns demonstrate the highly ordered lamellar packing of the polymer on GO with an edge-on orientation. The AFM images of the PDPP-TBT films grown on SiO_2 and GO-coated SiO_2 are shown in Fig. 1e and 1f. Both of the spin-cast thin films show uniform structures with fine grains with no obvious differences of surface morphology. Over all, the results suggest that the molecular packing of PDPP-TBT fundamentally remains unchanged when depositing on GO layer. The ambipolar transistors were fabricated on a heavily doped Si wafer (served as the gate electrode) with a thermally grown 100 nm thick SiO_2 layer (worked as the gate dielectric). The PDPP-TBT/GO hybrids were bridged between two gold electrodes (source and drain) on top of the dielectric layer in a bottom-contact bottom-gate geometry. Further details on the device fabrication could be found at the Method section. The PDPP-TBT has a lowest unoccupied molecular orbital (LUMO) level of 4.0 eV and highest occupied molecular orbital (HOMO) level of 5.2 eV, and Au has a Fermi

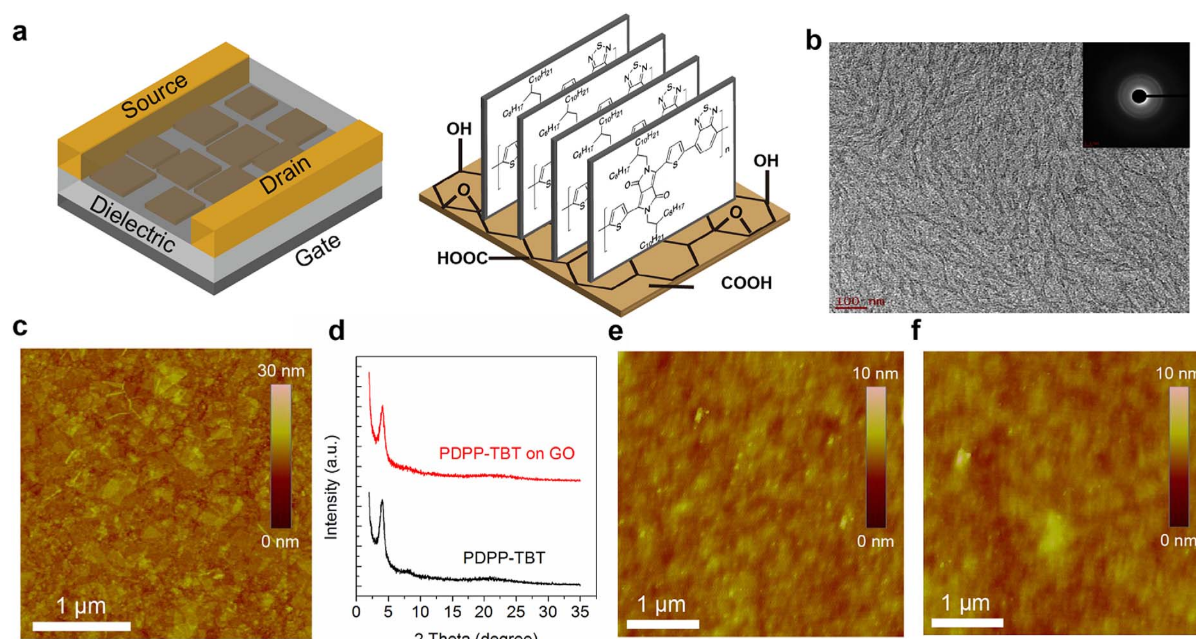

Figure 1 | Polymer/GO based ambipolar transistor. (a) Schematic illustration of the PDPP-TBT/GO hybrids adopted in the transistor structure. (b) TEM image and SAED pattern of the polymer. Scale bar, 200 nm. (c) AFM image of the GO layer. (d) XRD patterns of the polymer and polymer/GO hybrids. Scale bar, 1 μm. (e) AFM image of the polymer on SiO_2. Scale bar, 1 μm. (f) AFM image of the polymer on GO. Scale bar, 1 μm.

level in the range of 4.7–5.2 eV, therefore a low bandgap polymer is suitable as ambipolar semiconductor for hole and electron injection[44,50,51].

Electrical characteristics of the transistor. The typical output characteristics of the transistors based on PDPP-TBT/GO hybrids are shown in Fig. 2a and 2b. At both high positive and negative gate–source voltage (V_{GS}), saturation of the drain-source current (I_{DS}) is observed, indicating electrons and holes are accumulated at the respective V_{GS}. A slight reduction of I_{DS} occurred at high V_{DS} in electron-enhancement mode, which may be attributed to the polymer/GO interface electron trapping under large V_{GS}. At low V_{GS}, the transistors show diode-like curves with a rapid increase of I_{DS} with V_{DS}, which is a typical behavior of ambipolar transistors due to the Schottky barrier at the junctions between source/drain to the channel[52]. Fig. 2c and 2d clearly show the V-shape transfer curves in both hole-enhancement and electron-enhancement modes. The mobility was calculated at the saturation regime using the following equation: $I_{DS} = (W/2L)\,\mu C_i(V_{GS} - V_T)^2$, where I_{DS} is the drain-source current, W and L are the channel width and length, μ is the mobility, C_i is the capacitance per unit area of the gate dielectric and V_T is the threshold voltage. The hybrids exhibits a maximum hole mobility of 1.1×10^{-2} cm^2 V^{-1} s^{-1} and an electron mobility of 1.2×10^{-2} cm^2 V^{-1} s^{-1}. To investigate the degree of charge trapping, the corresponding density of traps (N_{SS}) were extracted using the equation: $N_{SS} = SS \log e/(kT/q - 1)(C_i/q)$, where SS is the sub-threshold slope, k is the Boltzmann's constant, T is the absolute temperature and q is the fundamental unit of charge[53]. The value of SS of the hole-enhancement mode and electron-enhancement mode were 17.2 and 21.6 V/decade, respectively. The calculated values of N_{SS} were 8.8×10^{12} and 1.1×10^{13} cm^{-2}, respectively.

Polarity conversion. Different voltage pulses were applied to the gate to control the device polarity before the measurements. For measuring the transfer curve at the hole-enhancement mode, V_{DS} was set as −30 V and V_{GS} was swept from 0 V to −30 V. For measuring the transfer curve at the electron-enhancement mode, V_{DS} was set as 30 V and V_{GS} was swept from 0 V to 30 V. The comparison between the transfer curves, as shown in Fig. 3a to 3d, provides a clear evidence of control over ambipolar (superimposition of both electrons and holes) properties of the transistors by the pre-applied gate bias. Fig. 3a shows the transfer characteristics at hole-enhancement mode after applying −40 V at the gate for various durations. The negatively shifted switch-on voltages indicate that more and more holes are trapped in the process and the potential evolves from these traps screens the gate voltage. When a positive (+40 V) bias is pre-applied to the gate and the switch-on voltage shifted towards the positive direction as shown in Fig. 3b. Due to the positive bias, the stored holes are neutralized by electrons and eventually electrons are trapped in the GO layer. The origin of charge carrier trapping in the hybrid materials is attributed to the inherent structural defects in chemically synthesized GO and the insulating gap of oxidized GO domains originated from the oxygenated functional group[54–56]. The ambipolar charge transport is controlled by the amount and polarity of trapped charges by GO. The trapped charge carriers in GO can screen the gate voltage and the switch-on voltage can be manipulated according to the

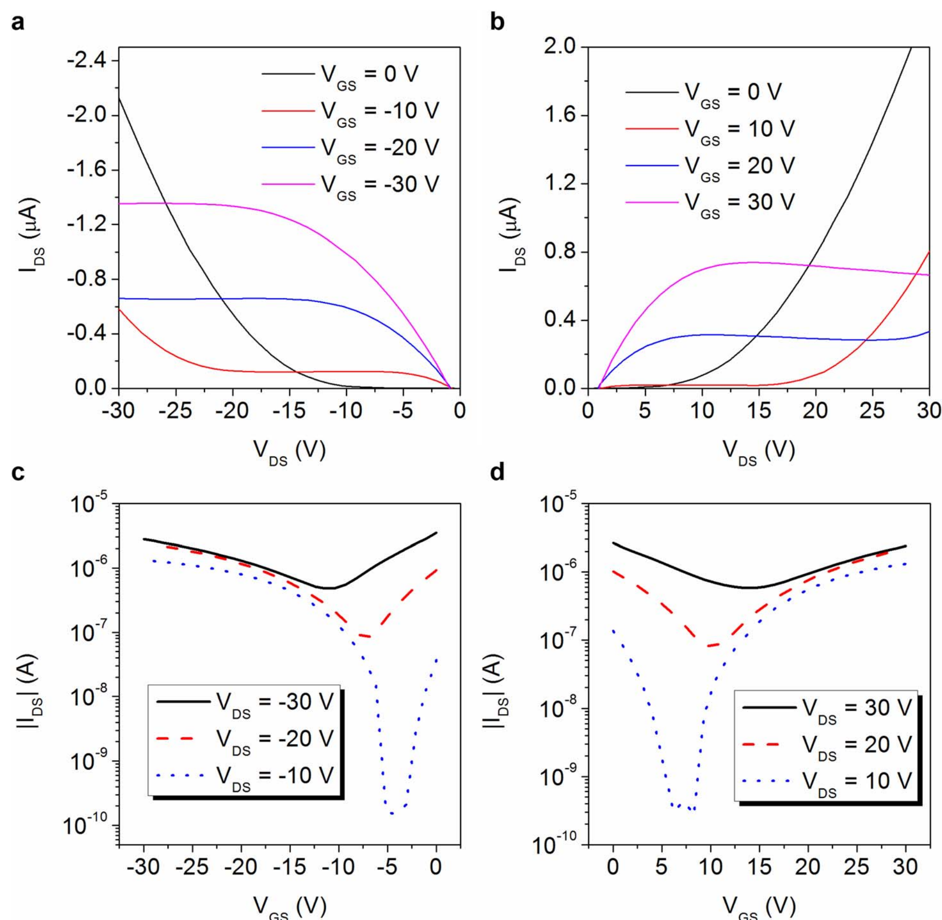

Figure 2 | Electrical performances of the polymer/GO transistor. (a) Output characteristics of the hybrids at hole-enhancement mode. (b) Output characteristics of the hybrids at electron-enhancement mode. (c) Transfer characteristics of the hybrids at hole-enhancement mode. (d) Transfer characteristics of the hybrids at electron-enhancement mode.

Figure 3 | **Dominant polarity conversion.** (a) Transfer characteristics of the hybrids at hole-enhancement mode ($V_{DS} = -30$ V) after negative gate pulse. (b) Transfer characteristics of the hybrids at hole-enhancement mode ($V_{DS} = -30$ V) after positive gate pulse. (c) Transfer characteristics of the hybrids at electron-enhancement mode ($V_{DS} = 30$ V) after positive gate pulse. (d) Transfer characteristics of the hybrids at electron-enhancement mode ($V_{DS} = 30$ V) after negative gate pulse. (e) Schematic illustration of the hole/electron trapping process. (f) Schematic illustration of the electron/hole trapping process. (g) SKPM image of the hole/electron trapping process. (h) SKPM image of the electron/hole trapping process.

polarity of the trapped charge carriers. The major charge carriers during operation can be determined with controlled switch-on voltage. A pre-applied −40 V gate pulse can induce an electron-rich device, and a pre-applied +40 V gate pulse can induce a hole-rich device. The schematic illustration of the mechanism is shown in Supplementary Figure 4. The transfer characteristics at the electron-enhancement mode have also been investigated as shown in Fig. 3c and 3d. The gate was biased by various durations of +40 V to trap the electrons at the GO layer. After the application of −40 V at the gate, the holes are hopping from the polymer to GO in order to compensate the trapped electrons. Further increase of gate bias time results in hole trapping and the transfer curves shift towards more negative direction. With selective voltage pulse programmed at the gate electrode, dominant p-type or n-type transport can be achieved in the ambipolar hybrid transistors. The device without GO was also fabricated as a control device and did not exhibit controlled transport using the same approach and the results are shown in Supplementary Figure 5. In order to further confirm this approach in general to any ambipolar polymer, a hybrid transistor using poly{3,6-difuran-2-yl-2,5-di(2-octyldodecyl)-pyrrolo[3,4-*c*]pyrrole-1,4-dione-alt-benzothidiazole} (PDPP-FBF)[57] based on the same device structure has been fabricated as shown in Supplementary Figure 6. The electrical characteristics of the ambipolar transistor are included in Supplementary Figure 7, and the hybrid transistor exhibits reliable and reversible conversion of the major charge carrier transport. The results shown here clearly demonstrate that the GO based bilayer hybrid structure is an efficient tool to manipulate the charge transport in an ambipolar semiconductor.

The working mechanism is schematically shown in Fig. 3e and 3f. The density of trapped holes and electrons in the conversion process is estimated from the equation $Q = C\Delta V_{th}$, where C is the capacitance per unit area and ΔV_{th} is the threshold voltage shift. The ΔV_{th} was 21.6 V for the electron-enhancement mode and 17.1 V for the hole-enhancement mode. The total density of traps density was found to be 4.7×10^{12} cm^{-2} for the electron-enhancement mode and 3.7×10^{12} cm^{-2} for the hole-enhancement mode. The high

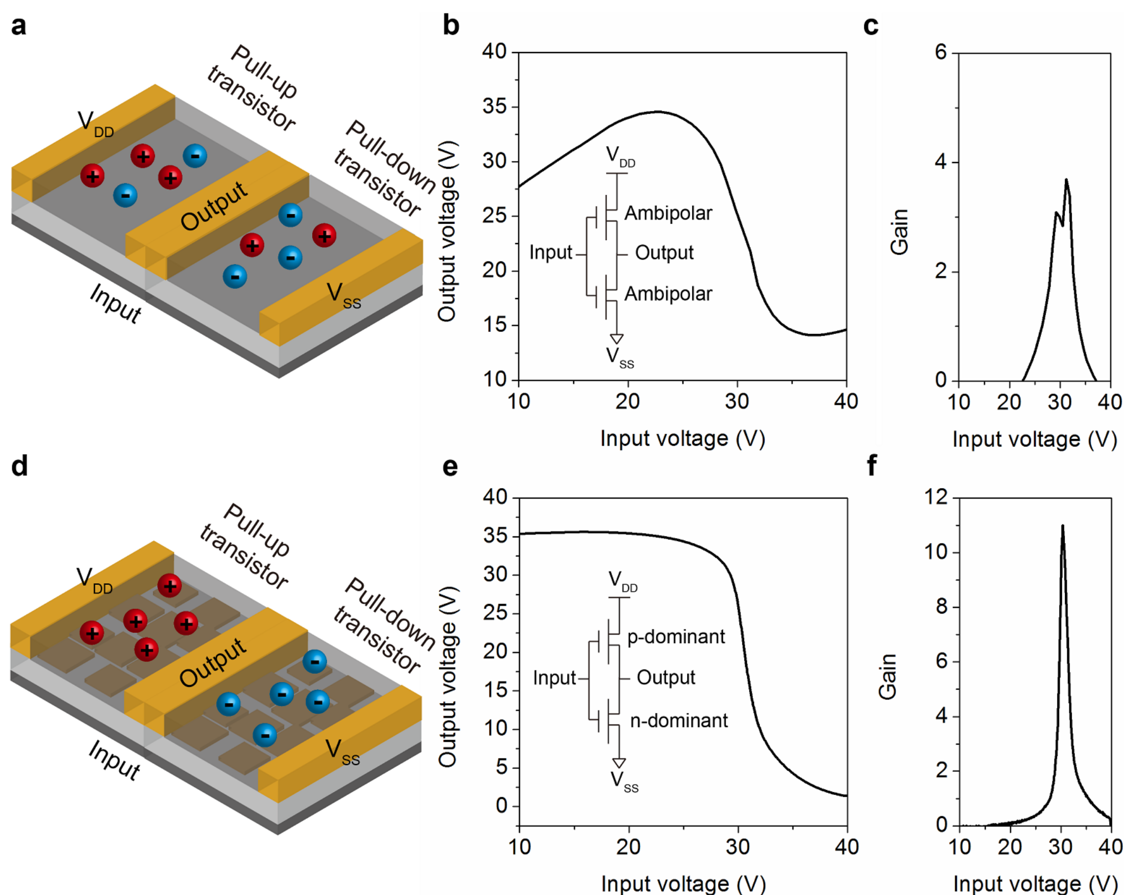

Figure 4 | Ambipolar inverters. (a) Schematic illustration of the PDPP-TBT based inverter. (b) Voltage transfer curve of the PDPP-TBT based inverter. (c) Signal gain of the PDPP-TBT based inverter. (d) Schematic illustration of the PDPP-TBT/GO based inverter. (e) Voltage transfer curve of the PDPP-TBT/GO based inverter. (f) Signal gain of the PDPP-TBT/GO based inverter.

density of charge traps indicates that large amounts of oxygen trap centers exit in the chemically synthesized GO thin films, which lead to efficient charge trapping and de-trapping of the hybrid films. In order to investigate the charge trapping ability of GO, scanning Kelvin probe microscopy (SKPM) was used for real-space imaging of hole and electron trapping states. Charges stored within the GO are detected from the changes in the surface potential and the detailed measuring methods can be found at the experimental section. The charge injection operation was first performed within an area of 4×4 μm² with +6 V bias applied at the tip and holes were confined in the GO. In the following process, the center 1×1 μm² was scanned by applying a −6 V bias. During this process, the originally trapped holes recombine with electrons and electron trapping occurs. Fig. 3g shows a typical real-space SKPM image of hole trapping states followed by electron trapping states. The yellow region identifies hole trapping state and dark region corresponds to electron trapping state. The potential difference between the two states was measured to be approximately 575 mV. The SKPM image of electron trapping states followed by hole trapping states is shown in Fig. 3h. A −6 V bias at the tip trapped the electrons within an area of 4×4 μm² followed by the scanning of the center 1×1 μm² with a +6 V bias to form hole trapping states. The potential difference between the two states was measured to be about 590 mV. These results show that GO can act as efficient hole/electron trapping elements and enables a wide range of traps in our device. The trapped charge carriers can remain inside the GO for more than 1 hour after the applied bias has been removed, resulting in a stable conversion of dominant polarity in the hybrid transistors.

Ambipolar inverter. In order to demonstrate the application of dominant polarity conversion in logic circuits, we constructed an ambipolar inverter based on the ambipolar transistors. Two identical ambipolar transistors are combined with a common gate as the input and a common drain as the output as shown in Fig. 4a. The voltage transfer characteristic (VTC) of the inverter with only PDPP-TBT is shown in Fig. 4b and the signal gain ($-dV_{OUT}/dV_{IN}$) is shown in Fig. 4c. Typical Z-shaped VTC was observed in the PDPP-TBT inverter, since both the pull-down (n-channel) transistor and pull-up (p-channel) transistor could not be switched off at low and high input voltage values. This will result in high static power consumption and limited noise margins compared with conventional complementary logic circuits[58,59]. Therefore, it is crucial to achieve unipolar operation in the p-channel and n-channel ambipolar transistors. We further applied the PDPP-TBT/GO hybrid transistors in the inverter structure as illustrated in Fig. 4d. The p-channel transistor was programmed with +40 V at gate for 10 s and the n-channel transistor was programmed with −40 V at gate for 10 s. The VTC and signal gain of the hybrid inverter are shown in Fig. 4e and 4f. The inverter exhibits clearly an improved static performance with large signal gain and sharp switching with rail-to-rail output swings, which is comparable with other reported inverters[60,61]. The realization of dominant p-type transport in pull-up transistor and dominant n-type transport in pull-down transistor play an important role in fabricating high performance ambipolar inverters. Further improvement of the ambipolar inverter's performance can be realized by systematical tuning of the pull-up and pull-down transistor with matched switch-on voltage.

Discussion

We have demonstrated an innovative way to manipulate the charge transport properties of ambipolar polymers by GO. The GO influences the majority carrier transport in the transistor operation when acting as electron/hole trapping site. The majority carrier type in the ambipolar polymer could be dynamically switched from one type to another with applied programming gate bias. The device works in a charge trapping mechanism and the electron/hole trapping ability has been confirmed by SKPM. High performance ambipolar inverter has been fabricated from the PDPP-TBT/GO hybrid transistors with well controlled dominant polarity. We believe that this method offers a versatile opportunity to achieve conversion of polarity in a controlled manner. The ambipolar polymer/GO hybrids would become potentially useful for high-throughput manufacturing of printed circuits for a wide range of electronic applications.

Methods

Materials. All chemicals were obtained from Aldrich and used without further purification. Detailed synthetic procedures for the preparation of PDPP-TBT and PDPP-FBF have been published previously[44,57].

Fabrication of ambipolar transistors. A highly doped silicon wafer with a thermally grown 100-nm-thick SiO_2 layer was utilized as the substrate for transistors. The 100-nm-thick gold source/drain electrodes were patterned by photolithography. The active channel length and width were 10 μm and 3000 μm, respectively. The wafers were subjected to cleaning using ultrasonication in acetone, iso-propanol and de-ionized water. The substrates were then dried under a nitrogen flow and treated in UV-ozone for 15 min before use. GO was synthesized by the Hummers method and exfoliated under ultrasonication to yield a brown dispersion of GO in water. The GO thin film was deposited on the cleaned substrate by spin-casting at 3000 rpm for 30 s from the prepared GO suspension (1 mg/ml). Next, the substrates were transferred into a nitrogen glove box for all subsequent processing steps. The PDPP-TBT was spin-casted from chloroform (7 mg/ml) on GO and then annealed at 140°C for 30 min. The PDPP-FBF was spin-casted from the polymer solution in chloroform (8 mg/ml) and subsequently annealed at 140°C for 30 min.

Characterization. The electrical characteristics were recorded in a nitrogen-filled glove box by using a Keithley 2612 source meter and 2400 source meter. Surface morphologies of the deposited films were studied using an atomic force microscope (AFM, Veeco Multimode V) in the tapping mode. The grazing incidence X-ray diffraction (GIXRD) patterns of PDPP-TBT films were recorded using an X-ray diffractometer (Rigaku SmartLab). Irradiation of parallel $CuK_{\alpha1,2}$ X-ray beam was fixed at a grazing incident angle of 0.5° and the detector was independently moved to collect the diffraction data with a step-size of 0.02°. The SKPM was performed in the AFM system (Bruker NanoScope 8) with metalized probes based on previous work[62]. Heavily n-doped Si wafers were used as the substrates and the GO were sandwiched between 30 nm thick Al_2O_3 and 10 nm thick PMMA. Al_2O_3 were deposited using a Savannah 100 atomic layer deposition (ALD) system at a substrate temperature of 80°C. PMMA films were spin-casted on top of GO from a solution containing 3 mg/ml PMMA in toluene and then annealed at 120°C for 1 hr. Potential images were realized under the lift-mode with a pre-defined lift height of 50 nm.

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Author contributions

Y.Z. and S.T.H. performed the experiments and wrote the paper. P.S. synthesized the polymer. X.M. and Z.Z. assisted with kelvin probe measurements. J.C. did the TEM measurements. V.A.L.R. acquires the idea, supervised the project and finalized the manuscript.

Additional information

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