Article

Analysis for DC and RF Characteristics Recessed-Gate GaN MOSFET Using Stacked TiO_2/Si_3N_4 Dual-Layer Insulator

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Abstract: The self-heating effects (SHEs) on the electrical characteristics of the GaN MOSFETs with a stacked TiO_2/Si_3N_4 dual-layer insulator are investigated by using rigorous TCAD simulations. To accurately analyze them, the GaN MOSFETs with Si_3N_4 single-layer insulator are conducted to the simulation works together. The stacked TiO_2/Si_3N_4 GaN MOSFET has a maximum on-state current of 743.8 mA/mm, which is the improved value due to the larger oxide capacitance of TiO_2/Si_3N_4 than that of a Si_3N_4 single-layer insulator. However, the electrical field and current density increased by the stacked TiO_2/Si_3N_4 layers make the device's temperature higher. That results in the degradation of the device's performance. We simulated and analyzed the operation mechanisms of the GaN MOSFETs modulated by the SHEs in view of high-power and high-frequency characteristics. The maximum temperature inside the device was increased to 409.89 K by the SHEs. In this case, the stacked TiO_2/Si_3N_4-based GaN MOSFETs had 25%-lower values for both the maximum on-state current and the maximum transconductance compared with the device where SHEs did not occur; R_{on} increased from 1.41 mΩ·cm^2 to 2.56 mΩ·cm^2, and the cut-off frequency was reduced by 26% from 5.45 GHz. Although the performance of the stacked TiO_2/Si_3N_4-based GaN MOSFET is degraded by SHEs, it shows superior electrical performance than GaN MOSFETs with Si_3N_4 single-layer insulator.

Keywords: gallium nitride (GaN); aluminum gallium nitride (AlGaN); self-heating effect (SHE); dual-layer insulator; silicon nitride (Si_3N_4); titanium dioxide (TiO_2); sapphire; silicon carbide (SiC); radio frequency (RF)

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1. Introduction

Silicon (Si) is widely used in the semiconductor industry as it is a material with very stable physical properties. However, recognizing the band gap limit, the research on compound semiconductors such as gallium nitride (GaN) that can be used stably at high voltage and high frequency is considered to be an important topic [1–3]. The AlGaN/GaN-based high-electron-mobility transistor (HEMT) is suitable for power switching applications. The two-dimensional electron gas (2DEG) formed between AlGaN and GaN layers results in a high switching speed, low on-resistance, large current handling capabilities, and high breakdown voltage [4,5]. In addition, it has long been established as a promising candidate for high-frequency operation because the high saturation velocity of the electrons significantly enhances the transport properties [6]. Overall, although HEMT devices operate in enhancement-mode, the normally off operation is more appropriate for GaN-based transistors to target high-voltage power switching applications for fail-safe requirements

and to simplify the design of driving circuits. Methods for normally off operations include gate-recess etching, fluorine plasma ion implantation, the p-type doped gate structure, and the gate-controlled tunnel junction, which has been proven to be capable of normally off operations [7–10]. Furthermore, HEMTs with a thin gate-insulator have a suppressed leakage current and high reliability due to their improved interface quality [11,12].

However, when the GaN devices operate at a high voltage region, the self-generated heat lowers the maximum power density and accelerates device failure [13]. The self-heating effects (SHEs) cause phonon scattering by increasing channel temperature, which limits the overall performance such as breakdown voltage, gate-leakage current, stability, and negatively sloped saturation curve. Thus, it is important to investigate and analyze models related to thermal behavior [14,15].

In our previous study, we compared the DC characteristics of recessed-gate MIS-HEMTs based on the variation of the Si_3N_4, TiO_2 insulator thickness and demonstrated that the application of an appropriate combination of two materials improves the device's DC electrical characteristics [16]. Further, detailed adjustments to the simulation parameters and models were performed, and it was examined that the results were observed to be the same in general. Although SHEs were applied, a thorough investigation of heat generation and RF properties for use in power amplifier applications were not included.

In conclusion, in this study, we compare the DC performance changes in GaN MOSFET using the stacked TiO_2/Si_3N_4 dual- or Si_3N_4 single-layer insulator depending on whether the SHEs is applied and analyze the operation at a large RF frequency, which is expected to change due to dispersion of temperature, considering the thermal mechanism. In terms of SHEs, the most critical factor in determining the level of thermal rise inside a device is the thermal conductivity of each material used for device fabrication. When a device is made of a material with high thermal conductivity, heat generated spontaneously during operation can easily escape to the outside, which suppresses the device's performance degradation [17]. Therefore, for the proposed device structure, we also experiment to explore the tendency and sensitivity of the performance change when materials with different thermal conductivities are used as substrates.

2. Materials and Methods

Figure 1 shows the cross-section of GaN MOSFET based on AlGaN/GaN heterostructure with a dual-layer insulator comprising Si_3N_4/TiO_2 (10/20 nm thickness) under the recessed gate. The single-layer insulator in the device compared with the proposed structure has only a 30 nm thick Si_3N_4, and all other details and conditions are the same. The length of the gate head (L_G) is 2 μm and the length from the gate to the source and drain is 5 μm each (L_{GS} and L_{GD}, respectively), which are symmetrical in structure. The AlGaN layer is 25 nm thick on both sides under the insulator (T_{AlGaN}), and the thickness of the GaN channel is 100 nm ($T_{channel}$); GaN and AlGaN also form a 2DEG layer based on the heterostructure. The 2DEG layer under the gate is removed because there is a recessed gate with a 25 nm depth in the center, implying that the channels that were naturally created by the two materials are not formed. Thus, it operates similarly to a MOSFET that forms a channel when a positive voltage is applied, and the normally off operation is possible by shifting the threshold voltage in the positive direction. GaN buffer layer thickness is 2 μm (T_{buffer}) under the channel and sapphire is used as a substrate.

Many studies have been conducted to determine an optimum substrate material and thickness to prevent instability and controllability degradation due to the temperature rise in the device. The method of changing the substrate does not require complicated procedures, is nondestructive, and simple to apply to existing technologies. Diamond, silicon carbide (SiC), Si, and sapphire have been compared as candidates for GaN substrates. Particularly, SiC and diamond, which have low thermal resistance when used with GaN, are suitable materials that can reduce the maximum temperature [18]. Table 1 shows that the thermal conductivity of sapphire and SiC is 35 and 420 W/mK, respectively, meaning SiC is more than 10 times higher; thus, the characteristic change can be confirmed due to

the difference in temperature distribution and heat circulation. Therefore, we additionally confirm the electrical properties and RF performance variation when the substrate material was changed from sapphire to SiC with different thermal conductivity.

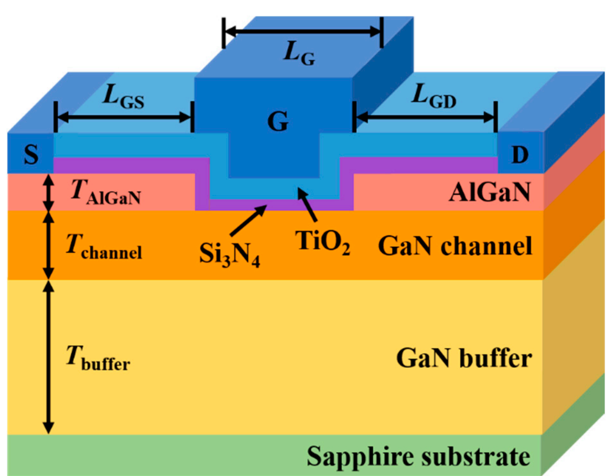

Figure 1. Schematic cross-section of a recessed-gate GaN MOSFET based on AlGaN/GaN heterostructure with TiO_2 and Si_3N_4 as dual-layer insulator.

Table 1. Thermal conductivity at 300 K of materials used in the proposed recessed-gate GaN MOSFET [19–22].

Material	Thermal Conductivity (W/mK)
Si_3N_4	30
TiO_2	8.4
GaN	150
AlGaN	30
SiC	420
Sapphire	35

In this study, various models were applied to include the phenomena that occur during the operation of the device through the ATLAS technology computer-aided design simulation (Silvaco Inc., Santa Clara, CA, USA). Considering the piezoelectric and spontaneous polarization in the 2DEG layer between AlGaN and GaN, the strain due to lattice mismatch was automatically calculated and Shockley–Read–Hall recombination was applied as a physical model. In addition, the device's DC characteristics were derived by adjusting the low and high field mobilities, and we obtained more accurate results by providing interface trap, thermal conductivity, impact ionization, lattice temperature, and permittivity values for each material.

When the device is turned on, a model that spontaneously increases the temperature is used, and this heat generation is explained by lattice heat flow and general thermal environments in the simulation. The equation for calculating the mechanism that changes due to heat generated by the SHEs can be expressed as follows:

$$C\frac{\mathrm{d}T_{\mathrm{L}}}{\mathrm{d}t} = \nabla(k\nabla T_{\mathrm{L}}) + H \quad (1)$$

where C is the heat capacitance per unit volume, T_{L} is the local lattice temperature, k is the thermal conductivity, and H is the heat generation. The peak of temperature and the temperature distribution are calculated and determined through numerical simulation when the temperature of the lattice increases by applying bias. This model calculates the lattice temperature depending on the material and transmission parameters. It also supports general thermal environment specifications using a combination of realistic heat sink construction, thermal impedance, and specified ambient temperature [23–26]. In

addition, for heat flow, the Neumann boundary condition is set as a default value at all boundaries except for the floor, if the model that controls the movement of heat to the floor is not applied; thus, we must provide the thermal resistance values to aid our calculations. Because the thermal contact is not set on the top to focus on the bottom, which is the path where heat escapes to the outside, the movement of heat in the device is determined to be in the direction of the bottom [27].

3. Results

3.1. Dependence of Heat Generation on Oxide Capacitance

Although SiO_2 as a gate-insulator material can prevent leakage current, it has low transconductance (g_m) and large pinch-off voltage, which causes many problems in terms of scaling the device down. Alternatively, high-k dielectrics, such as TiO_2, Al_2O_3, and HfO_2, minimize gate-leakage current, increase transconductance, and have high breakdown voltages, making it possible to have a performance suitable for power devices [28,29]. TiO_2 and Si_3N_4, which we adopted as high-k gate-insulator materials, have dielectric constants of 80 and 8, respectively. When TiO_2 is used alone as a gate-insulator, although the high dielectric constant can result in better electrical properties, its small band gap generates a large leakage current compared with other high-k materials. Furthermore, sputtering deposition directly on GaN produces poor quality that loses the function of the insulator to prevent leakage. Therefore, it is possible to maintain a high capacitance value by stacking TiO_2 on Si_3N, and Si_3N_4 is already frequently used for passivation of GaN devices, so it can solve the difficulties in the process. Deposition is possible through various methods such as in situ deposition in the metalorganic chemical vapor deposition (MOCVD) chamber, plasma-enhanced chemical vapor deposition (PECVD), and low-pressure chemical vapor deposition (LPCVD) [30]. The formula for calculating the capacitance of an insulator composed of two materials is as follows:

$$C_{TiO_2} = \frac{\varepsilon_{TiO_2} \cdot \varepsilon_0}{t_{TiO_2}} \quad (2)$$

$$C_{Si_3N_4} = \frac{\varepsilon_{Si_3N_4} \cdot \varepsilon_0}{t_{Si_3N_4}} \quad (3)$$

$$\frac{1}{C_{total}} = \frac{1}{C_{Si_3N_4}} + \frac{1}{C_{TiO_2}} \quad (4)$$

where ε_{TiO_2} and $\varepsilon_{Si_3N_4}$ are relative dielectric constants (ε_{TiO_2} = 80, $\varepsilon_{Si_3N_4}$ = 8) of TiO_2 and Si_3N_4, respectively; ε_0 is the vacuum permittivity. Using t_{TiO_2} and $t_{Si_3N_4}$ as the thicknesses of TiO_2 and Si_3N_4 (t_{TiO_2} = 20 nm, $t_{Si_3N_4}$ = 10 nm), respectively, C_{TiO_2} and $C_{Si_3N_4}$ can be calculated; in the case of a dual-layer insulator the accumulation capacitance (C_{total}) can be calculated from Equation (4), considering that the capacitors are connected in series. The calculated value of $C_{Si_3N_4}$ in the device with a single-layer insulator is 236 nF/cm^2, whereas the C_{total} in the device using a dual-layer insulator is about 590 nF/cm^2, which is roughly twice as large, implying superior current characteristics. Moreover, it shows that a high capacitance value can be induced under the condition that the ratio of t_{TiO_2} is greater than $t_{Si_3N_4}$ for a constant insulator thickness of 30 nm.

Figure 2a,b shows the drain current (I_D)-gate voltage (V_G) transfer curves when SHE is applied and not applied to recessed-gate GaN MOSFET devices with the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators, respectively. Without the SHE, when V_{GS} is applied from 4 to 10 V, the maximum I_D ($I_{D,\,max}$) in the device using the stacked TiO_2/Si_3N_4 dual-layer insulator at bias V_{DS} = 10 V is 743.80 mA/mm, which is over 15% higher than 643.98 mA/mm of the device with the Si_3N_4 single-layer insulator and their maximum transconductance ($g_{m,\,max}$) are 115.19 and 93.06 mS/mm, respectively. With the SHE, under the same conditions, $I_{D,\,max}$ is 555.15 mA/mm when a stacked TiO_2/Si_3N_4 dual-layer insulator is used, which is 12% higher than 495.61 mA/mm of the device with a Si_3N_4 single-layer insulator, and $g_{m,\,max}$ is 87.30, 69.55 mS/mm, respectively. In Figure 2a,b, the

V_G with the maximum value of transconductance moves in the negative direction under the influence of the SHE, confirming the tendency that the devices with the stacked TiO_2/Si_3N_4 dual-layer insulators have a larger value than devices with a Si_3N_4 single-layer insulator for both characteristics, whether the SHE is applied. As aforementioned, the capacitance value connected in series due to TiO_2 and Si_3N_4 is much larger than when only Si_3N_4 is used, and this is a significant factor that has a great influence on the current increase despite the performance degradation caused by SHEs.

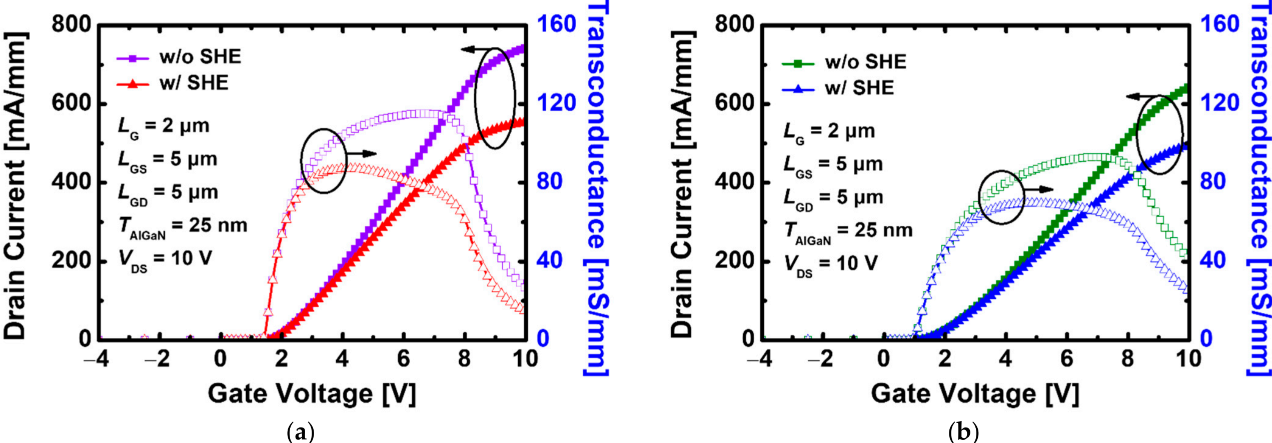

Figure 2. I_D-V_G transfer characteristics with and without SHE in recessed-gate GaN MOSFET using (**a**) the stacked TiO_2/Si_3N_4 dual-layer insulator, (**b**) Si_3N_4 single-layer insulator at V_{DS} = 10 V.

Before we analyze the effect of heat in this study based on the type and thickness of the material used as a gate insulator, it is necessary to first understand how the device's self-heating system works. In Silvaco ATLAS, the overall mechanism that changes due to heat generation and heat flow is calculated from the joule heating, and the equation is as follows:

$$H = \left(\vec{J}_n + \vec{J}_p \right) \cdot E \quad (5)$$

where H represents the generated heat, $\vec{J}_n$ and $\vec{J}_p$ represent the electron and hole current density, respectively, and E denotes the electric field. The heat generation in the GaN channel, which depends on the current density and electric field, contributes to the determination of the electrical properties according to insulator type; thus, the analysis of the correlation between these two factors is required.

Figure 3a,b can play an auxiliary role in the convenient visualization of theoretical content. Figure 3a shows the overall potential distribution for the entire region in the device using the stacked TiO_2/Si_3N_4 dual-layer insulator when a horizontal cutline is drawn along the channel where the 2DEG exists. In the off state (V_{GS} = 0 V) with V_{DS} applied to 20 V, an abrupt change occurs in the drain-side gate edge region, resulting in a large voltage drop. Figure 3b shows that the electric field is close to 0 due to the presence of Si_3N_4 instead of AlGaN under the recessed gate, and a distribution with a tendency similar to the potential that rapidly rises at the gate edge of the drain side is also shown. This means that it can withstand a strong electric field with the voltage drop which implies that it generates most of the heat and has the highest temperature value in this region [31].

3.2. Temperature Sensitivity Comparison

Figure 4a,b show the lattice temperature distribution in a device with the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators, in which heat flow is reflected and particle motions, such as mobility and scattering, are calculated under the bias V_{DS} = 20 V and V_{GS} = 10 V. In both cases, it indicates that the hottest part where the heat is concentrated is the drain-side gate edge region. The peak temperature in the device using the stacked TiO_2/Si_3N_4 dual-layer insulator with SHE is 409.89 K, whereas the device using the Si_3N_4

single-layer insulator rises to 398.75 K, which is 2.7% smaller according to Figure 4c. The field is formed relatively higher along the channel when the stacked TiO_2/Si_3N_4 dual-layer insulator is used, whereas the gate-edge portion where the strongest electric field is generated appears to be larger in the device using the Si_3N_4 single-layer insulator as shown in Figure 5. However, there is a more pronounced difference in the current density compared with the electric field for the two types of devices. Therefore, the maximum temperature at the hotspot is higher in GaN MOSFET with the stacked TiO_2/Si_3N_4 dual-layer insulator and the current density is much larger.

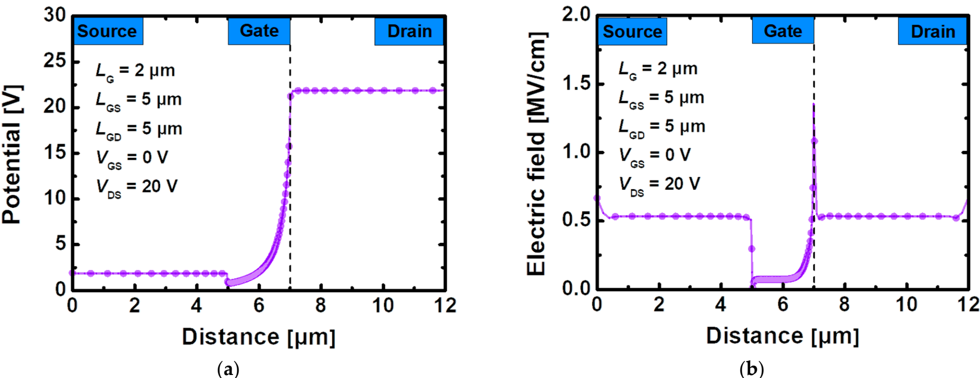

Figure 3. (**a**) Potential and (**b**) electric field in 2DEG layer between GaN and AlGaN under bias V_{GS} = 0 V, V_{DS} = 20 V for recessed-gate GaN MOSFET with the stacked TiO_2/Si_3N_4 dual-layer insulator.

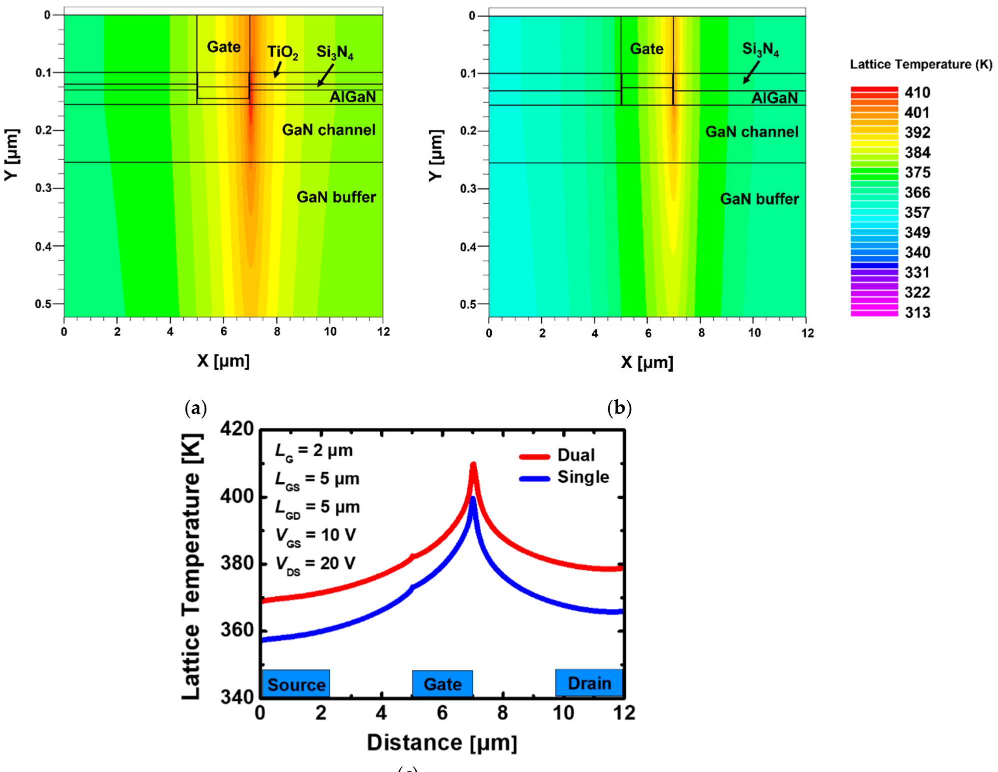

Figure 4. Cross-section of lattice temperature distribution in recessed-gate GaN MOSFET using (**a**) the stacked TiO_2/Si_3N_4 dual-layer insulator, (**b**) Si_3N_4 single-layer insulator and (**c**) lattice temperature distribution according to AlGaN/GaN interface and channel layer for (**a**,**b**) when self-heating effect is applied at V_{DS} = 20 V, V_{GS} = 10 V.

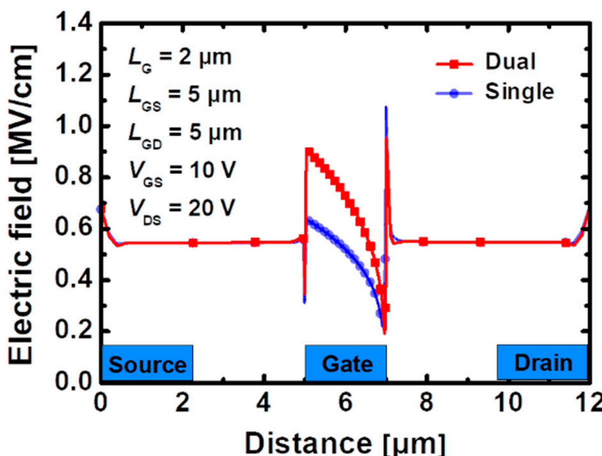

Figure 5. Electric field distribution across the 2-DEG channel layer when self-heating effect is applied in recessed-gate GaN MOSFET using the stacked TiO_2/Si_3N_4 dual-layer insulator and Si_3N_4 single-layer insulator under bias V_{GS} = 10 V, V_{DS} = 20 V.

Figure 6a,b shows the I_D-drain voltage (V_D) transfer curves for two types of devices with and without SHE. In the saturation region, as the slope of the curve decreases and the current tends to be constant, when SHE is not applied, whereas the saturation current is degraded when SHE is applied [32]. This phenomenon is because the increasing electric field and current density contribute to heat generation, and as thermal scattering is accelerated, electron mobility is reduced. When V_{GS} = 10 V, $I_{D,\,max}$ is 883.05 mA/mm for GaN MOSFET with the stacked TiO_2/Si_3N_4 dual-layer insulator without SHE, and the I_D decreases to 536.20 mA/mm when the heat is generated. Furthermore, $I_{D,\,max}$ of GaN MOSFET with a Si_3N_4 single-layer insulator is 727.71 and 463.98 mA/mm with and without SHE, respectively, and it is confirmed that the electrical performance is lowered by SHE. The lattice has a relatively larger peak temperature value when the stacked TiO_2/Si_3N_4 dual-layer insulator is used; however, it still has a higher I_D despite severe thermal scattering because the current density is significantly higher in an environment with a constant heat of 300 K. This implies that if the characteristics of both devices are analyzed at the same temperature, additional benefits in terms of current can be obtained when the dual-layer insulator is used.

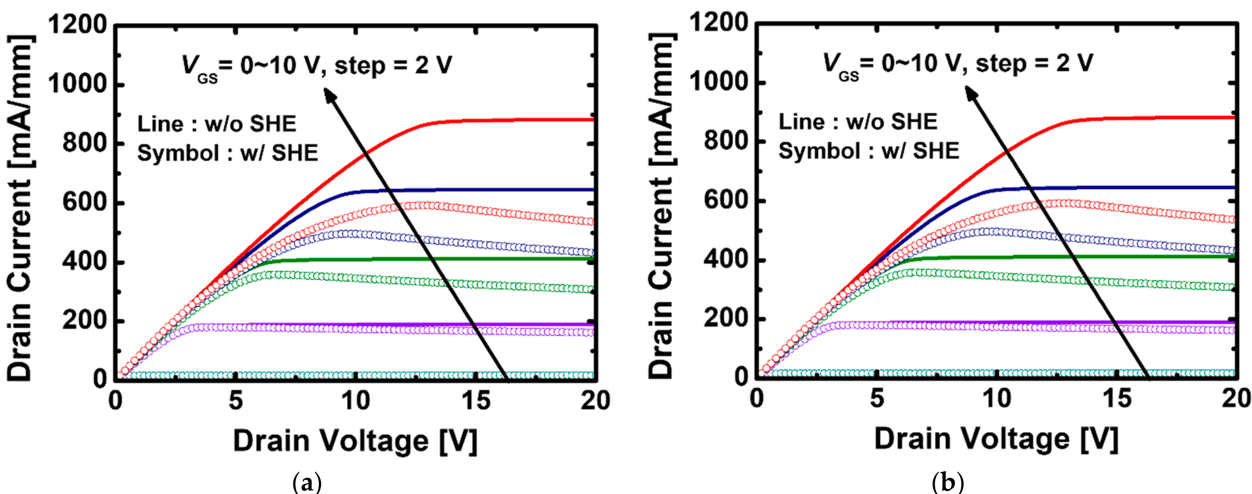

Figure 6. I_D-V_D transfer characteristics with and without self-heating effect in recessed-gate GaN MOSFET using (**a**) the stacked TiO_2/Si_3N_4 dual-layer insulator, (**b**) Si_3N_4 single-layer insulator.

Figure 7 shows the specific on resistance value extracted from the I_D-V_D transfer curve when the lattice temperature is increased from 300 K to 600 K to examine the change trend

of electrical characteristics under the same lattice temperature. The self-heating model produces temperature dispersion, but in this experiment, the temperature in all regions was set to be the constant. The resistance is calculated from the following equation:

$$R_{on,\,sp} = R_{on} \cdot W \cdot L_{SD} \tag{6}$$

where R_{on} is on resistance value when a model that sets the constant to 300–600 K is applied under bias V_{GS} = 10 V, W is the width of the device, and L_{SD} is the length from the source to the drain [33]. The difference in resistance for two devices is due to the change in the insulator type, and considering that the parasitic resistance is the same, we can expect that the $R_{channel}$ dominates. Regardless of the type of gate-insulator, the values of $R_{on,\,sp}$ tend to increase linearly with temperature increases. At 300 K, the resistance of the device with the stacked TiO_2/Si_3N_4 dual-layer insulator is 1.42 mΩ·cm^2, which is about 7.8% smaller than the resistance value of 1.54 mΩ·cm^2 for the device with a Si_3N_4 single-layer insulator and the resistance values of the GaN MOSFET with the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators are 6.02 and 7.00 mΩ·cm^2, respectively, which is about 16% larger, at 600 K.

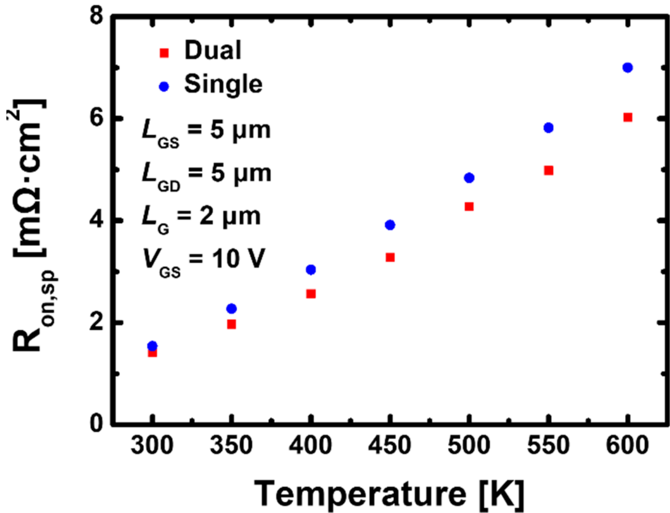

Figure 7. Specific on resistance according to internal temperature obtained from I_D-V_D curve in GaN device using the stacked TiO_2/Si_3N_4 dual-layer insulator and Si_3N_4 single-layer insulator.

Moreover, a Si_3N_4 single-layer insulator makes the slope of resistance steeper with increasing temperature. At high temperatures, the $R_{on,\,sp}$ of the recessed-gate GaN MOSFET using the stacked TiO_2/Si_3N_4 dual-layer insulator maintains a smaller value than that using the Si_3N_4 single-layer insulator; thus, it is estimated that carrier movement in the channel will be easier.

Figure 8 shows the breakdown voltage characteristics of the recessed-gate GaN MOSFET when the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators are used. We set the voltage at which the I_D = 1 µA/mm as the breakdown voltage and observed the breakdown voltage of the device composed of Si_3N_4 and TiO_2 and that composed of Si_3N_4 to be 178 and 158 V, respectively. The device with the stacked TiO_2/Si_3N_4 dual-layer insulator had a larger breakdown due to the effective dispersion when a high voltage is applied; thus, it has a stronger ability to withstand the high heat generated by the high voltage from a device operation perspective [16].

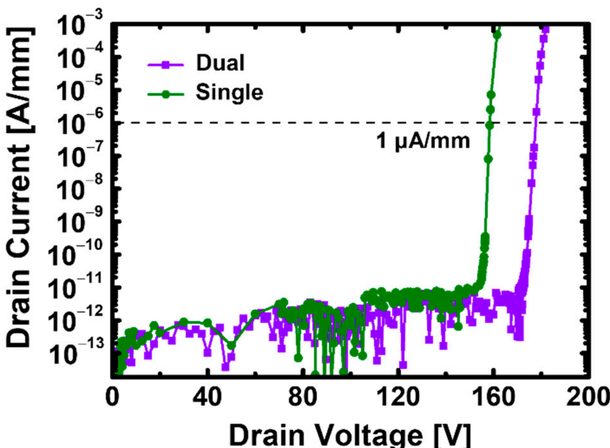

Figure 8. Breakdown voltage characteristics for recessed-gate GaN MOSFET based on AlGaN/GaN heterostructure with the stacked TiO_2/Si_3N_4 dual-layer insulator and Si_3N_4 single-layer insulator at V_{GS} = 0 V.

Figure 9a,b shows the current and unilateral gains based on frequency increase in the recessed-gate GaN MOSFET with the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators, where cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) values were extracted at high frequency with and without SHE. The RF characteristics analysis is possible using the equation derived from the Y-parameter, and the equation is as follows:

$$f_T = \frac{g_m}{2\pi\ (C_{gs} + C_{gd})} \tag{7}$$

$$f_{max} = \frac{f_T}{\sqrt{4R_g \cdot (g_{ds} + 2\pi f_T C_{gd})}} \tag{8}$$

where g_m represents the transconductance, C_{gs} and C_{gd} are the extrinsic gate–source and gate–drain capacitance (expressed as $C_{ox} = C_{gs} + C_{gd}$), respectively, R_g is the gate resistance, and g_{ds} is source-drain conductance. From the I_D-V_G transfer characteristics curve, the V_G at which g_m becomes maximum for each case was applied on the RF simulation. It was induced by increasing transconductance and oxide capacitance, since GaN MOSFET with the stacked TiO_2/Si_3N_4 dual-layer insulator aims to improve the DC characteristics; but Equation (5) shows that g_m and C_{ox} for f_T have opposite relationships, requiring a complex analysis. Table 2 summarizes the capacitance values and f_T calculated using the Y-parameter extracted by applying the AC signal model to each case. The cut-off frequency has a larger value when a Si_3N_4 single-layer insulator is used, and the SHE is not applied for GaN MOSFET as shown in Figure 9a.

Table 2. Cut-off frequency, gate to source capacitance, gate to drain capacitance and gate oxide capacitance values calculated (C_{ox} = C_{gs} + C_{gd}) according to whether SHE is applied or not in response to an AC signal is applied for recessed-gate GaN MOSFET with the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators.

Material	f_T [GHz]	C_{gs} [pF]	C_{gd} [pF]	C_{ox} [pF]
Dual w/o SHE	5.45	2.57	0.53	3.10
Dual w/SHE	3.98	3.04	0.30	3.34
Single w/o SHE	7.36	1.51	0.35	1.86
Single w/SHE	5.86	1.65	0.26	1.91

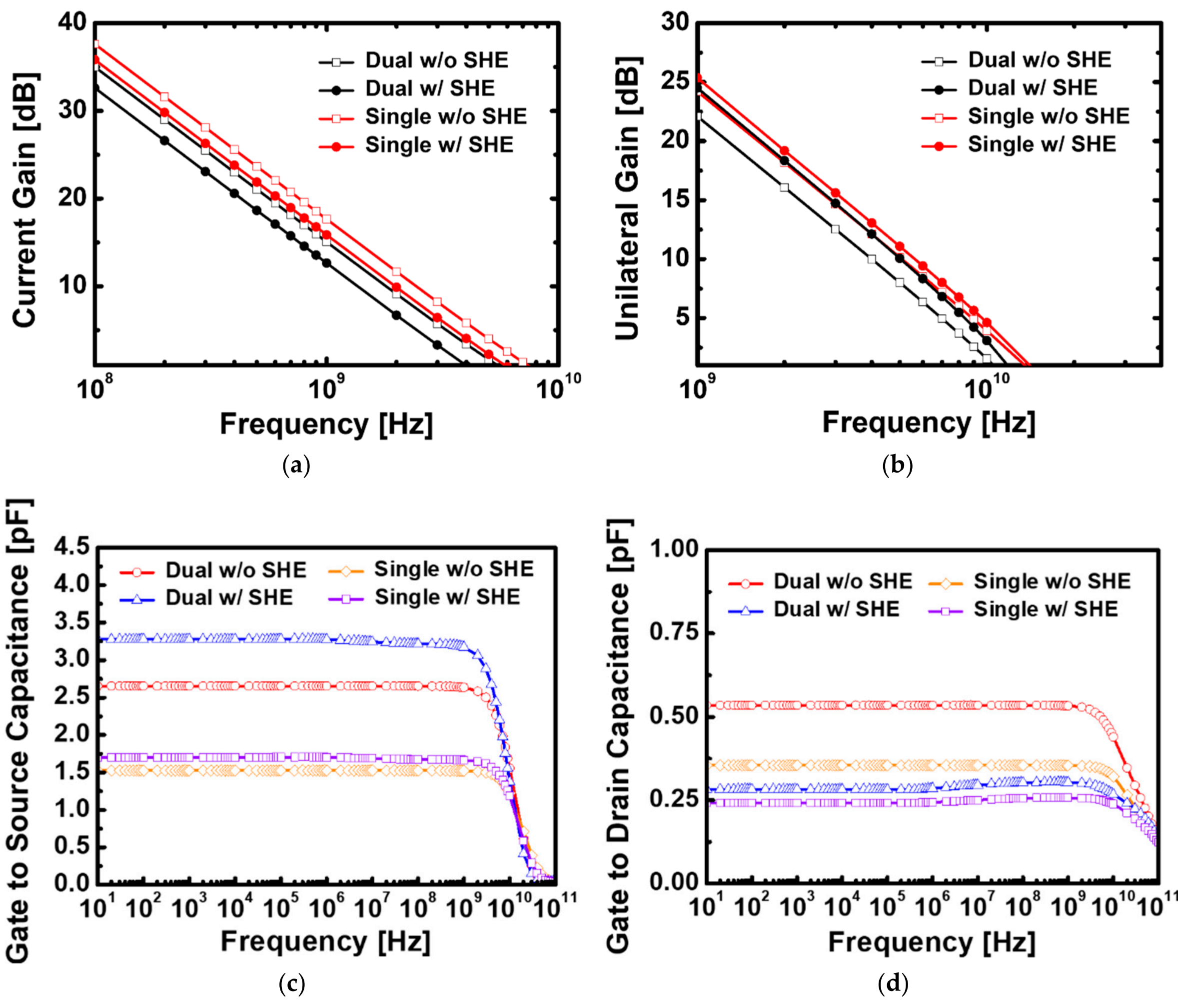

Figure 9. (**a**) Cut-off frequency, (**b**) maximum frequency and dependence of (**c**) gate to source capacitance and (**d**) gate to drain on frequency for the recessed-gate GaN MOSFET using the stacked TiO_2/Si_3N_4 dual-layer insulator and Si_3N_4 single-layer insulator with and without self-heating effect.

Because V_D and V_G are changed by AC signals, unlike in DC signals, which affect the charge of the channel and gate, the C_{gd} and C_{gs} should be separately analyzed; thus, the semiconductor oxide capacitance value can no longer be defined as only C_{ox}. Figure 9c,d shows C_{gd} and C_{gs} in the frequency range of 10–10^{11} Hz for the four cases in Figure 9a,b, where C_{gs} is dominant in determining the oxide capacitance value. The C_{gs} is larger for devices with SHE than those without SHE, which is due to a decrease in the thermally activated carriers' detrapping phenomena in the donor layer, resulting in a decrease in the equivalent doping level; thus, smaller C_{gs} is observed at lower temperatures [34]. We confirm from this capacitance analysis that the C_{gs} of devices with a stacked TiO_2/Si_3N_4 dual-layer insulator is large, as g_m has a significantly large value, whereas the g_m of devices with a Si_3N_4 single-layer insulator is relatively small. However, higher frequency operations in terms of RF characteristics are possible since C_{gs} is extremely small. The f_{max} to which the SHE is applied has a larger value than that to which the SHE is not applied in the two types of devices, unlike Figure 9a. Table 2 shows that the values of C_{gs} and C_{gd} are reversed based on whether SHE is applied because the value of the V_G in the section where g_m is the maximum decreases as the temperature increase; therefore, the capacitance value is estimated to be small when that value is applied during AC simulation, which affects these results. However, it is unchanged that the maximum frequency value is larger when GaN MOSFET is used as a Si_3N_4 single-layer insulator.

3.3. Heat Transfer Materials

Figure 10 shows the distribution of the lattice temperature when only the substrate material is changed to SiC under the same device structure and bias conditions. The overall temperature difference relatively reduces and the peak temperature value at the drain side gate-edge of the GaN MOSFET using the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators is 346.75 and 346.79 K, respectively; it exhibits an inverted trend compared to when the substrate is used as a sapphire. We demonstrate that SiC, which has excellent heat-transfer ability, can reduce the self-heating damage by preventing heat generated during device operation from being trapped inside and emitting it to the outside.

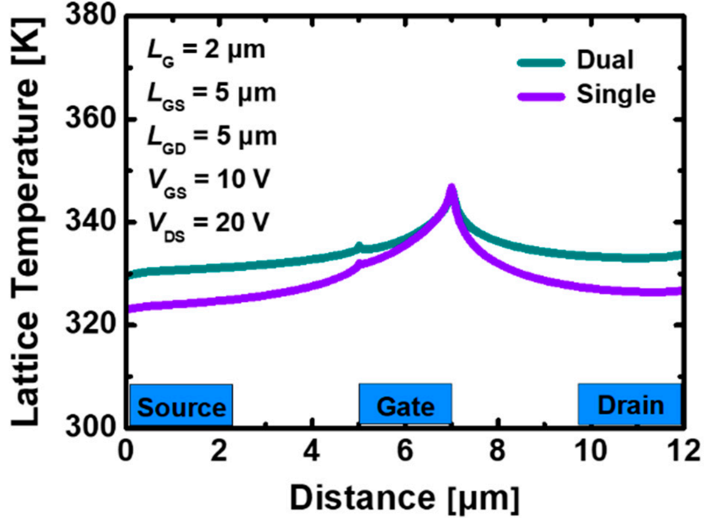

Figure 10. Lattice temperature distribution across the 2DEG channel layer with self-heating effect in recessed-gate GaN MOSFET using the stacked TiO_2/Si_3N_4 dual-layer insulator and Si_3N_4 single-layer insulator on SiC substrate under bias V_{GS} = 10 V, V_{DS} = 20 V.

Because the replacement of the substrate material has an effect only when heat transfer occurs due to an increase in internal temperature, it does not affect the overall device properties while maintaining a constant 300 K without SHE. Figure 11a,b show that the use of SiC increases the $I_{D,\,max}$ of the GaN MOSFET with the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators to 640.52 and 564.29 mA/mm, respectively, and narrows the performance gap with the device without a temperature change.

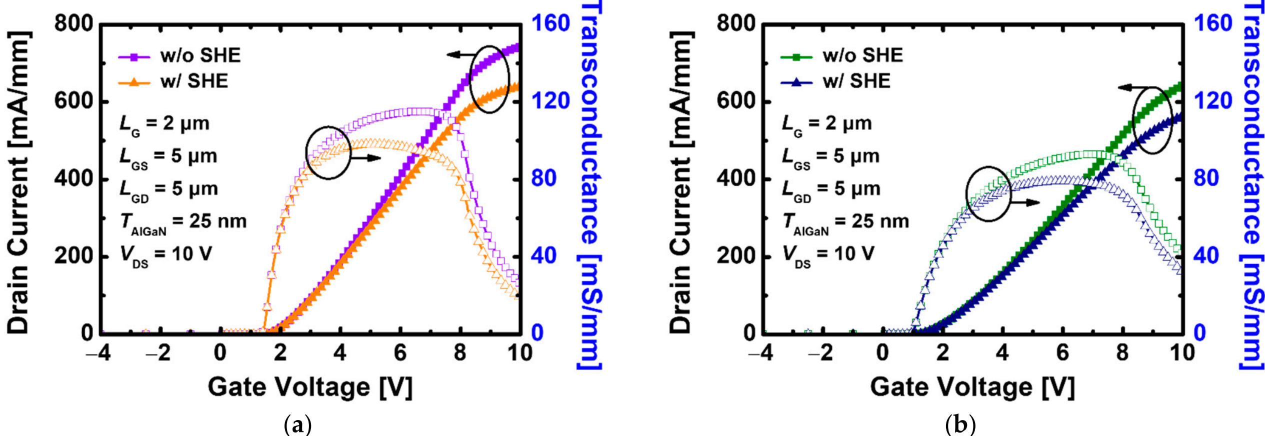

Figure 11. I_D-V_G transfer characteristics with and without SHE in recessed-gate GaN MOSFET on SiC using (**a**) the stacked TiO_2/Si_3N_4 dual-layer insulator, (**b**) Si_3N_4 single-layer insulator at V_{DS} = 10 V.

Figure 12a,b show the current and power gain based on the frequency obtained by applying the changed V_G at which g_m becomes maximum by changing the substrate to SiC. The RF characteristic remains constant regardless of the substrate material change without temperature rise. When SHE is applied, the f_T of devices with the stacked TiO_2/Si_3N_4 dual- and Si_3N_4 single-layer insulators is 4.7 and 6.64 GHz, respectively, which are improved by 18% and 13% compared with GaN on the sapphire. Consequently, the difference from the frequency without SHE is also minimized, and f_{max} results are improved, reflecting the same trend.

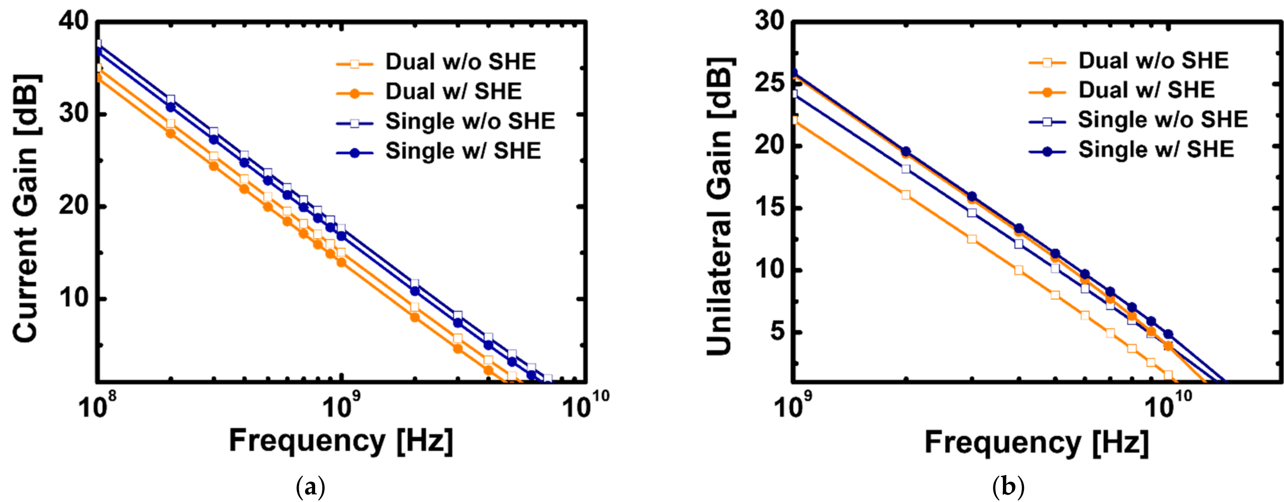

Figure 12. (**a**) Cut-off frequency and (**b**) maximum frequency of recessed-gate GaN MOSFET using the stacked TiO_2/Si_3N_4 dual-layer insulator and Si_3N_4 single-layer insulator with and without self-heating effect on SiC substrate.

4. Conclusions

We have analyzed the recessed-gate GaN MOSFET with the stacked TiO_2/Si_3N_4 dual-layer insulator for several DC and RF characteristics by using a TCAD simulation. By increasing the oxide capacitance of the Si_3N_4 and TiO_2 combination, we have confirmed that it has a smaller R_{on}, larger I_D and improved g_m compared with the device using a Si_3N_4 single-layer insulator. The breakdown voltage is also relatively high, so it has strength as a power device. Furthermore, RF characteristics including current gain and power gain were evaluated. In addition, the self-heating effects (SHEs) model were reflected in the simulation, and important changes in DC and RF characteristics occurred. The performance degradation by SHEs is more affected for GaN MOSFETs with the stacked TiO_2/Si_3N_4 dual-layer insulators due to its larger electric field and current density. Nevertheless, the dual-layer insulator induces the transistor to have enhanced DC performances. In conclusion, the recessed-gate GaN MOSFETs with the stacked TiO_2/Si_3N_4 dual-layer insulator can be expected to be candidates for devices with an attractive ability to deliver high power at high frequency.

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