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Electrical Characteristics of Diamond MOSFET with 2DHG on a Heteroepitaxial Diamond Substrate

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Abstract: In this work, hydrogen-terminated diamond (H-diamond) metal-oxide-semiconductor field-effect-transistors (MOSFETs) on a heteroepitaxial diamond substrate with an Al_2O_3 dielectric and a passivation layer were characterized. The full-width at half maximum value of the diamond (004) X-ray rocking curve was 205.9 arcsec. The maximum output current density and transconductance of the MOSFET were 172 mA/mm and 10.4 mS/mm, respectively. The effect of a low-temperature annealing process on electrical properties was also investigated. After the annealing process in N_2 atmosphere, the threshold voltage (V_{th}) and flat-band voltage (V_{FB}) shifts to negative direction due to loss of negative charges. After annealing at 423 K for 3 min, the maximum value of hole field effective mobility (μ_{eff}) increases by 27% at $V_{th} - V_{GS} = 2$ V. The results, which are not inferior to those based on homoepitaxial diamond, promote the application of heteroepitaxial diamond in the field of electronic devices.

Keywords: heteroepitaxial diamond; MOSFET; annealing

1. Introduction

Diamond semiconductors have been studied for decades due to their excellent properties, such as wide band gap energy (5.5 eV), high breakdown electrical field (>10 MV/cm), extremely high thermal conductivity (22 W/cm K), and high carrier mobility (3800 for holes and 4500 cm^2/Vs for electrons) [1–3]. Diamond is preferred for application in high-frequency, high-power electronic devices. Nevertheless, the traditional electronic device fabrication process for diamond is restricted because of the immature n type doping technique. Fortunately, when the hydrogen-terminated diamond (H-diamond) is exposed to air, some adsorbates forming at the H-diamond surface act as electron acceptors. Electrons at the H-diamond surface transfer to these adsorbates so that a two-dimension hole gas (2DHG) is induced [4]. Thanks to diamonds, field effect transistors (FET) have developed greatly [5–7]. Up to now, diamond FETs have exhibited excellent performance. K. Ueda et al. achieved a maximum oscillation frequency (fmax) of 120 GHz on high-quality homoepitaxial polycrystalline diamond [8]; Kawarada et al. demonstrated a high-performance H-diamond metal oxide semiconductor (MOSFET) with a maximum output power density of 3.8 W/mm@1GHz [9].

However, to date, the vast majority of diamond electronic devices have been fabricated on HTHP (high temperature and high pressure) and homoepitaxial CVD (chemical vapor deposition) substrates, whose size are greatly limited. This is averse to low cost and commercialization. Thus, in order to resolve this issue, another effective technology should

be developed to obtain large and high-quality single crystalline diamond substrates which can reduce costs and enable mass production. It is gratifying that diamond heteroepitaxy on Ir has been extensively developed. Not only the 4-inch size of heteroepitaxial diamond but also the low dislocation density of 9×10^6 cm^{-2} has been achieved [10,11]. Regarding the thick film growth and device fabrication, a-plane sapphire is a promising material to realize large free-standing (001) orientation diamond substrates [12]. Additionally, on this basis, Makoto et al. fabricated $Al_2O_3/NO_2/H$-diamond MOSFET with an extremely high breakdown voltage on heteroepitaxial single crystal diamond (HSCD) [13].

In this work, we fabricated ALD-Al_2O_3/H-diamond MOSFET on a free-standing HSCD. The size of the HSCD is $26 \times 26 \times 1$ mm^3, and the full-width at half maximum value of the (004) X-ray rocking curve is 209.5 arcsec. The output current density I_{DS}, maximum transconductance $g_{m(max)}$ and carrier density of MOSFET with the same size is much better than that we reported previously [14,15], and the effective mobility (μ_{eff}) and interface states density (D_{it}) are discussed pre- and post- annealing process at low temperature in N_2 atmosphere.

2. Materials and Methods

In this work, an a-plane (11–20) sapphire with a size of $26 \times 26 \times 1$ mm^3 was chosen as the substrate. Then, approximately 150 nm Ir was deposited at 900 °C using magnetron sputtering technology. Subsequently, bias enhanced nucleation (BEN) was conducted in direct current CVD (Flashforge dreamer©, Jinhua, China) [16]. After the BEN process, diamond epitaxy was carried out in horizontal type MPCVD for 100 h with a growth rate of 10 μm/h. The specific parameters of BEN and epitaxial growth process were reported elsewhere [16]. The insert image is the optical image of a polished heteroepitaxial diamond with a dimension of $26 \times 26 \times 1$ mm^3. Figure 1 shows the XRD (X-ray diffraction) characteristic of the HSCD. The FWHM of (004) X-ray rocking curve was measured as 209.52 arcsec, which is a relative high value with a size over 1 inch among the heteroepitaxial diamond [10–12,17] After cleaning the substrate with mixed acid (HNO_3:H_2SO_4) at 250 °C for 1 h and deionized water in turn, 100 nm homoepitaxial layer was grown on the HSCD with a MPCVD (microwave plasma chemical vapor deposition) system. The growth temperature, pressure, and time were 930~970 °C, 30 Torr, and 60 min. The H_2 and CH_4 flow rates were 300 and 0.6 sccm, respectively. The hydrogen plasma was maintained for 20 min to form H-diamond; after stopping CH_4 flow, 200 nm Au was deposited on the H-diamond surface as source and drain electrodes by the electron beam evaporation technique. Next, ultraviolet ozone (UV/O_3) was used to convert hydrogen termination into oxygen termination (OT) except for the channel. After that, a 30 nm Al_2O_3 passivation layer was deposited on the diamond in two steps by the atomic layer deposition (ALD) technique. Trimethylaluminum (TMA) and H_2O were adopted as the source and oxidant, respectively. First, a 5 nm Al_2O_3 layer was deposited at 90 °C to protect the C-H against oxidation. Second, a 25 nm Al_2O_3 layer was deposited at 250 °C. The Al_2O_3 on the electrodes was removed by H_3PO_4 solution to expose the electrodes for subsequent electrical characterization. Finally, 30/150 nm Ti/Au was deposited on the Al_2O_3 layer as the gate electrode. The device characteristics were measured at room temperature (RT).
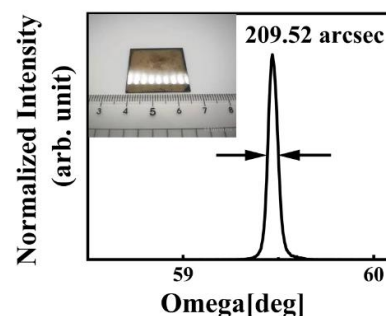

Figure 1. X-ray rocking curve of HSCD.

3. Results and Discussion

Figure 2a shows the schematic diagram of the MOSFET. The gate width (W_G), gate length (L_G) and distance source/drain are 100, 2, and 20 μm, respectively. L_{SG} and L_{GD} are 9 μm. Figure 2b illustrates the energy band diagram of H-diamond/Al$_2$O$_3$. The 2DHG under the diamond surface is accumulated due to negatively charged adsorbates, which lead to the energy band's upward bending at the diamond surface.
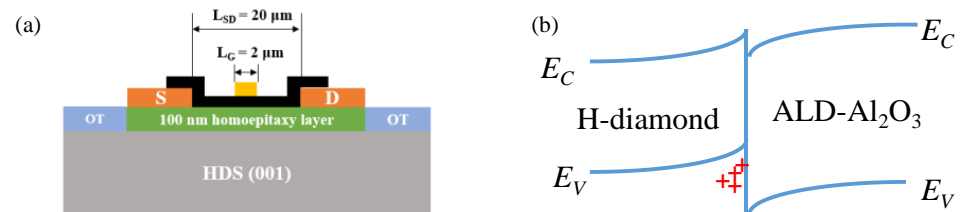
Figure 2. (**a**) Schematic diagram of the MOSFET; (**b**) energy band diagram of H-diamond/Al$_2$O$_3$ without gate bias.

Figure 3 shows the electrical characteristics. The I_{DS}-V_{DS} curve is shown in Figure 3a. The gate-source voltage (V_{GS}) varies from 12 V to −8 V in steps of −2 V. The maximum current density is 172 mA/mm at V_{GS} = −8 V; V_{DS} = −30 V. This value is much higher than that we reported based on the homoepitaxial diamond substrate previously [15,16]. It demonstrates the application potential of heteroepitaxy diamond to electronic devices. The on-resistance (R_{ON}) is evaluated to be 130.5 Ω·mm. As displayed in Figure 3b, the threshold voltage (V_{th}) is deduced to be 11.85 V, demonstrating a normally on performance which is obtained according to the relationship of $\sqrt{|I_{DS}|}$ and V_{GS}. The maximum transconductance $g_{m\,(max)}$ is 10.4 mS/mm. Figure 3c exhibits the relationship of $\log(|I_{DS}|)$ and V_{GS}. The subthreshold slop and on/off ratio can be observed to be 400 mV/dec and 10^5.
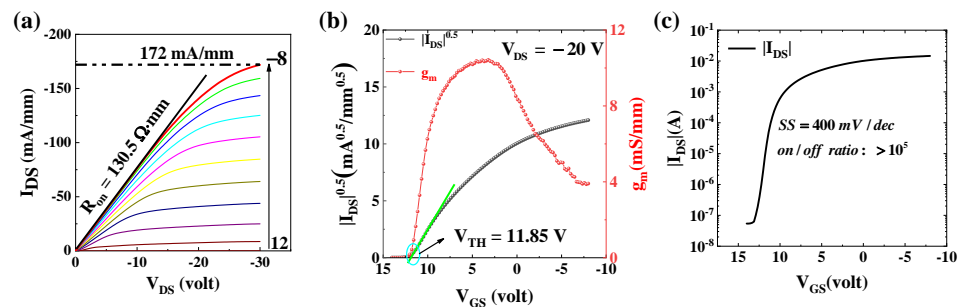
Figure 3. (**a**) Output characteristics of MOSFET; (**b**) transfer curve (**c**) (−I$_{DS}$)-V$_{GS}$ characteristics on a logarithmic scale.

The capacitance voltage (*CV*) characteristics were measured at a frequency of 1 MHz, as displayed in Figure 4a. V_{GS} swept from 18 to −10 V and −10 to 18 V for the black and red lines, respectively. *C-V* curves shift to the right relative to 0 V, which indicates that negative charges exist in the oxide layer. C_{ox} for the ALD-Al$_2$O$_3$ /H-diamond MOS is 2.7×10^{-7} F/cm^2. The flat band capacitance (C_{FB}) can be calculated from the following equation [18]:

$$C_{FB} = \frac{1}{\left(\frac{1}{C_{ox}} + \frac{L_D}{\varepsilon_0 \varepsilon_{dia}}\right)} \tag{1}$$

where L_D is the Debye length of H-diamond which can be determined to be 2 nm based on carrier concentration of 2×10^{18} cm^{-3} for-hydrogen terminated diamond at RT [19], ε_{dia} is relative permittivity of diamond (5.7). Thus, the C_{FB} can be calculated to be 2.5×10^{-7} F/cm^2. The flat band voltage (V_{FB}) is determined to be 9.1 and 11.7 V in the reverse (red line) and forward (black line) direction, respectively. The relationship of the

fixed negative charge density (N_{fc}) and flat band voltage can be described as the following equation:

$$N_{fc} = \frac{C_{ox}(V_{FB} + \Delta W/e)}{e} \tag{2}$$

where ΔW is the work function difference between H-terminated diamond (4.9 eV) [20] and the Ti (4.3 eV) gate electrode, e is the elementary charge of 1.6×10^{-19} C; therefore, the N_{fc} in Al_2O_3 layer can be determined to be $1.66 \times 10^{13}/cm^2$. The trapped charge density can be calculated to be $4.03 \times 10^{12}/cm^2$ according to the hysteresis loop (ΔV_{FB} = 2.6 V). Figure 4b shows the relationship between the hole density (ρ) and V_{GS}. The carrier density can be evaluated by $\rho = (\int CdV)/e$, and the result is $3.3 \times 10^{13}/cm^2$ obtained at $V_{GS} = -8$ V. A linear tendency reveals a uniform carrier distribution of H-diamond.
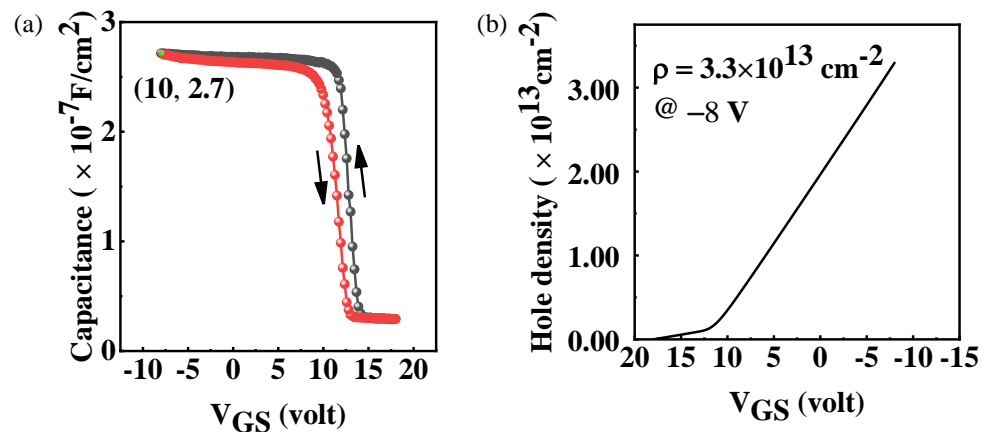
Figure 4. (**a**) C-V curve of Al_2O_3/H-terminated MOSFET; (**b**) hole density ρ-V_{GS} characteristic.

The field effective mobility μ_{eff} of the MOSFET can be calculated from the following equation:

$$I_{DS} = \frac{W_G \mu_{eff} C_{ox}(V_{GS} - V_{th})^2}{2L_G} \tag{3}$$

At RT, the μ_{eff} is determined to be 36.5 cm^2/Vs at V_{GS} = 10 V. For the off-state region, the interface state density D_{it} can be evaluated from the subthreshold swing SS, which is given by [21]

$$SS = \frac{kT(\ln 10)}{q}[1 + \frac{C_D + q^2 D_{it}}{C_{ox}}] \tag{4}$$

where k, T and e are the Boltzman constant, temperature and elementary charge, respectively. C_{ox} and C_D ($C_D \ll q^2 D_{it}$) are the capacitance of the Al_2O_3 layer and depletion layer. The subthreshold swing can be derived from Figure 3c. The minimum SS is 400 mV/dec at V_{GS} = 12 V. Hence, the D_{it} can be determined to be 1.07×10^{13} eV^{-1}/cm^2.

To investigate the effect of low-temperature annealing on electrical properties of the MOSFET, the sample was annealed in N_2 ambient at 423 K and 473 K for 3 min, sequentially. Threshold voltage (V_{th}) shifts negatively with increasing annealing temperature, as shown in Figure 5a. In Figure 5b, the *C-V* curve shifts to the negative direction. Additionally, the V_{FB} for each curve can be extracted to be 9.1 V (red), 6.8 V (green), and 3.3 V (black), respectively. The negatively shifted V_{FB} indicates that the annealing process decreases the negative charge density at the Al_2O_3/H-diamond interface [22]. The loss of negative charges which can induced holes beneath the diamond surface results in negatively shifted V_{th}, as shown in Figure 5a. Figure 6 presents the μ_{eff} at $V_{th} - V_{GS} = 2 \pm 0.2$ V and D_{it} as a function of annealing temperature. Obviously, all μ_{eff} and D_{it} values show completely inverse trends, which means that μ_{eff} strongly depends on D_{it}. When D_{it} is decreased to 8×10^{12} cm^{-2}·eV^{-1}, the μ_{eff}, from 36.5 to 46.5 cm^2/Vs, increases by 27% after the annealing process at 423 K. The possible reason is that when the annealing temperature is 423 K,

the quality of ALD-Al_2O_3/H-diamond interface was improved. On the contrary, when the annealing temperature increases to 473 K, the D_{it} increases dramatically and the μ_{eff} decreases sharply. It implies that 200 °C annealing process for 3 min possibly degrades the interface between Al_2O_3 and diamond [22,23]. After the 200 °C annealing process, the increased D_{it} which acts as charges at interface results in enhancement of coulomb scattering at the ALD-Al_2O_3/H-diamond interface.
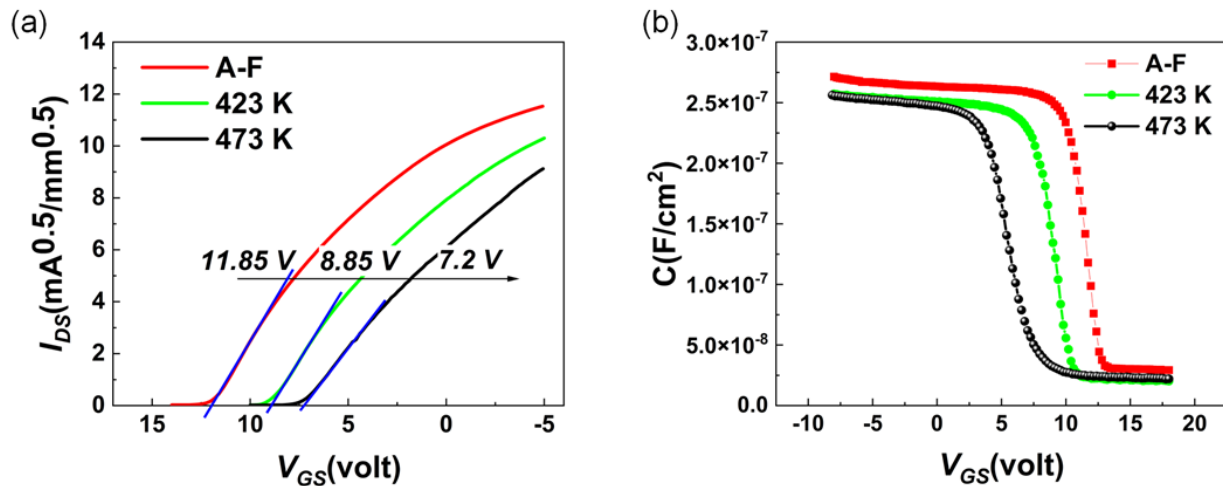
Figure 5. (**a**) transfer curve of MOSFET as-fabricated(A-F) and after annealing process at 423 K and 473 K for 3 min (**b**) *C-V* curve of MOSFET as-fabricated(A-F) and after annealing 150 °C and 200 °C process for 3 min.
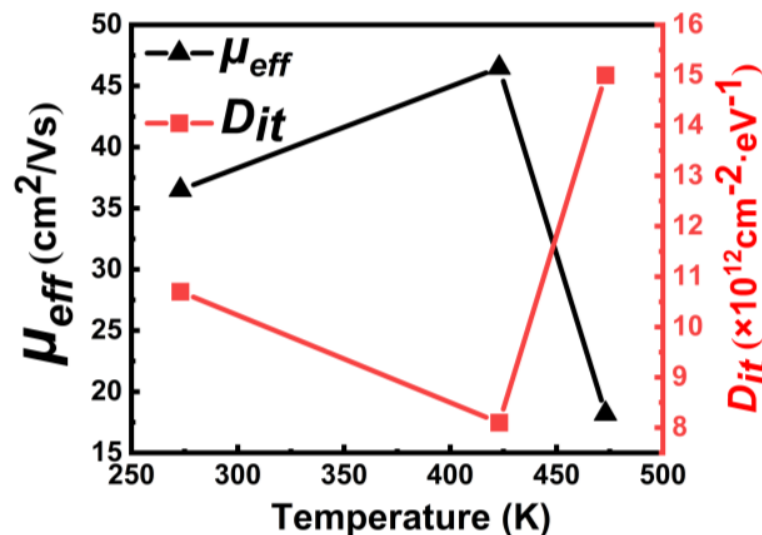
Figure 6. μ_{eff} at $V_{th} - V_{GS} = 2 \pm 0.2$ V and D_{it} as a function of annealing temperature.

4. Conclusions

In summary, ALD-Al_2O_3/H-diamond MOSFETs based on heteroepitaxial diamond substrate were fabricated and characterized. The output current density, carrier density and on-resistance R_{on} were 172 mA/mm, 3.3×10^{13}/cm^2 and 130.5 Ω·mm at $V_{GS} = -8$ V, respectively. Both the V_{th} and V_{FB} shifted to negative direction, which can be ascribed to loss of fixed negative charges. After annealing at 423 K, μ_{eff} increased by 27%, accompanying the decreased D_{it}. Yet, annealing at 473 K for 3 min possibly degrades the Al_2O_3/diamond interface. The annealing temperature and period for Al_2O_3/H-diamond need to be controlled precisely.

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